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Full-SiC Single-Chip Buck and Boost MOSFET-JBS Converters for Ultimate Efficient Power Vertical Integration

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Abstract— This paper aims at demonstrating the relevance of a new design perimeter for power switching cells through a monolithic vertical integration approach on a multi-terminal power chip with Wide-Band Gap material such as 4H silicon carbide (SiC). Multi-terminal monolithic architectures making use quasi-only of vertical unipolar switch (VDMOS) and JBS diode architecture within the context of a 600V/10A full integration of switching cells on 4H-SiC chips are proposed and validated through Sentaurus™ 2D numerical simulations. The key method to etch and to fill the metallic via needed to connect the VDMOS and the JBS from top to back side of the SiC wafer is presented. The first optimization of the electroplating process resulted in a Ni metal layer of about 5µm thick.

Keywords—Power switching cells; monolithic; VDMOS; JBS diode; 2D simulations; metallic via; electroplating process

I. INTRODUCTION

Silicon carbide (SiC) vertical power metal-oxide-semiconductor field-effect transistors (VDMOS) are of great interest since they are unipolar gate-controlled switches with high blocking voltage capability, low specific on-resistance and high frequency operation. With the growing industrial maturity of SiC VDMOS and their multi-sectorial widespread diffusion into the field of critical embedded power systems, there is a growing interest for the monolithic integration of dedicated power conversion functions in SiC dies [1]. As compared to the hybrid multi-chip integration approach, the monolithic integration offers reduced costs and manufacturing time through optimizing the number of steps within a single technology fab-chain. However, due to the chip size capability, monolithic integration remains targeted to low current ratings. Regarding high-performance applications, monolithic integration aims at minimizing the parasitic elements, resulting from the external interconnection wiring of different chips. The impact of these circuit parasitics becomes critical at higher switching frequencies as they can lead to unwanted oscillations, which degrade system performance and can damage devices. For instance, the parasitic inductances induce high-voltage overshoot during the switch turn-off that not only

adds electrical stress to the power dies but also lead to an increase of switching losses that degrades the overall efficiency and reliability.

In medium power applications, the gradual progress that took place, during many decades, in the monolithic integration of power conversion functions in silicon wafers permitted the design and realization of a great number of monolithic power functions built around the power IGBT switch. For some of these power functions, it required the set-up of new specific technological process bricks that were integrated within the basic IGBT technological process-flow [2-3]. Within this context, several monolithic power functions integrating auxiliary functions built around a single power IGBT switch such as protection functions [4-7] were reported. Moreover, regarding the monolithic integration of switching cells and generic power converter, within a minimum number of multi-terminal Si-chips, original integration approaches that make use of RC-IGBTs were reported [8-9]. These new and original multi-terminal chips involve the two-chip [10], three-chip [11] and the ultimate monolithic single chip-converter [10].

Up to date, few works reported on the monolithic integration in silicon carbide of power functions with the VDMOS. Indeed, those works mainly focused on the monolithic integration of auxiliary low voltage functions within a single high voltage VDMOS. Among the reported works, one can find the P-Well monolithic functionalization of a series normally-on cascode JFET current limiter [12], integration of auto-adjust JFET with VDMOS [13], integration of VDMOS with a CMOS gate buffer [14-15]. However, none of these works addressed or discussed the design of a complete full-SiC basic switching cell.

The present paper explores the monolithic integration of new and original switching cells made of a JBS diode and a SiC VDMOS in series within a single chip. It proposes new multi-terminal architectures, validates their operating modes through 2D TCAD Sentaurus™ simulations and proposes technological process steps, compatible with a standard SiC VDMOS process, in order to consider their future practical

integration on SiC wafers. This monolithic integration is interesting in order to improve further the performance, reliability and cost reduction of the currently used discrete-diodes-based switching cells. In addition, the design of medium power H-bridge converters will consequently require a minimum number of chips that will contribute to the improvement of the large-scale productivity of power converters and also to the reduction of their fabrication cost. Within this category, the monolithic integration on SiC material for the first time of two vertical VDMOS switches was reported in literature [16]. However, this last reference does not mention the extension of the proposed design to switching cell architecture. The current paper is organized as follows: in section II the design of a buck and a boost cells is depicted, in section III 2D TCAD Sentaurus™ simulations are performed and deeply analyzed, in section IV one of the major technological bricks of the concept is pre-evaluated, and finally in section V a conclusion is drawn.

II. CONCEPT OF INTEGRATION APPROACH

The main objective is to design new monolithic power switching cells on silicon carbide (4H-SiC). The proposed vertical monolithic integrated devices should support between 600 and 1200 V voltage and carry a nominal current of 25 A at 300 K.

In this context, two original elementary 3-terminal chip versions of Buck-type and Boost-type switching cells have been designed. Each one of the elementary chips co-integrates on the same wafer an efficient JBS diode and a VDMOS transistor in series. The physical and geometrical parameters of the VDMOS and the JBS diode illustrated in Fig. 1 were imposed by the CNM laboratory (Centro Nacional de Microelectrónica) process flow, an experienced and recognized technology center in Europe for SiC technology for more than twenty years and in particular in SiC MOSFETs [17-18].

The technological challenges for the realization of each chip are mainly related to the realization of the full vertical insulation, which combines a deep trench in the die backside filled with a dielectric, and a deep P⁺ implementation on the top side above this trench (Fig. 1). This insulation is essential to prevent any lateral current flow in both the N⁻ drift layer and the N⁺ substrate between the VDMOS-side and the JBS-side. A second challenge is the integration of the metal via, extending from the frontside of the chip to the backside N⁺ substrate, through the drift layer. This metallic via provides the electrical interconnection between the midpoint (MP) of the switching cell and the back-side N⁺ substrate (Fig. 1). So, the JBS cathode and the VDMOS source are fully internally connected to form a switching cell having an ultra-low stray inductance.

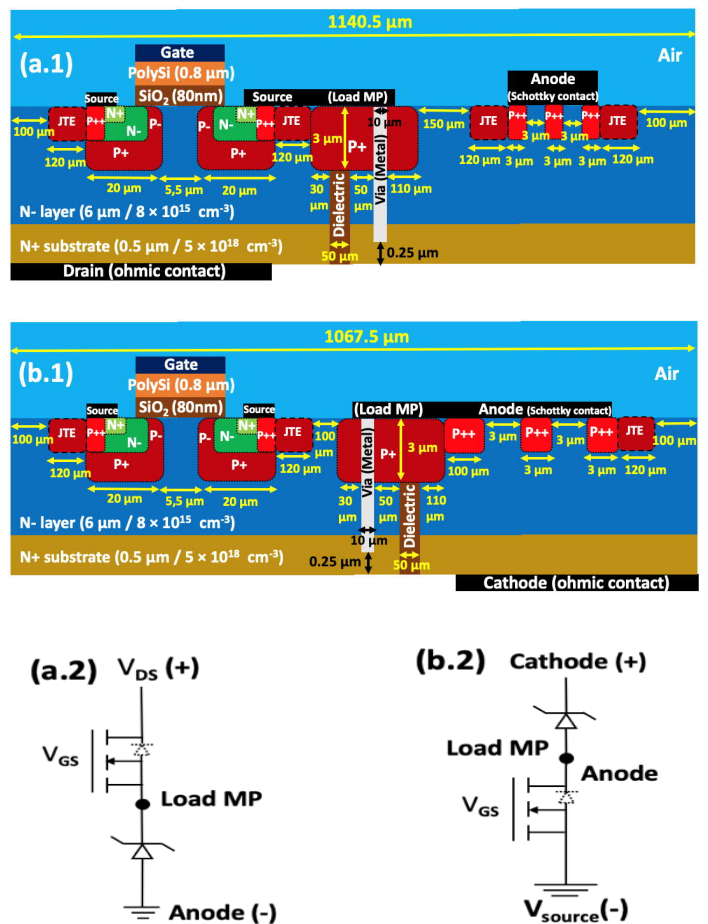


Fig. 1. (a) SiC VDMOS-JBS Buck-type switching cell concept: (a.1) Cross sectional view of the proposed 3-terminal chip with the different technological and geometrical parameters, (a.2) Simplified equivalent electrical circuit. (b) SiC VDMOS-JBS Boost-type switching cell concept: (b.1) Cross sectional view of the proposed elementary 3-terminal chip with the different technological and geometrical parameters, (b.2) Simplified equivalent electrical circuit.

III. SENTSAURUS™ MIXED MODE SIMULATION RESULTS

In this section, the operating modes of the two proposed monolithic structures were analyzed and validated by 2D Sentaurus™ simulations. Each switching cell was analyzed by observing the current densities, equipotential-lines and electric field distribution in each structure. The main objective is to see that when one section is in on-state and carries the imposed current, the other section is in off-state and withstand the applied voltage. The 2D numerical simulations are carried-out in mixed mode circuit – device using Sentaurus™ and at 300 K [19-20]. The thickness and the doping concentration of the drift region were chosen so that the devices can support a voltage higher than 600 V.

The simulation conditions correspond to a static state: when one section is in the on-state, the other must be in the off-state. A voltage of 600 V is applied and a current of 10 A simulates an ideal load modeled as a current source.

The technological parameters of the insulation area, consisting of an innovative deep trench and a deep P+ well located above this trench, have been chosen to withstand a voltage of 600 V and to prevent any lateral current flow (Fig. 1). These parameters are given in Fig. 1.

A. Buck-type switching cells

Fig. 1a) represents the 2D cross-sectional view of the elementary 3-pole chip of the Buck-type switching cells. Fig. 2 represents the equivalent electrical schematic of this switching cell.

The first validation study on the Buck-type switching cell requires to set the VDMOS in the OFF-state and the diode in the ON-state (Fig. 2a). Fig. 3 gives the corresponding distribution of equipotential lines and current density within the elementary chip. In the cases a) and b), one can notice that the JBS diode is in ON-state and the VDMOS supports the voltage of 600 V. On the other hand, if the VDMOS is ON and the diode is OFF (Fig. 2b), the JBS diode supports a voltage of 600 V (Fig. 3b.1) and the VDMOS carries a current density of 100 A/cm² (Fig. 3b.2). In all cases the maximum electric field peak value inside the structures does not exceed 2.1 MV/cm which is lower than the critical electrical field $E_{cr\text{SiC}} = 2.5$ MV/cm.

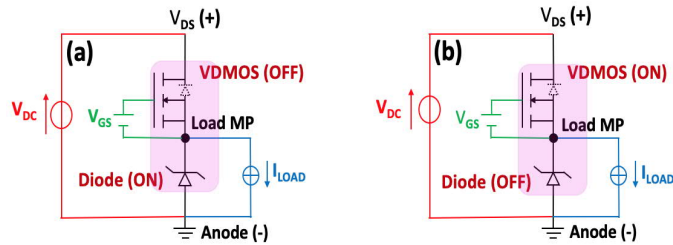


Fig. 2. Equivalent electrical schematic of the 3-terminal Buck-type switching cell at $V_{DC} = 600$ V, $I_{LOAD} = 10$ A, $T_{CASE} = 300$ K: (a) VDMOS in the OFF-state and the diode in the ON-state at $V_{GS} = 0$ V, (b) VDMOS in the ON-state and the diode in the OFF-state at $V_{GS} = 15$ V.

Fig. 4 shows the VDMOS drain-source and gate-source voltage/current waveforms, together with JBS anode-cathode voltage/current waveforms of the Buck-type switching cell. A voltage of 600 V is applied between the MOSFET drain and the JBS anode. A 10A load current is applied between the JBS anode and the midpoint (MP) which is connected to the metal via. An equivalent trapezoidal gate-source voltage was imposed from 0 to 15 V ($V_{gs} > V_{th}$) with a switching time (T_{switch}) of 10 μ s. This time was chosen to ease the convergence of the simulations and to reduce the computation time which resulted four times lower than for a usual switching time of the order of ns. The simulation of the turn-on and turn-off the VDMOS, and the observation of the different electrical parameters within the structure validate the proper functional operation of the Buck switching cell based on the JBS diode and the VDMOS.

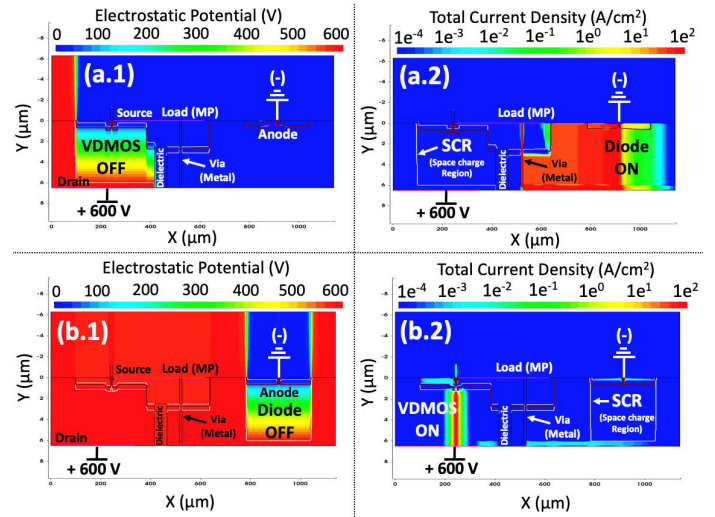


Fig. 3. Equipotential lines and current density distribution in the Buck-type switching cell (X to Y ratio: 30). (a) VDMOS in the OFF-state and the diode in the ON-state: (a.1) equipotential line distribution, (a.2) current density distribution. (b) VDMOS in the ON-state and the diode in the OFF-state: (b.1) equipotential line distribution, (b.2) current density distribution. (Leakage current = 6 μ A) ($E_{max\text{SiC}} = 2.1$ MV/cm)

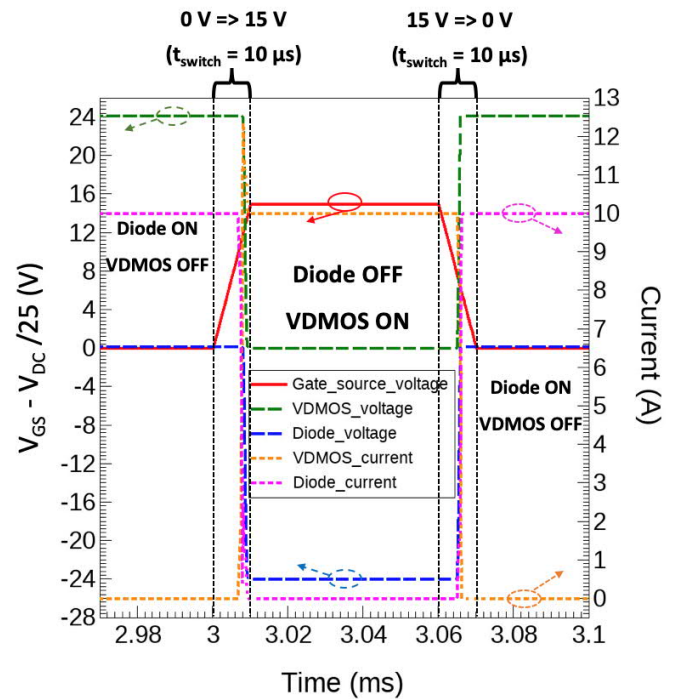


Fig. 4. VDMOS-part and JBS-part switching waveforms of the proposed 3-pole Buck-type switching cell at $V_{DC} = 600$ V, $I_{LOAD} = 10$ A, $V_{GS\text{max}} = 15$ V, $T_{CASE} = 300$ K.

B. Boost-type switching cells

Fig. 1b) represents the 2D cross-sectional view of the elementary 3-terminal chip of the Boost-type switching cell. Fig. 5 shows the simplified equivalent electrical schematics of this switching cell with the biasing conditions at 300 K used for the simulation.

The first validation phase on the 3-terminal Boost-type switching cell requires to put the VDMOS in the OFF-state and the diode in the ON-state (Fig. 5a). According to Fig. 6, which represents the distribution of equipotential lines and the current density in the elementary chip, in the cases a) and b), one can see that the JBS diode is ON and the VDMOS support the desired voltage of 600V. On the other hand, if the VDMOS-part is ON and the diode-part is OFF (Fig. 5b), the JBS is blocked and supports a voltage of 600V (Fig. 6b.1) and the VDMOS carries a current density of 100 A/cm² (Fig. 6b.2). In all cases the maximum electric field peak value does not exceed 2.1 MV/cm which is lower than the critical electrical field $E_{cr SiC} = 2.5$ MV/cm.

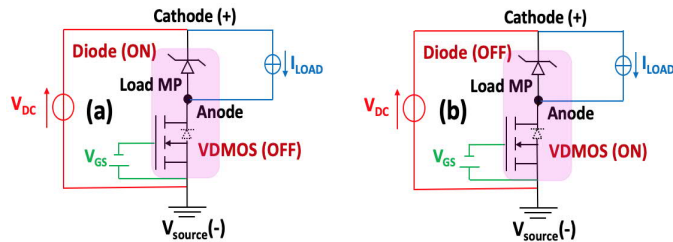


Fig. 5. Equivalent electrical schematic of the 3-terminal Boost-type switching cell at $V_{DC} = 600$ V, $I_{LOAD} = 10$ A, $T_{CASE} = 300$ K: (a) VDMOS in the OFF-state and the diode in the ON-state at $V_{GS} = 0$ V, (b) VDMOS in the ON-state and the diode in the OFF-state at $V_{GS} = 15$ V

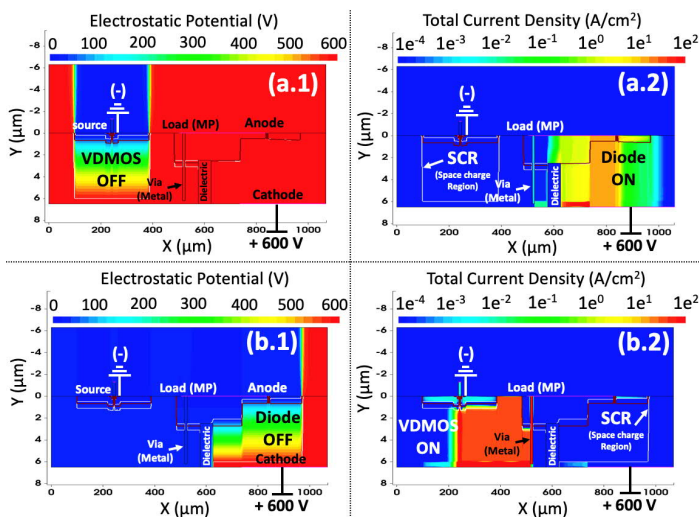


Fig. 6. Equipotential lines and current density distribution in the Boost-type switching cell (X to Y ratio: 30). (a) VDMOS in the OFF-state and the diode in the ON-state: (a.1) equipotential line distribution, (a.2) current density distribution. (b) VDMOS in the ON-state and the diode in the OFF-state: (b.1) equipotential line distribution, (b.2) current density distribution. (Leakage current = 6 μ A) ($E_{max SiC} = 2.1$ MV/cm)

Fig. 7 shows the VDMOS drain-source and gate voltage/current waveforms, together with the JBS anode-cathode waveforms of the Boost-type switching cell. A supply voltage of 600V is applied between the cathode and the source. A 10 A load current is applied between the diode cathode and the midpoint (MP) which is connected to the metal via. An equivalent trapezoidal gate-source voltage was imposed from 0 to 15 V ($V_{gs} > V_{th}$) for a switching time of 10 μ s. As in Buck-

type topology case, $T_{switch} = 10\mu s$ was chosen to facilitate the convergence of the simulations and to reduce the computation time. It can be seen that the proper turn-on then the turn-off the VDMOS, and the observation of the different electrical quantities within the structure validate the correct functional operation of the switching cell based on the JBS diode and the VDMOS for the elementary chip of the Buck-type switching cell.

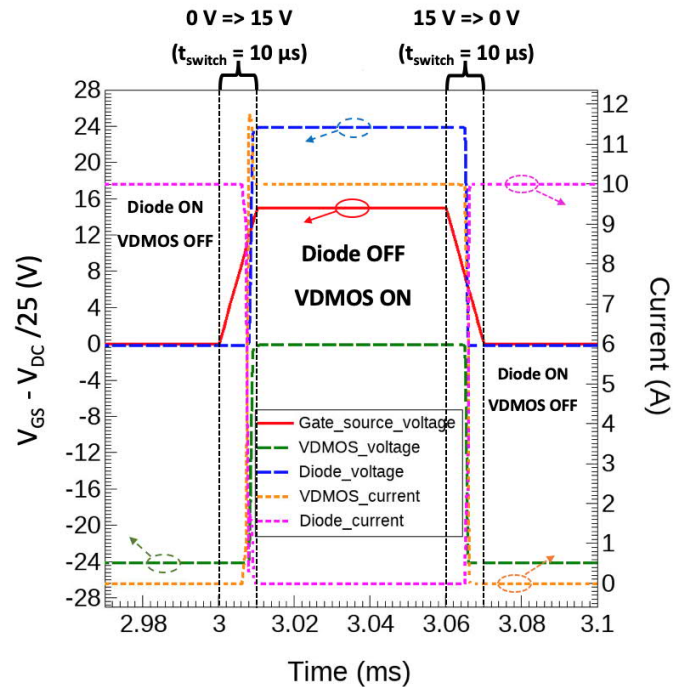


Fig. 7. VDMOS-part and JBS-part switching waveforms of the proposed 3-pole Boost-type switching cell at $V_{DC} = 600$ V, $I_{LOAD} = 10$ A, $V_{GS max} = 15$ V, $T_{CASE} = 300$ K.

IV. TECHNOLOGICAL BRICKS METAL VIA

In this last part, we highlight the major technological step needed to take the electrical contact from the front face through the epitaxial layer down to the substrate, which is essential to obtain the structures schematized in Fig. 1. We need to connect in series the JBS-cathode in back-side with the source-VDMOS in front side which is named load MP in Fig. 1. Therefore, to perform this embedded connection, we need to have conductive metal filling for the via connecting the upper side with the lower side. The metal tube used to fill this via must be compatible with SiC technology.

In previous studies, Ni was already used as a mask for SiC etching, as well as metal for ohmic contact [21-22]. In our work we propose to use Ni both as a mask for SiC etching and to fill the via up to the surface of the wafer. To have a good Ni adhesion on the SiC surface, we relied on our previously reported process using the growth of Pd nanoparticles on the SiC surface before Ni electroplating [23].

A. Fluorinated Plasma Etching

Fluorinated plasma techniques have been employed to etch SiC using SF₆ gasses. In our etching procedure, we combine both reactive ions etching and plasma etching in order to have a high source of ions and to etch SiC deeply. Previous studies have been carried out to investigate the optimum parameters to have high etch rates and smooth etched surface [22]. Relying on these parameters, we used 10 sccm of SF₆ gasses, 1000 W/180W ICP/RIE at a pressure equal to 8 mtorr and a bias equal to -450V. These parameters allow getting higher energetic ions with minimum collision that allow to have a high-etching rate equal to 0.6μm/min avoiding trenching and micromasking.

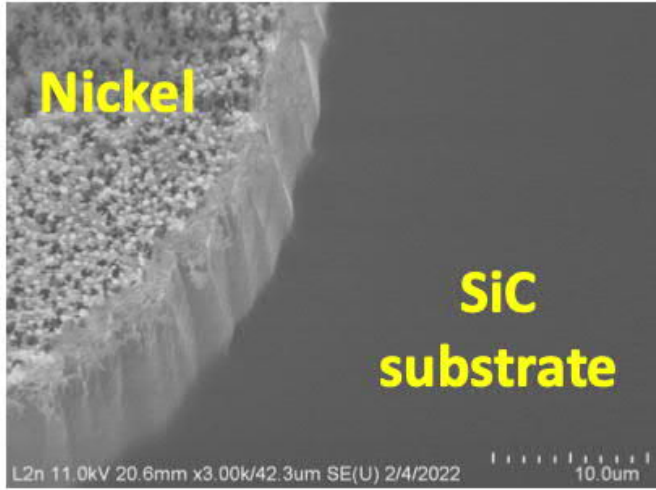


Fig. 8. Scanning electron microscopy (SEM) images of a 10μm thickness SiC substrate etched with Ni mask to perform the metallic via between the back-side cathode JBS-part and the front-side VDMOS-part.

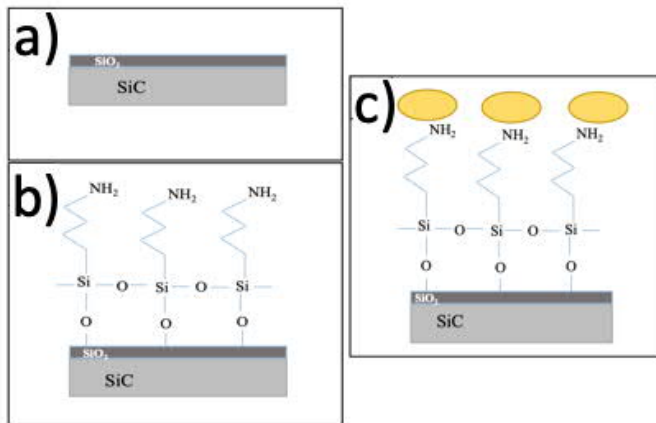


Fig. 9. Electroplating process to fill the via: a) SiO₂ natively presented on SiC, b) APTES functionalized SiC substrate, c) Palladium growth on APTES functionalized SiC.

Fig. 8 shows the scanning electron microscopy image of SiC substrate etched with fluorinated plasma using Ni as a mask, having an etching thickness equal to 10μm.

This fluorinated plasma etching experiment allows us to reach the targeted via we need. Such a via etching need a thick layer of Ni metal, which is not possible to be done by e-beam evaporator. Hence, we used advanced electroplating process in order to investigate the thick Ni deposition on top of the SiC substrate [23].

B. SiC functionalization and Ni electroplating

Aminopropyl triethoxysilane (APTES) was grafted on the SiO₂ thin layer natively present on the SiC surface. The APTES functionalized SiC was covered with a Pd precursor that allows Pd nanoparticles to grow on the surface as already described in our previous work[23] and shown in Fig. 9.

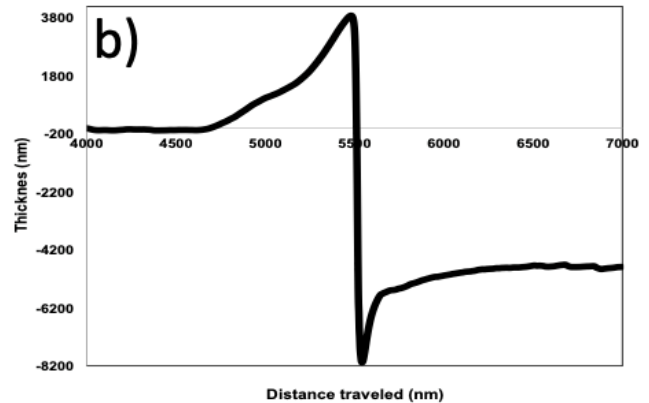
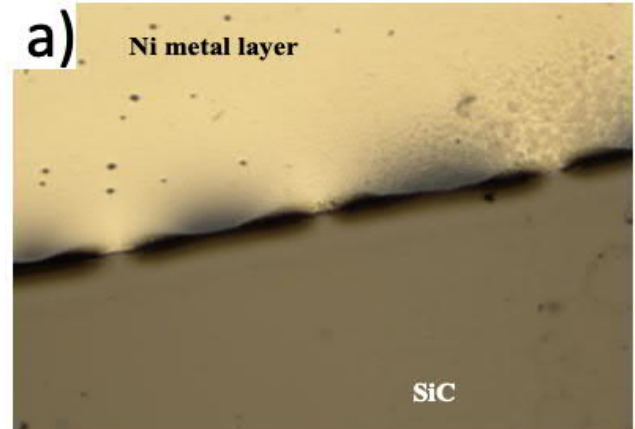


Fig. 10. a) optical image highlights the Ni electroplated layer on the SiC, b) The graph shows the Dektak™ Profiler measurement for the Ni metal layer performed.

After APTES functionalization and the growth of palladium on the surface of the functionalized SiC, a Ni electroplating process was applied. Concretely, the functionalized SiC was electroplated within a Ni sulfamate bath (plating cell from YAMAMOTO-MS™) at a temperature of 50°C and an applied current of 1.56A, the time of electroplating is 15 min.

The palladium treatment of the SiC substrate before Ni electroplating, allows a more compact and rigid Ni layer on the surface of the palladium treated SiC substrate compared to bare SiC substrate [21]. This electroplated Ni thick layer allows us

to have considerable etching depth [23]. In addition, we used this Ni electroplating method in order to obtain a thick layer of Ni metal in the vias.

Fig. 10 a) points out the micrometric layer of electroplated Ni metal layer on palladium activated SiC substrate. Graph in Fig. 10 b) gives out the thickness measurement of the Ni metal layer equal to approximately 5 μ m. This preliminary result allows us to define a process to etch and to fill the via on the surface of the SiC wafer.

V. CONCLUSION

In this paper, a new design perimeter for power switching cells through VDMOS-JBS monolithic vertical integration approach on original multi-terminal SiC power chips is proposed. The operating modes of the 3-terminal Buck-type and Boost-type switching cells were validated using 2D Sentaurus™ mixed-mode simulations. Electrical insulation using a deep trench in the back side and a deep P+ implementation above this trench is introduced. For the embedded metallic via connecting the upper side with the lower side, a nickel electroplating process is suggested. This electrodeposition technique is proposed to have a considerable thickness to fill the via trenching on the upper side and therefore to form the switching cell. The first result shows a Ni metal layer of 5 μ m thick. This promising result allows us to carry-out the etching and filling of the via on the surface of the SiC wafer which is a key technological step to put forward this concept.

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