



HAL
open science

On the Electro-Thermal 2D FEM Parametric Analysis of SiC Vertical Mosfet including Gate-Oxide Charge-Trapping Thermal Dependency. Application for Fast Transient Extreme Short-Circuit Operation

Thibauld Cazimajou, Emmanuel Sarraute, Frédéric Richardeau

► To cite this version:

Thibauld Cazimajou, Emmanuel Sarraute, Frédéric Richardeau. On the Electro-Thermal 2D FEM Parametric Analysis of SiC Vertical Mosfet including Gate-Oxide Charge-Trapping Thermal Dependency. Application for Fast Transient Extreme Short-Circuit Operation. IEEE 30th International Conference Mixed Design of Integrated Circuits and Systems, Institute of Computer Science of AGH University of Science and Technology, Jun 2023, Kraków, Poland. <https://www.mixdes.org/Mixdes3/10.23919/MIXDES58562.2023.10203258> . hal-04147859

HAL Id: hal-04147859

<https://hal.science/hal-04147859v1>

Submitted on 1 Jul 2023

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

On the Electro-Thermal 2D FEM Parametric Analysis of SiC Vertical Mosfet including Gate-Oxide Charge-Trapping Thermal Dependency. Application for Fast Transient Extreme Short-Circuit Operation.

Thibault Cazimajou
LAPLACE
Université de Toulouse,
CNRS, INPT, UPS
Toulouse, France
0000-0003-2650-5421

Emmanuel Sarraute
LAPLACE
Université de Toulouse,
CNRS, INPT, UPS
Toulouse, France
emmanuel.sarraute@laplace.univ-tlse.fr

Frédéric Richardeau
LAPLACE
Université de Toulouse,
CNRS, INPT, UPS
Toulouse, France
frederic.richardeau@laplace.univ-tlse.fr

Abstract—This article proposes a generic and complete electro-thermal 4H-SiC physical Mosfet model. Static and transient in hard short-circuit operation behaviors are successfully performed using 2D Comsol™ software. Influence of fixed charges and traps at the 4H-SiC/SiO₂ interface has been highlighted, both for static and transient. An additional mobility coefficient through Arora's mobility model was then suggested to fully fit the transient model in hard short-circuit operation.

Keywords—Finite Element Simulation, Power Electronics, SiC Mosfet, Oxide trapped-charges, Short-Circuit Operation.

I. INTRODUCTION

Physically, understanding the limits of the use of vertical 4H-SiC Mosfet in extreme operation such as hard short-circuit [1] is a major need in safe and fast protection design for smart gate-driver [2]. For this purpose, deep correlations between the stress parameters applied and the degradation-aging induced are essential. Typically, stress is the fault pulse time applied to the gate and the dissipated energy through the chip. The main physical stresses induced are the maximum current density, the electric field, the power density, and the transient hot spot in the channel region. Then a complete static and transient electro-thermal 2D FEM-type physical model is mandatory to highlight the main correlations. A wide range of voltage, current, and temperature modeling capabilities are also required in extreme operation. Main previous works such as G. Romano *et al.* [3], D. Kim *et al.* [4], and A. Tsibizov *et al.* [5] presented transient 2D electro-thermal models developed in TCAD Sentaurus™ software and specifically used to predict the drain-source current leakage until the parasite-bipolar latch-up events. Unfortunately, such models remain confined to electric and thermal domains. They are also not naturally suitable to be extended in other physics, such as metallurgy and mechanics (Partial excerpts in Sentaurus Interconnect™ tool), typically in strong coupling co-simulation mode. This limitation does not allow studying the electrode melting time / critical energy at high temperatures or the mechanical cracking time / critical energy of the internal-layer-dielectric around the gate, as

discussed by F.Boige *et al.* in [6]. To meet this challenge, authors present the use of Comsol Multiphysics™ software for the first time to implement a generic and complete electro-thermal 4H-SiC Mosfet model from static to transient operation. The proposed model focuses on the channel mobility fit, its dependency on the temperature, and considering the interface defects (fixed charges and trapping). In this submission, static pre-fitting J(V) behavior and transient final-fitting J(t) in hard short-circuit operation were performed in 2D Comsol™ software for the Semiconductor-Thermal embedded Toolboxes. This proposed generic and complete electro-thermal model can handle future multiphysics complex analyses such as metallurgical phase transition and thermo-mechanical stain-stress damage localization. The article is organized as follows: in section II, parametrization and Sentaurus TCAD™ comparison are depicted; in section III, static pre-fitting behavior of the proposed model is presented, including J_{xy} , E_{xy} , and Power density_{xy} maps; and finally, in section IV, transient short-circuit operation is presented, with an adjusted model with experimentation to extract junction temperature and trapped-charges density drift.

II. DEVICE DESIGN AND MODELING

The simulated base component is a 4H-SiC Vertical MOSFET with a planar gate strongly inspired by its geometry and doping of that Romano simulated in [3]. The considered cross-sectional view is shown in Fig. 1, with the parameters described in Table I. In this figure, the semiconductor part in 4H-SiC is divided into an intrinsic zone called thick bulk, of thickness t_{drain} , and a zone of heavily doped epitaxy, of thickness t_{drift} , enabling the depletion and spreading of the field at the imposed voltage across the device. The upper 4H-SiC chip is covered with a 50 nm deposited layer of SiO₂, including the Poly-Si gate finger. A protective layer of SiO₂, called ILD (Internal Layer Dielectric), covers this gate itself. A thin Titanium layer protects the ILD. ILD offers insulation between the gate contact and the source contact made of aluminum.

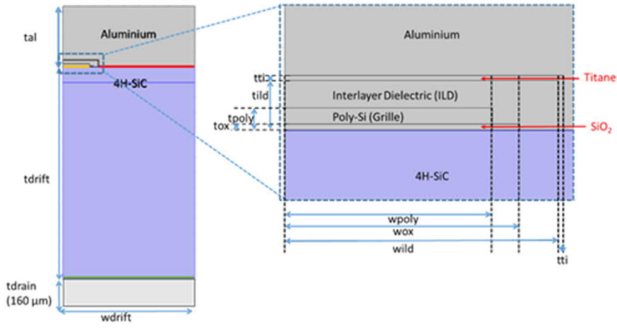


Fig. 1. Schematic 2D cross-sectional view of the simulated device. The values of the geometrical parameters are shown in Table 1. For most studies of semiconductor physics, the gate potential is applied on the orange line above the oxide, the source voltage on the red line, and the drain voltage on the green line. For the thermal study, it is necessary to consider the 160 μm t_{drain} thickness box, and the drain voltage is then applied in the lower part of this box.

TABLE I. GEOMETRIC PARAMETERS

| t_{drift} | 14 μm | w_{drift} | 8.7 μm |
|--------------------|------------------|--------------------|--------------------|
| t_{ox} | 50nm | w_{ox} | 2 μm |
| t_{poly} | 185nm | w_{poly} | 1.77 μm |
| t_{ild} | 416nm | w_{ild} | 2.33 μm |
| t_{ti} | 45nm | w_{al} | 8.7 μm |
| t_{al} | 4 μm | | |

For the study of aspects related to the physics of semiconductors, it has been decided to reduce the study in the epitaxy-layer purple-colored zone in Fig. 1, including the p-well, the inversion channel, and the gate-oxide layer regions. The metal parts are idealized, and the potentials or voltages are directly applied to the colored lines in Fig. 1.

These assumptions make it possible to reduce the calculation time by not considering areas where the physics of semiconductors will not give interesting results. Nevertheless, for the study of the electro-thermal aspects (Section IV), it will be necessary to consider the other zones, in particular the intrinsic bulk zone between the drain contact and the epitaxy layer, which will have an important role to play in the time constant heat diffusion because of its large thickness. On a prospective basis, it will also be important to consider the upper part during the complete study because it is in these zones that the mechanical rupture of SiO_2 is likely to occur, as well as the melting of the source metal and its diffusion within the SiO_2 (not the subject of this article). Additionally, it should be noted that the areas are completely rectangular, which may lead to differences in experience.

Doping regions are then added, following [3]. These regions are illustrated in Fig. 2, with their doping level. Geometric aspects (thickness and width) are detailed in Table 2. An essential parameter to adjust is the junction depth, which makes it possible to affect the Gaussian transition of the doping from one zone to another. Fig. 3 shows the doping profile at the channel level on ComsolTM with two junction depth values (10 nm and 100 nm), as well as a comparison with a doping profile extracted from TCAD SentaurusTM. In order of magnitude, a junction depth of 100 nm seems to be a better choice, and it is therefore the value chosen in this article.

To take physics into account, particular attention was paid to two parameters: mobility in 4H-SiC and defects in the SiC/SiO₂ interface.

Regarding the mobility, Arora's model has been used [3, 4, 7], considering a modification of the mobility with temperature and doping level. Arora's model for electron mobility μ_n as a function of temperature T and total doping N is represented by (1), including some other parameters $\mu_{\text{min},n}$, $\mu_{0,n}$, $N_{0,n}$ and α .

$$\mu_n = \mu_{\text{min},n} + \frac{\mu_{0,n}}{1 + \frac{N}{N_{0,n}}} \quad (1)$$

Parameters $\mu_{\text{min},n}$, $\mu_{0,n}$, $N_{0,n}$, and α are temperature dependent. This is taken into account by (2) in the case of $\mu_{\text{min},n}$.

$$\mu_{\text{min},n} = \mu_{\text{min},n}^{\text{ref}} \left(\frac{T}{T_{\text{ref}}} \right)^{\beta_1} \quad (2)$$

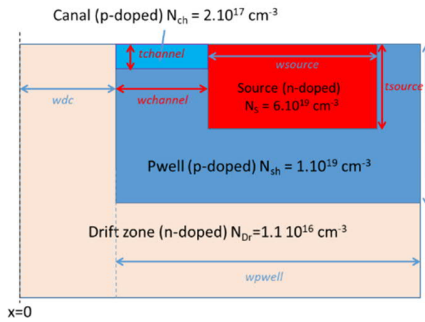


Fig. 2. Schematic 2D cross-sectional view of the simulated device, especially the 4H-SiC part close to the channel. The geometries of the doped areas are shown, with parameters whose values are given in Table 2. Note that the doping in the channel has been changed from 1.9 to 2.0.10¹⁷ cm⁻³ because of a reference problem.

TABLE II. DOPING PARAMETERS

| | w_{dc} | 1.3 μm | |
|----------------------|-----------------|----------------------|--------------------|
| t_{pwell} | 1 μm | w_{pwell} | 7.4 μm |
| t_{source} | 250nm | w_{source} | 1.29 μm |
| t_{channel} | 50nm | w_{channel} | 350nm |

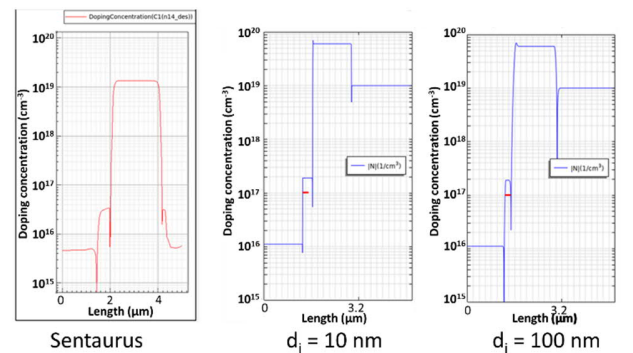


Fig. 3. Doping profile for a reference SiC transistor from SentaurusTM, compared to the doping profile obtained on ComsolTM for the dopings shown in Figure 2, with $N_{\text{ch}} = 1.9.10^{17}$ cm⁻³. The profile on ComsolTM is obtained with two junction depths (10 nm for (b) and 100 nm for (c)). The objective is to show that 100 nm appears more accurate compared to 10 nm.

In these equations, β_1 (resp. β_2, β_3 , and β_4) is the temperature-dependent parameter of $\mu_{\min,n}$ (resp. $\mu_{0,n}$, $N_{0,n}$, and α).

For electrons, it was decided to use the values proposed in [7], i.e., those indicated in Table III.

It is known that this model does not admit the same parameters depending on whether the bulk SiC or the channel is considered. Table III describes the parameters to be used in the case of the Bulk SiC, which can also be utilized to describe the mobility in the epitaxy region. For the part close to the gate oxide, another model must be used [3] with the parameters described in Table IV due to the defects in the SiC/SiO₂ interface. Two 4H-SiC materials were therefore defined in Comsol™, with different mobility parameters (the ones in Table IV for the "channel" domain and those in Table III for the rest of the structure).

It should be noted that the mobility model for the holes in the channel is not considered in a power law, as suggested in [3], but also follows Arora's law which is easier to implement using Comsol™. Because the conduction channel is composed of electrons, this choice of mobility is not supposed to have an impact.

The "channel" 4H-SiC mobility model was applied to a thickness of 7 nm under the oxide, while the "bulk" 4H-SiC was applied to the rest of the semiconductor part. This thickness of 7 nm was chosen so that this model applies to the entire current density crossing the conduction channel. Fig. 4 shows the current density along a vertical cross-section through the channel, showing that this current density can be negligible beyond 7 nm.

Concerning the implementation of the defects of the SiC/SiO₂ interface and volume, it is possible to add in Comsol™ a density of trapped fixed charges localized in the thickness (N_{i0}) and a density of traps at the interface ($N_{it} = N_{\text{trap}}$). This setting is very important on SiC Mosfet, where the local quality and stability of the interface states govern the macro stability of the V_{gsth} . This setting is fully accessible in the Comsol™ Semiconductor toolbox. Based on [3], it was decided to consider a density of positive fixed charges $N_{i0} = 2.68 \cdot 10^{12} \text{ cm}^{-2}$ and a density of traps according to the following characteristics: density of electron acceptor traps $N_{\text{trap}} = 7.10^{11} \text{ cm}^{-2}$ on an energy band of 0.1 eV around a central energy of 0.18 eV defined from E_c .

TABLE III. ARORA'S MOBILITY PARAMETERS FOR ELECTRONS IN BULK 4H-SiC

| | | | |
|-----------------------------|--|-----------|-------|
| $\mu_{\min,n}^{\text{ref}}$ | $0 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ | β_1 | 0 |
| $\mu_{0,n}^{\text{ref}}$ | $947 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ | β_2 | -2.15 |
| $N_{0,n}^{\text{ref}}$ | $1.94 \cdot 10^{17} \text{ cm}^{-3}$ | β_3 | 0 |
| α^{ref} | 0.61 | β_4 | 0 |

TABLE IV. ARORA'S MOBILITY PARAMETERS FOR ELECTRONS IN CLOSE-TO-THE-CHANNEL PART 4H-SiC

| | | | |
|-----------------------------|--|-----------|--------|
| $\mu_{\min,n}^{\text{ref}}$ | $53.92 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ | β_1 | -0.536 |
| $\mu_{0,n}^{\text{ref}}$ | $22.83 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ | β_2 | -2.2 |
| $N_{0,n}^{\text{ref}}$ | $2 \cdot 10^{17} \text{ cm}^{-3}$ | β_3 | 0.72 |
| α^{ref} | 0.76 | β_4 | 0.722 |

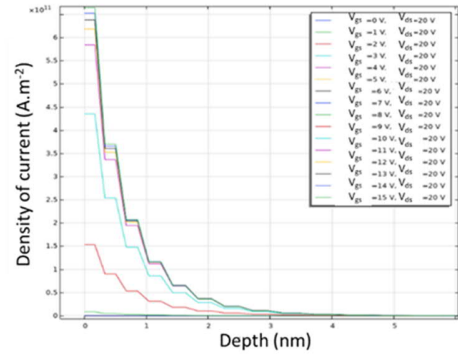


Fig. 4. Current density as a function of depth for a cut positioned approximately in the middle of the channel. It is important to note that the current density is concentrated in the first few nanometers.

III. RESULTS

A. Simulation parameters variation

In this part, it was decided to modify certain parameters of the model and to observe the consistency of its behavior through its current density characteristics = $f(V_{\text{gs}})$ to confirm its validity.

Fig. 5 shows the current density characteristic as a function of the gate voltage for different channel doping density values (from $2 \cdot 10^{17}$ to $8 \cdot 10^{17} \text{ cm}^{-3}$). It is deduced that the increase in channel doping leads to a shift of the characteristics toward positive voltages. This is consistent because increasing the doping in the channel region p-doped makes it more difficult to create an electron channel in this region.

Fig. 6 points out the current density as a function of w_{channel} . It is seen that increasing the channel length leads to an increase in the threshold voltage, as well as an increase in the channel resistance. This is a result that is visible in [8]. This setting is important in SiC Mosfet, where the manufacturer tends to minimize the channel length $< 500 \text{ nm}$ to reduce its contribution to the total R_{dson} at the expense of a higher sensitivity to V_{ds} and a weakening of V_{gsth} , making the transistor less robust.

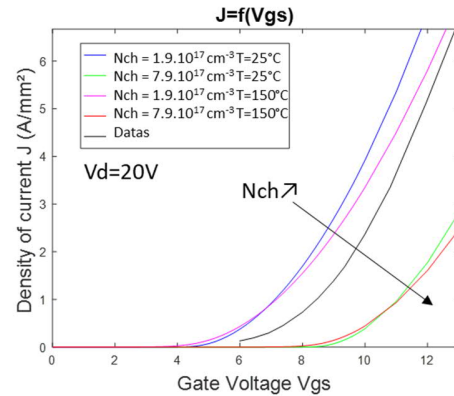


Fig. 5. Characteristic $J = f(V_{\text{gs}})$ for different channel doping values and temperatures, for $V_{\text{ds}} = 20 \text{ V}$ and $d_j = 10 \text{ nm}$. The data (in black) correspond to a case at $25 \text{ }^\circ\text{C}$.

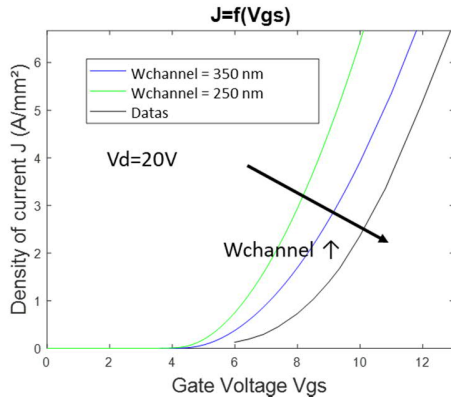


Fig. 6. Characteristic $J = f(V_{gs})$ for different channel width $W_{channel}$ values ($V_{ds} = 20$ V, $d_j = 10$ nm, $N_{ch} = 1.9 \cdot 10^{17}$ cm $^{-3}$, and $T = 25$ °C). The data (in black) correspond to a case at 25 °C.

Fig. 7 shows the current density as a function of the fixed charge density N_{t0} . It is visible that the increase of the fixed charges density leads to a shift of the characteristics towards the negative voltages and, therefore, the decrease of the threshold voltage. If the amount of positive charge at the interface increases, this facilitates the creation of a channel of electrons in the channel, resulting in a decrease in the threshold voltage.

Interestingly, this fixed charge density can be used to fit the simulations to theoretical data at a constant temperature. This dependence of the threshold voltage on the charge concentration can be described in (3).

$$\Delta V_{GsthNt0} = - \frac{qN_{t0}}{C_{ox}} \quad (3)$$

This relation shows the importance of the N_{t0} fixed charges parameter on the linear shift of the threshold voltage to fit the simulated characteristic.

Fig. 8 highlights the current density as a function of the voltage for different trap densities N_{trap} and temperatures.

For a first analysis, it is interesting to study the influence of the density of traps $N_{it} = N_{trap}$ for a constant temperature. The trapped charge density Q_{it} is defined on (4).[9]

$$Q_{it}(T) = -q \int_{E_t}^{E_c} D_{it}(E_t) \cdot f(\psi_s, T) dE_t \quad (4)$$

In this relation, $f(\psi_s, T)$, described in (5), is the occupancy probability and D_{it} is the trap density energy distribution.[10]

$$f(\psi_s, T) = \frac{1}{1 + \frac{n_i}{n_t^2 N_A^{-1} e^{-\psi_s/V_t}} \exp\left(\frac{E_t - E_i}{kT}\right)} \quad (5)$$

ComsolTM offers many options to set D_{it} , especially density of traps (in cm $^{-2}$) and shape of distribution in energy (gaussian, constant, etc). Based on [3], it was decided to consider a density of traps according to the following characteristics : density of electron acceptor traps with a constant distribution in energy band of 0.1 eV around a central energy of 0.18 eV defined from E_c . It is important to notice that D_{it} is proportionnal to N_{trap} .

On Fig. 8, it is visible that the increase in the density of electron acceptor traps leads to a shift of the characteristics toward the positive voltages, and therefore to an increase in the threshold voltage, at constant temperature. The threshold voltage variation can be related to Q_{it} with relation (6).

$$\Delta V_{GsthNtrap} = - \frac{Q_{it}(T)}{C_{ox}} \quad (6)$$

In (4), for a constant temperature, $f(\psi_s, T)$ will not have an influence on the threshold voltage. An increase of N_{trap} will lead to an increase of D_{it} , and therefore a decrease of Q_{it} . Based on (6), this decrease of Q_{it} will lead to an increase of threshold voltage, as observed in Fig. 8.

On Fig. 8, it is visible that the increase in temperature leads to two visible phenomena : a decrease in mobility and a shift in the threshold voltage towards negative voltages. The decrease in mobility can be simply explained by the Arora mobility model used to describe the 4H-SiC. Threshold voltage shift can be explained by the fact the traps are released with the increase in temperature, because of a variation of the occupancy probability (5). This detrapping mechanism will thus results in an increase of Q_{it} (4). Based on (6), this increase of Q_{it} will lead to a decrease of threshold voltage, as observed in Fig. 8.

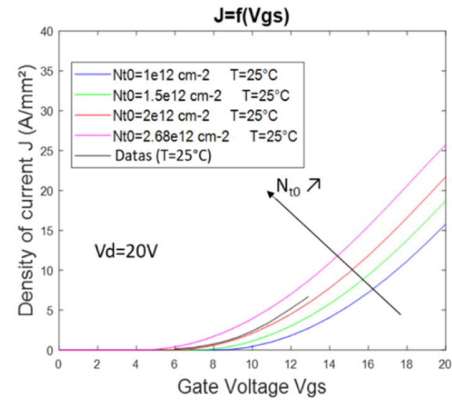


Fig. 7. Characteristic $J = f(V_{gs})$ for different values of N_{t0} , for a $V_{ds} = 20$ V, $d_j = 10$ nm, $N_{ch} = 1.9 \cdot 10^{17}$ cm $^{-3}$, $T = 25$ °C and $N_{trap} = 7.10^{11}$ cm $^{-2}$. The data (in black) correspond to a case at 25 °C.

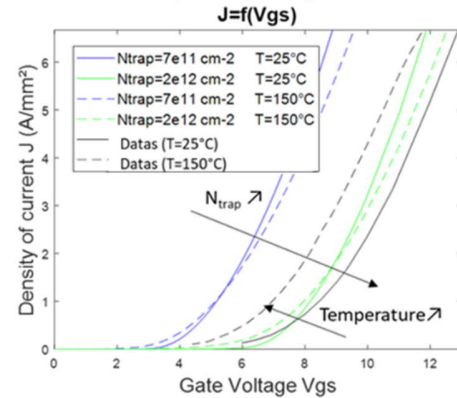


Fig. 8. Characteristic $J = f(V_{gs})$ for different values of N_{trap} and temperature, for $V_{ds} = 20$ V, $d_j = 100$ nm, $N_{ch} = 1.9 \cdot 10^{17}$ cm $^{-3}$, and $N_{t0} = 2.68 \cdot 10^{12}$ cm $^{-2}$.

B. 2D Maps

This part will illustrate 2D maps at different electrical parameters, such as current density and electric field, using only the epi-layer. For future applications in electro-thermal simulations, the bulk heavily doped 4H-SiC area of 160 μm should be considered.

Fig. 9 points out the operating point simulation ($V_{ds} = 600\text{ V}$, $V_{gs} = 20\text{ V}$) in short-circuit mode with 2D maps of the current density (a), the electric field (b), and the power density (c). Power density is obtained with a scalar product of the electric field and the current density. In Fig. 9 (a), it is possible to localize very dense areas in terms of current density, such as the central JFET part of the active cell and the channel (which is extremely thin, as illustrated in Fig. 3). In Fig. 9 (b), an electric field peak at the corners can also be localized. The maximum electric field is $260\text{ V}\cdot\mu\text{m}^{-1}$ in SiC, which remains lower than the breakdown field ($300\text{ V}\cdot\mu\text{m}^{-1}$). Fig. 9 (c) shows the power density in $\text{W}\cdot\text{m}^{-3}$. In this figure, the regions subjected to a high-temperature rise can be localized too. It is thus visible that the central JFET and channel regions of the Mosfet cell are subjected to maximum thermal stress.

It is important to specify here that, if the simulated device has characteristics close to the operation of the real device, it is visible that it would be possible to adjust I-V characteristic threshold voltage for different temperatures based on relation (7)

$$\Delta V_{Gsth} = \Delta V_{Gsth_{init}} + \Delta V_{Gsth_{NtO}} + \Delta V_{Gsth_{Ntrap}} \quad (7)$$

Based on (3) and (6), N_{tO} and N_{trap} can be used to adjust respectively $\Delta V_{Gsth_{NtO}}$ and $\Delta V_{Gsth_{Ntrap}}$. Especially, N_{trap} can be used to fit the variation of threshold voltage with the increase of temperature, and N_{tO} can be used to fit the threshold voltage at a constant temperature. For the simulation of the transient behavior, it was decided to keep the parameters N_{tO} and N_{trap} as defined in [3].

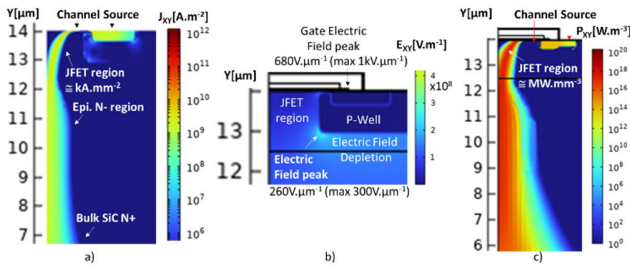


Fig. 9. 2D maps obtained for $V_{ds} = 600\text{ V}$ and $V_{gs} = 20\text{ V}$ of (a) current density, (b) electric field, and (c) power density.

IV. TRANSIENT

Finally, an analysis of the transient evolution of the drain-source current in the device under short-circuit conditions have been conducted. Simulations were performed in the strong coupling, with a temperature rise fed by the heat source, which physically corresponds to the map of the power density (as in Fig. 9 (c)). A temperature of $25\text{ }^\circ\text{C}$ is imposed at the back side, giving an initial thermal condition. The voltage V_{ds} is constant and maintained at 600 V , while a voltage step V_{gs} is applied from

0 to 21 V . This voltage step follows a specific profile, which still needs improvement.

Fig. 10 highlights the transient current function from the simulated device compared to experimentation. It is visible that a first phase increase follows the voltage V_{gs} step, then a second phase of decrease is governed by the reduction in mobility itself caused by the increase in temperature. If the current increase phase can be well followed, it is visible that the current decrease over time is much sharper in the experimentation than in the simulations.

To correct this, it was decided to adapt the mobility model so that it decreases more rapidly with the increase in temperature. For achieving that, a dedicated additional mobility model paralleled with the basic Arora's mobility model is suggested in (8). This one uses a power law temperature dependence as defined in (9).

$$\frac{1}{\mu_{total}} = \frac{1}{\mu_{power}} + \frac{1}{\mu_{Arora}} \quad (8)$$

$$\mu_{power} = \mu_{0,pl} \left(\frac{T}{T_{ref}} \right)^{\alpha_{PLM}} \quad (9)$$

For the bulk SiC, parameters of Arora's model from Table III have been kept. $\mu_{0,pl}$ and α_{PLM} have been chosen to obtain a μ_{power} term negligible compared to the μ_{Arora} term.

The power model mobility parameters described in [3] have been re-used for channel holes. Parameters of Arora's model of mobility have been chosen to obtain a μ_{Arora} term negligible compared to the μ_{power} term. For electrons in the channel, parameters of Arora's model of Table IV have been kept. Parameters $\mu_{0,pl}$ and α_{PLM} can be tuned for the additional power model to reproduce the experimental data. Adjusting the α_{PLM} parameter makes modifying the mobility attenuation with temperature. Fig. 11 shows the evolution of the current and the maximum junction temperature extracted as a function of time for different values of α_{PLM} . Thus, it is possible to fit the experimental data with the simulations with limited parameters and to provide an useful practical and physical chip thermal diagnosis for SOA analysis.

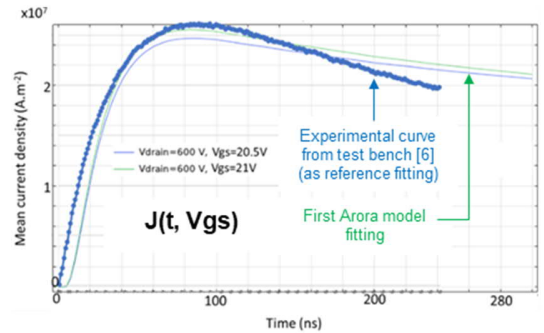


Fig. 10. Temporal response of the current density with the simulations (green and blue lines) and for the experimental data (blue dots), for $V_{gs} = 20\text{ V}$. First, the current density increases due to the increase in V_{gs} (t) from 0 to 21 V . In the second step, due to the temperature increase, the mobility decreases in the transistor and decreases the current density.

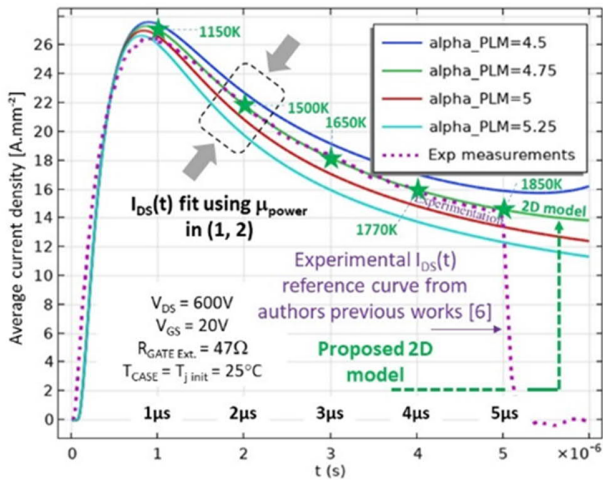


Fig. 11. Evolution of current and maximum junction temperature as a function of time for different values of α_{PLM} for $\mu_{0,PL} = 4000 \text{ cm}^2 \cdot \text{V}^{-2} \cdot \text{s}^{-1}$

In [11], the authors have recently extended the proposed model to simulate the transient metallurgical melting of the aluminum source electrode during the short-circuit, allowing finer and more realistic analysis which are unattainable by experimentation alone. In [12], the authors also extended the model for preliminary transient thermomechanical analysis purposes of the gate-region.

Finally, the N_{iO} and $N_{it} = N_{trap}$ charges densities values are analyzed in correlation with the current density $J(t)$ shape using the modeling depicted in section III. A). In Fig. 12 a), the higher the value of N_{iO} , the higher all the curve envelope because V_{gsth} is decreasing as pointed out in Fig. 7. In Fig. 12 b), the higher the value of N_{trap} , the lower the curve's peak because V_{gsth} is increasing as shown in Fig. 8 and also reported in [13]. In this last case, due to the temperature increase, the electrons de-trapping mechanism leads to a V_{gsth} increase saturation and therefore a quasi-convergent shape curves over a long-time short-circuit pulse. Practically, we can conclude that the N_{it} monitoring obtained by a regular retro-fitting between the proposed model and experimentation could offer an innovative and interesting health status of the SiC Mosfet oxide.

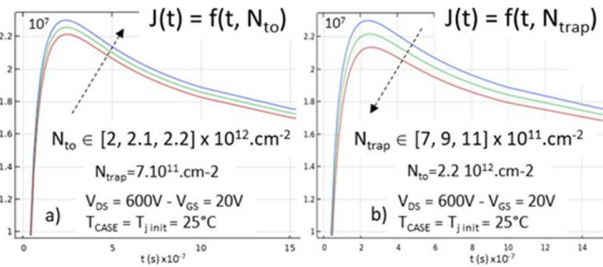


Fig. 12. Charges densities effect on $J(t)$ shape, (a) N_{iO} , (b) N_{it} .

V. CONCLUSION

This article proposes a generic and complete electro-thermal 4H-SiC physical Mosfet model. Static $J_{ds}(V_{gs})$ behavior and transient final-fitting $J_{ds}(t)$ in hard short-circuit operation were successfully performed using 2D Comsol™ software and, for the first time, the Semiconductor - Thermal embedded Toolboxes.

Fixed charges and charges-trapping / de-trapping could be used to pre-fit V_{gsth} thermal dependency in static mode. An additional mobility coefficient through Arora's mobility model was then introduced to fully fit the transient model in hard short-circuit operation. Such a model can now handle for temperature extraction, SiO₂/SiC trapped-charges drift, oxide health-monitoring and future multiphysics complex analyses such as metallurgical phase transition and thermo-mechanical stress damage localization.

ACKNOWLEDGMENT

Many thanks to Dr. Mustafa Shqair, a post-doctoral fellow at Lab. Laplace, for his help in the scientific presentation of the text of this article and for his contribution to the continuation of the work described in this article. We also thank our fellow researchers, Dr. Abdelhakim Bourenane and Dr. Amirouche Oumaziz at Laas-CNRS, for allowing us to perform comparison steps between Comsol™ and Sentaurus™.

REFERENCES

- [1] A. Castellazzi *et al.*, "Transient out-of-SOA robustness of SiC power MOSFETs," *2017 IEEE International Reliability Physics Symposium (IRPS)*, 2017, pp. 2A-3.1-2A-3.8, doi: 10.1109/IRPS.2017.7936255.
- [2] M. Wang *et al.*, "A Smart Gate Driver for SiC Power MOSFETs with Aging Compensation and Ringing Suppression," *2021 33rd International Symposium on Power Semiconductor Devices and ICs (ISPSD)*, Nagoya, Japan, 2021, pp. 67-70, doi: 10.23919/ISPSD50666.2021.9452261.
- [3] G. Romano *et al.*, "A Comprehensive Study of Short-Circuit Ruggedness of Silicon Carbide Power MOSFETs," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 978-987, Sept. 2016, doi: 10.1109/JESTPE.2016.2563220.
- [4] D. Kim, A. J. Morgan, N. Yun, W. Sung, A. Agarwal and R. Kaplar, "Non-Isothermal Simulations to Optimize SiC MOSFETs for Enhanced Short-Circuit Ruggedness," *2020 IEEE International Reliability Physics Symposium (IRPS)*, Dallas, TX, USA, 2020, pp. 1-6, doi: 10.1109/IRPS45951.2020.9128324.
- [5] A. Tsubizov, I. Kovačević-Badstübner, B. Kakarla and U. Grossner, "Accurate Temperature Estimation of SiC Power mosfets Under Extreme Operating Conditions," in *IEEE Transactions on Power Electronics*, vol. 35, no. 2, pp. 1855-1865, Feb. 2020, doi: 10.1109/TPEL.2019.2917221.
- [6] F. Boige *et al.*, "Investigation on damaged planar-oxide of 1200V SiC power MOSFETs in non-destructive short-circuit operation," *Microelectronics Reliability*, Volumes 76–77, 2017, Pages 500-506, <https://doi.org/10.1016/j.microrel.2017.06.085>.
- [7] M. Huang *et al.*, "Determining 4H silicon carbide electronic properties through combined use of device simulations and metal-semiconductor field-effect-transistor terminal characteristics", *Journal of Applied Physics*, Vol. 84, No. 4, Aug. 1998.
- [8] K. Tachiki *et al.*, "Estimation of Threshold Voltage in SiC Short-Channel MOSFETs." *IEEE Transactions on Electron Devices* 65 (2018): 3077-3080.
- [9] G. D. Licciardo, S. Bellone and L. Di Benedetto, "Analytical Model of the Forward Operation of 4H-SiC Vertical DMOSFET in the Safe Operating Temperature Range," in *IEEE Transactions on Power Electronics*, vol. 30, no. 10, pp. 5800-5809, Oct. 2015, doi: 10.1109/TPEL.2014.2376778.
- [10] Y. Zhou, H. Liu, S. Mu, Z. Chen and B. Wang, "Short-Circuit Failure Model of SiC MOSFET Including the Interface Trapped Charges," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 8, no. 1, pp. 90-98, March 2020, doi: 10.1109/JESTPE.2019.2939877.
- [11] E. Sarraute *et al.*, "Transient Thermal 2D FEM Analysis of SiC Mosfet in Short-Circuit Operation Including Solidus-Liquidus Phase Transition of the Aluminum Source Electrode," *EuroSimE 2023*, Graz, Austria, doi: 10.1109/EuroSimE56861.2023.10100775
- [12] M. Shqair *et al.*, "Thermo-Mechanical and Metallurgical Preliminary Analysis of SiC Mosfet Gate-Damage Mode under Short-Circuit based on a Complete Transient Multiphysics 2D FEM model," *ESREF 2023*, Toulouse, France (to be published in October 2023).
- [13] C. Unger *et al.*, "A Comparison of the Transient Behavior of the Drain Current Hysteresis in SiC-MOSFETs," *ESARS-ITEC 2018*, Nottingham, UK, 2018, pp. 1-5, doi: 10.1109/ESARS-ITEC.2018.8607785.