

Improvement of the thermal performance of printed circuit boards by embedding of graphite heat spreaders

IMAPS-THERMAL

Ahmed Sabry AHMED, Rémi PERRIN and Guillaume LEFEVRE (Mitsubishi Electric)

Cyril BUTTAY (AMPERE) and Jacques JAY (CETHIL)

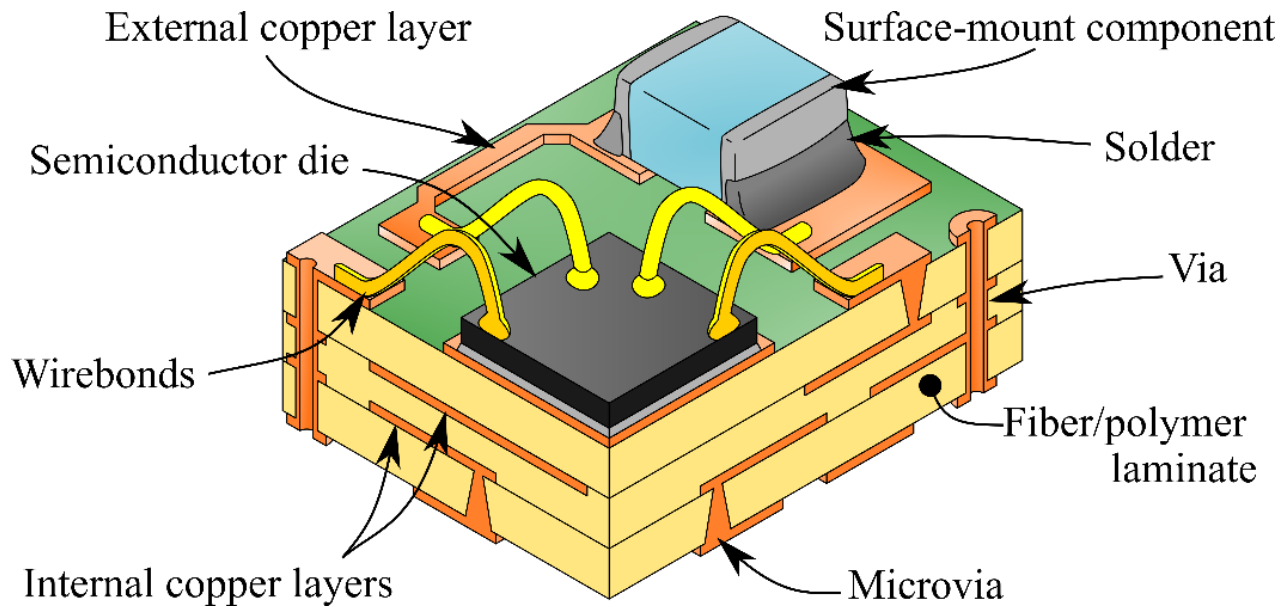
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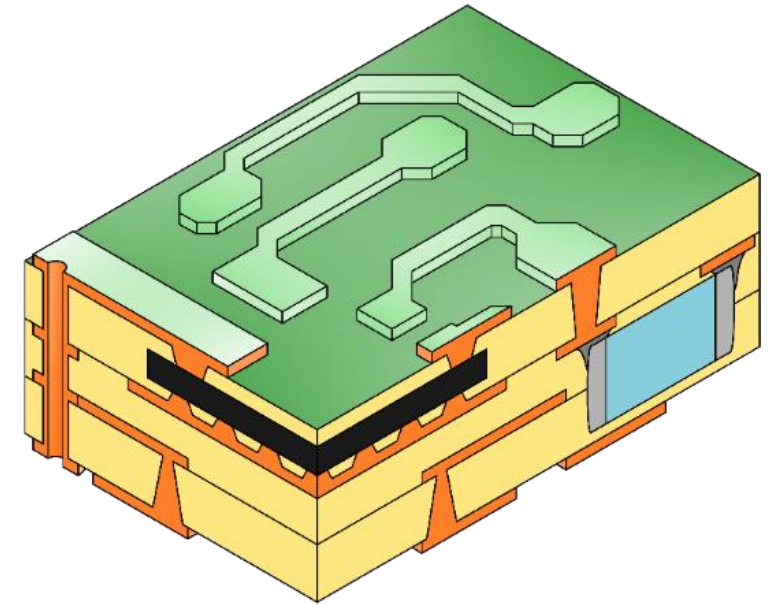
- Introduction to PCB embedding technology.
- Structure optimization of a graphite heat spreader for PCB.
- Experimental validation.
- Conclusion.

1

Introduction to PCB embedding technology



→
PCB embedding process



Printed Circuit Board (PCB) provides :

- Electrical connections
- Mechanical support.

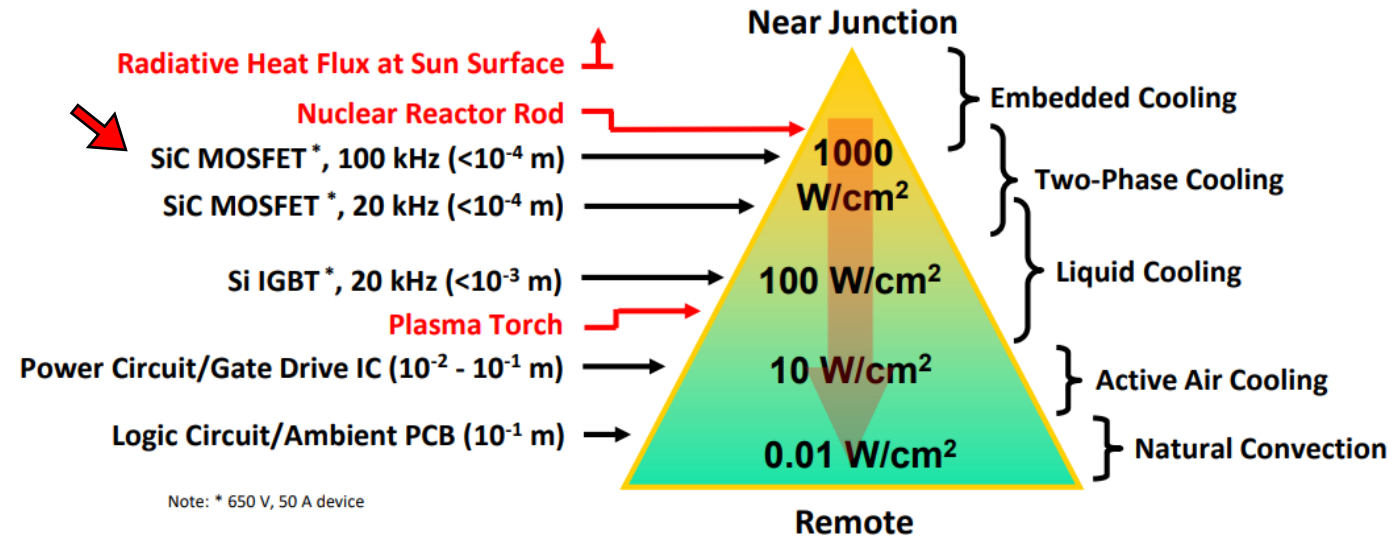
for electrical components of an electrical circuit to achieve certain function.

PCB embedding :

- Electrical benefits since it reduces circuit parasitics.
- Simplifying device packaging.
- Producing more compact systems.
- Thermal challenges due to compactness.



ROHM SiC die size shrinkage leading to high power loss density



Note: * 650 V, 50 A device

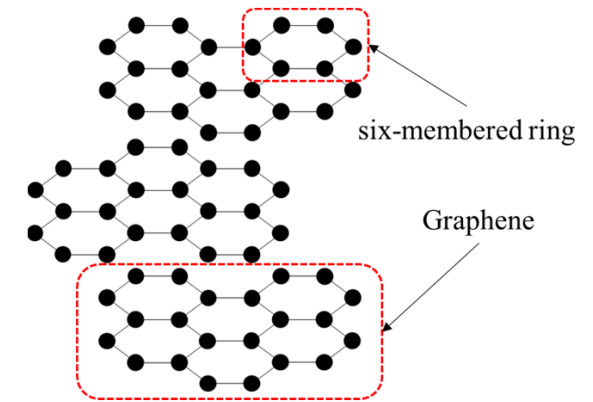
Thermal challenges :

- Reduction of semiconductor die size → Higher power loss density.
- Increasing power density in a PCB → High junction temperature.
- Poor thermal conductivity of dielectric materials → High thermal resistance.

➤ Need for an efficient heat spreader closer to the power die and compatible with PCB process.

Possible materials for the heat spreader:

- Copper → Conventional heat spreader
→ Good thermal conductivity 400 W/(m K).
- Diamond → 2000 W/(m K) isotropic thermal conductivity.
→ Very expensive.
- Graphite → Orthotropic → 2000 W/(m K) (in-plane); 15 W/(m K) (cross-plane).
→ Inexpensive.
→ Available in sheet form.
→ Electrically conductive.

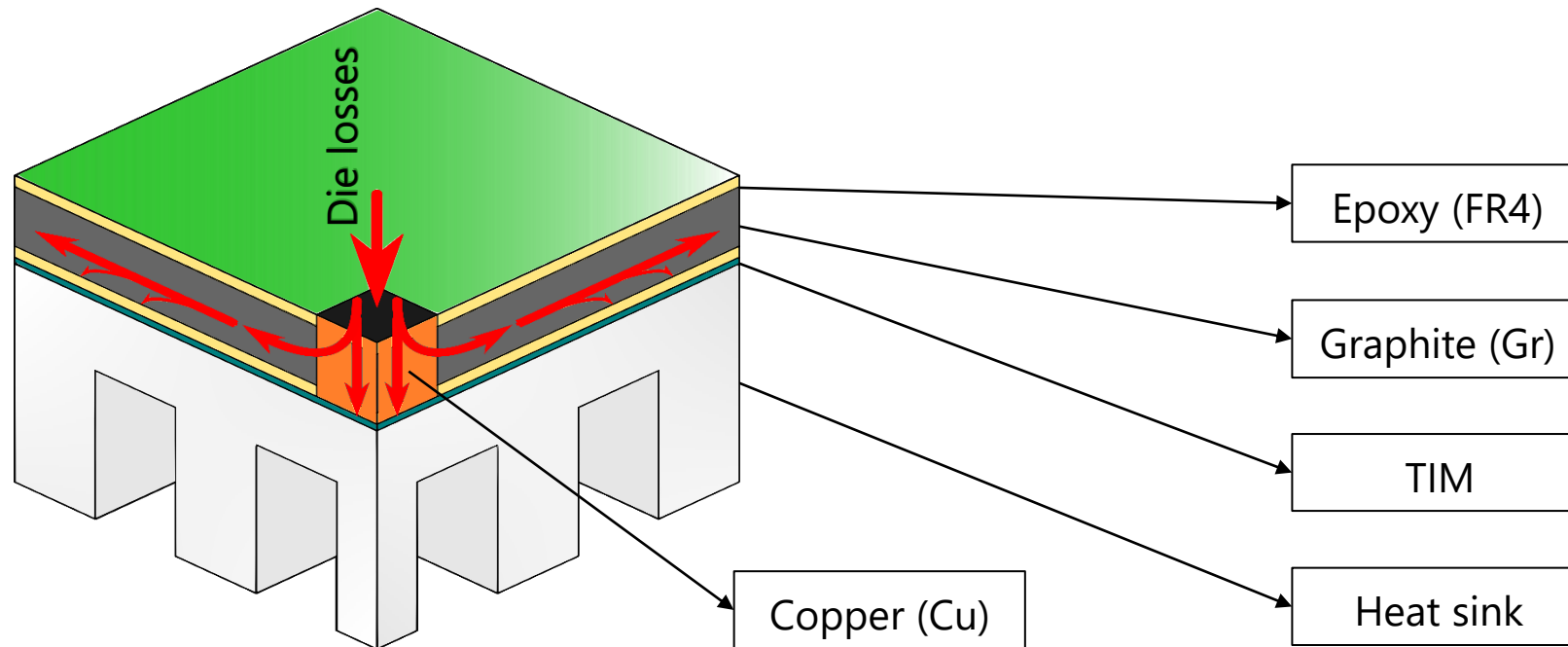


Crystal layered structure of Graphene with high in plane thermal conductivity [Fukunaga 2021]

- Graphite offers high thermal performance as well as sheet form suited to PCB lamination process.
- Can graphite be used as an embedded heat spreader in PCB ??

2

Structure optimization of a graphite heat spreader for PCB



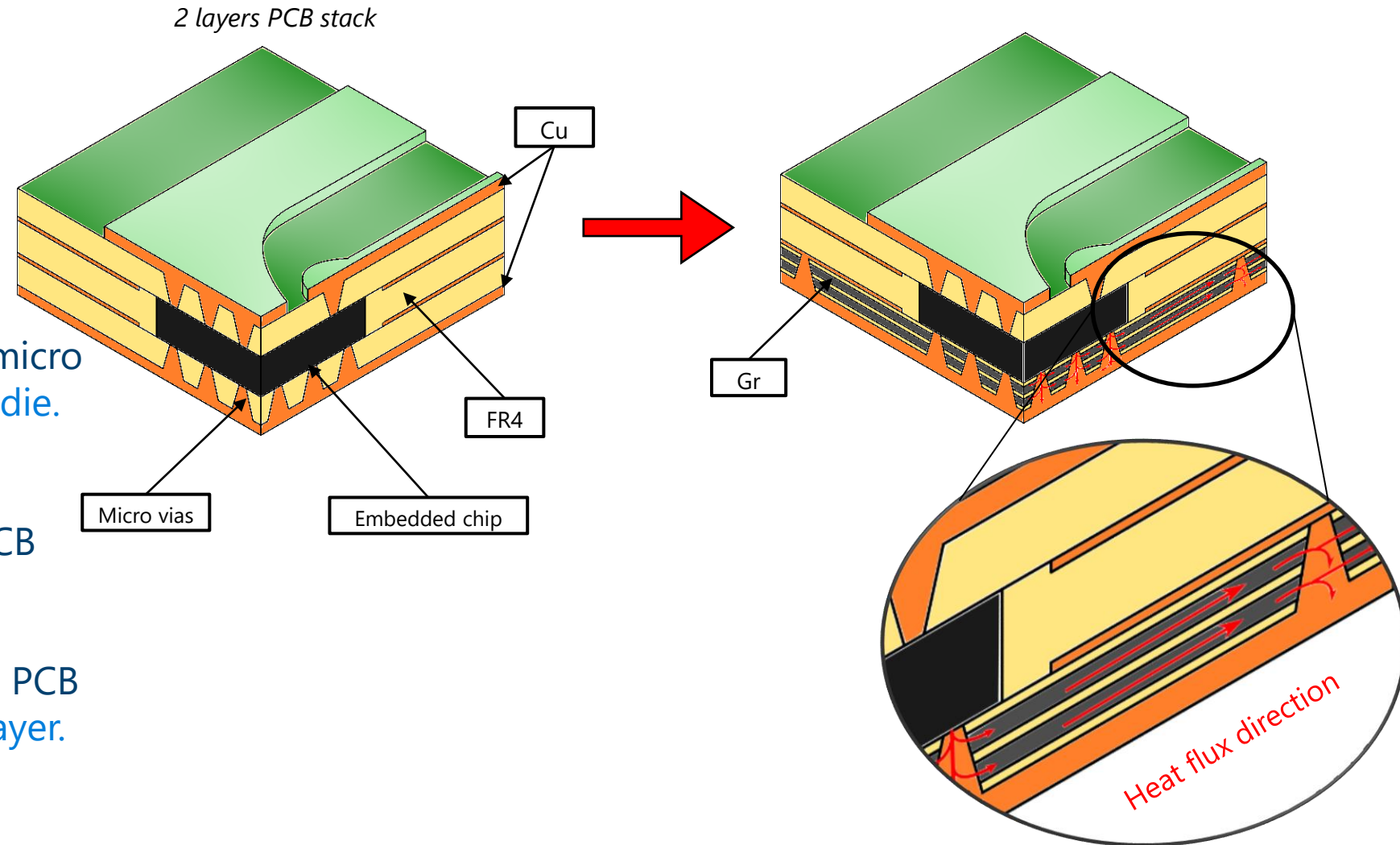
How to take advantage of the graphite in a PCB structure?

- Graphite is embedded in a PCB stack to improve heat spreading **near the die**.
- Lower thermal resistance path is offered for the heat:
 - Horizontally through graphite.
 - Vertically through copper.

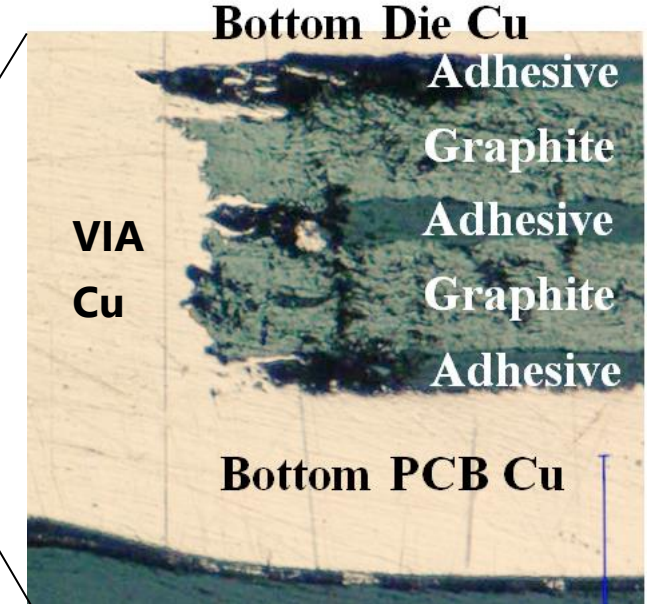
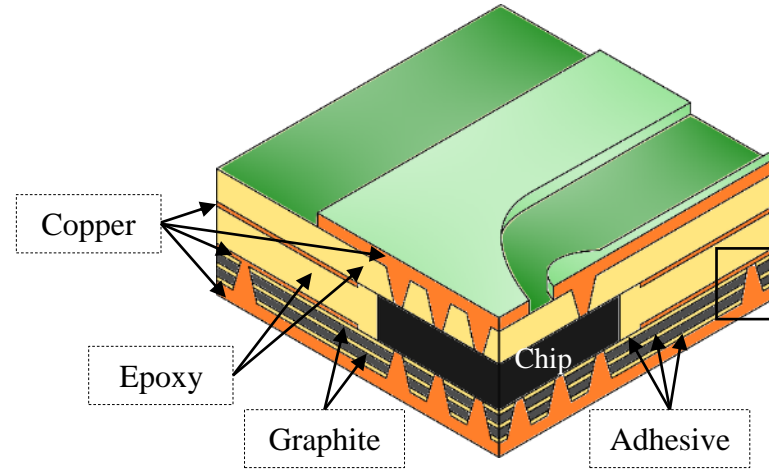
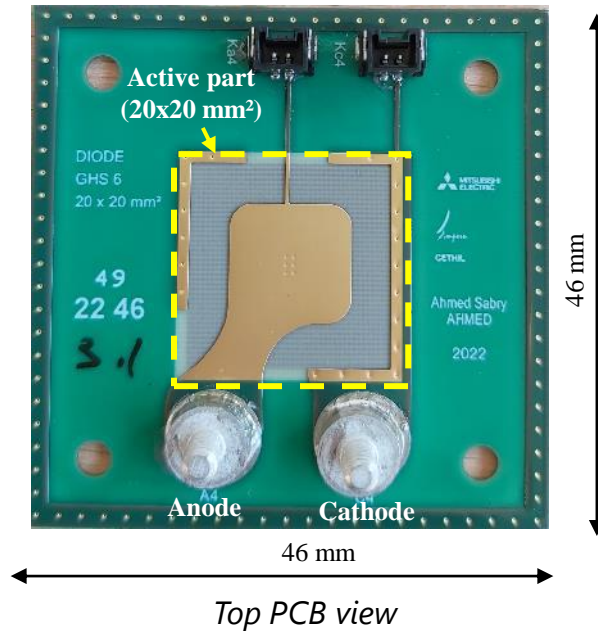
➤ **Graphite heat spreader near the die offers a horizontal heat path adding to the vertical one.**

The proposed PCB stack:

- 2 layers structure with laser micro via → Graphite closer to the die.
- Copper pillar is difficult to manufacture with classical PCB process. → Micro vias
- Graphite layers lamination in PCB stack → Need for adhesive layer.



➤ 2 layers PCB stack with near the die graphite embedding and laser-drilled micro via is chosen.



Cross section picture of the fabricated stack

Details of the PCB stack:

- Micro vias were laser-drilled → Electrical connection to the chip & Vertical thermal path for the dissipated heat.
- Adhesive layer interleaved with graphite → Compatibility with PCB process & structure stability.
- Via electrodeposition → Direct copper to graphite contact for optimal horizontal heat path.

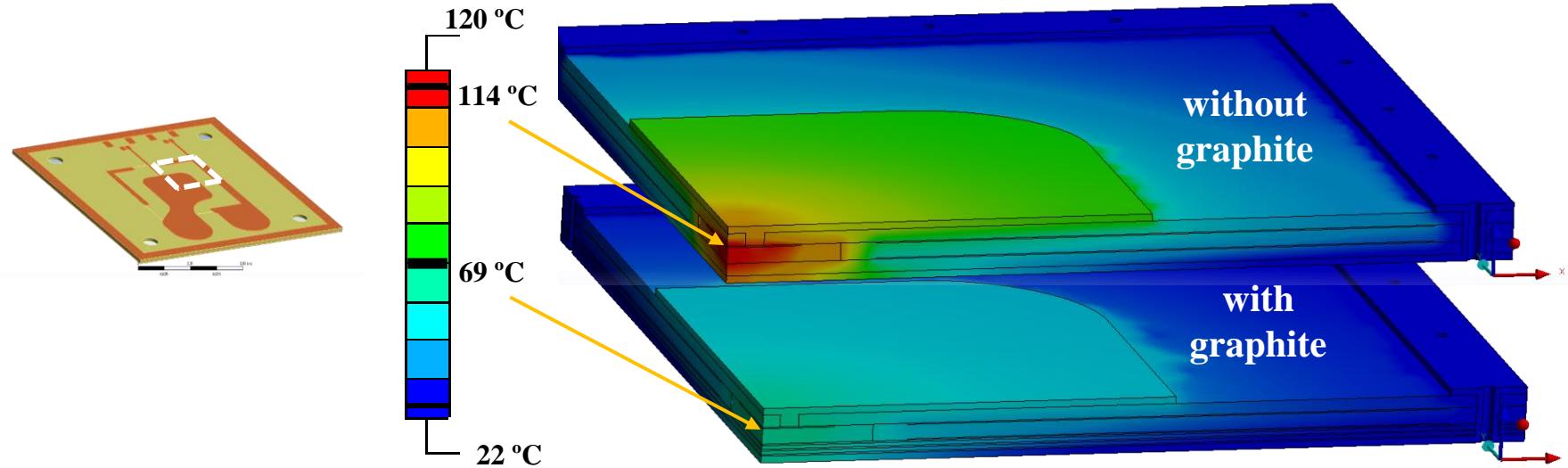
➤ **PCB samples with embedded SiC chips and graphite were successfully fabricated with classical PCB manufacturing process steps.**

2.4

FEM Simulation results of RthJA

Location	Boundary condition
Die power loss	20 W
Top surfaces	10 W/(m ² .K)
Bottom surface	5000 W/(m ² .K)

Material	Thermal conductivity
SiC	300 W/(m.K)
Cu	385 W/(m.K)
FR-4	0.3 W/(m.K)
Adhesive	0.22 W/(m.K)
Graphite	1300(XY),15(Z) W/(m.K)



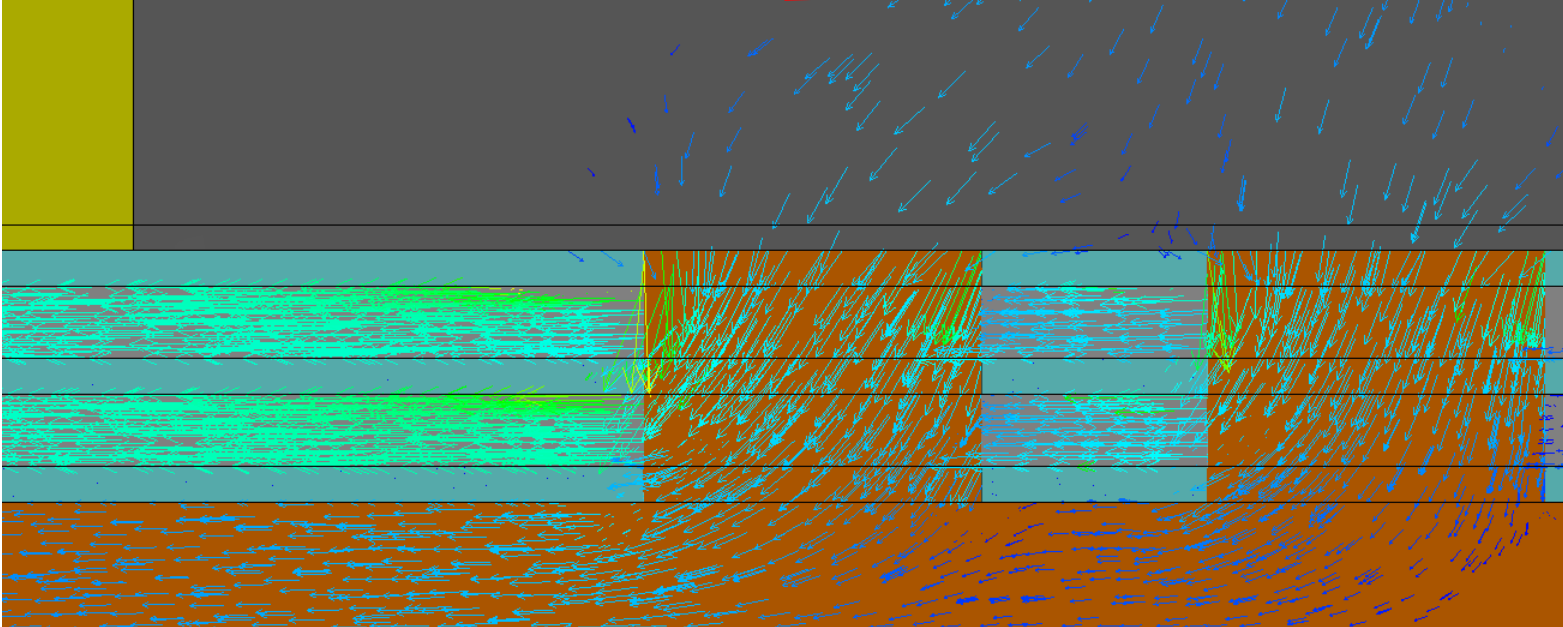
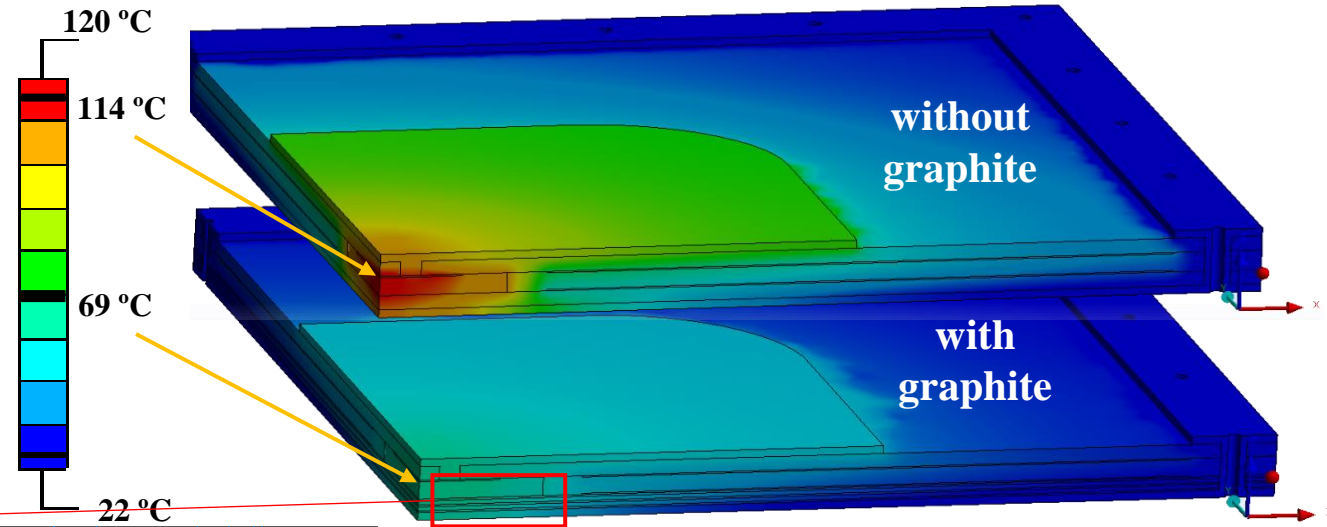
FEM thermal simulation provides confirmation of the thermal behavior:

- Only a quarter was considered to reduce calculation time by 1/5 ratio.
- Junction to ambient thermal resistance $\rightarrow R_{thJA} = \frac{T_{max} - 22^{\circ}C}{Power}$

➤ **49 % reduction in RthJA by embedding two graphite sheets**

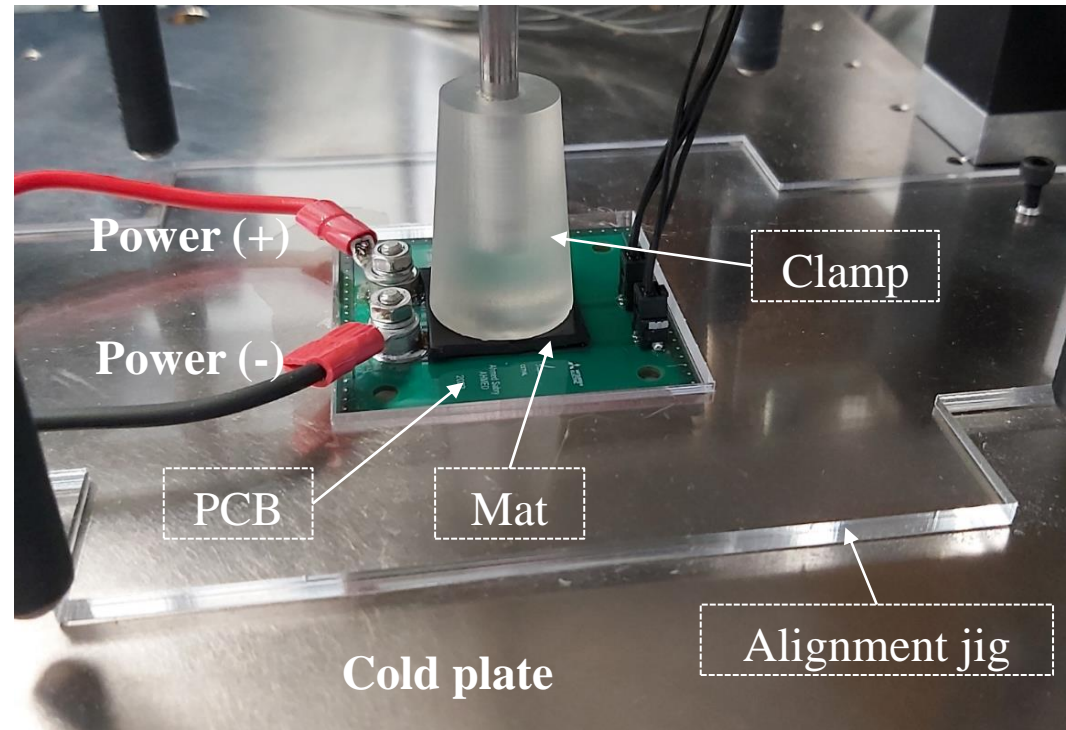
Sample Type	RthJA
Without Graphite	4.6 °C/W
With Graphite	2.3 °C/W

Heat flow vector direction figure shows that heat spreads vertically through copper vias and horizontally through graphite layers to achieve **more heat spreading** and **less thermal resistance**.



3

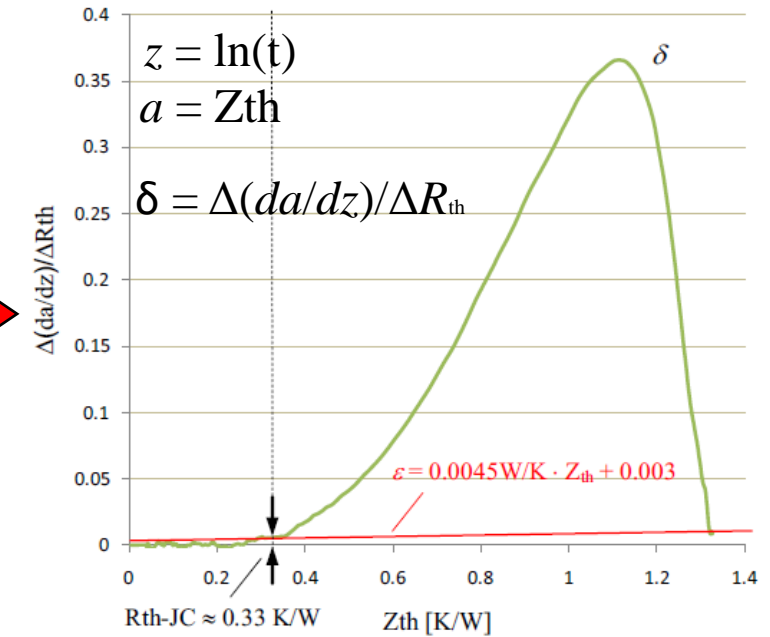
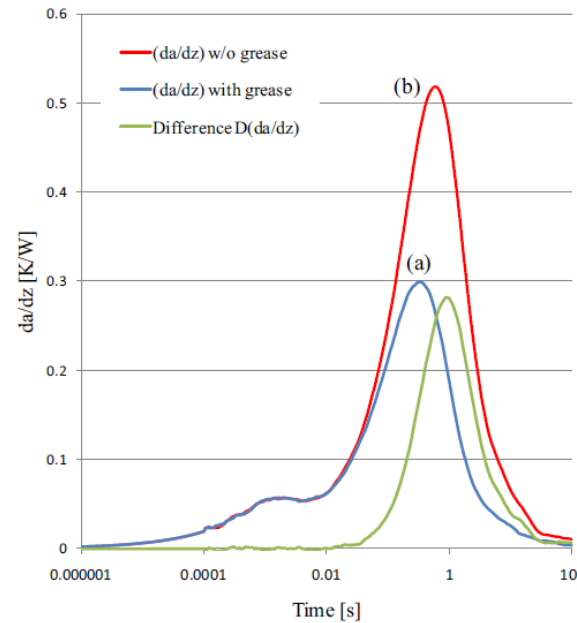
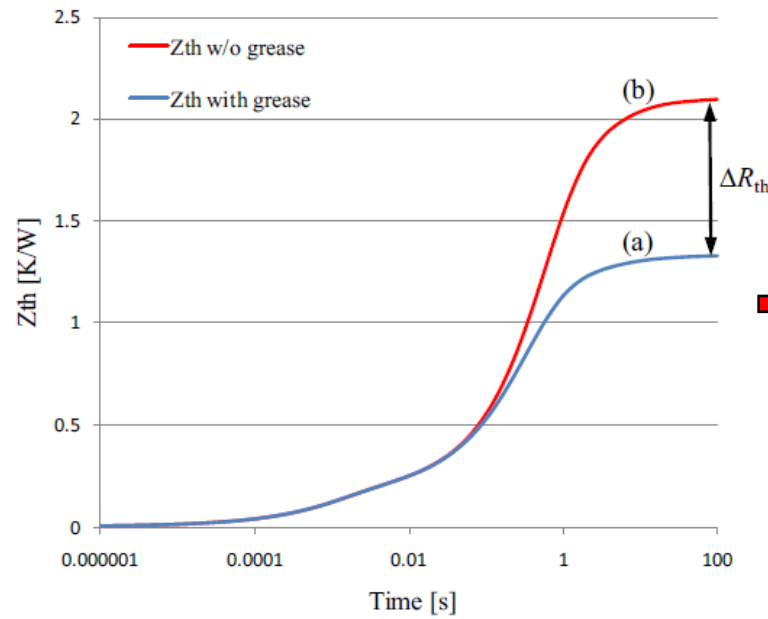
Experimental validation



Experimental test setup for thermal resistance measurements.

Experimental setup characteristics :

- The diode is first calibrated in an oven → Relation between T_j and the measured voltage (TSEP: thermal sensitive electrical parameter).
- The sample is clamped on a cold plate with a pressure of 1.8 bar → ensure good contact with baseplate
- A thermal interface material (TIM) is placed between the sample and the cold plate.
- A mat between the PCB and the clamp → Homogenous distribution of the pressure on the thin PCB sample.



RthJC calculation procedure. [Dirk Schweitzer, 2011]

Thermal dual interface method:

- TDIM is used to determine R_{thJC} following JEDEC51-14 standard → TDIM method has an accuracy within $\pm 20\%$. [Dirk Schweitzer, 2011]
- Two heating curves are obtained by using two TIMs of two different thermal resistances.
- R_{th} is determined by calculating the intersection point of δ and ϵ .

➤ **TDIM method is not ideal for low R_{th} packaging but offer a reference point for comparison between packages.**

3.3 Measurement of RthJC using TDIM: reference sample

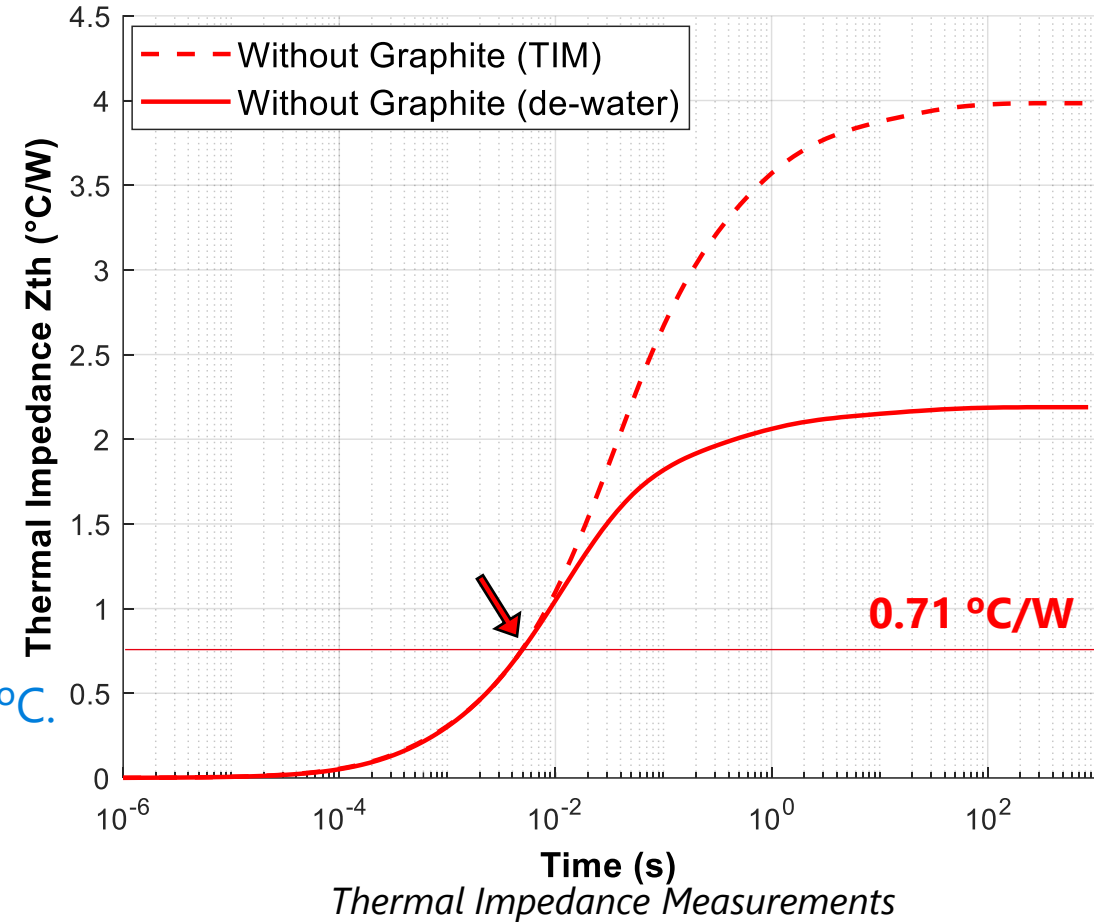


Experimental test conditions:

- The cold plate is cooled by water with an inlet temperature of 23.5 °C.
- At steady state, $R_{thJA} = Z_{thJA}$
- Applied power:
 - (Sil-Pad® 1500ST) → 11 W (without graphite)
 - (Sil-Pad® 1500ST) → 16 W (with graphite)
 - (De-water) → 20 W (without graphite)
 - (De-water) → 24 W (with graphite)

In order to keep maximum junction temperature @70 °C.

TIM	k (W/m.K)	Thickness
Sil-Pad® 1500ST	1.8	0.2 mm
Deionized water (3 drops)	0.58	<< 0.2 mm



➤ By Using TDIM method → $R_{thJC} = 0.71 \text{ °C/W}$ (without graphite)

3.3 Measurement of RthJC using TDIM: Graphite sample

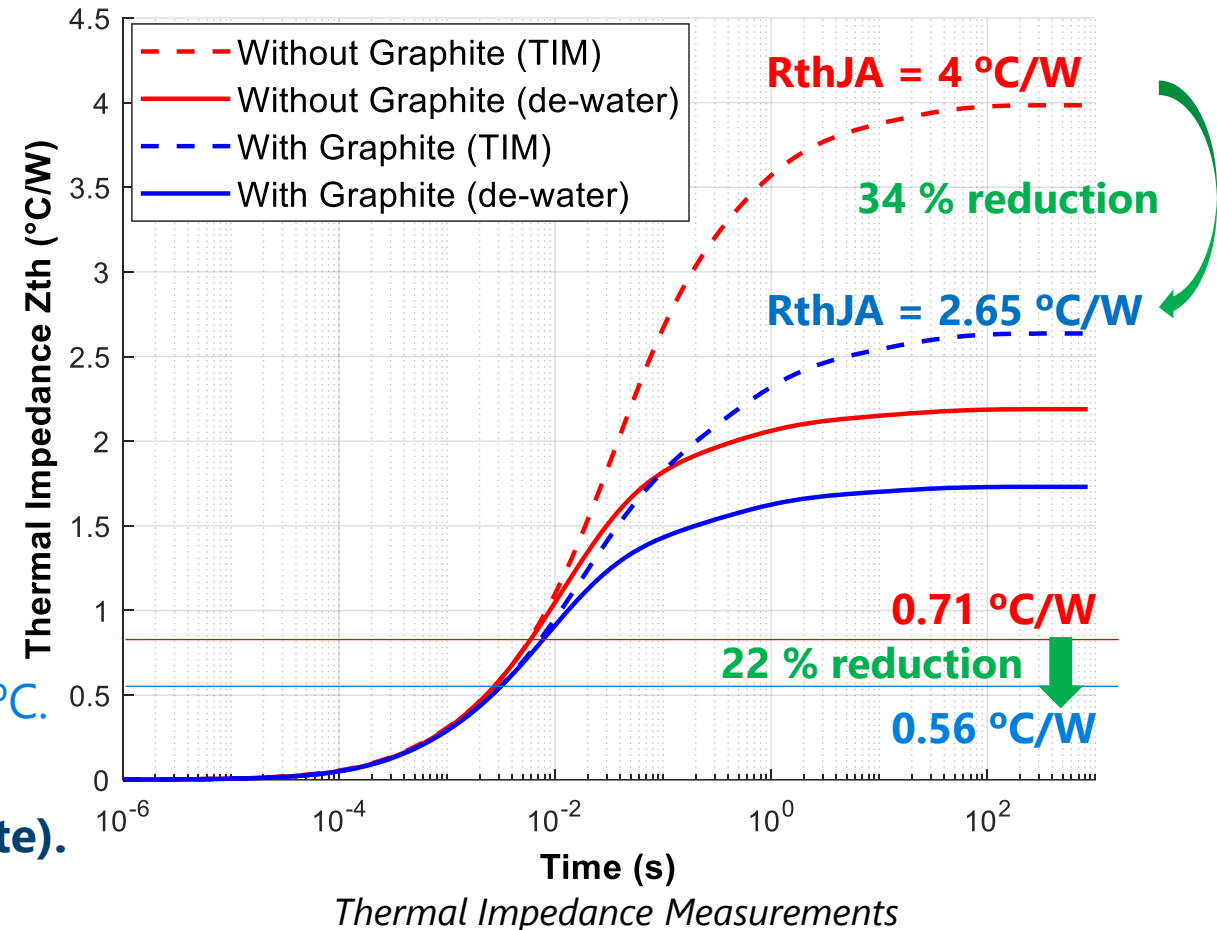


Experimental test conditions:

- The cold plate is cooled by water with an inlet temperature of 23.5 °C.
- At steady state, $R_{thJA} = Z_{thJA}$
- Applied power:
 - (Sil-Pad® 1500ST) → 11 W (without graphite).
 - (Sil-Pad® 1500ST) → 16 W (with graphite).
 - (De-water) → 20 W (without graphite).
 - (De-water) → 24 W (with graphite).

In order to keep maximum junction temperature @70 °C.

- Using TDIM → $R_{thJC} = 0.56 \text{ °C/W}$ (with graphite).



➤ Comparing to the reference sample, R_{thJC} was reduced by 22 %.

3.4

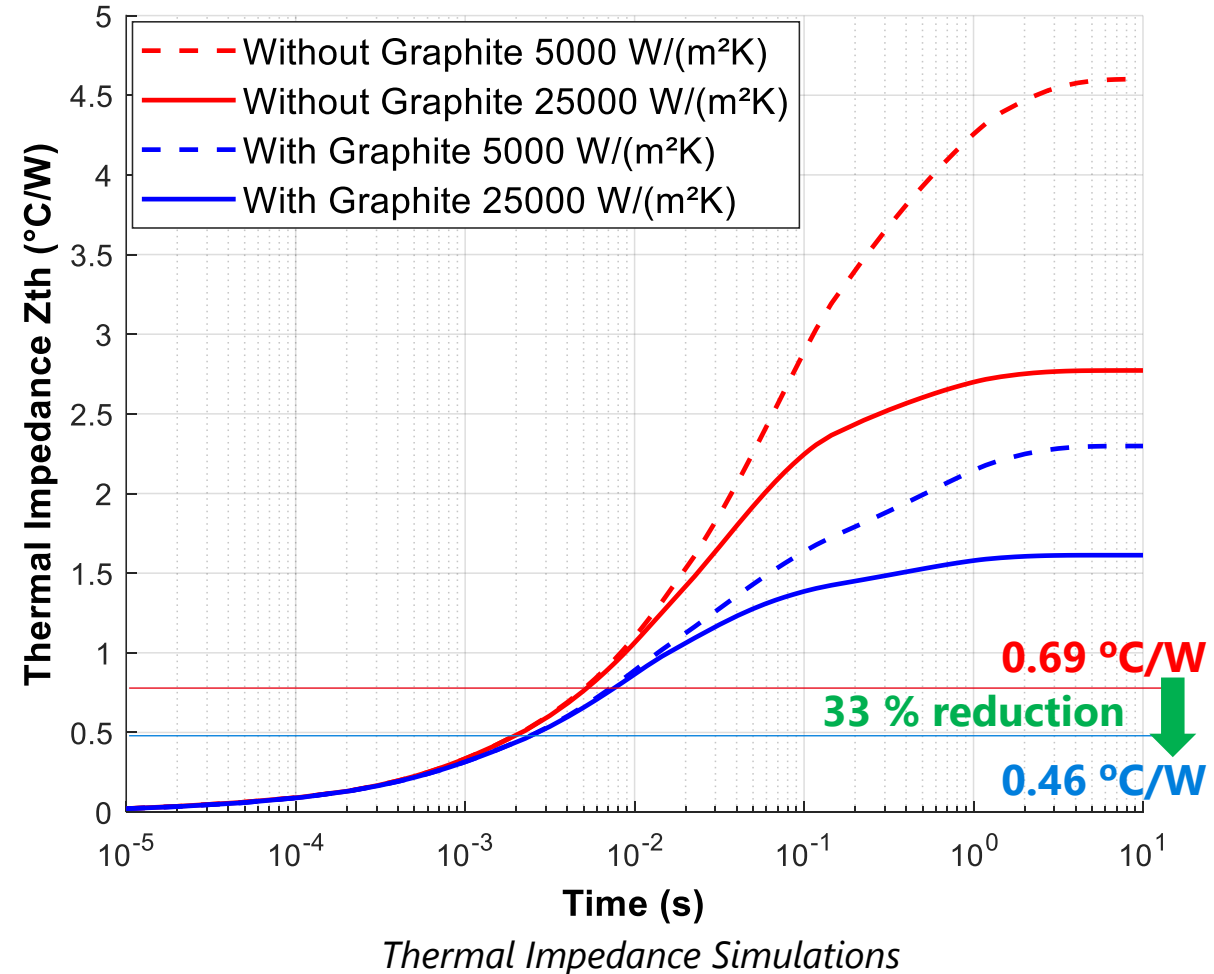
Mimic the TDIM method under FEM simulation



Simulation conditions:

- Zth curves were obtained by transient thermal simulations → In order to verify TDIM measurement value and explain the difference with ideal FEM simulation.
- TDIM was used to calculate RthJC → Assigning two different heat transfer coefficients on the bottom surface of the PCB.

Location	Boundary condition
Chip	20 W
Top surfaces	10 W/(m ² .K)
Bottom surface	5000 W/(m².K) or 25000 W/(m².K)



➤ Comparing to the reference sample, RthJC was reduced by 33 % according to simulations.

4

Conclusion

Conclusion:

- A heat spreading solution compatible with standard PCB manufacturing process was proposed by embedding graphite layers in PCB.
- PCB samples with embedded SiC diodes, were designed and fabricated successfully. PCB samples with graphite were compared to reference samples without graphite.
- FEM simulations predict junction to ambient thermal resistance **RthJA reduction of 49 %**. while thermal experimental results showed a **RthJA reduction of 34 %**.

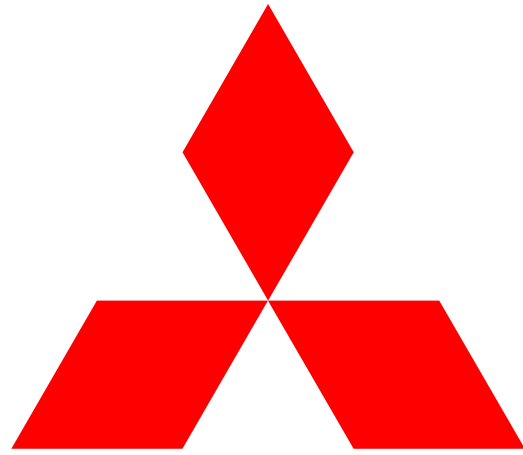
Package Type	Junction to case thermal resistance RthJC (°C/W) TDIM		
	Simulation	Experiment	Difference % w.r.t. simulation
Sample without Graphite	0.69	0.71	4 %
Sample with Graphite	0.46	0.56	20 %
Reduction in RthJC %	33 %	22 %	

Next step:

- Thermal characterization for all remaining samples of the same design to obtain statistical information.

Thank you

Questions ??



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