Modelling and Simulation of PCB Embedded Power Electronic Layouts

ECPE Workshop "Embedding and Advanced Integration Technologies in Power Electronics"



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- 1 Current design tools for power electronics
- 2 Proposition for PCB-embedded electronics
- 8 Export from eCAD
- 4 Electrical model
- 5 Thermal model







1 Current design tools for power electronics

- 2 Proposition for PCB-embedded electronics
- B Export from eCAD
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Design in Power Electronics - Current State



Specifications

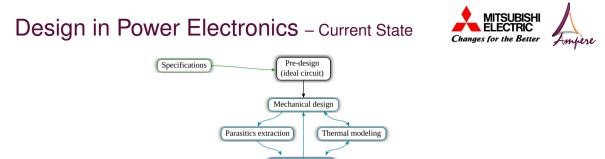


Design in Power Electronics - Current State







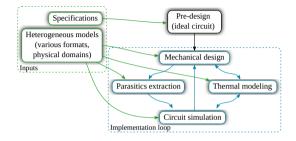


Circuit simulation

• Implementation is a complex affair:

Design in Power Electronics - Current State

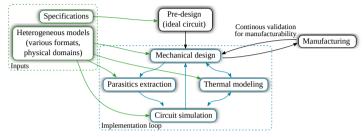




- Implementation is a complex affair:
 - No unified description

Design in Power Electronics – Current State

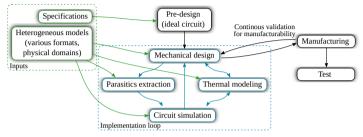




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 - No unified description
 - Or design rules...

Design in Power Electronics - Current State

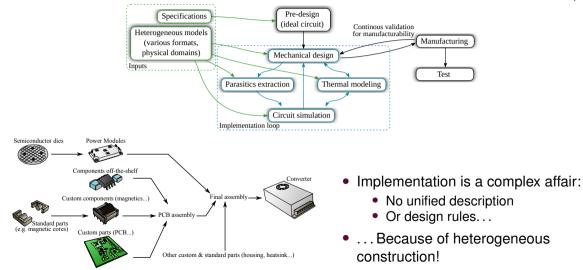




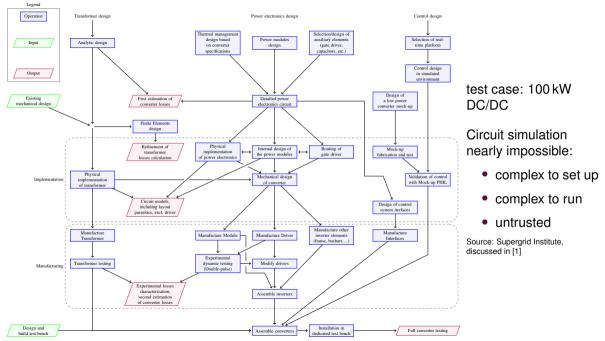
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Design in Power Electronics - Current State





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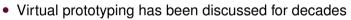


- · Virtual prototyping has been discussed for decades
 - + Fostered by more powerful computers, more capable software
 - Hampered by lack of unified description, poor models



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- It is needed more than ever!
 - · Integration means costlier prototypes, with longer lead times
 - Integrated systems cannot be debugged/repaired!





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→ Can we generate virtual prototypes for PCB embedded-electronics?





Current design tools for power electronics

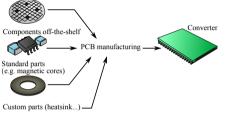
2 Proposition for PCB-embedded electronics

3 Export from eCAD

- 4 Electrical model
- 5 Thermal model



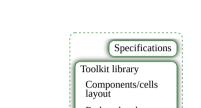
Design in Power Electronics – Proposition

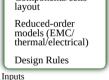


PCB (embedding) can bring:

Semiconductor dies

- more rationalized manufacturing:
 - fewer packaging levels
 - single-board-converters
- one-stop design tool (eCAD):
 - complete description of a design
 - design-rules validation (design for manufacturing)





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Changes for the Better

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7/26 23/11/2022

PCB (embedding) can bring:

Standard parts

(e.g. magnetic cores)

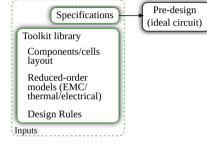
Custom parts (heatsink...

Semiconductor dies

Components off-the-shelf

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PCB manufacturing







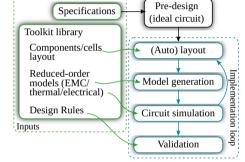
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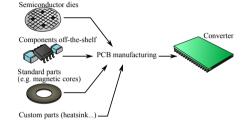
Simulation of PCB-embedded layouts

23/11/2022 7 / 26

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Design in Power Electronics – Proposition



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Design in Power Electronics – Proposition

PCB manufacturing

Converter

Simulation of PCB-embedded layouts



Standard parts

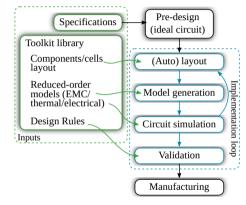
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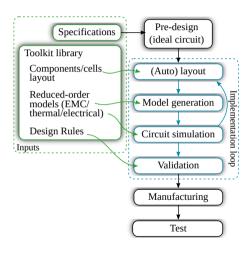


Design in Power Electronics – Proposition

- Components off-the-shelf PCB manufacturing Standard parts (e.g. magnetic cores) Custom parts (heatsink...)
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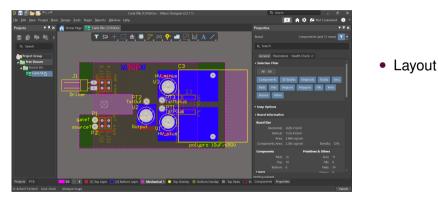
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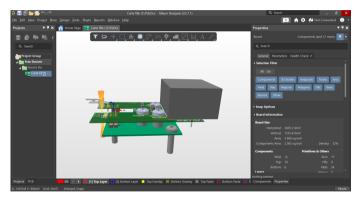




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- Layout
- Component location
- Z-positionning





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- Layout
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- Components info





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- And much more: schematic, materials...





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- And much more: schematic, materials...

Can we generate a virtual prototype from that description?

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To demonstrate systematic generation of electric and thermal models from eCAD

• Does the eCAD really contain all needed data? can they be exported?



To demonstrate systematic generation of electric and thermal models from eCAD

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- Are manual adjustments needed somewhere?



To demonstrate systematic generation of electric and thermal models from eCAD

- Does the eCAD really contain all needed data? can they be exported?
- Are manual adjustments needed somewhere?
- Are the generated models actually usable? (and if not, can automatic model simplification be implemented?)

Selection of commercial software

- eCAD: Altium
 - Already in use in our team



PCB Layout (Altium Designer)	eCAD
	,

Finite element simulation	
Thermal simulation (Ansys icepak)	Circuit parasitics calculation (Q3D)
	,

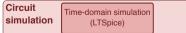


Selection of commercial software

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 - Already in use in our team
 - Can directly generate SPICE models of multiport layout



Finite element simulation	
Thermal simulation (Ansys icepak)	Circuit parasitics calculation (Q3D)
Circuit	





simulation

Simulation of PCB-embedded layouts

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 - · Here we only consider heat conduction



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(LTSpice)



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 - Models available for many power devices



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Thermal simulation (Ansys icepak)	Circuit parasitics calculation (Q3D)
Circuit Time-dom	pain simulation

(LTSpice)

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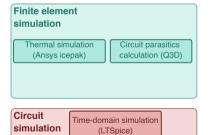
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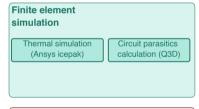


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 - Probably not so powerful













Current design tools for power electronics

2 Proposition for PCB-embedded electronics

8 Export from eCAD

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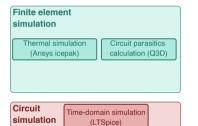






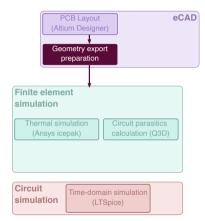
PCB Layout (Altium Designer)	eCAD

Many file format available for export;



File formats - [2]





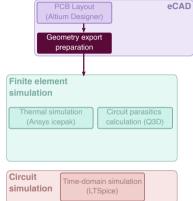
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In practice, when imported in Ansys:

· · · · ·				
	Gerber	ODB++	IPC-2581	EDB
3D-model		-	_	++
Layout details		_	+	++
(materials,Nets)				
Components details		_	+	++

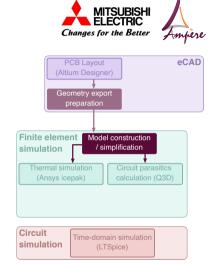
Geometry import



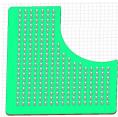




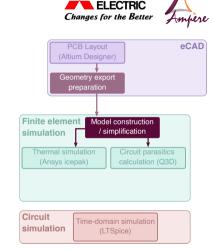
- Geometry import
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- Geometry import
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- 3 Simplification of the geometry
 - Faceting of round shapes (feature of Ansys)
 - Grouping of vias (custom routine)

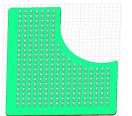




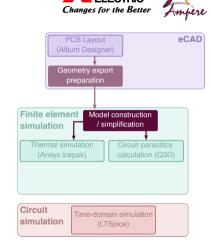


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Ø Further simulation-dependent pre-processing

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Simulation of PCB-embedded layouts

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Current design tools for power electronics

Proposition for PCB-embedded electronics

3 Export from eCAD



5 Thermal model



Computation of circuit parasitics



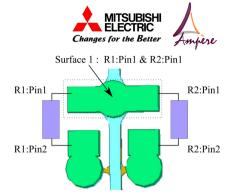
• Pre-processing:



Simulation of PCB-embedded layouts

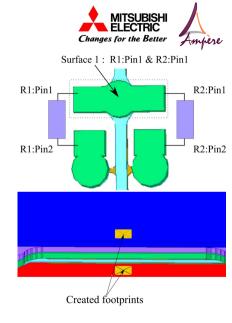
Computation of circuit parasitics

- Pre-processing:
 - Merge pads when too close (model simplification)



Computation of circuit parasitics

- Pre-processing:
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 - Create contact points on large surfaces



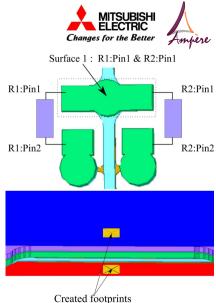
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Computation of circuit parasitics

• Automatically place terminals for computation ("sinks" and "source" in Q3D)



Simulation of PCB-embedded layouts

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Computation of circuit parasitics

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• Run calculation of stray R, L, C between all terminals

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	eometry expo preparation	ont -	
Finite elem		l constructio	n
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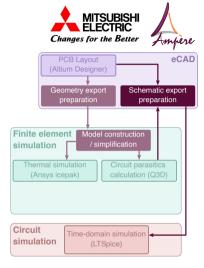
Computation of circuit parasitics

MITSUBISHI FI ECTRIC Chanaes for the Better Ampere eCAD Schematic export Geometry export preparation **Finite element** Model construction / simplification simulation Circuit Time-domain simulation simulation

Computation of circuit parasitics

• Pre-processing:

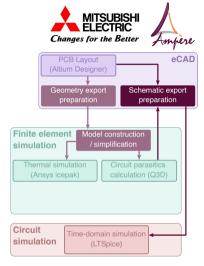
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- Return model and list of terminals to eCAD



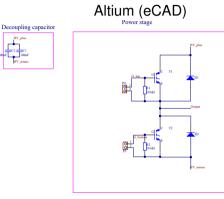
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- Generate LTSpice schematic



Circuit schematics



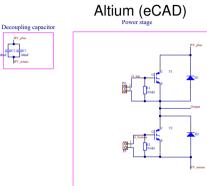


LTSpice (circuit simulation)

Circuit schematics

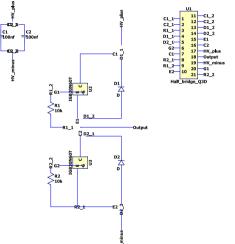






- Reproduce location of symbols
- Layout model as a single block
- Connections generated automatically



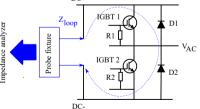


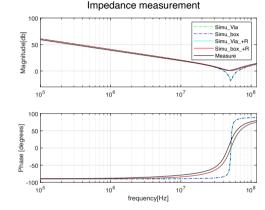
Experimental validation - Layout Impedance











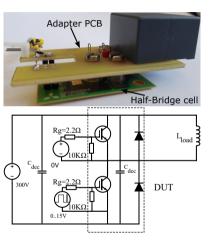
- No negative effect of via simplification
- Measurement accuracy limited (2-wire, contact probe...)
- Good simulation/experiment agreement overall

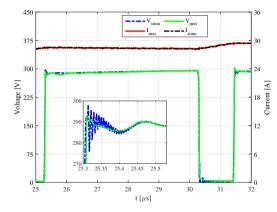
Impedance analyzer

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Experimental validation - Double-pulse test







- · Proof of concept for systematic model generation
 - No manual modification of Half Bridge PCB model
- No LTSpice model available for used IGBTs and diodes





Current design tools for power electronics

Proposition for PCB-embedded electronics

3 Export from eCAD

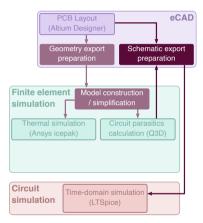
4 Electrical model

6 Thermal model



Generation of a thermal model



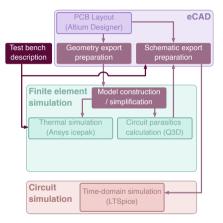


Starting from imported geometry:

- Define heat sources
 - Manual selection of the components to be considered in the eCAD export stage

Generation of a thermal model



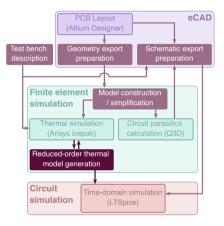


Starting from imported geometry:

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- 2 Application of boundary conditions
 - · Not implemented yet for electrical simulations
 - Approach similar to that of the VHDL "test benches"

Generation of a thermal model



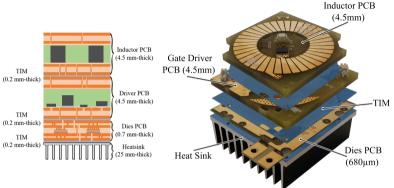


Starting from imported geometry:

- Define heat sources
 - Manual selection of the components to be considered in the eCAD export stage
- Application of boundary conditions
 - · Not implemented yet for electrical simulations
 - Approach similar to that of the VHDL "test benches"
- 3 Reduced-order thermal model generation
 - Sequentially "activate" each power source
 - Perform a FEM simulation (Ansys Icepak)
 - Export transient temp. rise of each component
 - Identify R_{Th}C_{Th} models and generate Spice Netlist

Geometry simplification – Description [3]



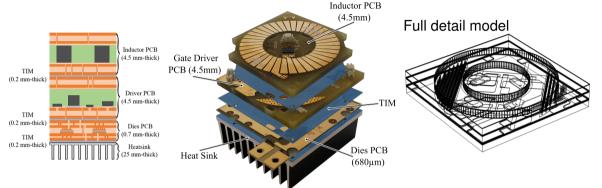


Two approaches investigated:

Geometry simplification – Description [3]





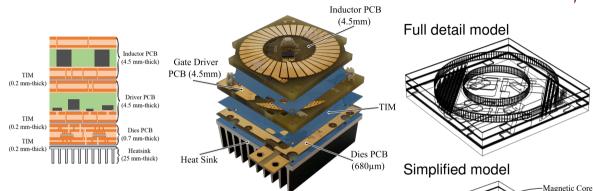


Two approaches investigated:

No simplification (inc. vias)

Geometry simplification – Description [3]





Two approaches investigated:

- No simplification (inc. vias)
- "Layer-based Homogenization" (uniform conductivity on each layer)

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Die HF

Die LF

Geometry Simplification – Results [3]



Simulations performed with Comsol **Full detail model:**

- 1.5 M elements
- thinest tracks had to be removed

Simplified model:

- 0.3 M elements
- Anisotropic conductivity for
 - via-filled areas
 - Cu layers with low copper filling

Validation of simulation results with experiments

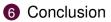
RTD location	Exp.	Simplified	Full
HF Die RTD	37 ℃	35 ℃	38 ℃
LF Die RTD	34 ℃	34 ℃	34 °C
Outer Ind. RTD	27 ℃	32 ℃	31 ℃
Inner Ind. RTD	30 ℃	33 ℃	31 ℃

(ΔT with ambient temperature for embedded sensors)





- Current design tools for power electronics
- Proposition for PCB-embedded electronics
- B Export from eCAD
- 4 Electrical model
- 5 Thermal model



Cyril BUTTAY

Conclusion

Progress so far

- Electrical model:
 - Full workflow demonstrated on simple circuit (half bridge)
 - "Test bench" to be implemented
 - automatic connection of input/outputs
 - modeling of external metal planes (such as heatsinks)
 - Validation to be performed on more complex boards
- Thermal model:
 - eCAD export / FEM import done (inc. selection of relevant components)
 - Currently working Zth calculations and reduced RC model generation







To demonstrate systematic generation of electric and thermal models from eCAD

- Does the eCAD really contain all needed data? can they be exported?
 - Export is possible with minimum losses
 - Special scripts required in addition to EDB export
 - Interface with outside world not included in eCAD



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- Are manual adjustments needed somewhere?
 - ✓ No manual adaptation of the models required so far
 - Manual selection of components to be considered for thermal analysis
- Are the generated models actually usable?
 - Simplification required for vias (but can be done automatically)
 - ? Test on larger circuits will show if this approach works

Bibliography I



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