Physics-based Strategies for Fast TDDB Testing and Lifetime Estimation in SiC Power MOSFETs

O. Aviñó-Salvadó, Cyril Buttay, F. Bonet, C. Raynaud, P. Bevilacqua, J. Rebollo, H. Morel, X. Perpiñà

Physics-based Strategies for Fast TDDB Testing and Lifetime Estimation in SiC Power MOSFETs

O. Aviñó-Salvadó, *Member, IEEE*, C. Buttay, *Senior Member, IEEE*, F. Bonet, C. Raynaud, P. Bevilacqua, J. Rebollo, H. Morel, *Senior Member, IEEE*, X. Perpiñà.

***Abstract*—To expedite testing, Time-Dependent Dielectric Breakdown (TDDB) analyses are conducted on commercial 4H-SiC MOSFETs at high gate-to-source voltages (V_{GS}), under Fowler-Nordheim conduction only. However, as inferred, such conditions induce impact ionization-generated holes in the dielectric layer (SiO_2), resulting in a state transition in the effective dipolar moment. This accelerates the SiO_2 degradation leading to an overestimation of its intrinsic lifetime at typical V_{GS} values for gate driving in power converters. To address this, a physics-based approach is proposed to design TDDB tests under such conditions and to correct the intrinsic lifetime prediction at nominal V_{GS} values, shortening the testing time by up to 2 orders of magnitude. Thus, the proposed method is a well-suited candidate to be considered in SiC power device qualification standards, still under development.**

***Index Terms*—Lifetime, SiC MOSFET, SiO_2, TDDB, Fowler-Nordheim, Impact Ionization, E-model, 1/E-model.**

NOMENCLATURE

$\mathscr{A}_0$	$= \ln(\frac{A_0}{t_0}) + \frac{\Delta H_0}{kT}$, dimensionless term.
$\mathscr{A}'_0$	$= \ln(\frac{A_0}{t_0}) + \frac{\Delta H'_0}{kT}$, dimensionless term.
A_0, C_0	E-model and 1/E-model pre-factor.
B	Fowler-Nordheim tunneling coefficient.
C_{GS}, C_{ox}	Gate-source capacitance, Gate oxide capacitance.
E, $\vec{E}_{loc}$	Electric field, Local electric field.
H	Impact-ionization coefficient.
h	Planck's constant.
I_G, $I_{G,FN}$	Gate current, I_G via FN mechanism.
J_{FN}	Fowler-Nordheim current density.
K_{ox}	Dielectric constant for Silica.
k	Boltzmann constant.
L, L_{eff}	Lorentz factor, Effective Lorentz factor.
L'_{eff}	Effective Lorentz factor for $V_{GS} \geq V_{GS,crit}$.
m_0	Free electron mass.
P_{eff}	Effective dipole moment.
Q_F, Q_M	Fixed and mobile charge in the oxide.
Q_l	SiC/SiO_2 interface charge.
q	Electron charge.
r_0	Equilibrium Si-O bond distance.
r'_0	r_0 for $V_{GS} \geq V_{GS,crit}$.
T, T'	Temperature, T used for t_{BD} correction.
t	Stress time.
t_{BD}	Time-to-breakdown.
t_{BD-E}	t_{BD} according to E-model.
$t_{BD-1/E}$	t_{BD} according to 1/E-model.
$t_{BD}(V_{GS,n})$	t_{BD} at $V_{GS,n}$.
t_{ox}, t'_{ox}	Oxide thickness, t_{ox} used for t_{BD} correction.
t_0	$= 1$ h, normalization term.
V_{GS}	Gate-to-source voltage.
$V_{GS,crit}$	V_{GS} value triggering impact ionization.
$V_{GS,n}$	V_{GS} at nominal voltage.
$V_{GS,0}$	V_{GS} value according to $V_{GS} > V_{GS,crit}$.
V_{FB}	Flat-band voltage.
V_{Poly}	Gate Polysilicon voltage drop.
V_0	$= V_{FB} + \psi_s + V_{Poly}$.
z^*	Number of electron charges of the Si ion.
β	Weibull slope.
γ	E-model voltage acceleration factor.
γ'	γ for $V_{GS} \geq V_{GS,crit}$.
ΔH_0	Zero-field activation energy.
$\Delta H'_0$	ΔH_0 for $V_{GS} \geq V_{GS,crit}$.
δ	Inhomogeneous or enhancement factor of $\vec{E}_{loc}$.
δ'	δ for $V_{GS} \geq V_{GS,crit}$.
$\eta(m,n)$	Mie-Grüneisen parameter for (m,n) exponents.
η	Mie-Grüneisen parameter for $V_{GS} < V_{GS,crit}$.
η'	Mie-Grüneisen parameter for $V_{GS} \geq V_{GS,crit}$.
η_w	Weibull scale-factor.
ϑ	Correction factor for t_{BD} estimation.
ϑ_{Calc}	Calculated values of ϑ.
ϑ_{Exp}	Experimental values of ϑ.
Ξ	Stretching factor at the SiC/SiO_2 interface.
Φ_{MS}	Polysilicon-semiconductor workfunction.
Φ_b	Barrier height.
ψ_s	Surface potential at the Si/SiO_2 interface.

In the framework of the PhD program in Physics of the UAB, this work was supported by AEI (contracts PID2021-126334OB-I00 and PCI2020-112028) and H2020-ECSEL (iRel40, H2020-662133), and AGAUR Funds (grants 2017-SGR-1384 2021-SGR-00496) and both European Social Fund and Spanish Youth Employment Initiative (contract MN19_CAT_IMB-CNM_003) and IMB-CNM (Trigger-195)."

O. Aviñó-Salvadó, F. Bonet, J. Rebollo and X. Perpiñà, are with IMB-CNM-CSIC, 08193 Bellaterra (Barcelona), Spain. e-mail:oriol.avino@imb-cnm.csic.es.

C. Buttay, C. Raynaud, P. Bevilacqua, H. Morel are with the Univ Lyon, CNRS, INSA Lyon, Université Claude Bernard Lyon 1, Ecole Centrale de Lyon, Ampère, F-69621, Villeurbanne, France.

I. INTRODUCTION

OVER the past two decades, Silicon Carbide (SiC) power devices have entered commercialization. It has long been demonstrated that in terms of thermal conductivity, electron velocity, energy gap and supported electric field, SiC outperforms Silicon (Si) and paves the way for power semiconductor devices capable of operating at higher voltages [1], switching frequencies [2] and temperatures [3].

Among all SiC power devices, 4H-SiC MOSFETs are particularly attractive, as they are real candidates for replacing Si IGBTs in medium voltage power applications (i.e., from 0.4 to 5 kV) [4]. Although they have improved noticeably since their market introduction [5], these devices still present reliability issues due to structural defects in both the gate dielectric (SiO_2) and SiC/SiO_2 interface [5]. Regarding the gate dielectric, defects are created as a degradation process, since in comparison to Si MOSFETs, the oxide surface electric field is higher and offers a lower barrier height Φ_b (2.70 eV vs. 3.15 eV), promoting larger gate leakage currents via tunnel effect [6], [7]. Conversely, the material transition at the semiconductor material/SiO_2 interface is, from a structural point of view, more complex in SiC substrates [5], [8], increasing the possibility of defects arising during the manufacturing process (e.g., dangling or strained bonds). In any case, all these defects introduce allowed states within the insulator band-gap and are responsible for charge trapping or detrapping processes while the device is under operation. Obviously, this has a negative impact on the device's electrical performance and may even result in its destruction once defects have percolated the gate dielectric [9], [10]. According to this, the main reliability concerns in SiC MOSFET gate dielectric are the bias thermal instabilities (BTI, causing device performance modulation) and time-dependent dielectric breakdown (TDDB, causing device failure). To study BTI and TDDB in SiC insulated-gate devices, current standard qualification test guides, such as JEDEC [11], require to be revisited [12], as they were designed for Si components. In fact, this action is more imperative in the case of TDDB tests, as BTIs have already been thoroughly investigated [13]–[15] and recent guidelines have been published [16] for their proper evaluation. In contrast, most TDDB studies so far have focused on thin and ultra-thin gate dielectrics for Si substrates ($\sim$ 1-10 nm), and a few works, e.g., [17]–[22], dealt with 4H-SiC power MOSFETs.

Generally, the gate ageing in TDDB studies is accelerated under constant temperature (T) and electrical stress, i.e., elevated gate to source voltage (V_{GS}) or constant gate current (I_G), until the dielectric breaks down. This approach aims to extract the characteristic time-to-breakdown of the dielectric (t_{BD}) for different stress levels, and then, extrapolate it to nominal conditions of use. Since TDDB tests entail a degradation process, t_{BD} is analyzed according to the Weibull statistics to determine several features of its behavior. This type of empirical analysis is widely accepted for gate oxides [23] and its cumulative distribution function $F(t)$ is

$$F(t) = 1 - \exp\left[-\left(\frac{t}{\eta_w}\right)^{\beta}\right], \tag{1}$$

where t makes reference to the stress time, η_w is a scale factor defined as the 63.2^{th} percentile value of t_{BD}, and β provides the shape distribution factor or Weibull slope. Concretely, for a given stress condition, a steep variation of β within the same data set commonly indicates a change on the gate dielectric failure mode (e.g., intrinsic or extrinsic) [24]. In TDDB tests, V_{GS} or I_G values must be chosen to be high enough to reduce the testing time, while ensuring that the resulting failure mechanism is the same as in real operating conditions. Once the stress conditions are set, models based on the gate oxide degradation physics are used to estimate t_{BD} in the final application. Although a JEDEC standard supports such an approach [11], it lacks criteria for the correct choice of values for V_{GS} or I_G, and/or T for TDDB tests, as well as guidance on the required extrapolation models.

To illustrate this, we select the publications [17], [18], which report on TDDB testing of commercial 1.2 kV SiC MOSFETs using the same extrapolation model. At $V_{GS} = 25$ V, Gajewski *et al.* [17] predict for $t_{ox} = 53$ nm [6], $t_{BD} \simeq 4 \times 10^5$ h, while Santini *et al.* [18] estimate for $t_{ox} = 63$ nm, $t_{BD} > 10^{10}$ h. This difference is because the voltage acceleration factor of the latter is almost twice. As devices with the same ratings and similar t_{ox} were considered in both studies, the large difference in extrapolated t_{BD} may be attributed to the stress test conditions: in [17], TDDB tests were run for V_{GS} ranging from 35 to 40 V ($6.6 < E < 7.5\,\mathrm{MV\,cm^{-1}}$), and between 58 and 60 V ($9.2 < E < 9.5\,\mathrm{MV\,cm^{-1}}$) in [18]. Because E exceeds a critical level, additional phenomena occur: the generation of holes by impact ionization in the dielectric [24], [25]. Performing TDDB tests beyond this critical E value may result in estimating a different β, and therefore a different t_{BD}.

From a practical perspective for improving power system reliability, TDDB tests are the most stringent and specialized method for evaluating gate dielectric degradation in 4H-SiC MOSFETs. Recent studies have revealed that pulsed driving is less stressful and representative for the dielectric compared to static tests [26], [27]. Specifically, [27] found that t_{BD} is approximately three times lower for static tests. Besides, [26] showed that a threshold voltage drift occurs when a gate pulsed bias is applied with a specific duty cycle. Since both degradation mechanisms may interfere, static stress resulting from TDDB analysis is a more reliable indicator for intrinsic dielectric failure prediction. Currently, screening strategies are being implemented to select and market SiC MOSFETs with the aim of achieving reliability levels comparable to those of their Si counterparts [28], [29]. These approaches also serve to mitigate the impact of possible extrinsic failures [30]. Therefore, accurate and fast TDDB tests are essential in this scenario for determining t_{BD} under nominal conditions.

In this paper, we present a new methodology consisting of several physics-based strategies according to the E-model, for V_{GS} range selection and t_{BD} correction at nominal gate bias. Thanks to this approach, the required time to perform these tests is reduced by up to 2 orders of magnitude. Nowadays, tests duration shows accumulated testing time of $\sim$ 1000 h [20], whereas the described methodology reduces the accumulated testing time to $\sim$ 11 h. Moreover, it enables accurate t_{BD} values to be determined at nominal gate bias, even if impact ionization occurs during the dielectric ageing. This topic is of major concern for reliable t_{BD} predictions, since even more recent studies [21], [22] are conducted to reduce the TDDB testing time, and use bias conditions in which holes generation occur because of impact ionization [25], overestimating t_{BD}. The proposed solutions will facilitate for a desired device lifetime, the optimization of the gate driving to obtain lower losses in the device and, thus, the converter.

This paper is organized as follows. Section II introduces

the existing degradation models for TDDB prediction, highlighting their limitations when applied to SiC MOSFETs. Section III describes the methodology followed to perform the TDDB tests and to study using electrical measurements the charge dynamics in the dielectric. Section IV covers the following topics. First, the variation of t_{BD} as a function of the stress conditions is analyzed theoretically and experimentally, considering all possible degradation models and charge transport mechanisms in the dielectric. Second, corrections based on geometrical and physical parameters of the dielectric are proposed to allow a reliable prediction of t_{BD} for TDDB tests at high V_{GS} values. Finally, Section V presents the main conclusions of this work.

II. t_{BD} Physical Models

The most appropriate models in our investigations to extrapolate t_{BD} at a given V_{GS} are described in detail here [31]. Firstly, the E-model, also known as thermochemical [32], assumes that by an electric field driven process, Si-O bonds can be first stretched, and then broken by charge carrier trapping, generating neutral dangling bond defects which will be precursors of gate oxide breakdown by setting percolation paths [9], [10]. This model was conceived for thin gate dielectrics ($t_{ox} \leq 10\,\text{nm}$) [9], [32], [33]. The t_{BD} based on this mechanism (t_{BD-E}) can be described as

$$t_{BD-E} = A_0 \cdot \exp\left[\frac{\Delta H_0}{kT} - \gamma \cdot (V_{GS} - V_0)\right], \tag{2}$$

where A_0 denotes a pre-factor, ΔH_0 refers to the zero-field activation energy, k is the Boltzmann constant, and γ represents the voltage acceleration factor related to the applied V_{GS}. V_{GS} relates to E as $E = (V_{GS} - V_{FB} - \psi_s - V_{Poly})/t_{ox}$, where ψ_s is the surface potential at the interface oxide-semiconductor (for SiC, $\psi_s \sim 3.75V$ in strong inversion mode [6]), V_{Poly} is the voltage drop in the gate polysilicon and V_{FB} is the flat band voltage, also used in the voltage $V_0 = V_{FB} + \psi_s + V_{Poly}$ which can be considered constant under high inversion conditions. In turn, V_{FB} writes as

$$V_{FB} = \Phi_{MS} - \frac{Q_F + Q_M + Q_I}{C_{OX}}, \tag{3}$$

where Φ_{MS} is the difference between the work functions of the degenerate poly-Si and the semiconductor. Q_F, Q_M and Q_I are respectively the fixed charge in the oxide, the mobile ions charge in the oxide and the charge trapped at the SiC/SiO_2 interface and C_{OX} is the gate oxide capacitance. If these parameters are unknown, V_{FB} can be graphically extracted from the C-V curve [6]. γ also is related to the effective dipole moment (P_{eff}), averaged within the dielectric, caused by the stretch of the SiO_2 bonds under the electric field induced at the molecular level. This local field is more relevant for weak bonds or coordination breakage in SiO_2 molecules presenting structural defects (e.g., oxygen vacancy or excess), strained bonds (e.g., close to or at semiconductor/dielectric interface), holes captured by Si ion [9], [34], or species release by carrier scattering [9], [34]. In fact, these species are positive ions (e.g., H^+ or N^+) intentionally introduced at the SiC/SiO_2 interface to passivate its negatively-charged dangling bonds so as to

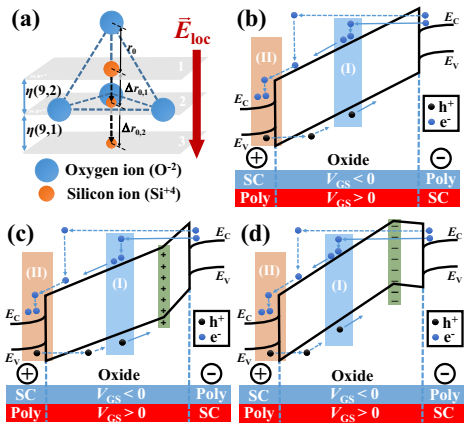

Fig. 1: (a) SiO_2 molecule showing the displacement of Si ion due to $\vec{E}_{loc}$ and its effects on bonding strength. Schematic band diagram of SiO_2 showing, as a function of V_{GS} polarity, the impact ionization phenomena initiated by electrons when trapped charge is null (b), positive (c) and negative (d). In region I of (b), (c) and (d), carrier generation occurs, whereas in region II, electrons reach the anode creating holes there. SC and Poly refer to semiconductor and gate polysilicon, respectively.

reduce the Coulomb scattering in the MOSFET channel and improve carrier mobility [5]. Considering this and (2),

$$\gamma = \frac{P_{eff}}{t_{ox} \cdot kT} = \frac{(z^* q) \cdot r_0}{t_{ox} \cdot kT \cdot \eta(m,n)} \cdot \left[1 + L_{eff} \cdot (K_{ox} - 1)\right], \tag{4}$$

where z^* represents the number of electron charges of the Si ion ($z^* \approx 2.4$ [35]), r_0 is the equilibrium Si-O bond distance (1.7 Å), and K_{ox} the dielectric constant for silica ($K_{ox} = 3.9$). $\eta(m,n)$ is the Mie-Grüneisen parameter and depends only on the bonding exponents m and n, weighting r_0 according to the relative position of Si ion within the SiO_2 molecule, as Fig. 1a shows. Namely, when a Si ion is placed within the SiO_2 molecule, it presents a more covalent bonding and $\eta(9,2) = 1.07$. However, when the Si ion is displaced by the local electric field within the molecule ($\vec{E}_{loc}$) by a distance longer than $\Delta r_{0,1}$ (basal plane location, see plane 2 in Fig. 1a), its Si-O bonding becomes ionic and $\eta(9,1) = 0.6$ (Pucker configuration). Notice that when holes are captured by Si ions, $\eta(9,1)$ is modified, theoretically increasing by 44.4% [34], obtaining positively-charged dangling bonds [10]. L_{eff} is the effective Lorentz factor that connects $\vec{E}_{loc}$ to an $\vec{E}$ inhomogeneously distributed across the dielectric due to device layout or trapped charge [36]. L_{eff} is [36]

$$L_{eff} = \frac{\delta \cdot [1 + L \cdot (K_{ox} - 1)] - 1}{K_{ox} - 1}, \tag{5}$$

where L is the classical Lorentz factor which relates $\vec{E}_{loc}$ with a homogeneous $\vec{E}$ ($L = 1/3$ for SiO_2 cubic symmetry [32]), and δ provides the inhomogeneous or enhancement factor associated to $\vec{E}_{loc}$ (e.g., $\delta = 2$ at device edge [32]). Notice that for non-polar dielectrics (i.e., $P_{eff} = 0$), their breakdown is not expected to occur by this mechanism [9].

Secondly, the 1/E-model [37] is a purely current/charge fluence driven process based on Fowler-Nordheim (FN) conduction through the oxide (tunnel effect) and charge carriers generation via impact ionization, which eventually induces oxide dielectric breakdown by Joule effect. In this process, a conduction-band electron with a very high energy collides

with another one located in the valence band. As a result, this last one also reaches the conduction band, generating an electron-hole pair, following an exponential dependence on $1/E$. Originally, the 1/E-model was developed for ultra-thick SiO_2 ($t_{ox} > 50\,\text{nm}$). It assumes that holes are generated within the dielectric layer by incoming electrons via intraband impact ionization processes [31] at $V_{GS} \geq V_{GS,crit}$, defined by this empirical expression extracted from Udo *et al.* [25]

$$V_{GS,crit} = \left(11.27 \cdot e^{\frac{-t_{ox}}{9.41}} + 5.55 \cdot e^{\frac{-t_{ox}}{59.38}} + 6.43\right) \cdot t_{ox} + V_0, \quad (6)$$

where t_{ox} units are nm. For thin oxides ($t_{ox} < 10\,\text{nm}$), this generation is produced at the anode, outside of the dielectric layer, and is referred to as anode hole injection (AHI). Both conduction and generation processes are depicted in the schematic band diagram of Fig. 1 depending on V_{GS} polarity, trapped charge is null (Fig. 1b), positive (Fig. 1c), or negative (Fig. 1d). In Fig. 1c (resp. Fig. 1d), positive (negative) trapped charge increases (decreases) the electric field at the semiconductor/SiO_2 interface while it narrows (widens) the effective tunneling barrier width. Under such conditions, electrons are accelerated from the cathode towards the anode. In region (I) of Figs. 1b-1d, carrier generation occurs within the dielectric, while in (II), electrons reach the anode producing holes. In both cases, a fraction of the created holes go back towards the cathode, and in some situations, remain trapped [37]. The t_{BD} in 1/E-model ($t_{BD-1/E}$) is

$$t_{BD-1/E} = C_0 \cdot \exp\left[\frac{(B+H)\cdot t_{ox}}{(V_{GS}-V_0)}\right], \quad (7)$$

where C_0, B, and H are the scale pre-factor, FN tunneling, and impact ionization coefficients, respectively. Concretely, $B = \frac{8\pi}{3\cdot q\cdot h} \cdot \sqrt{0.48 \cdot m_0 \cdot \Phi_b^3}$ [6], where q, m_0, and h are the electron charge, free electron mass, and Planck's constant, respectively.

In comparison to the E-model, the 1/E-model is more relevant at higher V_{GS} and lower T values [38], showing a complementary behavior. To predict their joint effect on the characteristic time-to-breakdown of the dielectric ($t_{BD-total}$), a merged model to cover at any given T, an extended V_{GS} range, calulated as $t_{BD-total} = \frac{t_{BD-E}\cdot t_{BD-1/E}}{t_{BD-E}+t_{BD-1/E}}$, has been proposed

$$t_{BD-total} = \frac{A_0 \cdot \exp\left[\dfrac{\Delta H_0}{kT} - \gamma\cdot(V_{GS}-V_0)\right]}{1+X(V_{GS})}, \quad (8)$$

where $X(V_{GS}) = \frac{A_0}{C_0}\cdot\exp\left[\left(\frac{\Delta H_0}{kT} - \gamma\cdot(V_{GS}-V_0)\right) - \left(\frac{(B+H)\cdot t_{ox}}{(V_{GS}-V_0)}\right)\right]$.

III. Methodology

Commercial 1.2 kV SiC planar MOSFETs (Wolfspeed C2M0080120D [39] with $t_{ox} \approx 53\,\text{nm}$ [6]) are investigated. In all measurements, their drain and source are short-circuited.

TDDB tests are performed as follows. By using a hot-plate (heating up time of 0.25 h), $T = 150\,^\circ\text{C}$ is set. Since this value is close to the maximum rated temperature of the devices, it represents one of the most stressful operation conditions in several applications [17], [18]. Besides, this value also represents the lowest temperature at which FN tunneling and electric field-driven bond distortion manifest equally [33]. During the TDDB tests, I_G is continuously monitored (SMU 2636B, Keithley) and the data is recorded for further analysis. To select the V_{GS} values for the tests, a two-step approach has been followed. Firstly, to fix a V_{GS} range, the $I_G(V_{GS})$ characteristics of ten devices are measured (SMU 2636B) at $T = 150\,^\circ\text{C}$, as Fig. 2 depicts. Starting at $V_{GS} = 20\,\text{V}$, the voltage is increased in steps of 50 mV until the dielectric breaks down. Each measurement is taken 1 s after incrementing the V_{GS} value to limit the displacement (capacitive) currents. This delay is defined in agreement with the gate to source MOSFET capacitance C_{GS} ($\approx 1\,\text{nF}$ [39]). The region where the injection by FN phenomena is predominant, can be clearly identified thanks to a FN current density (J_{FN}) model (dashed curve in Fig. 2). Its contribution to I_G is referred to as $I_{G,FN}$. For $V_{GS} \geq 44\,\text{V}$, the $I_G(V_{GS})$ characteristics deviation from the J_{FN} fit is $\sim 10\%$ increasing more rapidly with V_{GS}. At this point, in addition to FN, other conduction mechanisms start to become relevant. It is recommended to choose a maximum stress voltage slightly lower to avoid degradation processes derived from these phenomena. According to this, the V_{GS} range for the TDDB tests is fixed from 40 to 43.5 V ($< 5\%$ deviation, i.e., $I_{G,FN} > 0.95 I_G$). Secondly, within this voltage range, some fresh samples are stressed to determine the most suitable V_{GS} values to evaluate t_{BD} with a larger number of devices. In this way, t_{BD} is further measured at $V_{GS} = 40.5$, 41.5 and 42.5 V, using seven samples for each V_{GS} value. The time-to-breakdown extracted from each sample at a fixed V_{GS} is computed according to Weibull statistics, finally deriving t_{BD} as the median value of the seven samples. Notice that as $2.9 \lesssim \beta \lesssim 6.5$, $F(t)$ is almost symmetrical [40], and the data can be statistically portrayed by a Gaussian distribution. Then, the uncertainty in t_{BD} is calculated more precisely as twice the standard deviation of the values, since the uncertainties associated with the fits to identify β and η_w are avoided in the calculations. Proceeding like this, the total TDDB testing time is shortened, and t_{BD} properly extracted. Finally, based on the obtained results, t_{BD} is extrapolated in agreement with the E-model, also considering the data extracted in the aforementioned V_{GS} range [9]. As for γ, it is identified by representing these data in semi-logarithmic scale for linearization, and applying a least-squares linear regression. As a common practice, the log scale is set in base 10 instead of e, and the inferred slope corresponds to $\log(e)\cdot\gamma$.

To gain a better understanding of the charge dynamics within the dielectric layer during the tests, C_{GS} versus V_{GS} characterizations are additionally performed at room temperature. These measurements enable us to identify whether changes in the $C_{GS}(V_{GS})$ curve are caused by released mobile ions or hole/electron trapping, and to infer their impact on the electric field at the SiC/SiO_2 interface, which in turn affects FN injection. Two kind of measurements are carried out. Firstly, $C_{GS}(V_{GS})$ curves are performed at several time instants representative of the degradation process at $V_{GS} \approx V_{GS,crit}$. To do this, an additional device is stressed at $V_{GS} \approx V_{GS,crit}$ with a different TDDB test protocol. The dielectric ageing is stopped and resumed regularly so as to extract the $C_{GS}(V_{GS})$ (Keysight B1505) at room temperature after a cooling down time of 0.5 h. Notice that this sample is not used for t_{BD} extrapolation at

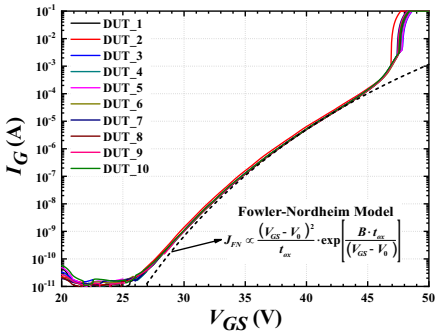

Fig. 2: $I_G(V_{GS})$ at T = 150 °C for 10 samples. The FN injection mechanism is predominant for V_{GS} between 35 and 44 V.

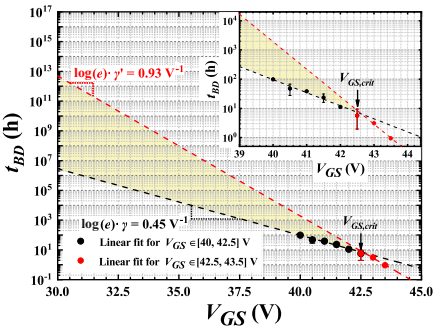

Fig. 3: t_{BD} extrapolations for C2M008120D MOSFETs. Inset zooms in within the V_{GS} range of interest.

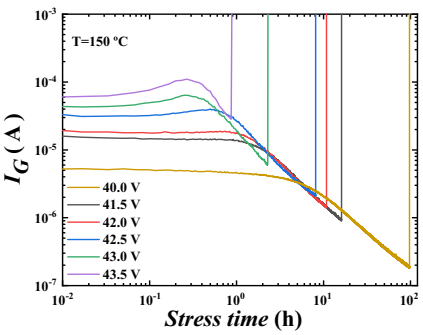

Fig. 4: I_G evolution during TDDB tests under several V_{GS} stresses, ranging from 40.0 to 43.5 V, at T = 150 °C.

operation-rated V_{GS} values. Secondly, to verify whether mobile ions are trapped within the dielectric, other $C_{GS}(V_{GS})$ curves are extracted from a pristine sample before, during, and after applying this stress profile: i) 0.5 h at I_G = +25 µA and ii) 0.5 h at I_G = -25 µA. According to previous I_G monitoring results, this stress precisely fixes the rate of injected charge keeping $V_{GS} \leq V_{GS,crit}$ (I_G = 25 µA) to mainly consider released mobile ions, while leaving enough time (0.5 h) for their trapping.

IV. Results and Discussion

A. Analysis of γ Dependence on Stress Conditions

Fig. 3 summarizes the t_{BD} extracted from all performed TDDB tests, as well as their corresponding extrapolation at lower V_{GS} values and $\log(e)\cdot\gamma$ slopes. It can be seen that depending on the datapoints used for the t_{BD} extrapolation (red/black points), the acceleration factor $\log(e)\cdot\gamma$ and, in turn, the predicted lifetime may vary widely. To discuss such effects and relate them with the theory introduced in Section II, the natural logarithm of (8) has been rewritten in the transition from a dominant electric field driven (E-model) process to a current/charge fluence driven one (1/E-model). To do this, a Taylor expansion of (8) has been performed around a given $V_{GS,0}$ value greater than $V_{GS,crit}$ in the interval of red data in Fig. 3. To observe this model transition in (8), $X(V_{GS}) << 1$ has been assumed. As a result, this expression is derived

$$\ln(t_{BD-total}) \approx \ln(A_0) + \left[\frac{\Delta H_0}{kT} - \gamma\cdot(V_{GS}-V_0)\right] + \frac{\gamma\cdot X(V_{GS,0})}{1+X(V_{GS,0})}\cdot\left(1-\frac{(B+H)\cdot t_{ox}}{\gamma\cdot(V_{GS,0}-V_0)}\right)\cdot(V_{GS}-V_{GS,0}). \quad (9)$$

From (9), one can define new activation energy for bond or coordination breakage ($\Delta H_0'$) and voltage acceleration factor (γ') as (10) and (11) respectively:

$$\Delta H_0' = \Delta H_0\cdot\left[1-\frac{\gamma\cdot(V_{GS,0}-V_0)\cdot kT\cdot X(V_{GS,0})}{\Delta H_0\cdot(1+X(V_{GS,0}))}\times\left(1-\frac{(B+H)\cdot t_{ox}}{\gamma\cdot(V_{GS,0}-V_0)}\right)\right] \quad (10)$$

$$\gamma' = \gamma\cdot\left[1-\frac{X(V_{GS,0})}{1+X(V_{GS,0})}\cdot\left(1-\frac{(B+H)\cdot t_{ox}}{\gamma\cdot(V_{GS,0}-V_0)}\right)\right]. \quad (11)$$

According to this, it can be inferred that $\Delta H_0' < \Delta H_0$ and $\gamma' < \gamma$, as $X(V_{GS,0}) > 0$ is always accomplished, while $\gamma\cdot(V_{GS,0}-V_0) < \Delta H_0/kT$ and $\gamma > ((B+H)\cdot t_{ox})/(V_{GS,0}-V_0)$ are fulfilled for the values measured in the present work. Notice that such a result differs from the experimental ones observed in Fig. 3, i.e., $\gamma' > \gamma$, where $\Delta H_0' > \Delta H_0$ can be also deduced. These changes cannot be only explained by the 1/E-model which considers FN conduction and carrier generation mechanisms. Thus, an additional phenomenon could be modulating ΔH_0 and γ: an electric field-driven coordination breakage due to carrier generation by impact ionization. In this process, two dielectric-averaged states of P_{eff} appear, one dominated by electrons and another involving holes or both [31], [32], [41], due to Si-O bonds modification by a high $\vec{E}_{loc}$ applied to the SiO_2 molecule when carrier generation by impact ionization takes place. When this occurs, Si ions can change their covalent bond to an ionic one (Pucker configuration), especially in strained bonds at the SiC/SiO_2 interface [9], [34]. As a result, an abrupt change in P_{eff} and in turn, in γ, is expected according to (4) and the values presented for each type of bond in Section II. From now on, this hypothesis is assessed by the tests outlined in Section III.

To check whether any possible event related to charge carrier generation by impact ionization or mobile ions release from the SiC/SiO_2 interface [5] occurs during TDDB tests, I_G is monitored when V_{GS} ranges from 40.0 to 43.5 V (Fig. 4). Two different behaviors can be observed, depending on V_{GS}. For measurements performed at V_{GS} < 42.5 V, I_G first presents a nearly constant plateau with a slight decrease followed by an exponential decay. This decay should be associated to the release of mobile ions used for the passivation of dangling bonds, which decrease the electric field in the SiC/SiO_2 interface and widen the effective tunneling barrier width during electrical stress [42]–[46]. This I_G pattern matches the expected one without involving any positive charge trapping in the dielectric, since the mobile ions travel towards the semiconductor without reaching the gate contact due to the V_{GS} polarity, as discussed further on.

For tests at $V_{GS} \geq$ 42.5 V, a transient increase in I_G can be observed, forming a current peak. This rise is more pronounced as V_{GS} increases. After this initial growth in I_G between 0.5 h to 1 h (depending on V_{GS}), I_G decreases as a result of the electron trapping in the new created defects until failure occurs, as already observed for V_{GS} < 42.5 V. Similar peaks in I_G have been reported in the literature. In Si and 4H-

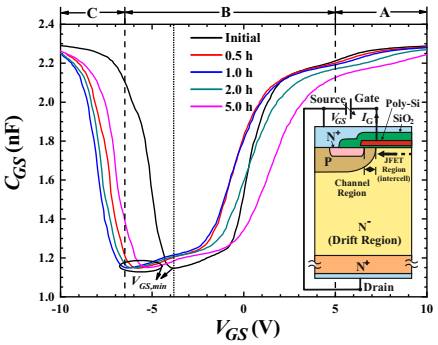

Fig. 5: C_{GS} evolution during TDDB tests at V_{GS}= $V_{GS,crit}$ = 42.5 V (room temperature).

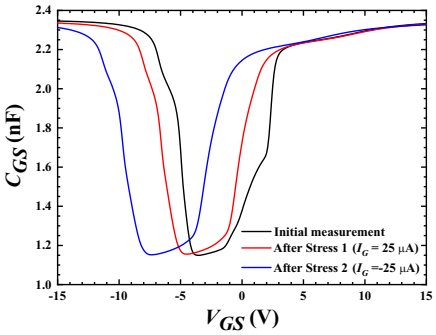

Fig. 6: C_{GS} characterization of a pristine device at room temperature.

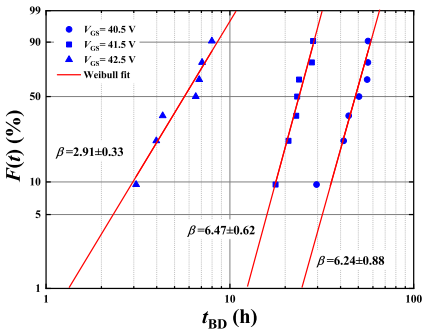

Fig. 7: Weibull plot for t_{BD} extracted at several V_{GS} stresses.

SiC MOS capacitors with $t_{ox} > 10$ nm, prior works [43]–[45] point out that the I_G rise is a consequence of the reduction of the effective tunneling barrier width due to the holes generated by impact ionization and trapped near the semiconductor/SiO_2 interface, which are balanced, in turn, by the recombination with electrons injected through FN tunneling [47]. In thinner gate oxides ($t_{ox} < 10$ nm) on Si, Okada *et al.* [42] reported a similar I_G peak pattern, but delayed after the initial I_G plateau due to holes generation in the anode (semiconductor) according to AHI model. In 4H-SiC LDMOS manufactured with heavy NO-annealed SiO_2 [46], the same pattern is found due to the positive trapped charge near the SiC/SiO_2 interface generated by impact ionization as well.

Unfortunately, the physical insight into γ change in Fig. 3 is not directly supported by the literature results for the following reasons. First, the energy loss originated from the interaction between charge carriers and the SiO_2 molecules is not sufficient to create defects by displacing ions, nor to differentiate among them. Second, carrier generation by impact ionization is not a necessary condition to induce this behavior. Only a high electric field should be locally achieved to enhance J_{FN} current and internally modify the Si ion position within the SiO_2 molecule. For instance, in [43], a similar behavior to that of Fig. 4 is qualitatively measured without carrier generation, as, according to (6), a higher electric field, i.e., $\geq 11.8\,\mathrm{MV\,cm^{-1}}$, was required to generate charge carriers by impact ionization in the considered samples ($t_{ox} = 20$ nm). Third, despite prior research on the trapping of impact generated holes by $\vec{E}_{loc}$-created dangling bonds, no explanation is provided about the origin of the negative trapped carriers required to understand the I_G pattern of Fig. 4 [44], [46]. Therefore, released mobile ions or charge carriers start to appear at $V_{GS} = 42.5$ V, but their typology should be identified. Moreover, P_{eff} is the only parameter that distinguishes these two states in γ depending on the $\vec{E}_{loc}$ strength, residual strain, and charge type trapped at or near the SiC/SiO_2 interface [34].

To gain a better insight into the I_G pattern of Fig. 4 in terms of the involved carriers (holes or mobile ions), several C_{GS}-V_{GS} measurements were run in two devices after undergoing different stress conditions as mentioned in Section III. Fig. 5 shows for $V_{GS} = V_{GS,crit} = 42.5$ V, the evolution of C_{GS}-V_{GS} characteristics at several time instants during TDDB tests, i.e.: initial, 0.5 h, 1.0 h, 2.0 h, and 5.0 h, together with a typical MOSFET basic cell for assisting the interpretation (see inset). $V_{GS,min}$ refers to the V_{GS} value at which C_{GS} reaches its minimum. Focusing on the initial $C_{GS}(V_{GS})$ curve, several regimes associated to the net charge located near to or at SiC/SiO_2 interface can be directly linked to certain device areas (the channel and JFET regions [48]) at which electrons are injected into the oxide layer during TDDB tests, as highlighted in the inset of Fig. 5. Thus, the shifts in the C_{GS} curve correspond to: the channel area when $V_{GS} > 5$ V (regime A), both channel and JFET region areas when $V_{GS,min} \leq V_{GS} \leq 5$ V (regime B), and the JFET region when $V_{GS} < V_{GS,min}$ (regime C) [48].

During the first hour of stress, a significant C_{GS} shift towards the left is observed in regime C (JFET region), while in regime A (channel), it slightly moves to the right. This is a consequence of different processes. In the JFET region, positive charges (holes or mobile ions) are trapped, while in the channel, mobile ions are released from the SiC/SiO_2 interface due to a scattering with the electrons injected into the dielectric by FN, leaving a net negative charge at the SiC/SiO_2 interface due to dangling bonds depassivation. These mobile ions are expected to travel to the semiconductor side (anode), as assessed further on. Consequently, a decrease in the slope dC_{GS}/dV_{GS} in regime B when $V_{GS,min} \leq V_{GS} < 1$ V and a wider C_{GS} valley are observed as a result of the net charge variation near or at the SiC/SiO_2 interface. In correlation to the pattern observed in Fig. 4, the main contribution to the I_G peak comes from the higher electron injection from the JFET region, as the FN conduction is enhanced in this area due to the positive charges in the oxide ($\vec{E}_{loc}$ rises) and slightly reduced in the channel due to depassivated dangling bonds ($\vec{E}_{loc}$ slightly decreases). In the subsequent time instants, the drift direction is maintained more markedly in regime A, while reverted in regimes B and C; still noticing a moderate decrease in dC_{GS}/dV_{GS} when $V_{GS,min} \leq V_{GS} < 2.5$ V and C_{GS} valley widens. These tendencies can be understood as a major damage of the SiC/SiO_2 interface due to electron scattering at both the channel (regime A) and JFET region (regime C) areas. This boosts the dangling bonds depassivation rate, widens the potential barrier and reduces $\vec{E}_{loc}$ at the SiC/SiO_2 interface, which decreases the electron injection by FN. In comparison to Fig. 4, this, jointly with the electron capture within the dielectric, explains the I_G decrease after 2 h of stress in great detail. Moreover, both phenomena agree with the change observed in the I_G decrease rate in Fig. 4 after 1.5 h of stress time. At the end of this $C_{GS}(V_{GS})$ characterization,

the capacitance curve does not recover its initial shape due to the dangling bonds depasivation (negatively charged) at SiC/SiO_2 interface, mainly at the channel area, and positive charge trapped within the oxide, especially at the JFET region.

To determine whether this positive trapped charge comes from holes or SiC/SiO_2 interface-released ions, such as N^+ [49], a second C_{GS} characterization in a pristine device is performed in two steps, as Fig. 6 presents. The first stress at I_G = +25 µA has induced a left shift of all the $C_{GS}(V_{GS})$ curve, as it was expected, without observing dangling bonds generation on top of the channel area (regime A). On the contrary, the subsequent stress at I_G = -25 µA did not result in the expected right shift of the $C_{GS}(V_{GS})$ curves if mobile ions were involved. Instead of this, this negative stress resulted in an additional left shift of all the $C_{GS}(V_{GS})$ curve (see Fig. 6), noticing a slight left drift in regime A due to holes capture by $\vec{E}_{loc}$-created neutral dangling bonds at or near the SiC/SiO_2 interface. In all this process, impact ionization and hole trapping occur simultaneously, being consistent with the conclusions of [44], [50] and $V_{GS,crit}$ predictions of (6).

To evidence that the failure mode evolves according to a P_{eff} mixed state as predicted by thermochemical model, β of the t_{BD} data set has been extracted for different V_{GS} values. Fig. 7 depicts F(t) dependence on t_{BD} data at V_{GS} values of 40.5, 41.5 and 42.5 V. From this graph, it may be inferred that β is the same for $V_{GS} < 42.5$ V, reducing its value at $V_{GS} = 42.5$ V. This steep change in β indicates a P_{eff} variation due to carrier trapping, as stated in Section II.

B. γ' Correction and Practical Guidelines for TDDB Tests

To expedite the testing process, it is necessary to develop a new strategy for estimating the proper t_{BD} from extracted parameters in TDDB measurements at $V_{GS} > V_{GS,crit}$, when FN injection is the predominant mechanism (i.e., $I_{G,FN} > 0.95$). This approach should involve inferring γ and the dimensionless independent term $\mathscr{A}_0$ from their modified values as a result of P_{eff} transition, i.e., γ' and $\mathscr{A}'_0$. Specifically, $\mathscr{A}'_0$ and $\mathscr{A}_0$ are defined respectively as $\mathscr{A}'_0 = \ln(\frac{A_0}{t_0}) + \frac{\Delta H'_0}{kT}$ and $\mathscr{A}_0 = \ln(\frac{A_0}{t_0}) + \frac{\Delta H_0}{kT}$, where t_0 is 1 h. To determine the relationship between γ and γ', (4) is used to derive a correction factor ϑ that accounts for the P_{eff} state attained for a given V_{GS} value relative to $V_{GS,crit}$, as follows:

$$\vartheta = \frac{\gamma}{\gamma'} = \frac{\eta' \cdot r_0}{\eta \cdot r'_0} \cdot \left[\frac{1 + L_{eff} \cdot (K_{ox} - 1)}{1 + L'_{eff} \cdot (K_{ox} - 1)}\right] \cdot \frac{T' \cdot t'_{ox}}{T \cdot t_{ox}}, \quad (12)$$

which is valid for any dielectric (η, t_{ox}, r_0) and stretched degree of the Si-O bond within the interface (r'_0). Even, (12) enables the comparison of the behavior between devices stressed at V_{GS} values lower or higher than $V_{GS,crit}$ with different: layouts/electric field boundary conditions (L_{eff}), oxide thicknesses (t_{ox}), and stress temperatures (T). Besides, the stretching/strain factor at the SiC/SiO_2 interface, defined as $\Xi = (r'_0/r_0) - 1$, can be extracted. Typically, a Si-O bond can support a tensile load such that r_0 can be increased by 20% (i.e., $\Xi = 0.2$) of its initial value without breaking [34].

To deduce the relation between the dimensionless parameters $\mathscr{A}_0$ and $\mathscr{A}'_0$, the following steps have been followed. First, (2) has been linearized by applying the natural logarithm, and has been made dimensionless by subtracting $\ln(t_0)$ on both sides. After this, the parameters at a given point ($V_{GS,0}$, $[t_{BD}(V_{GS,0})]/t_0$) such that $V_{GS,0} \geq V_{GS,crit}$ are written as

$$\ln\left[\frac{t_{BD}(V_{GS})}{t_0}\right] = \ln\left[\frac{t_{BD}(V_{GS,crit})}{t_0}\right] - \gamma' \cdot \left[V_{GS} - V_{GS,crit}\right], \quad (13)$$

where ($V_{GS,crit}$, $\frac{t_{BD}(V_{GS,crit})}{t_0}$) is a given point of (13) to extract γ' and $\mathscr{A}'_0$, calculated as

$$\mathscr{A}'_0 = \ln\left[\frac{t_{BD}(V_{GS,crit})}{t_0}\right] + \gamma' \cdot V_{GS,crit}. \quad (14)$$

To make (13) valid for $V_{GS,0} < V_{GS,crit}$, it is necessary to substitute γ' by $\gamma' \cdot \vartheta$ in (13) and compute $\mathscr{A}_0$ as

$$\mathscr{A}_0 = \ln\left[\frac{t_{BD}(V_{GS,crit})}{t_0}\right] + \gamma' \cdot \vartheta \cdot V_{GS,crit}. \quad (15)$$

To express $\mathscr{A}_0$ in terms of $\mathscr{A}'_0$, ϑ, and γ', (15) is rewritten using (14), as follows

$$\mathscr{A}_0 = \mathscr{A}'_0 - (1 - \vartheta) \cdot \gamma' \cdot V_{GS,crit}. \quad (16)$$

Prior to establishing a procedure for extracting γ and $\mathscr{A}_0$ from the devices studied in this work, ϑ^{-1} values obtained experimentally (ϑ^{-1}_{Exp}) are compared to the predictions provided by (12) (ϑ^{-1}_{Calc}) to assess whether (12) is applicable beyond the present study. To this end, Table I presents, together with the results obtained in the present work, $\log(e) \cdot \gamma$, $\log(e) \cdot \gamma'$, and ϑ^{-1}_{Exp} directly extracted from TDDB tests reported in the literature, performed on commercial 4H-SiC 1.2 kV MOSFETs (Gajewski *et al.* [17], Santini *et al.* [18], Liu *et al.* [19]), research-grade 4H-SiC 1.2 kV DMOSFETs (Matocha *et al.* [24]), and MOS capacitors used as test structures implemented on both 4H-SiC (Gurfinkel *et al.* [45], Matocha *et al.* [24]) and Si (thin dielectric layer, Abadeer *et al.* [51]). Table I also contains the other variables required to evaluate (12) and eventually determine ϑ^{-1}_{Calc}, i.e., T, t_{ox}, r'_0/r_0, L_{eff}, L'_{eff}, δ and δ'. In this table, L_{eff} (L'_{eff}) and δ (δ') have been inferred from $\log(e) \cdot \gamma$ ($\log(e) \cdot \gamma'$) using (4) and (5), respectively. In these calculations, $r_0 = 1.7$ nm has been assumed [9], as no bonding modification is expected along the gate dielectric thickness, only at or close to the dielectric/semiconductor interface in certain situations mentioned above. Table I also includes the experimental errors properly determined for each variable, to facilitate comparison and analysis. Regarding η/η', this ratio and its associated error have been calculated respectively as the mean and twice the standard deviation values corresponding to a set of numbers calculated as $\eta(m,2)/\eta(m,1)$, where m ranges from 6 to 12. Finally, r'_0/r_0 has been used as a fit parameter to match ϑ^{-1}_{Calc} to ϑ^{-1}_{Exp}, not providing any error in this calculation. In general, the values for $\log(e) \cdot \gamma$ and $\log(e) \cdot \gamma'$ for SiO_2 layers on 4H-SiC substrates provide a higher P_{eff} (twice) than typical values reported for thinner oxides and smaller devices/test structures in Si [34], [35]. In fact, the higher values in δ and δ' can be associated to higher $\vec{E}_{loc}$ fields resulting from the boundary conditions mainly fixed by the layout [52], where $\delta \approx 2$ is reported for MOS capacitors on Si. As a result, higher L_eff and L'_eff can be achieved in the case of 4H-SiC substrates.

TABLE I
COMPARISON OF $\log(e)\cdot\gamma$, $\log(e)\cdot\gamma'$, ϑ_{Exp}^{-1} AND ϑ_{Calc}^{-1} DETERMINED IN THIS WORK WITH THOSE EXTRACTED FROM TDDB TESTS REPORTED ON COMMERCIALLY-AVAILABLE AND RESEARCH-GRADE 4H-SIC 1.2 KV MOSFETS, AS WELL AS MOS CAPACITORS IMPLEMENTED ON 4H-SIC AND SI SUBSTRATES. T, t_{ox}, r_0'/r_0, L_{eff}, L_{eff}', δ AND δ' FOR EACH CASE ARE ALSO INCLUDED. N.A. MEANS "NOT AVAILABLE".

Data Source	$\log(e)\cdot\gamma$ (V^{-1})	$\log(e)\cdot\gamma'$ (V^{-1})	T (°C)	t_{ox} (nm)	η/η' ( )	ϑ_{Exp}^{-1} ( )	ϑ_{Calc}^{-1} ( )	r_0'/r_0 ( )	L_{eff} ( )	L_{eff}' ( )	δ ( )	δ' ( )
This work[a]	0.450 ±0.026	0.930 ±0.016	150	53.0		2.07 ±0.25	2.06 ±0.02	1.16	1.46 ±0.16	1.46 ±0.14	2.67 ±0.29	2.67 ±0.25
Gajewski et al. [17][a]	0.300 ±0.031	N.A.	150	53.0		1.83 ±0.22	1.83 ±0.04	1.00	0.86 ±0.09	N.A.	1.78 ±0.18	N.A.
Santini et al. [18][a]	*Gajewski et al.* used	0.550 ±0.031	150	62.5					*Gajewski et al.* used	1.12 ±0.06	*Gajewski et al.* used	2.15 ±0.12
T. Liu et al. [19][a]	*Gajewski et al.* used	0.397 ±0.008	28	45.0	1.78 ±0.04	1.32 ±0.28	1.32 ±0.03	1.00	*Gajewski et al.* used	0.20 ±0.01	*Gajewski et al.* used	0.80 ±0.02
	Gajewski et al. used	0.697 ±0.039	150	45.0		2.31 ±0.21	2.32 ±0.05	1.18	*Gajewski et al.* used	0.99 ±0.05	*Gajewski et al.* used	1.97 ±0.11
	Gajewski et al. used	0.801 ±0.062	175	45.0		2.67 ±0.43	2.67 ±0.06	1.18	*Gajewski et al.* used	1.28 ±0.10	*Gajewski et al.* used	2.40 ±0.18
Gurfinkel et al. [45][b]	0.142 ±0.007	0.269 ±0.015	230	43.0		1.89 ±0.14	1.88 ±0.04	1.06	0.21 ±0.10	0.21 ±0.12	0.82 ±0.04	0.82 ±0.05
Matocha et al. [24][b, c]	0.163 ±0.008[c]	0.518 ±0.042[c]	200	43.0		3.17 ±0.60[c]	3.17 ±0.07	1.20	0.25 ±0.01	0.54 ±0.04	0.88 ±0.04	1.30 ±0.11
	0.200 ±0.015[b]	0.491 ±0.015[b]	200	43.0		2.45 ±0.20[b]	2.45 ±0.05	1.20	0.38 ±0.03	0.49 ±0.01	1.08 ±0.08	1.23 ±0.04
Abadeer et al. [51][d]	0.890 ±0.020	1.148 ±0.031	30	10		1.29 ±0.05	1.29 ±0.04	1.00	0.14 ±0.01	0.0052 ±0.0001	0.71 ±0.02	0.52 ±0.01

[a] Commercial 4H-SiC 1.2 kV MOSFETs; [b] MOS capacitors on 4H-SiC; [c] Research-grade 4H-SiC DMOSFETs; [d] MOS capacitors on Si.

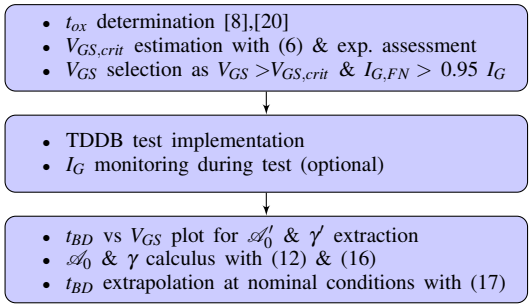

Fig. 8: Workflow diagram for t_{BD} determination at nominal operation conditions.

In the case of commercial 4H-SiC 1.2kV MOSFETs, $\log(e)\cdot\gamma$ and $\log(e)\cdot\gamma'$ are not available for each TDDB test but, thanks to (13), all involved variables can be linked between different technologies and TDDB tests conditions. This makes the determination of ϑ^{-1} possible in each case by taking the data when $V_{GS} < V_{GS,crit}$ or $V_{GS} > V_{GS,crit}$. Thus, $\log(e)\cdot\gamma$ is extracted from [17], while $\log(e)\cdot\gamma'$ is inferred from [18] and [19] at several T's. According to this comparison, ϑ_{Calc}^{-1} agrees with ϑ_{Exp}^{-1} and Ξ ranges from 0.00 to 0.18, being lower than the maximum value expected in the literature (0.20 [34]).

In the case of the present work, research-grade devices [24] and test structures [45] on 4H-SiC, $\log(e)\cdot\gamma$ and $\log(e)\cdot\gamma'$ are available for each TDDB test. In [24], the highest value for ϑ_{Exp}^{-1} is observed in the 1.2 kV 4H-SiC DMOSFET, probably as a result of the gate dielectric breakdown mechanism transitioning from E-model to 1/E-model, while a sudden change in γ occurs. This transition between models close to $V_{GS,crit}$ can be attributed to a gate dielectric layer with a poorer quality (higher traps density), as the high strain inferred suggests ($r_0'/r_0 = 1.2$). Moreover, $L_{eff} \neq L_{eff}'$ and $r_0'/r_0 = 1.2$ also support this behavior for the test structures presented in [24], as $\vec{E}_{loc}$ is modified. By contrast, in [45] and the present work, $L_{eff} = L_{eff}'$ and $r_0'/r_0 < 1.2$ are derived. In the case of studies carried out in gate oxides on Si, thin dielectrics in MOS capacitors have been analyzed. Again, ϑ_{Calc}^{-1} and ϑ_{Exp}^{-1} agree and $L_{eff} \neq L_{eff}'$. Here, the impact generation is produced outside the SiO_2, and the carrier dynamics reduce $\vec{E}_{loc}$, as L decreases [36], [52].

As a result, it has been observed that when the SiO_2 degradation mechanisms are provoked by thermochemical stress and FN conduction, $\Xi < 0.20$. This fact provides a criterion for evaluating (12) and (16) to infer γ and $\mathscr{A}_0$: calculate them considering $\Xi = 0$ and $\Xi = 0.20$ and determine their mean and standard deviation values to also estimate the error. Proceeding like this, $\log(e)\cdot\gamma_{Calc} = 0.480 \pm 0.043$ and $\mathscr{A}_{0,Calc} = 49.65 \pm 4.32$ are obtained that in comparison to the values extracted from the fitting, i.e., $\log(e)\cdot\gamma_{Exp} = 0.450 \pm 0.026$ V^{-1} and $\mathscr{A}_{0,Exp} = 49.61 \pm 4.32$, the proposed method provides a deviation lower than 10%. In the case of Gurfinkel *et al.* [45], a good match is also observed: $\log(e)\cdot\gamma_{Calc} = 0.152 \pm 0.014$ V^{-1} and $\mathscr{A}_{0,Calc} = 17.04 \pm 0.93$, while the values extracted from the fitting are $\log(e)\cdot\gamma_{Exp} = 0.142 \pm 0.007$ V^{-1} and $\mathscr{A}_{0,Exp} = 18.23 \pm 0.40$.

Fig. 8 depicts the workflow to infer t_{BD} at nominal conditions $[t_{BD}(V_{GS,n})]$ from TDDB tests carried out at $V_{GS} > V_{GS,crit}$ and under FN conduction. First, t_{ox} is found by indirect [6] or direct measurements [18] to calculate $V_{GS,crit}$ with (6). Next, this value is determined in several devices to assure that around $V_{GS,crit}$, the current transport is mainly due to FN (see Fig. 2). Then, the V_{GS} stress range is fixed by $V_{GS} > V_{GS,crit}$ and $I_{G,FN} > 0.95\ I_G$. At this point, TDDB tests are set and ready to start. Optionally, during the tests, I_G can be monitored to assess whether holes generation takes place. After the tests, the measured t_{BD} is plotted as a function of V_{GS} to extract

γ' and $\mathscr{A}'_0$. To obtain γ and $\mathscr{A}_0$, γ' and $\mathscr{A}'_0$ are corrected according to (12) and (16). Finally, known γ and $\mathscr{A}_0$, t_{BD} is extrapolated at nominal operation V_{GS} conditions ($V_{GS,n}$) with

$$t_{BD}(V_{GS,n}) = t_0 \cdot \exp\left[\mathscr{A}_0 - \gamma \cdot V_{GS,n}\right]. \tag{17}$$

V. Conclusions

The impact of TDDB test conditions on accurately estimating the oxide intrinsic lifetime has been investigated in SiC power MOSFETs. Specifically, the behavior of the device dielectric layer has been studied under high gate bias when only the Fowler-Nordheim conduction mechanism occurs. Unfortunately, these stress conditions have led to an overestimation of the voltage acceleration factor γ, resulting in overly optimistic forecasts for the oxide lifetime under nominal operation. To address this issue, several physics-based strategies have been proposed to establish criteria to properly set TDDB conditions and infer a correction factor from the thermochemical model, which relates the regimes of the voltage acceleration coefficient γ. Their effectiveness has been demonstrated by comparing the results obtained to those reported in the literature. The accuracy of the predictions enables not only a significant reduction in the duration of TDDB test (from months to a few hours), but also the optimization of gate driving to achieve lower losses for a desired device lifetime. Finally, guidelines have been provided to facilitate the effective implementation of TDDB testing in industrial scenarios and to complement the current qualification standard for SiC power MOSFETs.

References

[1] Y. Nakakohara, H. Otake, T. M. Evans, T. Yoshida, M. Tsuruya, and K. Nakahara, "Three-phase LLC series resonant DC/DC converter using SiC MOSFETs to realize high-voltage and high-frequency operation," *IEEE Trans. Ind. Electron.*, vol. 63, no. 4, pp. 2103–2110, 2016, doi:10.1109/TIE.2015.2499721.

[2] H. Li, Z. Zhang, S. Wang, J. Tang, X. Ren, and Q. Chen, "A 300-kHz 6.6-kW SiC bidirectional LLC onboard charger," *IEEE Trans. Ind. Electron.*, vol. 67, no. 2, pp. 1435–1445, 2019, doi:10.1109/TIE.2019.2910048.

[3] J. O. Gonzalez, R. Wu, S. Jahdi, and O. Alatise, "Performance and reliability review of 650 V and 900 V Silicon and SiC devices: MOSFETs, cascode JFETs and IGBTs," *IEEE Trans. Ind. Electron.*, vol. 67, no. 9, pp. 7375–7385, 2020, doi:10.1109/TIE.2019.2945299.

[4] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A survey of wide bandgap power semiconductor devices," *IEEE Trans. Power Electron.*, vol. 29, no. 5, pp. 2155–2163, 2014, doi:10.1109/TPEL.2013.2268900.

[5] M. Cabello, V. Soler, G. Rius, J. Montserrat, J. Rebollo, and P. Godignon, "Advanced processing for mobility improvement in 4H-SiC MOSFETs: A review," *Mater. Sci. Semicond. Process.*, vol. 78, pp. 22–31, 2018, doi:10.1016/j.mssp.2017.10.030.

[6] O. Aviñó-Salvadó, B. Asllani, C. Buttay, C. Raynaud, and H. Morel, "Extraction of the 4H-SiC/SiO2 barrier height over temperature," *IEEE Trans. Electron Devices*, vol. 67, no. 1, pp. 63–68, 2019, doi:10.1109/TED.2019.2955181.

[7] K. Matocha, "Challenges in sic power mosfet design," *Solid-State Electronics*, vol. 52, no. 10, pp. 1631–1635, 2008.

[8] L. Zhao, "Surface defects in 4H-SiC homoepitaxial layers," *Nanotechnology and Precision Engineering*, vol. 3, no. 4, pp. 229–234, 2020, doi:10.1016/j.npe.2020.12.001.

[9] J.-W. McPherson, "Time dependent dielectric breakdown physics–models revisited," *Microelectron. Reliab.*, vol. 52, no. 9-10, pp. 1753–1760, 2012, doi:10.1016/j.microrel.2012.06.007.

[10] M. Boero, A. Oshiyama, and P. L. Silvestrelli, "E' centers in silicon dioxide: First-principles molecular dynamics studies," *Mod. Phys. Lett. B*, vol. 18, no. 15, pp. 707–724, 2004, doi:10.1142/S0217984904007256.

[11] Joint Electron Device Engineering Council (JEDEC) Solid State Technology Association, *JEDEC Standard - Procedure for Characterizing Time-Dependent Dielectric Breakdown of Ultra-Thin Gate Dielectrics, JESD92*, Aug. 2003.

[12] D. Gajewsky, "Challenges and peculiarities in developing new standards for SiC," in *2020 IEEE Int. Rel. Phys. Symp. (IRPS)*, vol. 615, 2020, pp. 311–314, doi:10.4028/www.scientific.net/MSF.615-617.311.

[13] O. A. Salvado, H. Morel, C. Buttay, D. Labrousse, and S. Lefebvre, "Threshold voltage instability in SiC MOSFETs as a consequence of current conduction in their body diode," *Microelectron. Reliab.*, vol. 88, pp. 636–640, 2018, doi:10.1016/j.microrel.2018.06.033.

[14] H. Luo, F. Iannuzzo, and M. Turnaturi, "Role of threshold voltage shift in highly accelerated power cycling tests for SiC MOSFET modules," *IEEE Trans. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 2, pp. 1657–1667, 2020, doi:10.1109/JESTPE.2019.2894717.

[15] B. Asllani, A. Castellazzi, O. A. Salvado, A. Fayyaz, H. Morel, and D. Planson, "$V_T H$-hysteresis and interface states characterisation in SiC Power MOSFETs with Planar and Trench Gate," in *2019 IEEE Int. Rel. Phys. Symp. (IRPS)*. IEEE, 2019, pp. 1–6.

[16] JEDEC Solid State Technology Association, *Guideline for evaluating Bias Temperature Instability of Silicon Carbide Metal-Oxide-Semiconductor Devices for Power Electronic Conversion, JEP 184*, Mar. 2021.

[17] D.A. Gajewski *et al.*, "SiC power device reliability," in *IEEE Int. Integr. Rel. Workshop (IIRW)*, 2016, pp. 29–34, doi:10.1109/IIRW.2016.7904895.

[18] T. Santini, M. Sebastien, M. Florent, L.-V. Phung, and B. Allard, "Gate oxide reliability assessment of a SiC MOSFET for high temperature aeronautic applications," in *IEEE ECCE Asia Downunder*, 2013, pp. 385–391, doi:10.1109/ECCE-Asia.2013.6579125.

[19] T. Liu, S. Zhu, S. Yu, D. Xing, A. Salemi, M. Kang, K. Booth, M. H. White, and A. K. Agarwal, "Gate oxide reliability studies of commercial 1.2 kV 4H-SiC power MOSFETs," in *2020 IEEE Int. Rel. Phys. Symp. (IRPS)*, 2020, pp. 1–5.

[20] D. t. Lichtenwalner, "Accelerated testing of sic power devices," in *2020 IEEE International Integrated Reliability Workshop (IIRW)*. IEEE, 2020, pp. 1–6.

[21] K. Matocha, I.-H. Ji, X. Zhang, and S. Chowdhury, "SiC power MOSFETs: Designing for reliability in wide-bandgap semiconductors," in *2019 IEEE Int. Rel. Phys. Symp. (IRPS)*, 2019, pp. 1–8, doi:10.1109/IRPS.2019.8720509.

[22] T. Liu, S. Zhu, M. White, A. Salemi, D. Sheridan, and A. Agarwal, "Time-Dependent Dielectric Breakdown of commercial 1.2 kV 4H-SiC power MOSFETs," *IEEE J. Electron Devices Soc.*, vol. 9, pp. 633–639, 2021, doi:10.1109/JEDS.2021.3091898.

[23] J. B. Bernstein, M. Gurfinkel, X. Li, J. Walters, Y. Shapira, and M. Talmor, "Electronic circuit reliability modeling," *Microelectron. Reliab.*, vol. 46, no. 12, pp. 1957–1979, 2006, doi:10.1016/j.microrel.2005.12.004.

[24] K. Matocha, G. Dunne, S. Soloviev, and R. Beaupre, "Time-dependent dielectric breakdown of 4H-SiC MOS capacitors and DMOSFETs," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 1830–1834, 2008, doi:10.1109/TED.2008.926595.

[25] U. Schwalke, M. Pölzl, T. Sekinger, and M. Kerber, "Ultra-thick gate oxides: charge generation and its impact on reliability," *Microelectron. Reliab.*, vol. 41, no. 7, pp. 1007–1010, 2001, doi:10.1016/S0026-2714(01)00058-0.

[26] O. Avino-Salvado, C. Cheng, C. Buttay, H. Morel, D. Labrousse, S. Lefebvre, and M. Ali, "Sic mosfets robustness for diode-less applications," *EPE Journal*, vol. 28, no. 3, pp. 128–135, 2018.

[27] S.-I. Hayashi and K. Wada, "Accelerated aging for gate oxide of sic mosfets under continuous switching conditions by applying advanced htgb test," *Microelectronics Reliability*, vol. 126, p. 114213, 2021.

[28] T. Aichinger and M. Schmidt, "Gate-oxide reliability and failure-rate reduction of industrial sic mosfets," in *2020 IEEE International Reliability Physics Symposium (IRPS)*. IEEE, 2020, pp. 1–6.

[29] M. Beier-Moebius and J. Lutz, "Breakdown of gate oxide of sic-mosfets and si-igbts under high temperature and high gate voltage," in *PCIM Europe 2017; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*. VDE, 2017, pp. 1–8.

[30] K. P. Cheung, "Sic power mosfet gate oxide breakdown reliability—current status," in *2018 IEEE International Reliability Physics Symposium (IRPS)*. IEEE, 2018, pp. 2B–3.

[31] E. Y. Wu, "Facts and myths of dielectric breakdown processes—part I: Statistics, experimental, and physical acceleration models," *IEEE Trans. Electron Devices*, vol. 66, no. 11, pp. 4523–4534, 2019, doi:10.1109/TED.2019.2933612.

[32] J.-W. McPherson and H. Mogul, "Underlying physics of the thermochemical E-model in describing low-field time-dependent dielectric breakdown in SiO_2 thin films," *J.Appl. Phys.*, vol. 84, no. 3, pp. 1513–1523, 1998, doi:10.1063/1.368217.

[33] A. Shanware, R. B. Khamankar, and J.-W. McPherson, "Resolving the non-uniqueness of the activation energy associated with TDDB for SiO_2 thin films," in *Int. Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138)*, 2000, pp. 549–552, doi:10.1109/IEDM.2000.904378.

[34] J.-W. McPherson, "Extended Mie-Grüneisen molecular model for time dependent dielectric breakdown in silica detailing the critical roles of O–Si≡O3 tetragonal bonding, stretched bonds, hole capture, and hydrogen release," *J.Appl. Phys.*, vol. 99, no. 8, p. 083501, 2006, doi:10.1063/1.2189930.

[35] J. W. McPherson, "Determination of the nature of molecular bonding in silica from time-dependent dielectric breakdown data," *J.Appl. Phys.*, vol. 95, no. 12, pp. 8101–8109, 2004, doi: 10.1063/1.1728288.

[36] J.-W. McPherson, "Lorentz factor determination for local electric fields in semiconductor devices utilizing hyper-thin dielectrics," *J.Appl. Phys.*, vol. 118, no. 20, p. 204106, 2015, doi:10.1063/1.4936271.

[37] I.-C. Chen, S. Holland, and C. Hu, "Electrical breakdown in thin gate and tunneling oxides," *IEEE Trans. Electron Devices*, vol. 32, no. 2, pp. 413–422, 1985, doi:10.1109/T-ED.1985.21957.

[38] M. Rudan, *Physics of semiconductor devices*. Springer, 2015, doi:10.1007/978-3-319-63154-7.

[39] Cree, *C2M0080120D Silicon Carbide Power MOSFET Datasheet, Rev. C*, Durham, NC, USA, Oct. 2015.

[40] M. N. Sharif and M. N. Islam, "The weibull distribution as a general model for forecasting technological change," *Technol. Forecast. Soc. Change*, vol. 18, no. 3, pp. 247–256, 1980, doi:10.1016/0040-1625(80)90026-8.

[41] K. Okada, M. Kamei, and S. Ohno, "Reconsideration of dielectric breakdown mechanism of gate dielectrics on basis of dominant carrier change model," *IEEE Trans. Electron Devices*, vol. 64, no. 11, pp. 4386–4392, 2017, doi:10.1109/TED.2017.2747580.

[42] K. Okada, K. Kurimoto, and M. Suzuki, "Anomalous TDDB statistics of gate dielectrics caused by charging-induced dynamic stress relaxation under constant–voltage stress," *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2268–2274, 2016, doi:10.1109/TED.2016.2549555.

[43] M. Le-Huu *et al.*, "Investigation of the reliability of 4H-SiC MOS devices for high temperature applications," *Microelectron. Reliab.*, vol. 51, pp. 1345–1350, 2011, doi:10.1016/j.microrel.2011.03.015.

[44] E. Bano, T. Ouisse, C. Leonhard, A. Gölz, and E. S. von Kamienski, "High-field Fowler-Nordheim stress of N-type silicon carbide metal-oxide-semiconductor capacitors," *Semicond. Sci. Technol.*, vol. 12, no. 5, pp. 525–528, 1997, doi:10.1088/0268-1242/12/5/0023.

[45] M. Gurfinkel *et al.*, "Time-dependent dielectric breakdown of 4H-SiC/SiO_2 MOS capacitors," *IEEE Trans. Device. Mater. Reliab.*, vol. 8, no. 4, pp. 635–641, 2008, doi:10.1109/TDMR.2008.2001182.

[46] E. Murakami and M. Okamoto, "Anomalous behavior of gate current and TDDB lifetime by constant voltage stress in NO-annealed SiC-MOSFETs," *IEEE Trans. Electron Devices*, vol. 68, no. 3, pp. 1207–1213, 2021, doi:10.1109/TED.2020.3049114.

[47] N. Xu and R. Latham, "Chapter 5: Electron emission based breakdown mechanisms," in *High Voltage Vacuum Insulation: Basic Concepts and Technological Practice*, R. V. Latham, Ed., 1995, pp. 165–204, doi:10.1016/B978-012437175-0/50009-9.

[48] J. Wei *et. al.*, "Interfacial damage extraction method for SiC power MOSFETs based on CV characteristics," in *2017 29th Int. Symp. on Power Semic. Devices and IC's (ISPSD)*. IEEE, 2017, pp. 359–362, doi:10.23919/ISPSD.2017.7988992.

[49] J. Rozen *et al.*, "Increase in oxide hole trap density associated with nitrogen incorporation at the SiO_2/SiC interface," *J.Appl. Phys.*, vol. 103, no. 12, pp. 124 513(1–5), 2008, doi:10.1063/1.2940736.

[50] D. DiMaria, E. Cartier, and D. Arnold, "Impact ionization, trap creation, degradation, and breakdown in silicon dioxide films on silicon," *J.Appl. Phys.*, vol. 73, no. 7, pp. 3367–3384, 1993, doi:10.1063/1.352936.

[51] W. Abadeer *et al.*, "Correlation between theory and data for mechanisms leading to dielectric breakdown," in *Proc. of 1994 VLSI Technol. Symp.*, 1994, pp. 43–44, doi:10.1109/VLSIT.1994.324386.

[52] J.-W. McPherson, "Polarity dependent thermochemical E-model for describing time dependent dielectric breakdown in metal-oxide-semiconductor devices with hyper-thin gate dielectrics," *J.Appl. Phys.*, vol. 120, no. 10, p. 104102, 2016, doi:10.1063/1.4962320.