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# Towards a Common Mode Current Free Packaging Solution for High Voltage Series Connected SiC MOSFET Switches.

Cedric Mathieu de Vienne<sup>1,2</sup>, Besar Asllani<sup>1</sup>, Hugo Reynes<sup>1</sup>, Martin Guillet<sup>1</sup>, Amin Al-Hinai<sup>3</sup>, Pierre Lefranc<sup>2</sup>, Pierre-Olivier Jeannin<sup>2</sup>, Bruno Lefebvre<sup>1</sup>, Cyril Buttay<sup>4</sup>, Till Huesgen<sup>3</sup>

<sup>1</sup> SuperGrid Institute, 23 Rue Cyprian, CS 50289 69628 Villeurbanne Cedex – France

<sup>2</sup> Univ. Grenoble Alpes, CNRS, Grenoble INP, G2ELAB, 38000 Grenoble, France

<sup>3</sup> Electronics Integration Laboratory, Kempten University of Applied Sciences, Germany

<sup>4</sup> Univ Lyon, CNRS, INSA Lyon, Université Claude Bernard Lyon 1, Ecole Centrale de Lyon, Ampère, UMR5005, 69621, Villeurbanne, France

Corresponding author: Besar Asllani, besar.asllani@supergrid-institute.com

Speaker: Cedric Mathieu de Vienne, cedric.mathieudevienne@supergrid-institute.com

## Abstract

Tests are carried out on two different series-connected switches made of six SiC MOSFETs capable of blocking 10 kV and 20 kV respectively. High voltage capacitors are connected to the drain terminals of the MOSFETs to emulate the common mode currents' paths due to parasitic capacitances of the packaging. Due to high  $dV/dt$ , common mode currents become dangerous to the switch as they unsettle the voltage sharing during turn-off and unbalance switching losses. This could lead some of the MOSFETs to experience avalanche breakdown. A novel packaging approach that suppresses or balances the common mode currents is introduced.

## 1 Introduction

Medium Voltage converters for grid applications require high voltage switching solutions capable of fast and efficient switching. While Wide Band Gap transistors such as SiC MOSFETs and GaN HEMTs have confirmed their advantages compared to Si IGBTs in terms of performance [1], their voltage ratings are still far from the required ones. High Voltage SiC MOSFETs have been demonstrated in the past [2], [3], but their actual cost is prohibitory. Thus, as of March 2023, the highest commercially available voltage rating for discrete and modules is 3.3 kV. One way to overcome this problem is to connect several devices in series. Power electronics topologies such as Neutral Point Clamped converters, Flying Capacitor or Multi-level Modular Converters can also be applied to comply with the high voltage requirements, but they are more complicated to drive and may not have the same advantages in terms of losses and switching speed.

Series connection of switches has been known and applied since the early days of power conversion, but seldom on fast devices such as SiC MOSFETs [4]. The main problem related to the se-

ries connection of individual power semiconductor switches is voltage imbalance between the devices. Depending on the state of a transistor (on, off, transitioning -turn-on, turn-off-), the deviation of its characteristics from their nominal values ( $C_{iss}$ ,  $C_{oss}$ ,  $C_{rss}$ ,  $V_{th}$ ,  $R_{dson}$ ) and its position in the string, it may experience overvoltage and even be destroyed. This can be catastrophic to the switching string and must be prevented at any cost. For this reason, passive solutions such as snubbers and clamping elements or active solutions such as active gate drive have been developed and implemented successfully in silicon or SiC series connected switches [5], [6]. Passive solutions are simple to implement but increase the losses of the assembly while reducing its performance. Active gate drive is a promising new trend which can lead to the suppression or reduction of the snubber thus leading to better performances. Its implementation may be complex and still needs to be demonstrated and compared to snubbers.

One issue with series-connected devices is the driver's power supply. Each gate electrode needs to be biased in a synchronized manner and all the gate drivers need to be powered independently of

the voltage they are sitting at. This requires an isolated power supply capable of withstanding high voltage and providing enough energy for the gate driver to function while introducing the smallest parasitic capacitances. Several solutions exist to either power the gate drivers by collecting the required energy locally [7] or by cascaded power supplies [8]. To avoid this, super-cascode JFETs [9] or MOSFETs [10] solutions have been presented in the past, where only one device is driven externally by a gate driver and the others are biased by a passive circuit (capacitors and diodes) because of the  $dV/dt$  of the first device. While super-cascode shows very promising performances, it is uncertain on how it behaves in an application where the bus voltage or load varies extensively.

Series-connected switches are also prone to conducted EMI. Due to the high potential at which the switches sit at off state and the parasitic capacitances between their terminals and the ground, common mode currents are generated during the switching events. This has several noxious consequences which will be detailed in the next section. The origin of the parasitic capacitances is usually the common mode capacitance of the gate driver/power supply or the packaging. In this paper a solution is proposed to mitigate the parasitic capacitances associated with the packaging.

The paper is organized as follows: introduction, a section where the common mode current paths are analyzed and modeled, a section on the device under test and the test setup, a section on the test results and conclusions.

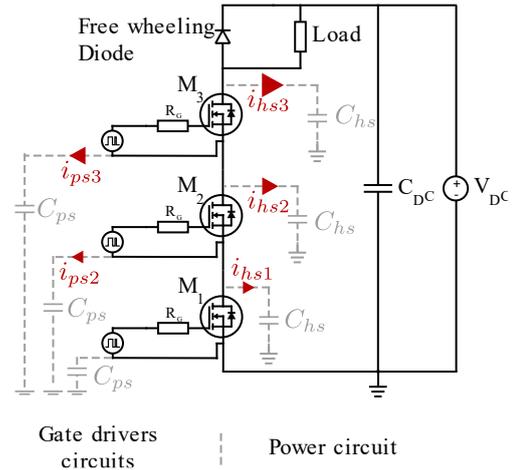
## 2 Common mode currents in series connected switches

### 2.1 The problem with common mode currents

Parasitic capacitances between power terminals and the ground are the focus of this section. As it is modeled in Fig. 1, they provide an additional path to the current in the string during transient events. As a result, different switches in the string are switching at different current levels. Depending on the value of the capacitance and the  $dV/dt$  during the switching event, the common mode current can be a fraction of the load current [11].

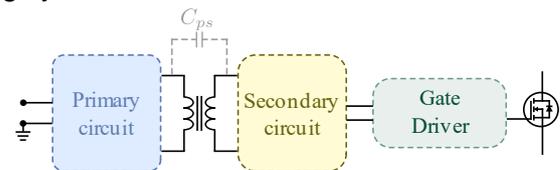
### 2.2 Gate driver power supply common mode currents and mitigation

Gate drivers are connected between the gate and source terminals of each power MOSFETs. Alt-



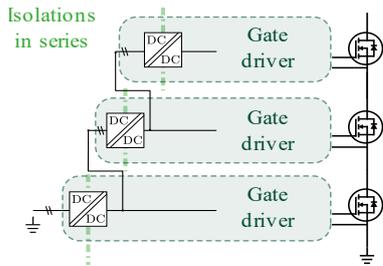
**Fig. 1** Displacement current in parasitic capacitors of gate drivers power supplies isolation and in heat sink isolation connected to the ground.

though they are isolated from the ground, they provide an additional path for the current to flow during the switching event through the common mode capacitance of their power supplies. The common mode capacitance illustrated in Fig. 2 connects the two sides of the isolation barrier. Besides leading to conducted EMI concerns, they can also unsettle the voltage balance of the power MOSFETs, which is highly undesirable.



**Fig. 2** Schematic representation of the gate driver's power supply and its parasitic common mode capacitance between primary and secondary circuits on each side of the isolation barrier.

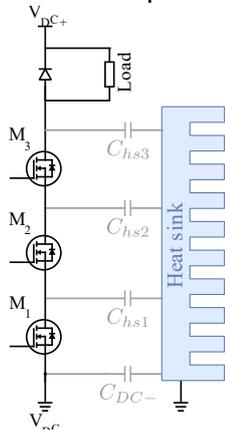
To mitigate the resulting unbalance, one can try to get rid of the common mode capacitance by employing self-supplying strategies or balance the common mode currents [12]. It can be deduced that the only way to balance them is to compensate the value of the common mode capacitances on each single level. In literature there are several strategies that try to reduce the common mode capacitance of higher levels gate drivers, rather than adding capacitances to balance the currents [13]. One elegant strategy, illustrated in Fig. 3, is to connect the power supplies in series so that the resulting common mode capacitances are connected in series [8]. Assuming that the common mode capacitances of each power supply are identical, the resulting parasitic capacitance to ground is a fraction of the single capacitance while the  $dV/dt$  of the terminal to which it is connected is a multiple of the lowest level. As a result, the assembly forms a voltage divider where the voltage is equally shared and the common mode currents are equal.



**Fig. 3** Cascaded power supplies of gate drivers in a series connected switch for common mode current balancing.

### 2.3 Packaging related common mode capacitances

Packaging of a series-connected switch can contribute introduce parasitic capacitances. In order to integrate the solution, it could be interesting to place all the series connected devices on the same support similar to that of a “classical” power module. In this case the thermal impedance of each device to the heat sink is identical, but so does the parasitic capacitance. The parasitic capacitances are modelled as in Fig. 4. Since the  $dV/dt$  depends on the position of the device in the string, the resulting parasitic current will be in exact proportion. This means that the series-connected devices will be switching at different electrical conditions, leading in voltage and power loss uneven distribution. The dangers related to voltage unbalance have been explained in the introduction. Power loss unbalance leads to additional unbalance in terms of operating temperature.



**Fig. 4** Modelling of the common mode parasitic capacitors introduced by the packaging/heat sink of high voltage series connected switch.

Since the conduction resistance of SiC MOSFETs is also related to operating temperature, it can unbalance the on-state losses and lead to a higher thermal disparity amongst the transistors. This can have long term impact on the reliability of the string, as different devices may age at different rates due to operating temperature disparity. The thickness of the ceramic substrate required to

withstand 20 kV in partial discharge free conditions and a clean environment is 3 mm [14]. Based on this value, the parasitic capacitance to ground (assuming that the heat sink is referenced to ground) can be estimated to 23 pF per transistor. Depending on the position of the device in the string,  $dV/dt$  can reach up to 500 V/ns [15] resulting to a common mode current peak of 11.5 A. This value is not negligible (one sixth) compared to the current rating of the power MOSFET.

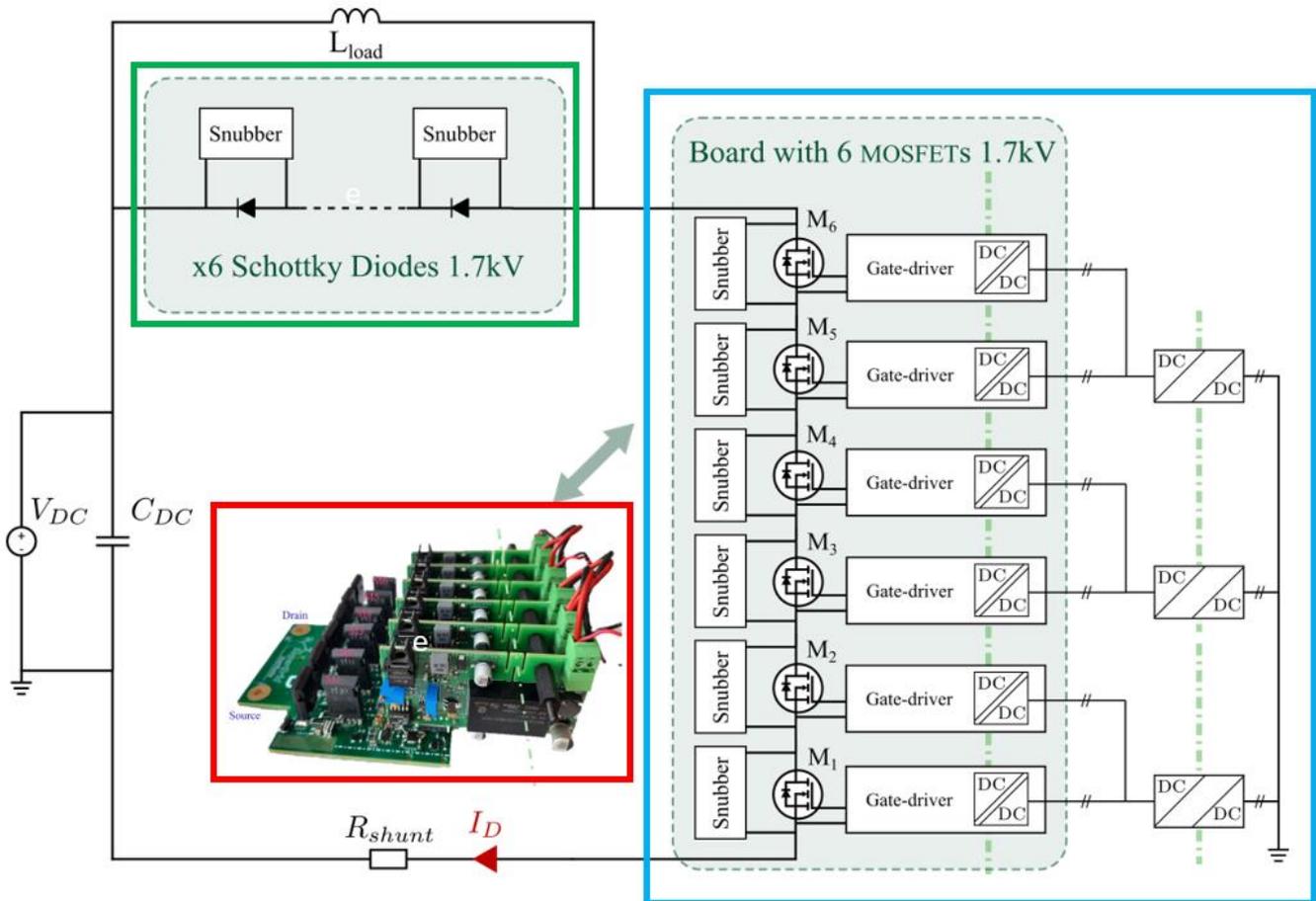
## 3 High Voltage Switch concept and test setup description

### 3.1 The High Voltage Switch concept

The schematic of the High Voltage Switch is shown in the blue rectangle in Fig. 5. The photograph in the red rectangle depicts the first prototype built using 1.7 kV – 45 mΩ. Power MOSFETs (Wolfspeed), which was presented at ECSCRM 2021 [15] and constitutes the 10kV switch. The second prototype used in this paper (the 20kV switch) uses 3.3 kV – 50 mΩ MOSFETs (Genesic), with a similar package (TO-247-4), so it is visually identical. The goal is to obtain a 20 kV – 50 A switch for double pulse testing purposes. As no continuous operation is intended, the power devices do not require a cooling system. Below we detail the gate driver and the voltage balancing circuit (snubber).

#### 3.1.1 Gate drivers

Every power MOSFET is driven separately by a gate driver IC soldered on the switch’s PCB. It delivers 20 V for on state and - 5 V for off state through a 10 Ohm gate resistor. The driving signal is supplied through fiber optics and a “star” board is used to distribute the six signals. The star board allows for timing adjustment between the different gate driver signals. Each gate driver is powered by a 5 kV isolated DC/DC power supply. The six power supplies are the vertical PCB cards shown in the red rectangle of Fig. 5. They embed the regulation of the different voltages and the optical fiber connector. Ultimately, 3 additional 15 kV isolated DC/DC flyback power supplies are used to power the gate drivers by pairs as illustrated in the blue rectangle in Fig. 5. This is necessary, as the DC/DC supplies mounted on the gate drive boards can only sustain 5 kV, i.e., the voltage across two transistors only. The gate drivers are identical for both test configurations (10kV and 20kV switches, based on 1.7 kV and 3.3 kV MOSFETs respectively).



**Fig. 5** Schematic representation of the High Voltage series connected SiC MOSFET switch (blue rectangle) connected on the low side of the double pulse tests bench. On the high side is found the schematic representation of the freewheeling diode (green rectangle) and load inductor. Some elements of the double pulse test bench are also represented in the schematic. A picture of the high voltage switch with its embedded gate driver power supplies is included (red rectangle).

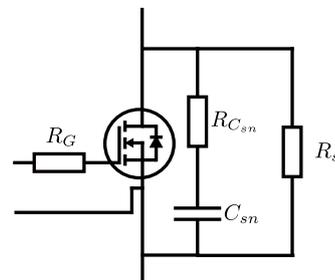
### 3.1.2 Balancing solution

The voltage balancing solutions chosen for the HV switch are chosen for their simplicity. The simplest passive solution was employed both for static and dynamic conditions as illustrated in Fig. 6. For both the 10 kV and the 20 kV HV switches, a grading resistor is placed between drain and source terminals of the 1.7 kV and 3.3 kV SiC MOSFET respectively. The leakage of the single MOSFET is at least three orders of magnitude lower than that of the grading resistors, but for practical reasons the value was fixed to 10 M $\Omega$ . The dynamic snubber has been customized based on the  $C_{OSS}$  value of the MOSFETs. The snubber capacitor value has been chosen at least 5 times that of the  $C_{OSS}$  at high voltage [16]. Since the 1.7 kV and 3.3 kV have a  $C_{OSS}$  of 170 pF and 130 pF at high voltage, the snubber capacitors values are 2.2 nF and 650 pF respectively. The snubber resistors are chosen to damp the oscillations and limit the turn on current

of the MOSFET. 33  $\Omega$  and 50  $\Omega$  are employed for the 10 kV and 20 kV switches respectively.

### 3.2 High voltage Double Pulse test bench

A High Voltage Double Pulse test bench is designed for 10 kV – 100 A diode and/or switch testing. A 20 kV power source from Tektronix supplies



**Fig. 6** Schematic of a power MOSFET with its snubber. The resistive branch is the static voltage grading circuit whereas the capacitive branch is the transient voltage grading one.

two parallel 10 kV – 10 uF bus capacitors. Two 20 kV – 100 nF decoupling capacitors are implemented on the switch PCB to limit the effect of the stray inductance (estimated at 400nH between DC capacitors and PCB). A 700 uH inductor is used as load. The clamping diode on high side is made of six 1.7 kV SiC JBS diodes from Wolfspeed connected in series. A 25 mΩ current viewer resistor from T&M Research is placed on low side in order to accurately measure the current flowing through the DUT. The shunt signal is fed into the scope using a 50Ω coaxial cable. Two high-voltage (40 kV) P6015A passive probes are used to measure the bus voltage and the switch voltage. For intermediate voltages four ISOVU low common mode, optically isolated, 200 MHz bandwidth differential probes from Tektronix are used to measure the gate-source and drain-source voltage. To measure all the voltages of series-connected transistors, the four probes are used two by two. Three successive pulsing sequences are required to acquire all the voltages of the six series connected switches. The complete test setup with its constituting elements and the DUT is presented in Fig. 5.

## 4 Test procedure and results

### 4.1 Test procedure (Methodology)

The goal of this paper is to characterize the impact of the packaging/heat sink on the common mode currents of series-connected switches and propose a new packaging solution to mitigate them. To do so, four series of tests have been carried on the 10 kV prototype:

**Tab. 1** Four test cases performed on the 10 kV prototype (6 MOSFETs 1.7 kV)

	RC snubber	Common mode capacitance related to packaging
Case 1	without	without
Case 2	with	without
Case 3	without	with
Case 4	with	with

To mimic the common mode capacitances that a classical module type packaging would introduce, a set of capacitors have been connected between drain terminals and ground of each power MOSFET as shown in Fig. 7 (orange components, 10 pF – 6 kV).

All the tests have been carried out at 4.2 kV and different current levels (9 A, 34 A, 67 A and 99 A)



**Fig. 7** A photograph of the 10 kV switch with capacitances connected between the drain terminals and the ground. The capacitances emulate the parasitic common mode capacitance introduced by packaging.

in order to obtain a comparison for different operating points. Varying the bus voltage has low impact on the  $dV/dt$  compared to varying the current. The unbalance has been defined as the relative difference of each level with bus voltage divided by the number of levels. Eq. 1 is the mathematical expression of the unbalance:

$$Unbal_n = \frac{V_{DSOFF,n} - V_{Bus}/N}{V_{Bus}/N} \cdot 100\% \quad (1)$$

Test results are reported and discussed below to justify the need for an efficient balancing solution and a new type of module/heat sink that mitigates common mode currents while reducing the thermal impedance of the series connected high voltage switch.

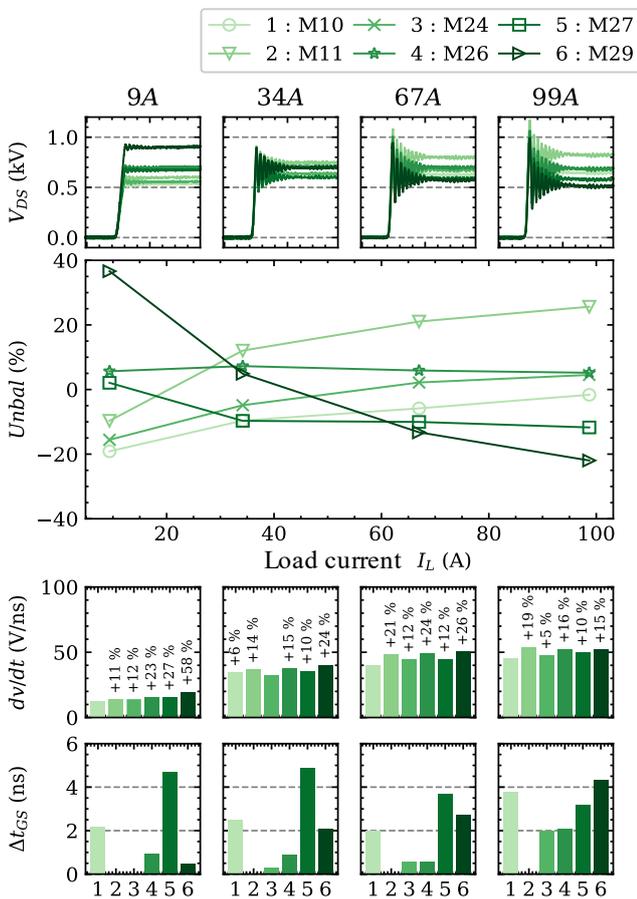
### 4.2 Case 1: Natural voltage unbalance (no packaging and no snubber)

In this configuration, without snubber circuits, only the parametric spread of power MOSFETs and the common mode current through the gate drivers' power supplies are affecting the voltage balancing of the series connected high voltage switch. The results shown in Fig. 8 demonstrate that without a passive or active balancing solution, the drain source voltages are unevenly distributed independently of the current value. First observation: at low currents (9 A) the device withstanding the highest voltage is the uppermost MOSFET. The tendency changes between 30 A and 40 A and is completely reversed at high currents (99 A). Second observation: at low currents the  $dV/dt$  depends on the position of the switch. The uppermost has the highest one and the lowermost the lowest one, with the power supplies affecting the voltage balancing of the series connected high voltage switch. Third observation: at low currents

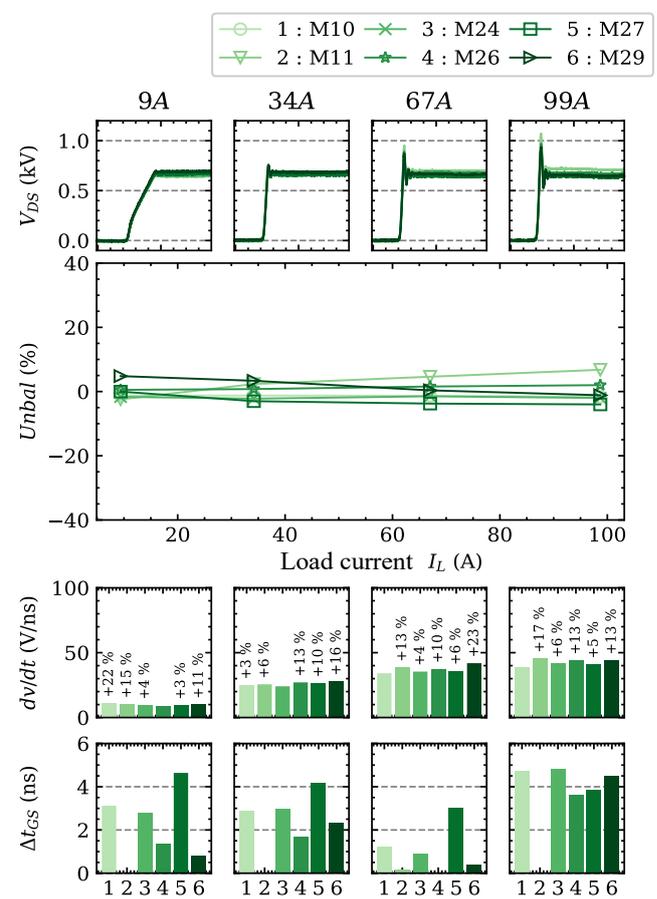
the  $dV/dt$  depends on the position of the switch. The uppermost has the highest one and the lowermost the lowest one, while the others are in the same order. Fourth observation, at higher currents the  $dV/dt$  are grouped in the same way as the power supplies of the gate drivers, two by two. Moreover, they do not increase extensively after 34 A, leading to a saturation of the evolution of the common mode current.

The analysis of these observations points towards the dependence of the switching speed on the switching current and the proportion of common mode current that makes the total current through each individual MOSFET. As a matter of fact, at low currents, the portion of common mode current is higher and since it depends on the position of the MOSFET, it means that there is a significant difference in switching current where the lowest MOSFET is the one having the lowest current and

the uppermost one has the highest current by far. With the increasing load current, although the  $dV/dt$  increases slightly, the difference in current between different positions in the string due to common mode is relatively smaller. As a result, for higher currents the biggest influence on the balancing comes from the delays between the gate source voltages. Said gate source voltage delays depend on triggering instants (delays between optical signals) and the Miller plateau of each single MOSFET (intrinsic parameter spread such as gate threshold voltage) which is current dependent. The highest unbalance level recorded without snubbers happens at the lowest current with almost 40% unbalance. It is thus not desirable to operate a series connected high voltage SiC MOSFET switch without a balancing solution especially in an inverter where the current level varies very often.



**Fig. 8** Case 1: 10 kV switch without snubber or added parasitic capacitance. On top graph turn-off sequences of the six MOSFETs of the for four different current levels. The unbalance ratio as a function of current followed by the  $dV/dt$  graph as function of the current and the position of the power MOSFETs. Last set of graphs are the delays of gate source voltages depending on the switching current and the position.



**Fig. 9** Case 2: 10 kV switch with snubber without added parasitic capacitance. See Fig 8 for the description of the various graphs.

### 4.3 Case 2: Snubber balancing efficiency

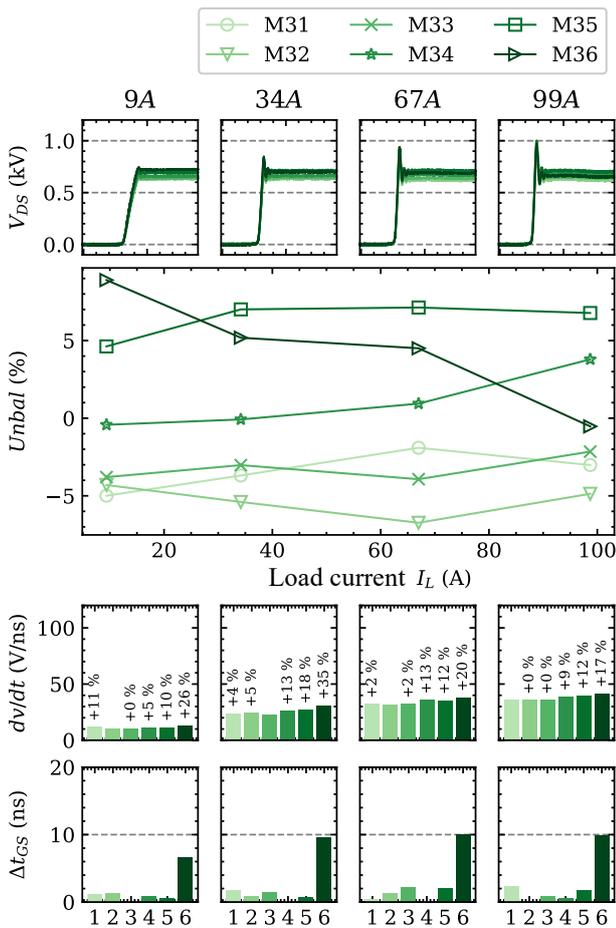
Snubber circuits were added to balance voltages in the string. The test results obtained on the 10 kV switch are shown in Fig. 9. The presence of

snubbers has greatly reduced the unbalance. Moreover, the voltage unbalance is less dependent on the load current. The maximum recorded unbalance is contained in the 10% range. The same tests have been carried out on the 20 kV prototype. The results are reported in Fig. 10, where similar conclusions can be drawn on the balancing efficiency of the snubber. With snubbers the voltage unbalance is lower than 10%. As such, snubbers are excellent candidates for balancing series connected SiC MOSFET as they prove to be efficient and cost effective. But is voltage balancing the only issue with series connection of SiC MOSFETs?

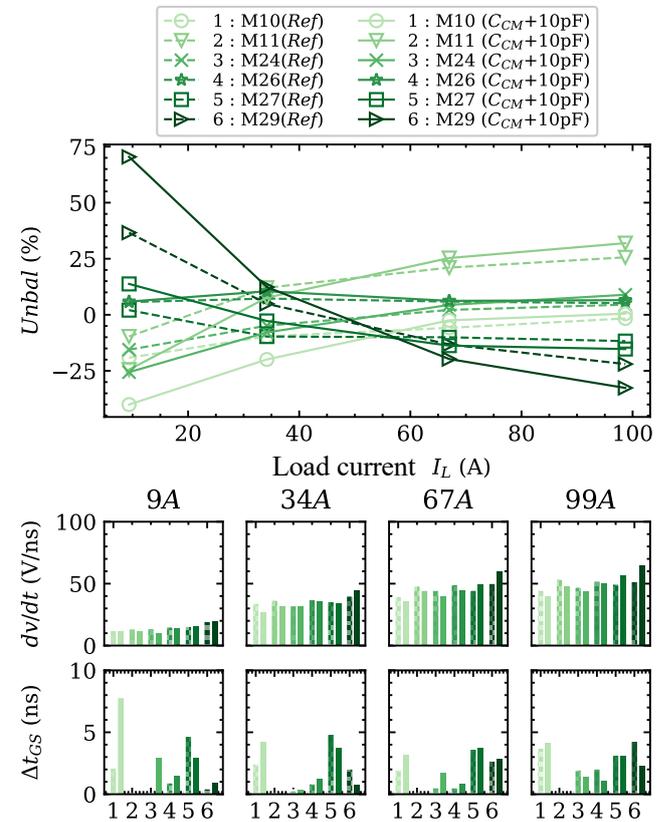
#### 4.4 Case 3: Common mode introduced by packaging/heat sink

In this configuration, there are no snubber circuits and the heat sink parasitic capacitance is modelled by addition of six 10 pF – 6 kV capacitors connected between each drain electrode and ground. The results are shown in Fig. 11 as a comparison with the first case study (no snubber and no additional common mode currents incumbent

to the heat sink: Fig. 8). It can be noticed that the unbalance is aggravated at any current level by the additional common mode current. This effect is even higher at low switching current. As a matter of fact, the portion of common mode current is even bigger in this case, thus leading to very different current levels at turn-off depending on the position of the MOSFETs. It can be observed that this increases the difference of  $dV/dt$ . At higher switching currents the unbalance is affected as well since the total common mode current is larger as compared to the first case study, thus accounting for a bigger part of the switched current. The two-by-two influence of the gate driver power supply common mode capacitance has less visible impact on the  $dV/dt$ . In the case 3 it almost depends only on the position of the switch in the string. In these conditions, the common mode current incumbent to packaging has catastrophic consequences.



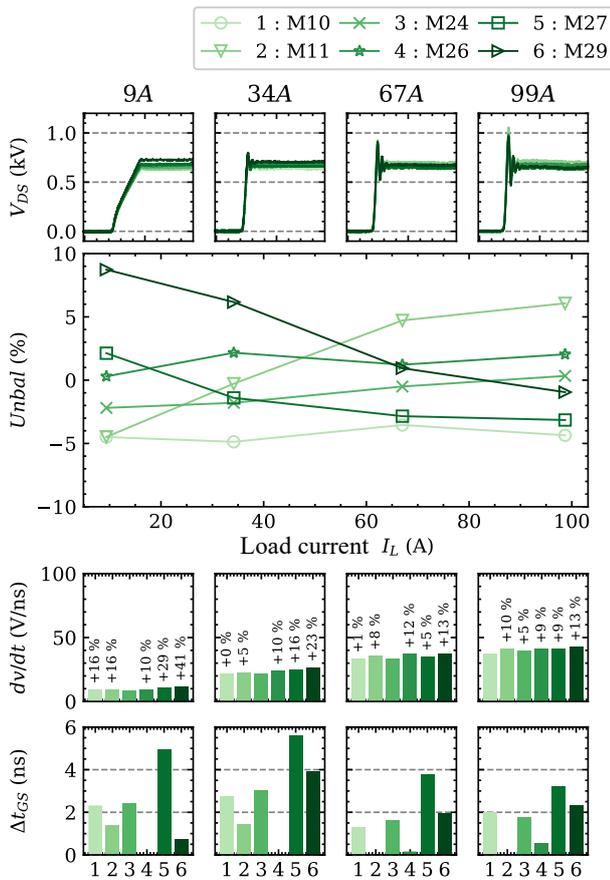
**Fig. 10** Case 2: 20 kV switch with snubber without added parasitic capacitance. See Fig 8 for the description of the various graphs.



**Fig. 11** Case 3: Comparison of tests with and without added parasitic capacitance on the 10 kV switch without snubbers. On top graph the unbalance ratio as a function of current followed by the  $dV/dt$  graph as a function of the current and the position of the power MOSFETs. Last set of graphs are the delays of gate source voltages depending on the switching current and the position.

### 4.5 Case 4: Snubber efficiency on common mode introduced by packaging

As shown previously, the snubber is an efficient balancing solution when it comes to natural unbalance. In Fig. 12 are compared the results obtained with a snubber circuit without packaging related capacitances and with them. Once again, the snubbers confirm their utility, by greatly improving the unbalance, but for low currents the unbalance is slightly aggravated since the common mode currents are greater. Nevertheless, reducing the current differences between series connected devices is paramount. The consequences of unbalanced switching currents are discussed below.

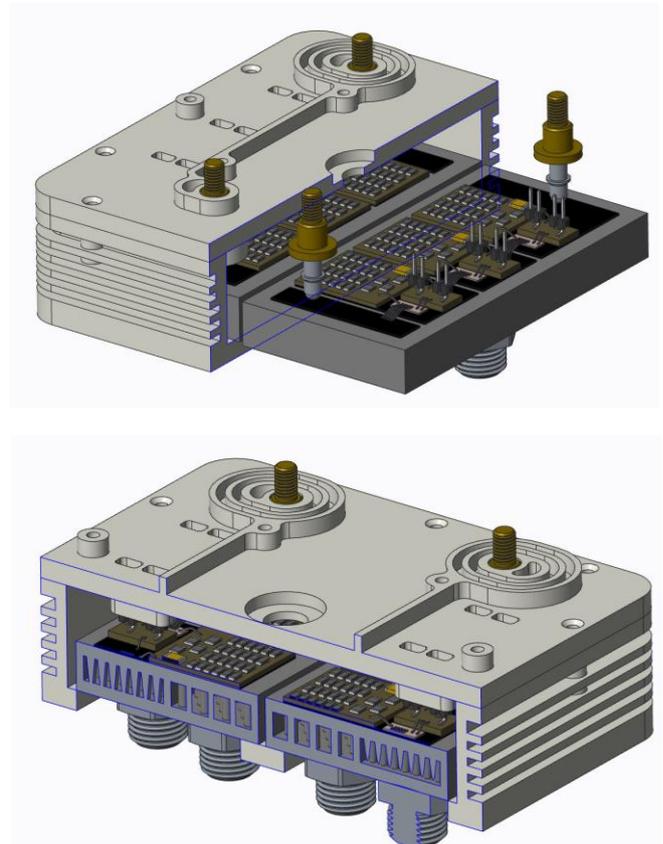


**Fig. 12 Case 4: 10 kV switch with snubbers added parasitic snubbers.** See Fig 8 for the description of the various graphs.

### 4.6 Discussion

The uppermost switch is the one submitted to the higher stress, especially at low currents. Consequently, common mode currents and especially those related to the packaging/heatsink must be avoided or at least balanced for series connected SiC MOSFETs. For practical and safety reasons tests with common mode were carried out on the 10 kV prototype, but is this applicable to the 20 kV

series connected prototype? For a 20 kV switch implemented in a power module, the ceramic insulation baseplate thickness is estimated to 3 mm. For a 3.3 kV SiC MOSFET with its associated snubber the total conductive area facing the heatsink is 880 mm<sup>2</sup> corresponding to a common mode capacitance value of 23 pF. In these conditions, with more than twice the capacitance of that used in the tests and twice the  $dV/dt$ , it is expected that the common mode currents will increase dramatically. It is thus mandatory to avoid or at least drastically reduce the common mode capacitance. Reducing the area of the MOSFET and snubber is impossible, so the only way is to increase their distance to the heat sink, thus to increase the ceramic thickness. This is not a desirable solution as it dramatically increases the thermal impedance and limits the cooling performance. To overcome this limitation, the concept of a thick ceramic with architected structure allowing for liquid cooling has been introduced [17]. In this way, by thinning the ceramic layer between the electrical contacts and



**Fig. 13 3D rendering of the common mode free 20 kV insulated power module with series connected SiC MOSFETs.** On top, the cut allows observing power MOSFETs, the snubbers, the power connections and the creepage paths. The bottom cut focuses on the architecture ceramics shape and its connections to the dielectric fluid cooling system.

the liquid and using a liquid with a dielectric constant close to that of the ceramics, a good electrical and thermal performance can be assured, while leading to virtually no common mode capacitance. Thermal simulation has been carried out to define the architecture of the cooling ceramics and have led to the design presented in [18]. The design of the module frame considers creepage for high voltage insulation and provides power connections as well as driver terminals for each MOSFET. The resulting power module is shown in Fig. 13.

## 5 Conclusions

The present paper demonstrates the need for a good voltage balancing solution and common mode package-related parasitic capacitances mitigation. While balancing has been achieved to a good extent ( $< 10\%$ ) with passive snubbers, it has been demonstrated that the classical module packaging would introduce unsatisfactory level of current unbalance due to common mode currents. The new architected ceramic structure should allow for the mitigation of the package-related common mode currents, by drastically decreasing the parasitic capacitances while maintaining a good cooling performance. This new concept will be tested in future work to verify if it can be applied to High Voltage SiC power modules.

## 6 Acknowledgements

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