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# Flexible dc-MMC interconnecting a bipole and a symmetrical monopole

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**Abstract**—HVDC transmission lines have been used to exchange bulk power across long distances. A future dc network or meshed grid can be imagined from the benefit found with the HVDC lines. The development of the future dc grid will require additional devices capable to adapt the voltage level or grounding strategies between portions of the aforementioned grid. These devices are dc-dc converters. This paper presents the flexible dc-MMC interconnecting a bipole and a symmetric monopole. The converter is tested in a detailed simulation including the cable, average ac-dc converters models, fault detection strategy, and detailed converter sizing. The simulations include normal and fault operation to evaluate their impact on the system. The simulation results show that the flexible dc-MMC can isolate a fault without triggering the healthy parts of the system, providing also the possibility to exchange power after the fault clearance.

**Index Terms**—Flexible dc-MMC, dc-dc converters, HVDC, grid topologies, multi-terminal dc grid, dc-MMC.

## I. INTRODUCTION

High voltage direct current (HVDC) technologies have been used to transmit bulk power over long distances, interconnect asynchronous regions (due to the absence of frequency), with reduced losses and total cost compared to an equivalent ac line. Currently, there are mainly HVDC links interconnecting only two points. However, multi-terminal schemes start to be used to connect more than two HVDC stations. Further evolution is expected to achieve the development of dc grids.

The development of a future dc grid could require additional dc-dc converters to provide supplementary control capabilities, also allowing the interconnection between dc system with different characteristics (e.g., different voltage or different grounding scheme) [1]–[3]. Some publications have studied and summarised the converters proposed in the literature [4]–[6]. Two of these converters stand out from the others: the front-to-front modular multi-level converter (F2F-MMC) and the dc-MMC. These converters have been proposed to interconnect not only links with different dc voltages but also different line topologies. The line topologies used currently used in HVDC systems are [7], [8]: asymmetric

monopole (AM), symmetric monopole (SyM), bipole (B), and rigid bipole (RB).

The F2F-MMC uses two ac-dc MMCs and an ac transformer, all three elements rated to the full power of the dc-dc converter [9], [10]. This structure could require a considerable space due to the volume occupied by the converter arms and the ac transformer. The volume can be reduced if the operating frequency is increased at the cost of increasing the switching and transformer losses [1], [11]. To further reduce the volume of the F2F-MMC, non-isolated converters are proposed in the literature [3], [12].

The dc-MMC is one of the most studied non-isolated dc-dc converters in the literature due to its advantages with respect to the F2F-MMC, such as the reduction of volume due to the lack of ac transformer, the reduced number of elements (e.g. switches) and losses [3], [13]–[19]. The monopolar dc-MMC (i.e., interconnecting two monopoles) is the most studied converter in the literature [18], [20]–[24], and only a few publications address a structure allowing the interconnection of, at least, one bipole (bipolar structure) [16], [17], [25].

The monopolar dc-MMC can interconnect two HVDC grids with similar grid topologies sharing a dc terminal, i.e. the interconnections AM-AM sharing the reference point. The bipolar dc-MMC can be used to interconnect two bipoles or a bipole with a SyM but, only the normal operation has been studied in the literature [16], [17], [25]. In case of a fault in one pole of the bipole, the control proposed in the literature is unable to continue in a degraded mode, i.e. interconnecting an AM with a SyM, because it is designed only for the normal operation.

Based on the bipolar dc-MMC, the flexible dc-MMC was introduced in [8] to have the capacity to interconnect different line topologies (AM, SyM, B, and RB). The main advantage of the flexible dc-MMC is that it provides a degraded mode for the interconnections B-SyM, i.e. after a fault on the B the converter can be adapted to operate with the healthy pole only (equivalent to an interconnection AM-SyM). In this paper, the interconnection between a bipole and a symmetric monopole is studied. This case study allows to evaluate the capacity of the dc-dc converter to stop fault currents avoiding the trigger of the protection on the healthy parts of the system (i.e. firewall capability) and to check the behavior after a fault on the B line. The operation of the converter after a fault on the bipole or

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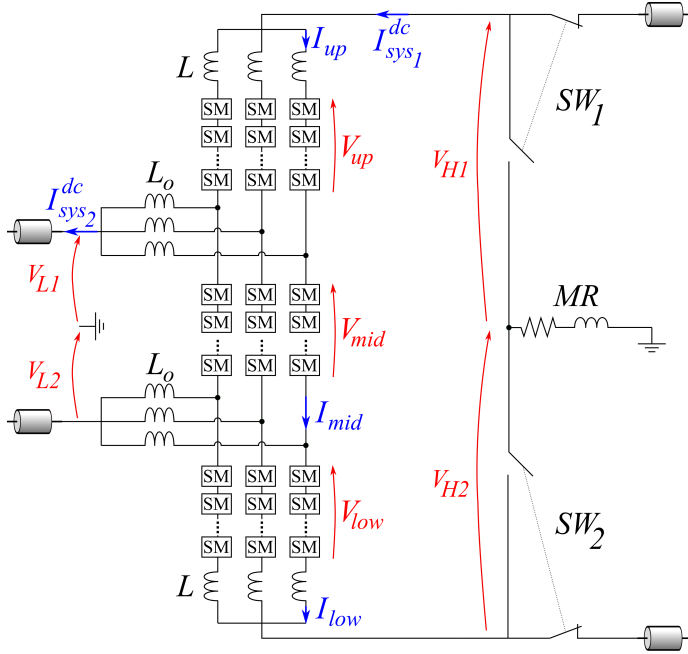


Fig. 1. Flexible dc-MMC with three legs. The metallic return (MR) is presented on the B side.  $SW_1$  and  $SW_2$  are disconnector switches to isolate a fault on the B side.

RB side is called degraded operation. Details on the converter operation, the calculation of the internal references, and the fault detection strategy are also presented.

The paper introduces the flexible dc-MMC in Section II presenting the steady-state analysis. Then, the generalities of the control strategy are presented in Section III. The case study and the parameters of the application chosen for this paper are presented in Section IV. The simulation results and conclusions are presented in Sections V and VI respectively.

## II. FLEXIBLE DC-MMC

The flexible dc-MMC is presented in Fig. 1. It is composed of three arms: upper, middle, and lower. Contrary to the bipolar dc-MMC, the new converter does not have a connection to ground, which allows to unify the middle arms, removing the arm inductor. Each arm has a series connection of sub-modules (SMs) which can be either half bridge (HB) or full bridge (FB). Each arm is capable to insert or bypass the SMs to generate a voltage ( $V_{up}$ ,  $V_{mid}$ , and  $V_{low}$ ). The arms could employ an arm inductor  $L$  to control the arm currents. For this paper, the inductor in the middle is not considered. The arm currents are also identified in Fig. 1 ( $I_{up}$ ,  $I_{mid}$ , and  $I_{low}$ ). The arm voltages and currents contain ac and dc components. The dc components are used to exchange power between the dc systems while the ac components are used to keep the energy balance between the arms [8], [17], [18]. To maintain the dc systems free of ac components, additional passive filters are considered ( $L_o$ ). The dc currents of the dc systems are  $I_{sys1}^{dc}$  and  $I_{sys2}^{dc}$ .

As mentioned above, the flexible dc-MMC allows the interconnection of different line topologies. For the interconnection

of a B with a SyM the dc-dc converter should be able to isolate the faulted pole and continue with the degraded operation. For this, the converter requires additional disconnectors ( $SW_1$  and  $SW_2$  in Fig. 1) to isolate the faulted pole and reconnect the converter to the metallic return.

### A. Dc steady-state

The arm dc currents can be expressed in terms of the system dc currents and voltages. The flexible dc-MMC has two system dc currents:  $I_{sys1}^{dc}$  and  $I_{sys2}^{dc}$ , which can be expressed as:

$$I_{sys1}^{dc} = \frac{P_T^{dc}}{V_{H1} + V_{H2}} \quad (1)$$

$$I_{sys2}^{dc} = \frac{P_T^{dc}}{V_{L1} + V_{L2}} \quad (2)$$

where  $P_T^{dc}$  is the dc power transmitted through the dc-dc converter.

Then, the arm dc currents, per leg, are obtained as follows:

$$I_{up}^{dc} = \frac{I_{sys1}^{dc}}{N_{legs}} = \frac{1}{V_{H1} + V_{H2}} \frac{P_T^{dc}}{N_{legs}} \quad (3)$$

$$\begin{aligned} I_{mid}^{dc} &= \frac{I_{sys1}^{dc} - I_{sys2}^{dc}}{N_{legs}} \\ &= \left( \frac{1}{V_{H1} + V_{H2}} - \frac{1}{V_{L1} + V_{L2}} \right) \frac{P_T^{dc}}{N_{legs}} \end{aligned} \quad (4)$$

$$I_{low}^{dc} = \frac{I_{sys1}^{dc}}{N_{legs}} = \frac{1}{V_{H1} + V_{H2}} \frac{P_T^{dc}}{N_{legs}} \quad (5)$$

where  $N_{legs}$  is the number of legs of the converter (three for this paper).

The arm dc voltages can be also estimated from the system dc voltages ( $V_{H1}$ ,  $V_{H2}$ ,  $V_{L1}$ , and  $V_{L2}$ ), as follows:

$$V_{up}^{dc} = V_{H1} - V_{L1} \quad (6)$$

$$V_{mid}^{dc} = V_{L1} + V_{L2} \quad (7)$$

$$V_{low}^{dc} = -V_{L2} - (-V_{H2}) \quad (8)$$

Using the arm dc currents (3)-(5) and arm dc voltages (6)-(8), the arm dc power can be expressed as:

$$P_{up}^{dc} = \frac{V_{H1} - V_{L1}}{V_{H1} + V_{H2}} \frac{P_T^{dc}}{N_{legs}} \quad (9)$$

$$P_{mid}^{dc} = \left( \frac{V_{L1} + V_{L2}}{V_{H1} + V_{H2}} - 1 \right) \frac{P_T^{dc}}{N_{legs}} \quad (10)$$

$$P_{low}^{dc} = \frac{V_{H2} - V_{L2}}{V_{H1} + V_{H2}} \frac{P_T^{dc}}{N_{legs}} \quad (11)$$

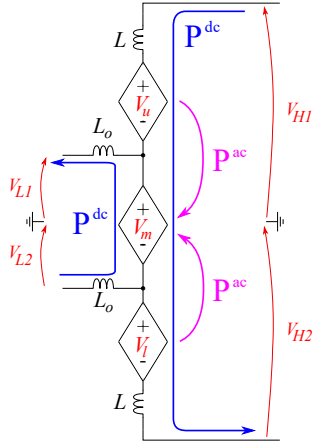


Fig. 2. Power exchanges between the arms in the flexible dc-MMC to keep the energy balanced. Only one leg is presented.

### B. Ac steady-state analysis

The flexible dc-MMC requires an ac power circulating inside the converter to exchange power between arms, without disturbing the interconnected dc systems. The average power balance per arm (neglecting the losses) is given in (12).

$$\langle P_{arm}^{dc} + P_{arm}^{ac} \rangle = 0 \quad (12)$$

Assuming that only the first harmonic is used the arm voltages and currents can be expressed as follows:

$$V_i = V_i^{dc} + |V_i^{ac}| \cos(\theta_{V_i}) \quad (13)$$

$$I_i = I_i^{dc} + |I_i^{ac}| \cos(\theta_{I_i}) \quad (14)$$

where  $V_i$  and  $I_i$  are the magnitudes of the arm voltage and current. The voltage and current phases are expressed as  $\theta_{V_i}$  and  $\theta_{I_i}$  respectively, for  $i \in up, mid, low$ .

Using equations (13) and (14), the expression (12) can be detailed as in (15).

$$V_i^{dc} I_i^{dc} = - |V_i^{ac}| |I_i^{ac}| \cos(\theta_{V_i} - \theta_{I_i}) \quad (15)$$

Using (15) the ac power per arm can be found. Assuming a power transfer from the high voltage side ( $V_H$ ) to the low voltage side ( $V_L$ ), the power exchanges between the arms can be estimated as presented in Fig. 2.

However, finding the magnitudes and phases of the arm voltages can be cumbersome. Similar to the approach used in [8], an optimization problem is solved to find the ac voltages. The optimization aims to reduce the arm current as follows:

$$\min f(x) = N_{sm_{up}} \cdot I_{up_{RMS}}^2 + N_{sm_{mid}} \cdot I_{mid_{RMS}}^2 + N_{sm_{low}} \cdot I_{low_{RMS}}^2 \quad (16)$$

with  $N_{sm_i}$  a weight factor depending on the number and type of SMs used per arm, defined below:

$$N_{sm_i} = N_{sm_{HB_i}} + 2N_{sm_{FB_i}} \quad (17)$$

where  $N_{sm_{HB_i}}$  is the number of HBSMs and  $N_{sm_{FB_i}}$  is the number of FBSMs per arm.

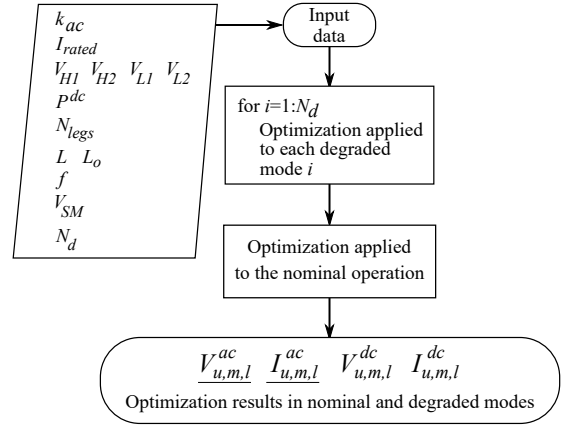


Fig. 3. General flowchart representing the process used to calculate the steady-state solution of the flexible dc-MMC.

The optimization problem is used to determine the ac voltages in normal and degraded operation. For an interconnection between a B and a SyM, two degraded operations are possible: after a fault in the positive pole of the B and after a fault on the negative pole. A general flow chart of the optimization process is presented in Fig. 3. The process requires some input data such as: the ratio between the ac amplitude and the maximum voltage that the arm can generate (related to the number of SMs)  $k_{ac}$ ; the nominal current of semiconductors  $I_{rated}$ ; the system dc voltages  $V_{H1}$ ,  $V_{H2}$ ,  $V_{L1}$ , and  $V_{L2}$ ; the nominal power  $P^{dc}$ ; the number of legs  $N_{legs}$ ; the arm inductors  $L$ ; the output filters  $L_o$ ; the operating frequency  $f$ ; the voltage per SM  $V_{SM}$ ; and the number of possible degraded operations  $N_d$ .

### III. CONTROL STRUCTURE

The control strategy is based on a linear change of variables from the *up*, *mid*, *low* to 1, 2, 3. The new variables are decoupled allowing to design simple controllers such as proportional-integral (PI).

The general control strategy is presented in Fig. 4, it has as inputs the measurements of the equivalent arm capacitor voltages ( $V_{C_{eq_i}}$ ) and the arm currents translated into the 1, 2, 3 domain. The control strategy is based on the energy control, to set the references of some of the current controllers. The rest of the references comes from additional controllers such as: the pole balancing control (keeping  $V_{L1} = V_{L2}$  on the SyM side [8]), the power calculation, and directly from the optimization results. Then, the current controllers give the references for the arm voltages in the converter. Further details on the energy and current controller design and the linear transformations can be found in [8].

### IV. CASE STUDY

To test the flexible dc-MMC and its capacity to isolate a fault on the bipole and operate in degraded mode, a case study interconnecting a B with a SyM is proposed. The interconnection is modeled in Simulink/Matlab environment. The model employs six ac-dc converters (four for the B and two for

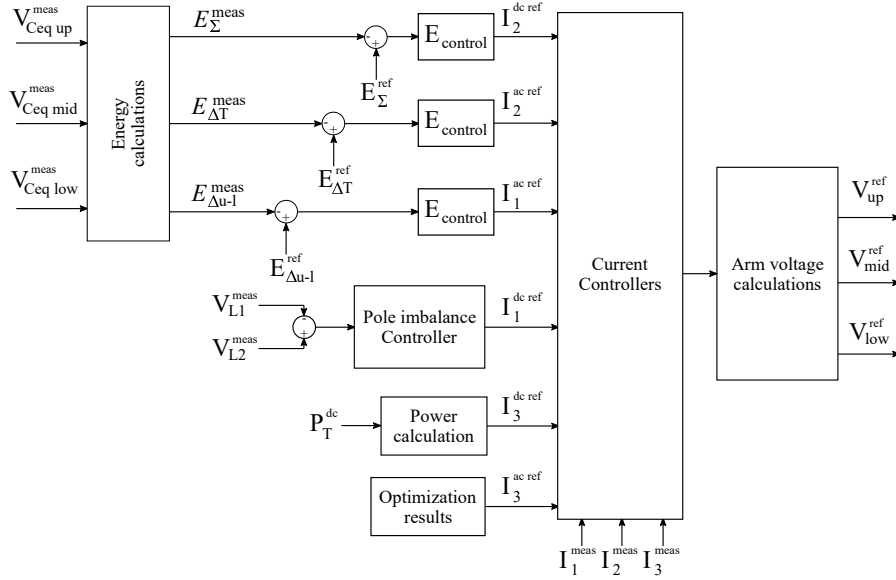


Fig. 4. General control strategy implemented for the flexible dc-MMC.

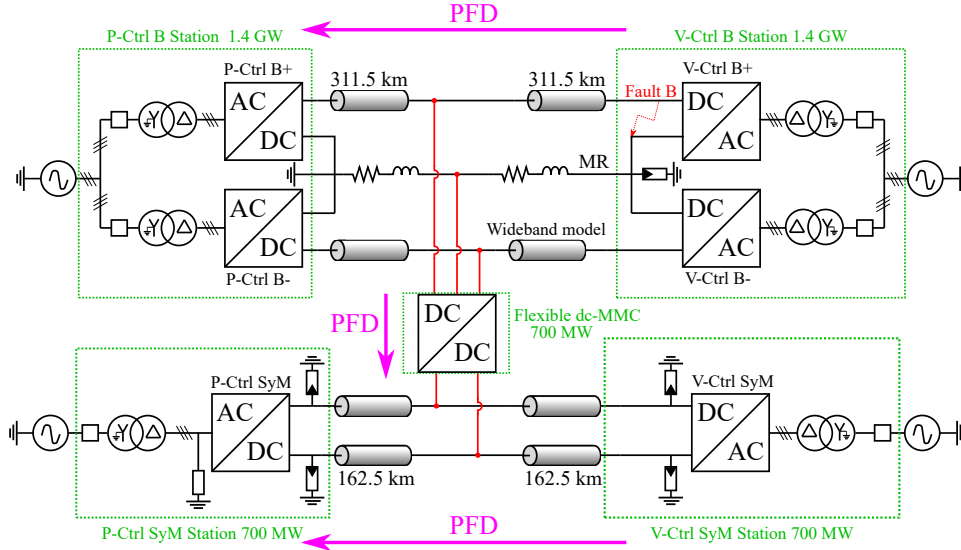


Fig. 5. General scheme for the case study interconnection. The positive conventions for the power flow directions (PFD) in the system are presented in magenta.

the SyM line) and one dc-dc converter. Each ac-dc converter is implemented with the average arm model to reduce the simulation time while keeping the dominant transient behavior [26], [27]. The control of the ac-dc MMCs used in this case study follows the design presented in [28], which implements the virtual capacitor concept for the voltage control of the HVDC links. Additional ac circuit breakers (ACCB) (squares in Fig. 5) are also included, which are triggered in the case of fault detection. The ACCBs have a time delay of 100 ms to simulate the opening time of a real ACCB. Figure 5 presents also the position of five surge arresters included to limit the overvoltages during the fault events.

The lines are controlled in a classical master-slave strategy, where one station controls the dc voltage while the remaining station controls the power. The dc-dc converter is in power

TABLE I  
MAIN PARAMETERS OF THE INTERCONNECTED LINES

Parameter	Bipole	Symmetric monopole
Power	1400 MW	700 MW
Dc voltage	$\pm 525$ kV	$\pm 320$ kV
Length	623 km	325 km

control mode, similar to a slave ac-dc converter. The dc-dc converter is connected in the middle of the two lines. The principal line parameters were based in the NordLink (for the B), and the COBRA cable (for the SyM). The parameters are presented in Table I.

The bipolar line includes a RL model for the metallic return (MR). The HV cables are modelled with the universal

TABLE II  
CABLE PARAMETERS

Section	Cable 320 kV [30]	Cable 525 kV
Length	325 km 2 sections of 162.5 km	623 km 2 sections of 311.5 km
Core ( $R_{in}$ )	$R_{in} = 25.1$ mm $\rho = 1.7e^{-8}$ $\Omega$ m	$R_{in} = 25.95$ mm $\rho = 1.7e^{-8}$ $\Omega$ m
Insulator ( $R_{out}$ )	$R_{out} = 74$ mm $\epsilon_r = 2.5$ $\mu_r = 1$	$R_{out} = 73.5$ mm $\epsilon_r = 2.5$ $\mu_r = 1$

line model (ULM) developed in the Best Paths project [29]. The principal characteristics are presented in Table II, where  $R_{in}$  is the radius of the main conductor and  $R_{out}$  is the radius of the insulator. Based on the cable geometries, the equivalent capacitances are:  $C_{525} = 178.9$  nF/km and  $C_{320} = 175.9$  nF/km.

The ac-dc converters implement a fault detection scheme based on the measurement of the variation of the arm current ( $di/dt$ ), the dc voltage, and arm currents. A fault is detected if any of the measurements cross a set of predefined thresholds. The arm currents are limited to 3 kA to avoid the maximum current supported by the semiconductor devices (3.6 kA for an IGBT [31]). The maximum current variation in the time is limited to 6.4 A/ $\mu$ s. Then, the voltage transients are limited depending on their magnitude and their duration in time. Fast overvoltage transients shorter than 1 ms with 1.2 p.u. of magnitude are allowed as well as the undervoltage transients of 0.85 p.u. during 4 ms. Then, in steady-state (more than 200 ms) the voltage should remain between 0.85 and 1.05 p.u. If the voltage or current measurements reach or crosses any of these conditions, the ac-dc converter considers that a fault event has occurred and it is blocked.

The flexible dc-MMC is rated to the minimum power between the two interconnected lines, i.e. 700 MW. To respect the maximum  $di/dt$  in case of a pole-to-pole fault, the arm and output inductors are set to 82 mH and 200 mH respectively. The flexible dc-MMC also includes the fault detection criteria allowing semi-fast undervoltage transients below 0.2 p.u. Reducing the lower limit increases the voltage support to the dc systems but, the converter might reach the current limit as the power reference does not change, i.e. fixing the power reference with a lower dc voltage increases the dc current.

For this study a single fault on the positive pole of the bipole is considered, in the voltage-controlled station as shown in Fig. 5.

## V. RESULTS

### A. Converter design parameters

Based on the parameters of the case study such as the dc voltages and rated power of the flexible dc-MMC, and assuming  $k_{ac} = 0.92$ ,  $I_{rated} = 1.8$  kA,  $f = 150$  Hz,  $V_{SM} = 1.6$  kV, and  $N_d = 2$  (for a possible fault on each of the poles of the B), the problem proposed in (16) can be solved numerically. The results obtained are presented in

TABLE III  
PARAMETERS FOR THE NOMINAL OPERATION OF THE FLEXIBLE DC-MMC.

Arm	Number HBSMs	Number FBSMs	$V^{ac}$ (kV)	$I^{ac}$ (kA)
Upper	0	372	$225\angle -171.2^\circ$	$0.5\angle -27.6^\circ$
Middle	661	0	$409\angle 0^\circ$	$0.96\angle 62.35^\circ$
Lower	0	372	$225\angle -171.2^\circ$	$0.5\angle -27.6^\circ$

TABLE IV  
STEADY-STATE SOLUTION FOR THE DEGRADED OPERATION OF THE FLEXIBLE DC-MMC. THE EXTERNAL ARMS (UPPER AND LOWER) CHANGE THEIR OPERATING POINTS DEPENDING ON THE LOCATION OF THE FAULT.

Arm	$V^{dc}$ (kV)	$I^{dc}$ (kA)	$V^{ac}$ (kV)	$I^{ac}$ (kA)
Next to faulted pole	-320	0.222	$276\angle 145^\circ$	$0.68\angle -173^\circ$
Middle	640	0.04	$417\angle 0^\circ$	$1.09\angle 96.4^\circ$
Next to healthy pole	205	0.222	$238\angle -144^\circ$	$0.44\angle 6.4^\circ$

Table III for the nominal operation and details on the degraded operation are presented in Table IV. In Table III it can be observed that the upper and lower arm are composed of only FBSMs while the middle arm has only HBSMs. This is because during the degraded, operation the external arms need to withstand, and modulate negative voltages (see Table IV). It can also be evidenced a symmetry between the upper and lower arms as they have equal behavior in normal operation and complementary during degraded operation.

Additionally, the capacitor values per SM are calculated based on the energy variation following the approach presented in [27], [32], [33] and allowing a voltage ripple of 10%. The external arms (upper and lower) have a capacitance of 2.1 mF while the middle arm uses SMs with 4.4 mF capacitances.

### B. Simulation results

The simulation results of the flexible dc-MMC interconnecting a B and a SyM are presented in Fig. 6. It presents the total simulation time at the left and a zoom in the fault event on the right. The simulation can be divided into five stages: initialization (t: 0-1.5 s), lines startup (t: 1.5-2.4 s), dc-dc converter startup (t: 2.4-3.65 s), fault event (t=3.7), and post-fault (t>3.7). The initialization ensure a clean startup of the elements. At 1.5 s the B and SyM lines start to exchange power with a reference that ramps-up to a final value of -200 MW for the SyM and -900 MW for the B. According to Fig. 5 these references indicate a power flow from the power-controlled stations to the voltage-controlled ones. After reaching steady-state conditions ( $\sim 2.4$  s), the dc-dc converter starts to exchange -500 MW (from the SyM to the B). At t=3.7 s a fault on the bipole is simulated. After the fault detection, described in Section IV, the flexible dc-MMC is blocked to stop the fault current, and the switch  $SW_1$  is actuated. A delay of 140 ms is added to simulate the time to reconfigure the flexible dc-MMC and to restart it. The power is ramped-up around 4.1 s to exchange -250 MW

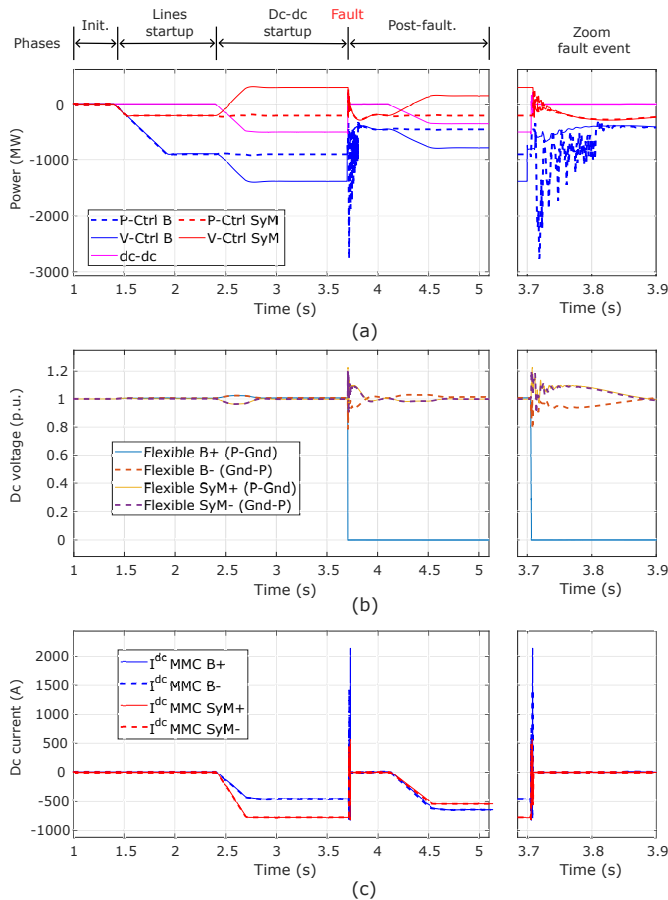


Fig. 6. Simulation results for the flexible dc-MMC when a fault on the B line is simulated. (a) The power per converter station, (b) the dc voltages at the terminals of the dc-dc converter, and (c) the dc currents at the terminals of the flexible dc-MMC.

(half of the initial power reference). The power changes during the simulation time can be detailed in Fig. 6a. It can be noticed that the power-controlled stations (dashed lines) do not change their power when the dc-dc converter is started. On the other hand, the voltage-controlled stations adapt their power exchanged with the external ac systems to keep the dc voltage stable.

The dc voltage measured at the terminals of the flexible dc-MMC are presented in Fig. 6b. It can be noticed that the dc voltages have a small disturbance when the power reference are changed, e.g. around 2.5 s with the dc-dc converter startup. During the fault event fast transients are measured in both lines. However, they do not trigger the fault detection in any of the ac-dc converters. The system recovers nearly steady-state after around 400 ms ( $t=4.1$  s), where the voltage is disturbed again during the change of power reference in the dc-dc converter.

The dc currents through the dc-dc converter are presented in Fig. 6c. It can be seen that the currents follow the power reference of the flexible dc-MMC. At the time of the fault the current has a considerable peak of 2 kA. However, this fault current is stopped in less than 10 ms due to the fast blocking of the dc-dc converter and the presence of FBSMs in the

circuit. It can be noticed that the duration of this fast current transient is negligible compared to the power or DC voltage transients. The effect of the peak current on the semiconductor devices is not evaluated in this paper, including the effect of the modulation technique.

## VI. CONCLUSIONS

The flexible dc-MMC is a new converter proposed for the interconnection between HVDC lines with different topologies. In this paper the converter was studied to interconnect a bipole with a symmetric monopole. To provide redundancy after a fault on the bipole line, the dc-dc converter was adapted and simulated. The adaptations include the consideration of additional switches and the analysis of the degraded operation. The converter was modeled and simulated in a Simulink/Matlab environment. The results have shown that the flexible dc-MMC provides firewall capability and that it is able to continue the degraded operation without triggering the fault detection of the healthy parts of the system. Further studies should be carried out to determine the impact of the fault location on the converter behavior. The impact of the fault currents in the equipment should be also considered in future studies. The impact of the transients on the semiconductor devices could be also studied. The converter can be validated in a future laboratory implementation.

## REFERENCES

- [1] C. Barker, C. Davidson, D. Trainer, and R. Whitehouse, "Requirements of dc-dc converters to facilitate large dc grids," *Cigre, SC B4 HVDC and Power Electronics*, 2012.
- [2] S. K. Kolparambath, J. A. Suul, and E. Tedeschi, "Dc/dc converters for interconnecting independent HVDC systems into multiterminal dc grids," in *2015 IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference*, Nov 2015, pp. 1–6.
- [3] D. Jovic, G. Kish, A. Darbandi, D. Woodford, J. Robinson, and O. Gomis *et al.*, "Dc-dc converters in HVDC grids and for connections to HVDC systems," Cigré, Tech. Rep., March 2021.
- [4] J. D. Páez, D. Frey, J. Maneiro, S. Bacha, and P. Dworakowski, "Overview of dc-dc converters dedicated to HVdc grids," *IEEE Trans. on Power Delivery*, vol. 34, no. 1, pp. 119–128, Feb 2019.
- [5] G. J. Kish, "On the emerging class of non-isolated modular multilevel dc-dc converters for dc and hybrid ac-dc systems," *IEEE Trans. on Smart Grid*, 2017.
- [6] G. P. Adam, I. A. Gowaid, S. J. Finney, D. Holliday, and B. W. Williams, "Review of dc-dc converters for multi-terminal HVDC transmission networks," *IET Power Electronics*, vol. 9, no. 2, pp. 281–296, 2016.
- [7] D. Gómez, J. D. Páez, M. Cheah-Mane, J. Maneiro, P. Dworakowski, O. Gomis-Bellmunt, and F. Morel, "Requirements for interconnection of HVDC links with dc-dc converters," in *IECON 2019-45th Annual Conference of the IEEE Industrial Electronics Society*, vol. 1. IEEE, 2019, pp. 4854–4860.
- [8] D. Gómez A., M. Cheah-Mane, J. D. Páez, F. Morel, O. Gomis-Bellmunt, and P. Dworakowski, "Dc-MMC for the interconnection of HVDC grids with different line topologies," *IEEE Transactions on Power Delivery*, vol. 37, no. 3, pp. 1692–1703, 2022.
- [9] S. Kedia and H. J. Bahirat, "Dc-dc converter for HVDC grid application," in *2017 National Power Electronics Conference (NPEC)*. IEEE, 2017, pp. 346–351.
- [10] F. Sasongko, M. Hagiwara, and H. Akagi, "A front-to-front (ftf) system consisting of two modular multilevel cascade converters based on double-star chopper-cells," in *2013 1st International Future Energy Electronics Conference (IFEEC)*, 2013, pp. 488–493.
- [11] T. Lüth, M. M. C. Merlin, T. C. Green, F. Hassan, and C. D. Barker, "High-frequency operation of a dc/ac/dc system for HVDC applications," *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 4107–4115, 2014.

- [12] J. Páez, J. Maneiro, S. Bacha, D. Frey, and P. Dworakowski, "Influence of the operating frequency on dc-dc converters for HVDC grids," in *2019 21st European Conference on Power Electronics and Applications (EPE'19 ECCE Europe)*. IEEE, 2019, pp. P-1.
- [13] S. Norrga, L. Ångquist, and A. Antonopoulos, "The polyphase cascaded-cell dc/dc converter," in *2013 IEEE Energy Conversion Congress and Exposition*, Sep. 2013, pp. 4082-4088.
- [14] J. A. Ferreira, "The multilevel modular dc converter," *IEEE Trans. on Power Electronics*, vol. 28, no. 10, pp. 4460-4465, 2013.
- [15] Y. Gao, N. Faria, and G. J. Kish, "Dynamic model of an interleaved modular multilevel dc-dc converter for MVDC and HVDC systems," in *2017 IEEE Electrical Power and Energy Conference (EPEC)*, 2017, pp. 1-8.
- [16] G. J. Kish and P. W. Lehn, "A modular bidirectional dc power flow controller with fault blocking capability for dc networks," in *2013 IEEE 14th Workshop on Control and Modeling for Power Electronics (COMPEL)*, June 2013, pp. 1-7.
- [17] G. J. Kish and P. W. Lehn, "Modeling techniques for dynamic and steady-state analysis of modular multilevel dc/dc converters," *IEEE Trans. on Power Delivery*, vol. 31, no. 6, pp. 2502-2510, 2015.
- [18] M. Cheah-Mane, J. Arevalo-Soler, E. P. Araujo, and O. Gomis-Bellmunt, "Energy-based control of a dc modular multilevel converter for HVDC grids," *IEEE Trans. on Power Delivery*, 2019.
- [19] S. P. Engel, M. Stieneker, N. Soltan, S. Rabiee, H. Stage, and R. W. De Doncker, "Comparison of the modular multilevel dc converter and the dual-active bridge converter for power conversion in HVDC and MVDC grids," *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 124-137, 2014.
- [20] F. Gruson, Y. Li, P. Le Moigne, P. Delarue, F. Colas, and X. Guillaud, "Full state regulation of the modular multilevel dc converter (m2dc) achieving minimization of circulating currents," *IEEE Trans. on Power Delivery*, vol. 35, no. 1, pp. 301-309, 2019.
- [21] A. Jamshidi Far, D. Jovcic, A. Nami, and Y. Okazaki, "Selecting frequency and parameters of dc-fault tolerant non-isolated high power MMC dc/dc converter," *Electric Power Systems Research*, vol. 191, p. 106896, 2021. [Online]. Available: <https://www.sciencedirect.com/science/article/pii/S0378779620306945>
- [22] H. Yang, J. Qin, S. Debnath, and M. Saeedifard, "Phasor domain steady-state modeling and design of the dc-dc modular multilevel converter," *IEEE Transactions on Power Delivery*, vol. 31, no. 5, pp. 2054-2063, 2016.
- [23] F. Zhang, W. Li, and G. Joós, "A transformerless hybrid modular multilevel dc-dc converter with dc fault ride-through capability," *IEEE Trans. on Industrial Electronics*, vol. 66, no. 3, pp. 2217-2226, March 2019.
- [24] D. Jovcic, P. Dworakowski, G. Kish, A. Jamshidi Far, A. Nami Abb, A. Darbandi, and X. Guillaud, "Case study of non-isolated MMC dc-dc converter in HVDC grids," in *CIGRE Symposium 2019*, 6 2019, pp. 1-7.
- [25] G. J. Kish, M. Ranjram, and P. W. Lehn, "A modular multilevel dc/dc converter with fault blocking capability for HVDC interconnects," *IEEE Trans. on Power Electronics*, vol. 30, no. 1, pp. 148-162, Jan 2015.
- [26] R. Wachal, A. Jindal, S. Dennetiere, H. Saad, O. Rui, S. Cole, M. Barnes, L. Zhang, Z. Song, J. Jardini, J. Garcia, F. Mosallat, H. Suriyaarachich, P. Le-Huy, A. Totterdell, L. Zeni, S. Kodsi, D. Tiku, P. Thepparat, and Y. Yang, "Guide for the development of models for HVDC converters in a HVDC grid," CIGRE working group B4.57, Tech. Rep., 12 2014.
- [27] J. Páez Alvarez, "DC-DC converter for the interconnection of HVDC grids," Theses, Université Grenoble Alpes, Dec. 2019. [Online]. Available: <https://tel.archives-ouvertes.fr/tel-03132552>
- [28] K. Shinoda, A. Benchaib, J. Dai, and X. Guillaud, "Virtual capacitor control: Mitigation of dc voltage fluctuations in MMC-based HVdc systems," *IEEE Transactions on Power Delivery*, vol. 33, no. 1, pp. 455-465, 2018.
- [29] B. Paths. Simulation toolbox demo 1. Online. Best Paths. Feb. 25, 2019. [Online]. Available: <http://www.bestpaths-project.eu/en/publications>
- [30] X. Gu, Y. Liu, Y. Xu, Y. Yan, Y. Cong, S. Xie, and H. Zhang, "Development and qualification of the extruded cable system for Xiamen ± 320 kV VSC-HVDC project," in *Proc. CIGRE*, 08 2018, pp. 1-10.
- [31] *High Voltage Insulated Gate Bipolar Transistor: HVIGBT*, Mitsubishi Electric, September 2020. [Online]. Available: [https://www.mitsubishielectric.com/semiconductors/content/product/powermodule/hvigt\\_ipm/x\\_series/cm1800hc-66x\\_e.pdf](https://www.mitsubishielectric.com/semiconductors/content/product/powermodule/hvigt_ipm/x_series/cm1800hc-66x_e.pdf)
- [32] R. Marquardt, A. Lesnicar, J. Hildinger *et al.*, "Modulares stromrichter-konzept für netzkupplungsanwendung bei hohen spannungen." *ETG symposium, Bad Nauheim, Germany*, vol. 114, 2002.
- [33] M. M. C. Merlin, T. C. Green, P. D. Mitcheson, F. J. Moreno, K. J. Dyke, and D. R. Trainer, "Cell capacitor sizing in modular multilevel converters and hybrid topologies," in *2014 16th European Conference on Power Electronics and Applications*, 2014, pp. 1-10.