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ABSTRACT

In this paper, we introduce a novel approach for the design of robust low-noise amplifiers (LNAs) using wide-bandgap GaN MMIC technology. The objective of this work is to compare two robust LNA design strategies. While a method already mentioned in the literature reaches high linearity performance levels by making use of highly sized device at the price of noise figure (NF) degradation, this work proposes an alternative design option which allows to switch in a reversive way from optimum NF performance to optimum power compression point, by suitably changing the quiescent point of the transistor. This second strategy of design implies beforehand an adequate selection of the transistor's sizing taking into account its capacity to be matched at its input and at its output whatever the biasing condition. Thus, a comparison is performed for the two different LNA design strategies, results are presented and discussed. It is proven that the proposed reconfigurable LNA achieves the best NF results under nominal biasing conditions, while it can be DC-voltage tuned to improve its linearity close to that of the highly sized transistor LNA: this operating mode allows the receiver to operate under electromagnetic aggression conditions. The new proposed LNA achieves an average noise figure of 1.05 dB for a small signal gain higher than 10 dB over the X-Band, and with an input compression point (IP_{1dB}) that can increase by 10 dB between the two quiescent point, up to IP_{1dB} of 14 dBm (IP_{1dB} of 19 dBm is achieved for the non-tunable design, with a NF 0.2 dB higher than our design).
Keywords—Low-noise amplifier, LNA, Gallium Nitride, HEMTs, Linearity, Circuit Topology, Reconfigurable, MMICs.

I - INTRODUCTION

GaN HEMT active devices offer higher linear performance and robustness than their GaAs or SiGe counterparts. With power density 6 to 10 times higher, their use to design RF power amplifiers (PAs) has been widely democratized. Additionally, it has been proven that GaN-based semiconductors can provide interesting high-frequency noise properties. The combination of these two features makes these technologies excellent candidates for robust low noise applications. The combination of these properties makes GaN technologies a natural choice for military or altimetry systems that require high RF input levels while ensuring optimal detectivity. GaN-based receivers are advantageous for their ability to withstand high jamming powers without being degraded or destroyed [1]. It is then possible to partially or totally dispense with the protection devices placed before the LNA [2]. This improves the overall receiver block complexity (SWaP), as well as the overall NF (noise factor equals losses for passive protection systems). In order to build a robust LNA, one strategy is to oversize the transistor: this means larger physical sizing and/or electrical biasing of the transistor than that used for optimum low noise conditions [3]. In this way, non-linear performance is improved at the expense of the four noise parameters. We propose a new method which, by changing the quiescent point of the transistor, allows reconciling the low noise properties of GaN HEMT while exploiting to the maximum the linearity performances of a design. This paper presents a comparative study on the two different strategies for the design of robust GaN LNAs: our reconfigurable design ($LNA_{\#1}$) and the classical approach with a larger sized transistor ($LNA_{\#2}$). The measurements on single stage designs are presented for a fair comparison between each of these options, even if multi-stage LNAs have been designed and measured [4]. In the literature, other methods aiming at implementing robust LNAs are also proposed, each offering different advantages depending on the targeted application [5] [6] [7] [8].
The first part of this article will be devoted to the choice of the most suitable active element relative to our repolarization strategy. The second part will focus on the precautions taken at the design circuit layout level. Finally, the last part will detail the simulations and measurements specific to each design, with a discussion on the two design strategies.

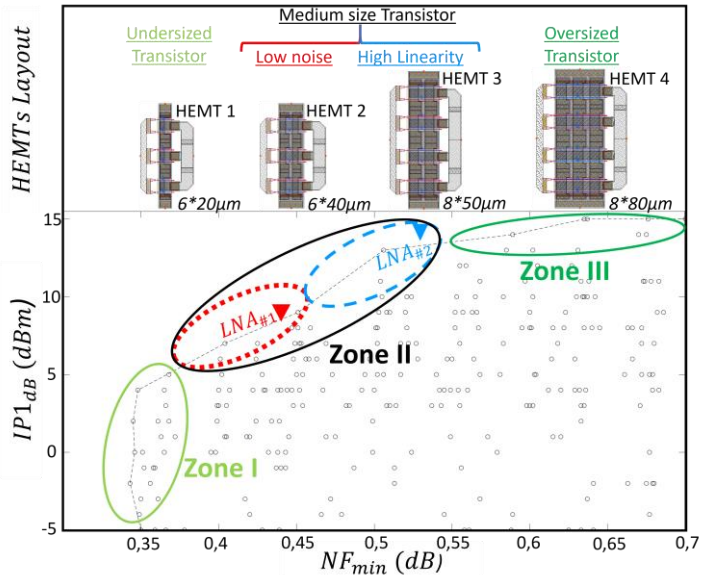


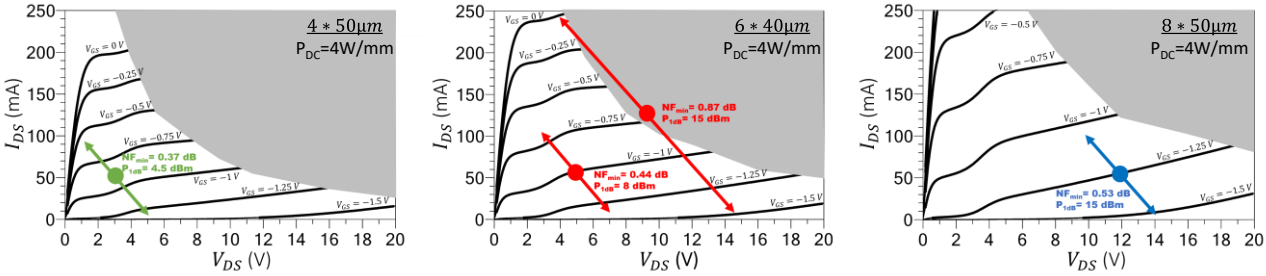
Fig. 1 : Device biasing and sizing selection for Low Noise or high compression IP1dB purposes (NFmin versus IP1dB @10 GHz). Sizing is for number of gate fingers and gate individual width respectively ranging between [2;4;6;8] and [20 µm to 100 µm by step of 20 µm], while biasing on V_{GS} and V_{DS} respectively range between [-1,7 V to 0 V by step of 0.2 V] and [3V;5V;8V;12V;20V]. The number of random sizing/ DC biasing combinations is 1000.

The GaN technology selected for this comparative study on LNAs is the OMMIC D01GH process on silicon substrate. It provides HEMT devices with a transition frequency of 110 GHz, high breakdown voltage of 36 V, and a good power density of 4 W/mm. This process is suitable for RF High Power Amplifier (HPA), robust LNA and Transceiver modules.

II - SIZING OF THE ACTIVE ELEMENT

In a conventional LNA design, the optimization of the first stage is realized based on the four noise parameters (minimum achievable noise figure NF_{min}, equivalent noise resistance R_n and complex optimum noise reflexion coefficient Γ_{opt}) and on the small signal parameters [S] criteria to respect the technical specifications imposed by the FRIIS formula [9] in the reception system under study. The transistor sizing (number of gate fingers and gate length for a High Electron Mobility Transistors, HEMT) and its static biasing (V_{GS}; V_{DS}) are then selected according to these aspects. Linearity of the receiver is then imposed by this selection. In Fig. 1, the input compression point IP_{1dB} is plotted versus the minimum noise figure NF_{min} at the center frequency of 10 GHz. This mapping of the HEMT is developed for various sizing (number of gate fingers, gate individual length) and different biasing (V_{GS} and V_{DS}). The objective is to appreciate the possibility to get simultaneously low NF_{min} and high IP_{1dB} in a first intention (even if these two parameters are not the only one to be considered for the design of an LNA). Four different transistors are reported in Fig. 1 as a possible illustration of these main trade-offs to operate for selecting the HEMT providing the appropriate value pairs (NF_{min}, IP_{1dB}) (one small, two medium and one large size devices). Of course, second order criteria such as the small signal gain, the noise or small-signal reflection coefficient magnitudes, the equivalent noise resistor are used to refine the active device selection. Three main areas are evidenced. It is admitted that all LNAs can be biased at several quiescent points more or less close to each other; the objective of our design strategy is to take maximum advantage of the elasticity of the electrical noise and power linearity performance of a component. The objective is therefore to make a judicious choice on the dimension of the component, which allows a maximum variation of the 1dB compression point (P_{1dB}) of the device while keeping stable matching parameters (S_{11} & S_{22}) as well as the small-signal gain (S_{21}).

-The area labelled as zone I is not eligible for this study: indeed, to have the best NFmin performance, the associated DC biases are around 3V and 5V and -0.9V and -0.7V. However, as we can see on Fig. 1.a, to increase the P_{1dB} of the transistor, it is imperative to increase the drain voltage while keeping a stable gate voltage in order to place the component in a zone of higher linearity. It is then complicated, if not impossible, to increase the drain voltage without strongly changing the S_{22} parameter (4-6 dB worse). On top of that, even if NF_{min} is the best for this technology, the sizing and biasing of the transistor also increases the space between Γ_{opt} and the conjugate of S_{11} for matching conditions, and that can be sensed through an increase of ΔNF (defined as $\Delta NF=NF_{50\Omega}-NF_{min}$). The design effort of the input matching



(a) (b) (c)

Fig. 2 : Static characteristics [$I_{DS}(V_{DS})$] for three transistor dimensions (4*50µm, 6*40µm & 8*50µm). Each quiescent point appears with NFmin and associated P1dB. The areas of maximum DC power dissipation are shown in gray.

network (IMN) tends to degrade the noise performance and offers, in fine, a $NF_{50\Omega}$ of equivalent level to a slightly larger sized transistor.

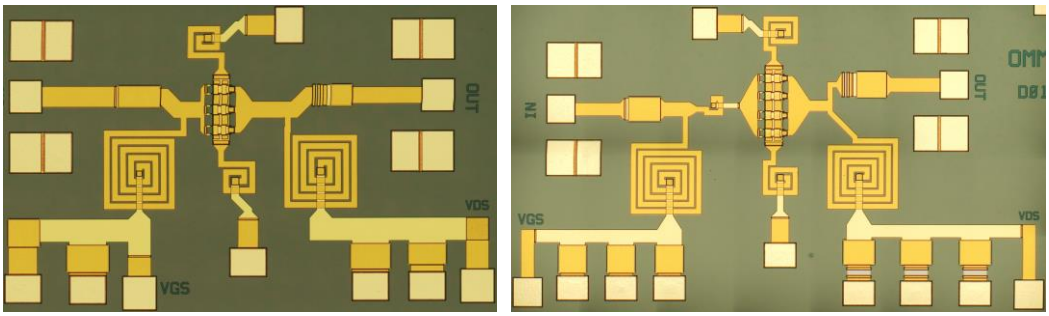
In order to avoid the deterioration of the output matching when the drain voltage increases, the only solution is also to open the channel of the transistor. Thus, the coherence on the V_{GS}/V_{DS} couple is a needed prerogative to keep the matching parameters relatively stable.

-Zone II is related to transistors exhibiting a low NF_{min}, and a high IP_{1dB} near the inflection between the low-noise and high- linearity sections in Fig. 1. The lower trend zone (red dotted section) represents the most interesting features for our reconfigurable strategy ($LNA_{\#1}$) because it allows to have the best final $NF_{50\Omega}$, while the upper trend zone (blue dashed section) is more suitable for obtaining a highly linear device ($LNA_{\#2}$). The larger transistors, although advantageous from the point of view of their linear performance, are not eligible to further increase their compression point because they are located at the edge of what the technology can offer in terms of recommended maximum output power. Moreover, these components (8*50µm or equivalent gate dimension) are located in an area with degraded noise parameters, so their size does not allow to guarantee a gain as high as for a transistor of smaller size (6*40µm or equivalent).

-In zone III, the increase on NF_{min} for a poor benefit on IP_{1dB} will prevent the selection of these HEMT biasing and sizing solutions for the design of an LNA. Moreover, as the size of the component increases, the gain also tends to decrease.

Fig. 2 reports the static output characteristics for specifically selected HEMT sizing and biasing, also with the 50 Ω load line and safe operating area (SOA) set at 4 W/mm static power per mm of overall gate width [10]. As we can see on Fig. 2.b, the transistor whose dimensions are optimal for a low noise application (6*40µm) can also achieve the same high IP_{1dB} as what a larger transistor can propose. This is done at the expense of the noise figure degradation, which increases significantly while moving the DC gate/drain quiescent point of this selected. The incursion of the quiescent point in the area of maximum continuous power dissipation (P_{DC}=4W/mm) is acceptable thanks to the RF power considered at the input of the device. Indeed, by taking into consideration the compression point at the input of the device and its gain, it is possible to deduce the RF power evacuated by the device. This RF power comes to reduce the thermal stress caused by the DC bias applied to the transistor. In view of the high RF levels involved at the input of robust GaN LNAs, the considerations usually reserved for power amplifiers (PAs) are applicable here [11].

In consideration of the compromise on NF and IP_{1dB}, and taking into account the maximum achievable power considerations, the 6*40µm transistor is therefore selected for our voltage-reconfigurable design ($LNA_{\#1}$), while the 8*50µm device is selected to realize a classic robust LNA ($LNA_{\#2}$) for comparison.



(a) (b)

Fig. 3 : Layout of the two LNAs considered for the study: (a) LNA#1 with the 6*40µm transistor, (b) LNA#2 with the 8*50µm transistor.

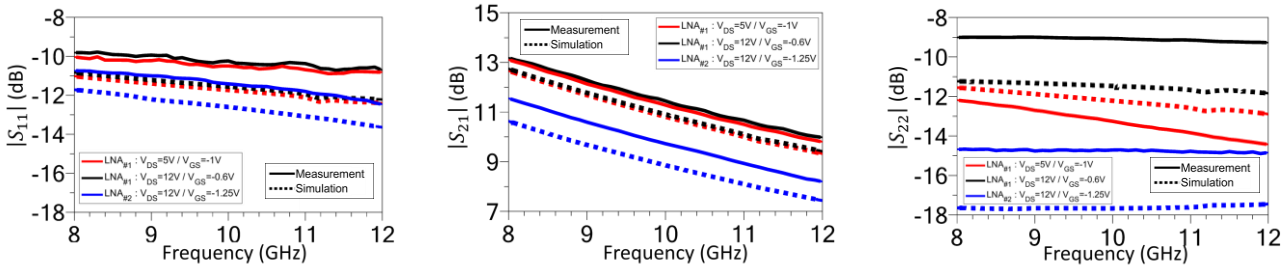


Fig. 4 : Simulated and measured S-parameters of $LNA_{\#1}$ [in its low noise configuration (V_{DS}=5V / V_{GS}=-1V), in **EM aggression mode (V_{DS}=12V / V_{GS}=-0.6V)**] and of $LNA_{\#2}$ (V_{DS}=12V / V_{GS}=-1.25V)

III – LAYOUT OF THE LNAS

Once the active components are selected, input (IMN) and output (OMN) matching network are implemented.
In the case of the two layouts implemented on Fig. 3, the goal is to get two realizations with the lowest possible noise; the inductive feedback on the gate access is mandatory to bring the optimum noise reflection coefficient S_{opt} closer to the conjugate of S_{11}. Concerning the classical robust LNA (8*50µm) this feedback appears as a critical element. Indeed, if the noise matching effort seems to require significant feedback, the latter has the effect of reducing the gain. Consequently, the small signal gain is all the lower as the size of the transistor is high. A compromise is made to ensure a minimum gain of 7.5 dB at 12 GHz. Beyond that, a series inductor and a decoupling system mixing capacitance and resistance are added to guarantee the stability at medium frequency. The decrease in gain caused during the design steps of the final layout has the effect of increasing IP_{1dB} by 4dB.
Concerning our voltage reconfigurable $LNA_{\#1}$ strategy, the feedback appears to be a less critical parameter due to the higher gain of the transistor (6*40µm) in X band. The IMN and OMN are implemented by checking the stability of the small signal gain as well as the matching parameters stability versus the two quiescent points with the objective of ensuring maximum elasticity of the linearity performances (ΔP_{1dB}). As for the classical robust design $LNA_{\#2}$, the decrease of the gain will increase the IP_{1dB}. Considering the RF power levels at the input and output of the device and the limit of the power dissipated by the technology, it is thus possible to bias the device at V_{DS}=12V and V_{GS}=-0.6V. The ΔP_{1dB} increases to reach 8dB of elasticity over its compression point, the P_{1dB} going from 12dBm under low noise bias, to 20 dBm under aggression mode bias.

IV – SIMULATIONS AND RESULTS

$LNA_{\#1}$ will be presented in red for its low noise configuration and black for its DC biasing in EM aggression mode. The classical robust LNA, also noted $LNA_{\#2}$, is presented in blue.
Before presenting the noise and nonlinear performances of the amplifiers, it is important to validate the S-parameters according to the chosen quiescent points. As can be seen on Fig. 4, the S-parameters for the two LNAs present measurements in good agreement with simulations. The measured small-signal gain is 0.5 dB higher than the simulation, but remains constant while switching between the two quiescent points for $LNA_{\#1}$. Matching parameters are slightly degraded compared to the simulations, but they still show similar trends. Despite a degradation of S_{22} in the order of 2 dB, the return losses for $LNA_{\#1}$ are better than 9 dB. Concerning $LNA_{\#2}$, its return losses are better than 11 dB for a gain varying between 11.5 dB and 8 dB in X-band. Concerning the non-linear characteristics of the devices, we observe IP_{1dB} worse than those expected in simulation. This degradation of this figure of merit is explained by the increase in gain

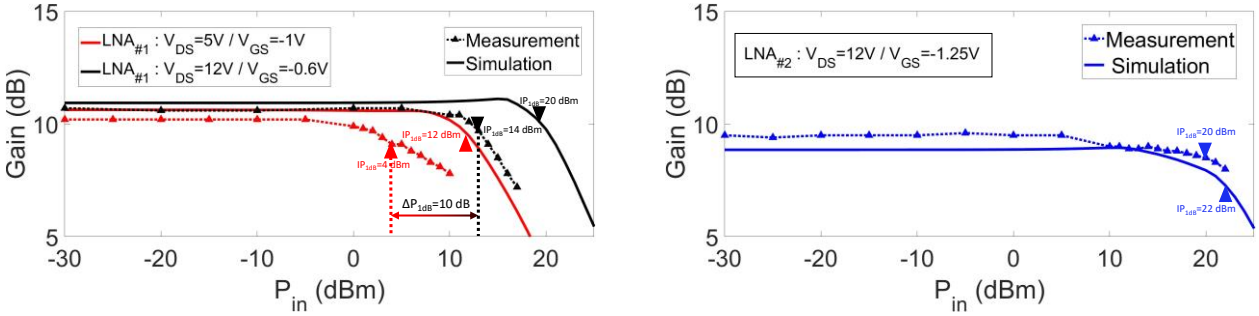


Fig. 5 : Simulated and measured gain vs. RF power at LNAs input for $LNA_{\#1}$ [in its low noise configuration (V_{DS}=5V / V_{GS}=-1V), in **EM aggression mode (V_{DS}=12V / V_{GS}=-0.6V)**] and for $LNA_{\#2}$ (V_{DS}=12V / V_{GS}=-1.25V)

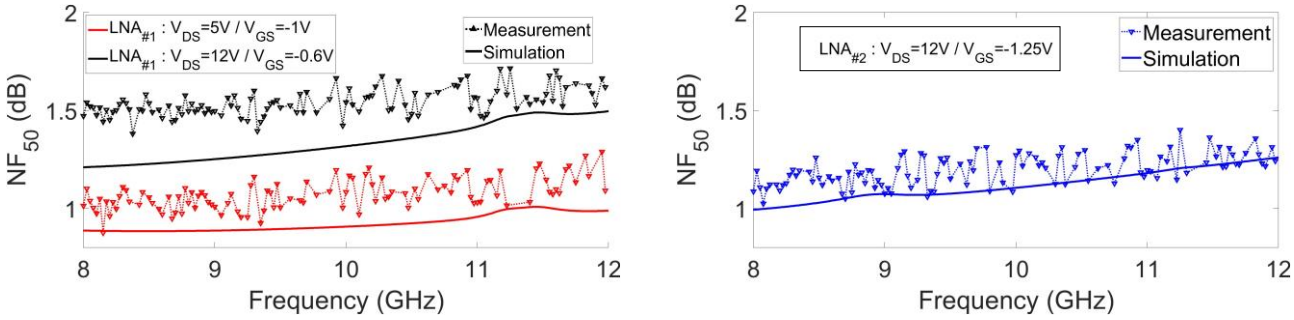


Fig. 6 : Simulated and measured X-band noise figure for $LNA_{\#1}$ [in its low noise configuration (V_{DS}=5V / V_{GS}=-1V), in **EM aggression mode (V_{DS}=12V / V_{GS}=-0.6V)**] and for $LNA_{\#2}$ (V_{DS}=12V / V_{GS}=-1.25V)

between simulation and measurement. For $LNA_{\#1}$, the observed differences between measurement and simulation can be explained by the fact that for a voltage couple of V_{DS}=12V & V_{GS}=-0.6V, the associated drain current is simulated at 140 mA, whereas a value of I_{DS}=73 mA is measured in practice. This offset of the quiescent point when opening the channel does not take advantage of the theoretical maximum excursion along the 50 Ω load line, which allows maximizing IP_{1dB}. Moreover, one cannot benefit from the increase in gain due to the improvement in power that one observes on the simulated plot of Fig. 5. Despite this, the $LNA_{\#1}$ present a ΔP_{1dB} variation of 10 dB, which is consistent with the simulations. The classic robust LNA that does not need to operate at high drain current (I_{DS}=48 mA) achieves a IP_{1dB} of 20 dBm. This represents almost the limit of what the technology can provide in terms of linear output power for a single stage architecture.

Noise figure measurements were performed with the PNA-X N5244B from Keysight, using the accurate low NF measurement option 029. A fair correlation is found between simulations and measurements, with a difference between 0.1 dB and 0.3 dB. Regarding the noise performance, Fig. 6 shows that the average noise figure of the $LNA_{\#1}$ under low noise configuration is as low as 1.05 dB, while the $LNA_{\#2}$ features a reasonable average noise figure of 1.2 dB over the X band. When biased under EM aggression mode, the NF50 of the $LNA_{\#1}$ increases by 0.5 dB.

CONCLUSION

In this paper, a new strategy for designing robust GaN LNA is proposed. By an appropriate selection of the sizing and biasing of the device, it makes it possible to alternately manage an optimal noise figure and a high linearity at the input of the designed amplifier. The proposed voltage reconfigurable LNA has an average noise figure of 1.05 dB over the X-band. Its IP_{1dB} is scalable and has an elasticity of 10 dB. This study on single-stage LNAs demonstrates the opportunity offered by this original strategy of reconfigurable LNA, as an alternative to robust LNA (or to the combination of a device protection prior to the LNA) as needed when the receiver operates under RF jamming aggressions. Indeed, with a lower noise figure and a better gain than that of $LNA_{\#2}$, $LNA_{\#1}$ stands as a good candidate for implementation in a multistage architecture, and even more so in a global reception chain: a two-stage version of the LNA using the proposed strategy of switchable biasing have been successfully implemented. The final objective of this work is to design a voltage reconfigurable system that can switch from a nominal low noise mode to an "EM aggression" protection mode. The design roadmap is to keep the system operating in a linear configuration, to still allow the detectivity of the desired signals. This design method is not limited to the X-band as proposed; indeed, a larger variety of selection in the adjustment parameters is obtained for lower frequencies. In contrast, the design paradigms on the transistor size/bias selection tend to tighten as frequency increases.

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