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Integration of $\text{Li}_4\text{Ti}_5\text{O}_{12}$ Crystalline Films on Silicon towards High-Rate Performance Lithionic Devices

Steven D. Lacey^{1*}, *Elisa Gilardi*², *Elisabeth Müller*³, *Clement Merckling*⁴, *Guillaume Saint-Girons*⁵, *Claude Botella*⁵, *Romain Bachelet*⁵, *Daniele Pergolesi*², and *Mario El Kazzi*^{1*}

Dr. S. D. Lacey, Dr. M. El Kazzi
Electrochemistry Laboratory, Paul Scherrer Institut, CH-5232 Villigen PSI, Switzerland
E-mail: steven.lacey@psi.ch ; mario.el-kazzi@psi.ch

Dr. E. Gilardi, Dr. D. Pergolesi
Multiscale Materials Experiments Laboratory, Paul Scherrer Institut, CH-5232 Villigen PSI, Switzerland

Dr. E. Müller
Electron Microscopy Facility, Paul Scherrer Institut, CH-5232 Villigen PSI, Switzerland

Prof. Dr. C. Merckling
Imec, Kapeldreef 75, Leuven 3001, Belgium

Dr. G. Saint-Girons, Dr. C. Botella, Dr. R. Bachelet
Institut des Nanotechnologies de Lyon (INL-CNRS UMR 5270), Université de Lyon, Ecole Centrale de Lyon, Ecully Cedex 69134, France

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Abstract: The integration of crystalline Li-based oxide thin films on silicon substrates is essential in order to fabricate high performance solid-state lithionic devices. However, growing crystalline oxide films directly on silicon requires high temperatures and oxygen partial pressures, which leads to undesirable interface species that compromise the crystal quality of the oxide films. In this work, we employ a 2 nm $\gamma\text{-Al}_2\text{O}_3$ buffer layer grown on Si(111) substrates in order to grow 90 nm and 50 nm $\text{Li}_4\text{Ti}_5\text{O}_{12}$ (LTO) films. The ultrathin 2 nm $\gamma\text{-Al}_2\text{O}_3$ enables the formation of a stable heterostructure with sharp interfaces and drastically improves the LTO crystallinity. The excellent electrochemical performance of the LTO stacks is verified in liquid-based half-cells. Long-term galvanostatic cycling at 3C (154 mAh g⁻¹ at 1,000 cycles for 90 nm LTO) and 100C (169.5 mAh g⁻¹ at 5,000 cycles for 50 nm LTO) demonstrates 96.5% and 91.2% capacity retention, respectively. A rigorous set of rate capability tests is also performed, where the 50 nm LTO stack attains 55.5 mAh g⁻¹ at an

exceptional C-rate of 5,000C (15 mA cm^{-2}). Finally, delithiation of the 50 nm LTO is successful with sub-millisecond current pulse tests (0.2 ms pulse, 3 mA cm^{-2}) showcasing rapid ionic transport.

1. Introduction

In an ever-growing autonomous world, further technological developments within the internet-of-things (IoT) rely on monolithic integration and miniaturization of functional devices on-chip such as microbatteries,¹ memristive neuromorphic architectures,² and gas sensors.³ Solid-state lithionic devices, formed by integrating oxide-based Li-ion conducting thin films on silicon substrates, offer a very promising solution for the aforementioned applications especially when combined with thin film solid electrolytes.⁴ The Li-ion migration mechanism within such lithionic devices enables operation over a multitude of applications: (i) for energy storage, especially by employing three dimensional solid-state microbattery architectures to achieve high energy and power capability;⁵ (ii) for resistive memory in two-terminal⁶ or three-terminal^{7,8} memristive devices, where fast and low-energy operation (i.e. nonvolatile resistant switching) can be achieved between multilevel analog states; (iii) for electrochemical gas sensing and environmental monitoring/tracking devices, with enhanced stability and selectivity towards gaseous species compared to small commercial gas sensor technologies (i.e. resistive, electrochemical, dispersive infrared radiation absorption, and photoionization detection sensors).^{4,9,10} Accordingly, the use of Li-containing ceramics offers a path towards on-chip multipurpose (energy and memory-based) storage and sensing devices.

In order to achieve optimal performance of the aforementioned lithionic devices, the grown oxide-based thin films (i.e. Li-ion conductors including solid electrolytes) must exhibit excellent Li-ion conductivity as well as (electro-)chemical, structural, and mechanical properties. Moreover, achieving the desired Li stoichiometry, the purest phase, a high degree of crystallinity, and sharp/stable interfaces will facilitate rapid Li-ion transport throughout the

bulk and at the interfaces leading to a device with superior rate performance.⁴ However, integrating epitaxial films of functional Li-based oxides directly onto silicon substrates remains a challenging task due to the large lattice mismatch between these materials as well as substrate reactivity at elevated deposition temperatures and high oxygen partial pressures.¹¹⁻¹³ Such unwanted oxygen-containing species formed at the interface between the silicon (Si) substrate and the Li ceramic compromise the growth quality while building up interfacial resistance, which could reduce overall device performance.

The aim of this study is to enable epitaxial growth of Li-based thin film oxides onto silicon via an ultrathin buffer layer in order to fabricate lithionic devices with exceptional electrochemical performance: (i) excellent cycle life over thousands of cycles⁷ (ii) with high specific capacity, close to the theoretical value, as well as (iii) cycling at exceptionally high C-rates to showcase fast Li-ion diffusivity. Specifically, ~2 nm epitaxial γ -Al₂O₃ films are grown on commercial silicon substrates in order to improve the overall crystal quality of subsequently grown Li-containing oxide films through the formation of a sharp and stable interface. The choice of γ -Al₂O₃ as an ideal buffer material is due to the following attributes: (i) its stability up to 900 °C and 10⁻⁵ Torr pressures on silicon,^{14, 15} (ii) its (111)-oriented growth on Si(001) and Si(111) substrates producing an abrupt interface without the formation of silica or silicates,¹⁶⁻¹⁸ and (iii) its near matching lattice parameter ($a_0 = 7.887 \text{ \AA}$) with most Li-based oxides, which promotes high quality growth of functional oxide layers and fabrication of high performance lithionic devices.

Li₄Ti₅O₁₂ (LTO) is the representative Li-containing oxide material chosen for subsequent deposition on the surface-engineered γ -Al₂O₃/Si(111) substrate in order to verify the LTO growth quality and electrochemical properties. LTO is an ideal candidate due to its spinel structure and lattice parameter of $a_0 = 8.357 \text{ \AA}$, which closely matches γ -Al₂O₃, as well as its wide technological application in both energy- and memory-based storage devices.⁶ Specifically, LTO is a commercialized Li-ion battery electrode material (Toshiba SCiB cell)

with a relatively high theoretical capacity (175 mAh g^{-1}) that offers long cycle life, rapid charging, and high power capabilities in LIBs.¹⁹ For both microbatteries and redox memory devices, LTO offers an additional benefit relating to zero-strain insertion of Li ions. In this case, the LTO thin film experiences negligible volume expansion upon (de)lithiation and thus, the integrity of the thin film stack will be maintained throughout long-term electrochemical cycling.^{20, 21} For memory-based storage, LTO has potential low power computing capabilities, unlike other Li ceramics such as LiCoO_2 , due to its lower operating (de)lithiation potential plateau at 1.55 V vs. Li^+/Li . Moreover, LTO has the ability to undergo metal–insulator transition under applied bias during (de)lithiation,^{22, 23} which allows its intrinsic resistive switching and retention characteristics to be well-controlled.

To the best of our knowledge, this study demonstrates the thinnest barrier layer (~2 nm) in order to grow high quality LTO films on silicon substrates, even at temperatures (500 °C) that are lower than previously reported in literature. The results described hereafter verify the crystal growth and interface quality of LTO/ $\gamma\text{-Al}_2\text{O}_3$ /Si(111) thin film stacks through in-depth structural and chemical characterizations including X-ray diffraction (XRD), transmission electron microscopy (TEM), and X-ray photoelectron spectroscopy (XPS). Additionally, excellent electrochemical performance is demonstrated by cycling the LTO stacks against Li metal in liquid electrolyte with the highly doped Si substrate acting as the current collector.

2. Results and Discussion

The growth of $\gamma\text{-Al}_2\text{O}_3$ with a controlled thickness of 2 nm was conducted in a molecular beam epitaxy (MBE) reactor onto a 4 inch n-type (As-doped) Si(111) wafer using a previously reported procedure.^{14, 24} Note that $\gamma\text{-Al}_2\text{O}_3$ grows along the (111) out-of-plane orientation on Si(111) with a two-for-three unit cell relationship in-plane (i.e. lattice mismatch of -3.2%), which enables high quality epitaxial growth and a sharp, stable interface with the

silicon substrate as previously observed by our collaborators.^{14, 18} To monitor the 2 nm γ -Al₂O₃ thin film crystal quality, reflection high-energy electron diffraction (RHEED) patterns were taken on the Si(111) before and after 2 nm γ -Al₂O₃ growth (**Figure S1**).

Different LTO film thicknesses (2 nm, 30 nm, 50 nm and 90 nm) were directly grown at 500 °C by pulsed laser deposition (PLD) on 2 nm γ -Al₂O₃/Si(111) 9×9 mm² substrates (section 4. *Experimental Section/Methods*). *Ex-situ* XPS measurements acquired at multiple core levels (Si2p, Al2p, and Ti2p) elucidate the composition of the thin films and their interfacial chemical stability when LTO is grown on Si(111) with and without γ -Al₂O₃ as a buffer layer (**Figure 1**, **Figure S2**). Comparisons between the surface modified 2 nm γ -Al₂O₃/Si(111) and as-received commercial As-doped Si(111) substrates show that these doped Si(111) substrates already have a significant amount of native SiO₂, as indicated by the component at 104 eV in the Si2p spectra (**Figure 1a**).²⁵ However, as expected from previous reports,^{15, 17} the Si2p spectra acquired on the 2 nm γ -Al₂O₃/Si(111) does not show any SiO₂ or silicate components indicative of a sharp interface despite the MBE growth process exposing the cleaned silicon substrate to high temperature (750 °C) and high oxygen partial pressure (around 10⁻⁵ Torr) during alumina growth (**Figure 1b**).¹⁴ Note that these samples including the 2 nm γ -Al₂O₃/Si(111) stack were stored in air for several months before the aforementioned *ex-situ* XPS measurements, which further demonstrates the exceptional interface stability when the alumina buffer layer is present. Such a stable interface is also expected to minimize interfacial resistance, which is an important aspect for high performance microdevices that will benefit from using 2 nm γ -Al₂O₃/Si(111) as a standalone current collector. Additionally, the Al2p core level located around 75 eV attest the proper Al oxidation state (3+) for spinel Al₂O₃ grown on Si substrates without (**Figure 1b**) and with LTO (**Figure 1c**). When 2 nm LTO is grown on the 2 nm γ -Al₂O₃/Si(111) substrate, the two characteristic components (2p_{1/2} and 2p_{3/2}) in the Ti2p core level match the expected oxidation state for spinel LTO: Ti⁴⁺ (**Figure 1c**). However, a small amount of SiO_x/silicate is observed

around 103 eV in the Si2p core level (**Figure 1c**),¹³ assumed to be related to the epitaxial Si-O-Al interface since its signal became detectable after the 2 nm LTO growth. The formation of an epitaxial interface between 2 nm γ -Al₂O₃ and Si(111) via Si-O-Al bonds has been reported previously¹⁵. However, we cannot exclude the possibility that a small amount of Li and oxygen could have diffused through the 2 nm γ -Al₂O₃ layer and reacted with the surface of the Si substrate during the PLD growth at 500 °C. Unlike the LTO grown on the engineered 2 nm γ -Al₂O₃/Si(111), the growth of LTO directly on Si(111) led to a significant amount of silicate formation confirmed by the intense component at higher binding energy in the Si2p core level (**Figure 1d**). This result confirms the importance of the alumina buffer layer to mitigate the interfacial reactivity with the Si substrate upon subsequent oxide growth.

The surface reactivity of LTO and γ -Al₂O₃ in contact with ambient air is also investigated by acquiring the C1s, O1s, and Li1s core levels (**Figure S2**). Lithium carbonate (Li₂CO₃) is not detected in the C1s core level acquired on LTO/2 nm γ -Al₂O₃/Si(111) (**Figure S2c**), which confirms a higher stability to air and alludes to higher crystallinity of the LTO film when the γ -Al₂O₃ buffer layer is implemented. Unsurprisingly, a significant amount of lithium carbonate and O-C=O species reside on the surface of the 2 nm LTO grown directly on Si(111), as confirmed by the intense components in the C1s core level located at 291 eV and 289 eV, respectively (**Figure S2d**). Additional intense signals located at 56 eV and 533 eV in the Li1s and O1s core levels, respectively, are further affirmation of the instability of the LTO film grown directly on Si(111) when exposed to ambient air. XPS measurements on a 90 nm LTO/2 nm γ -Al₂O₃/Si(111) stack can be found in Supporting Information (**Figure S3**), which also confirms both air stability and high quality growth of thick LTO on alumina.

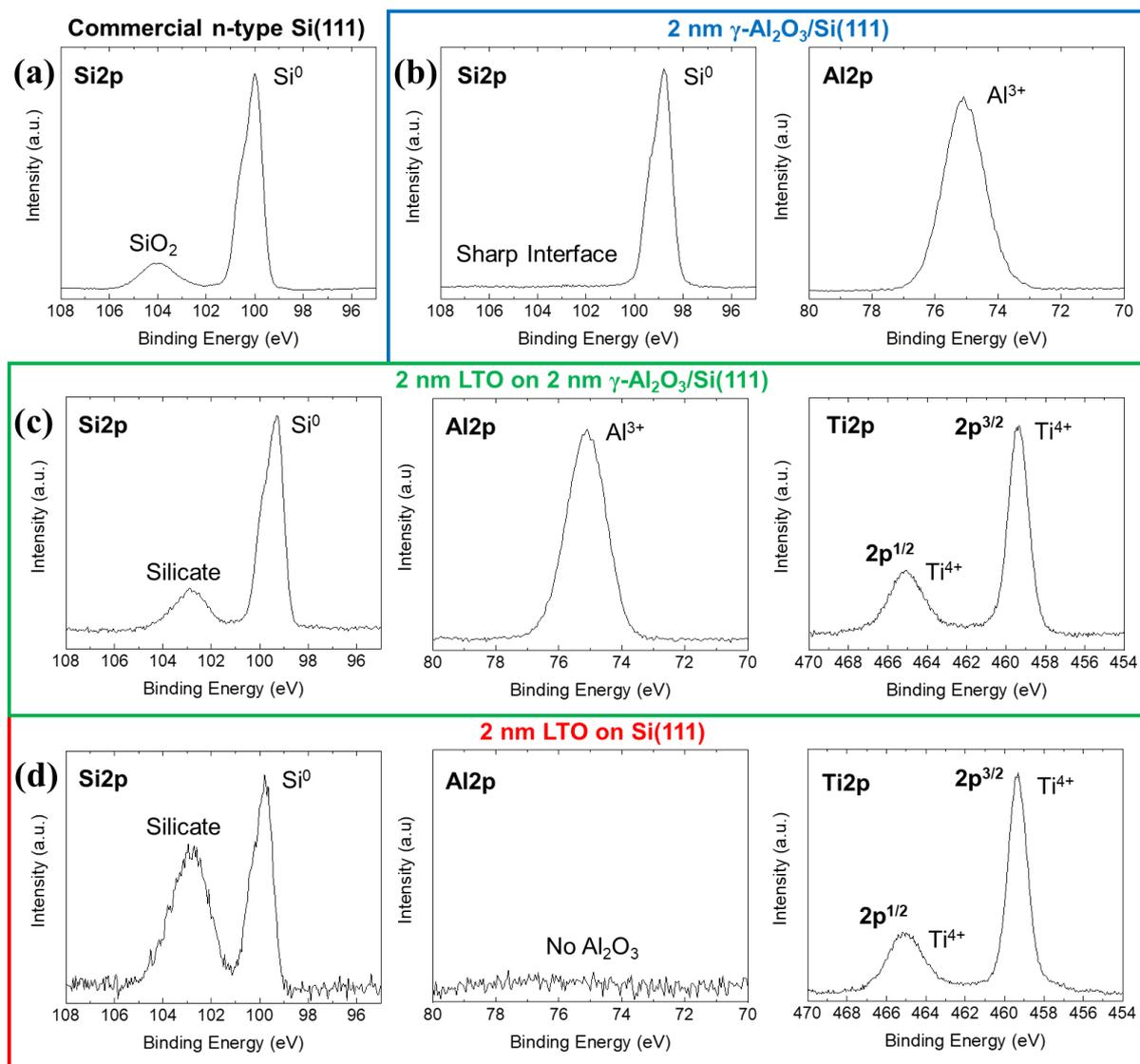


Figure 1. XPS Si2p, Al2p, and Ti2p core levels acquired on: (a) the as-received commercial As-doped Si(111) substrate; (b) 2 nm γ -Al₂O₃/Si(111); (c) 2 nm LTO on 2 nm γ -Al₂O₃/Si(111) and (d) 2 nm LTO on Si(111).

The structural quality of the LTO films was elucidated by out-of-plane XRD measurements performed on 90 nm LTO grown directly on Si(111) and the surface modified 2 nm γ -Al₂O₃/Si(111) substrates (**Figure S4**). These results confirm that LTO is (111)-oriented regardless of the γ -Al₂O₃ buffer layer. However, using such a low deposition temperature (i.e. 500 °C) causes the LTO grown directly on Si(111) to have a lower degree of crystallinity due to both thermal budget concerns and attempting to grow on an uneven Si surface covered with SiO₂ and silicates. In this case, a higher thermal budget for nucleation is required in order to grow crystalline LTO films on such an inferior initial Si surface.

Accordingly, LTO depositions reported in literature on SiO_2 ^{26, 27} or TiN ²⁸⁻³⁰ layers typically occur at higher temperatures (600-700 °C) in order to obtain more crystalline films. However, this can lead to additional undesirable reactions such as Li loss within the oxide film or even enhanced reactions between Li and oxygen with the surface of the Si substrate or the barrier film (e.g. TiN oxidizing under growth conditions, which diminishes the intrinsic barrier characteristics of nitride materials).

This is not the case for the 2 nm $\gamma\text{-Al}_2\text{O}_3/\text{Si}(111)$ substrate, where the LTO is highly crystalline even when grown at 500 °C, since nucleation is more energetically favorable on epitaxial alumina and abrupt stable interfaces in general. Furthermore, when aligning LTO(111) and $\gamma\text{-Al}_2\text{O}_3(111)$ cube-to-cube, there is a relatively small lattice mismatch of 6% compared to the 54% cube-on-cube mismatch between LTO(111) and Si(111) (**Table S1, Figure S5**). This promotes more continuity throughout the nucleation growth process and even enables preferential crystal orientations when the alumina buffer layer is employed. More in-depth XRD analysis on a thinner 30 nm LTO deposited on 2 nm $\gamma\text{-Al}_2\text{O}_3/\text{Si}(111)$ stack using both out-of-plane and in-plane radial scans yields information regarding the lattice parameters and the in-plane LTO orientation with respect to the Si(111) substrate (**Figure 2a-2b**). Specifically, LTO(111) and Si(111) have out-of-plane lattice parameters of 8.296 Å and 8.37 Å, respectively, confirming that the 30 nm LTO film is under tensile strain. **Figure 2c-2d** shows the in-plane Si(220) and LTO(440) pole figures, where in-plane and asymmetric reflections are indicated by arrows and circles, respectively. As expected, the Si(111) substrate has three-fold symmetry with intense peaks every 120° towards the Si <001> directions. Notably, the deposited LTO has six-fold symmetry, which is an indication of bidomains where two in-plane orientations are rotated by 180° around the growth direction. The LTO bidomains could arise from either the presence of stacking faults or from the $\gamma\text{-Al}_2\text{O}_3$ buffer layer itself, the latter of which has been previously reported for $\gamma\text{-Al}_2\text{O}_3/\text{Si}(111)$ where two in-plane orientations are rotated by 180°: i.e., a direct relationship with the

substrate, $[11-2]\gamma\text{-Al}_2\text{O}_3(111)//[11-2]\text{Si}(111)$, and a mirror relationship, $[-1-12]\gamma\text{-Al}_2\text{O}_3(111)//[11-2]\text{Si}(111)$.¹⁸ Similar bidomain orientations have also been observed for a different spinel material (CoFe_2O_4) deposited on $\gamma\text{-Al}_2\text{O}_3/\text{Si}(111)$.³¹ A low mosaicity of 0.89° further indicates the favorable alignment between the crystal orientations, as expected by the relatively small lattice mismatch between spinel LTO and $\gamma\text{-Al}_2\text{O}_3$ (**Figure S6**).

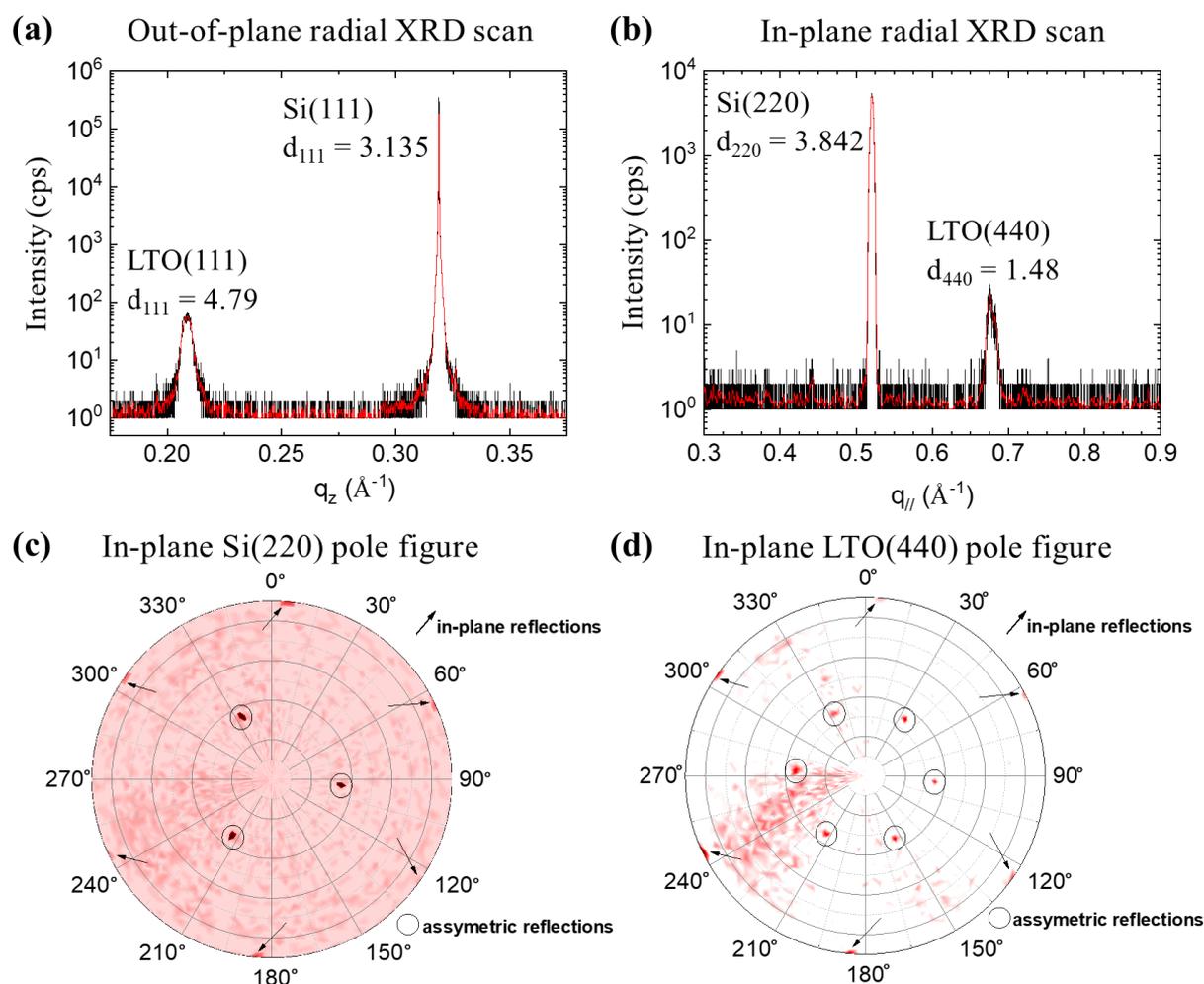


Figure 2. (a) Out-of-plane and (b) in-plane radial XRD scans of a 30 nm LTO/2 nm $\gamma\text{-Al}_2\text{O}_3/\text{Si}(111)$ stack with corresponding lattice parameters. In-plane (c) Si(220) and (d) LTO(440) pole figures, where silicon has three-fold symmetry while LTO has six-fold symmetry. This indicates that PLD growth on the surface modified 2 nm $\gamma\text{-Al}_2\text{O}_3/\text{Si}(111)$ substrate results in LTO bidomains rotated by 180° around the growth direction.

TEM, FFT patterns, and EDX maps (**Figure 3, Figure S7**) of a 90 nm LTO/2 nm $\gamma\text{-Al}_2\text{O}_3/\text{Si}(111)$ stack were taken after electrochemical cycling over 1,000 cycles at a 3C rate, which further confirm the presence of sharp interfaces and LTO grain orientations. Note that

the TEM lamella was carefully thinned along the Si(110) direction by a focused ion beam (FIB) tool in order to allow HRTEM imaging (section 4. *Experimental Section/Methods*). **Figure 3a** shows the distinct stack layers including the Si(111) substrate, ~2 nm γ -Al₂O₃, and 90 nm LTO, of which the latter is composed of multiple (defective) grains formed by columnar growth. By visual inspection, the interfaces with Si and LTO are abrupt and the LTO layer is not a single crystalline layer but is composed of numerous grains, which contain stacking faults/twins that give rise to different in-plane crystal orientations. The electron diffraction pattern acquired along the Si[110] zone axis further confirms the presence of crystalline LTO grains, which are in a majority oriented with a LTO plane parallel to the Si(111) growth plane. The stacking faults give rise to diffraction lines crowded with spots (**Figure S8**). Due to the size of the selected area electron diffraction aperture, this electron diffraction pattern originates from a specimen area of 150-200 nm in diameter. However, since the individual LTO grains are much smaller than this, FFT patterns were taken from multiple areas to confirm the orientation of these individual sections (**Figure 3b-3e**). Unsurprisingly, the silicon substrate (white square in **Figure 3a**) and an LTO grain (red square) are single crystalline. Note the pink and green dashed lines that highlight the two equivalent [111] crystallographic directions, with the latter at an oblique angle with respect to the preferred growth direction (pink). **Figure 3d** (bright blue square) and **Figure 3e** (orange square) show more streaky FFT patterns of the aforementioned TEM image, which are areas characterized by less regular stacking along one of the two [111] directions. The FFTs confirm the presence of mainly two crystal orientations differing from each other by a 180° rotation around the [111] growth direction, where PLD growth likely starts from small crystallites that can have either orientation with respect to the substrate. Alternatively, they form at a later stage of the layer growth due to stacking fault formation. Note that a minor amount of stacking faults are observed, which creates crystallites with an orientation relation, with respect to the previously mentioned two types of grains, rotated by 180° around a [111]

direction that differs from the growth direction (green dashed line in **Figure 3c-3d**). This result confirms the six-fold symmetry also seen from the in-plane XRD results presented in **Figure 2**.

A higher resolution TEM image and EDX maps explore the integrity of individual layers of the 90 nm LTO/2 nm γ -Al₂O₃/Si(111) stack (**Figure 3f-3h**). **Figure 3f** shows that the interface of the Si(111) substrate is not completely straight, where it increases layer by layer with a deviation of ~ 3 - 4° . The white lines denote three dot layers along the [111], which corresponds to ~ 0.9 nm, as expected for Si(111) substrates. A thin (~ 2 nm) alumina layer separates the silicon from the LTO layer yet, it seems to be less crystalline than the other stack layers. This lower degree of crystallinity could be caused by damage during FIB preparation of the lamellae. There is a significant amount of contrast in the LTO layer, which corresponds to crystallites growing along different [111] directions as well as stacking faults/twinning with respect to the (111) plane. This creates strong interference patterns in the image. To ensure that the alumina layer is distinctly separating the Si(111) and LTO layers, EDX mapping has been performed (**Figure 3g-3h**). By comparing the Si-Al-O overlay to the Si-Al-Ti overlay, it is clear that there is overlap between Al (blue) and O (red), as shown by the purple stripe in **Figure 3g**. Yet, there is no overlap between Al (blue) and Ti (red) signals in **Figure 3h** or any of these signals with Si (green), which confirms that this 2 nm γ -Al₂O₃ buffer layer is not composed of silica, silicates or amorphous LTO. This finding corroborates with the aforementioned *ex-situ* XPS data (**Figure 1c**), where the component observed in the Si2p core level at 103 eV is associated with the epitaxial Si-O-Al interface.¹⁵ Further proof of the sharp interface formed by the 2 nm γ -Al₂O₃ layer is shown in the individual elemental maps (**Figure S7**).

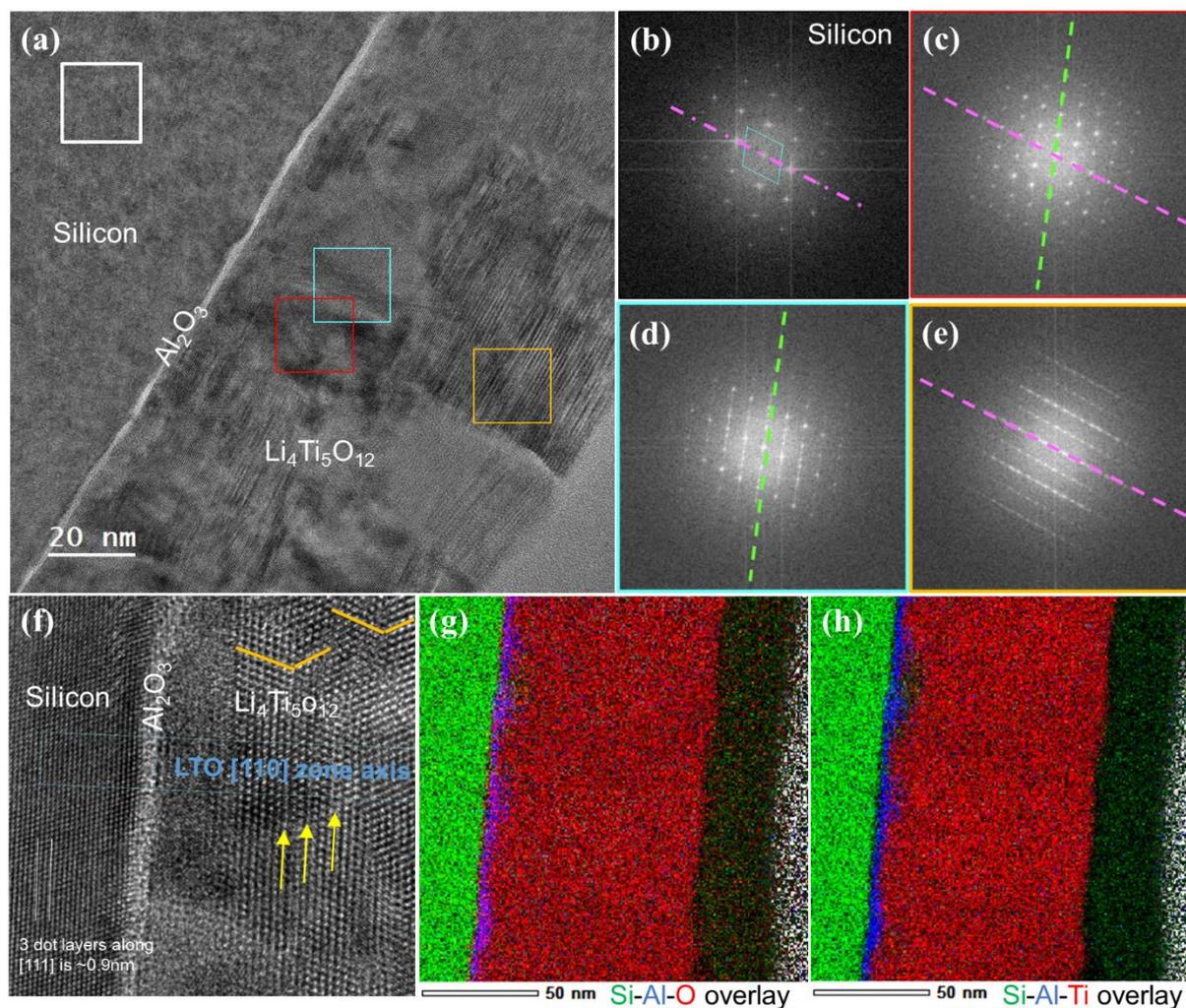


Figure 3. (a) TEM image acquired along Si(110) of the 90 nm LTO/2 nm γ -Al₂O₃/Si(111) stack, which was electrochemically cycled over 1,000 cycles at a 3C rate. (b-e) FFT patterns on different LTO areas as well as the Si substrate, which enables crystal orientation analysis of small LTO grains. LTO is aligned in mainly two in-plane orientations with respect to Si. The crystallographic axes of LTO are (d, blue square in a) parallel (green dashes) to the Si substrate and (e, yellow square in a) rotated around the growth axis (pink dashes) by 180° due to stacking faults. The red area shown as (c) has the combination of these two crystal orientations. (f) HRTEM image at the interfaces displaying twins (orange lines) and interference contrast due to stacking faults (yellow arrows). (g-h) EDX overlay maps showing the distinct interfaces between Si(111), 2 nm γ -Al₂O₃, and LTO. Based on the overlays, the buffer layer can only be composed of alumina.

After confirming the crystal quality of the LTO growth and the interfacial stability between LTO/ γ -Al₂O₃ and γ -Al₂O₃/Si(111), subsequent galvanostatic tests were performed on thin film stacks in a half-cell configuration using conventional liquid electrolyte (LC30) and metallic Li as a counter electrode. **Figure 4** displays the electrochemical validation of the 90 nm LTO/2 nm γ -Al₂O₃/Si(111) stack, where the highly doped Si(111) substrate acts directly

as the current collector. Notably, the 90 nm LTO stack successfully cycles at high rates up to 30C with a reversible capacity of 132 mAh g⁻¹ within a shallow potential cutoff window from 1.4 to 1.7 V vs. Li⁺/Li (Figure 4a). Corresponding voltage profiles are shown in Figure S9. Beyond rate capability, the PLD-grown LTO film cycles reversibly with 96.5% capacity retention even after one thousand cycles at 3C (Figure 4b). The inset shows a typical voltage profile at a rate of 3C, where the characteristic 1.55V (de)lithiation plateau for LTO can be observed. The overall rate capability and long-term cycling stability of the 90 nm LTO/2 nm γ -Al₂O₃/Si(111) stack is indicative of the PLD growth quality and LTO crystallinity albeit deposited at low temperature (500 °C). Additionally, the reversibility of the (de)lithiation process showcases the successful implementation of doped Si(111) as a standalone current collector for on-chip Si-based microbatteries.

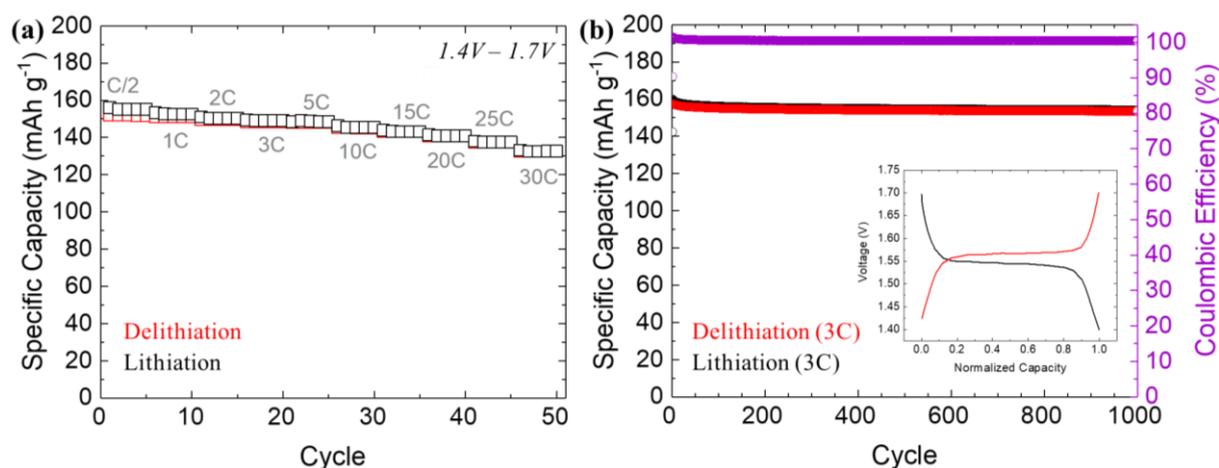


Figure 4. Electrochemical cycling performance of the 90 nm LTO/2 nm γ -Al₂O₃/Si(111) stack: (a) rate performance from C/2 to 30C and (b) long-term 3C cycling within an operating window of 1.4-1.7 V vs. Li⁺/Li. The inset in (b) is a typical voltage profile of the PLD-grown LTO stack at a rate of 3C with the characteristic 1.55V voltage plateaus for (de)lithiated LTO.

The film thickness is an important parameter to explore in order to optimize the fabrication and performance of lithionic devices. For thin film microbatteries, the thickness of the electrode material strongly dictates the electrochemistry since surface-based contributions become more dominant. Accordingly, a thinner 50 nm LTO/2 nm γ -Al₂O₃/Si(111) stack was fabricated and galvanostatically cycled. Figure S10 compares normalized voltage profiles for

thin (50 nm) and thick (90 nm) LTO/2 nm γ -Al₂O₃/Si(111) films operating between 1.4 and 1.7 V vs. Li⁺/Li. At 3C, the voltage profiles match well between the two thicknesses with similar overpotentials; however, as the cycling rate increases above 10 C, the thick (90 nm) LTO suffers from larger overpotentials in comparison, which also limits the achievable capacity when cycling in such a shallow voltage window. To avoid potential limitations, the potential window for subsequent electrochemical measurements was extended to 1-2.5 V vs. Li⁺/Li (**Figure 5**).

Figure 5 showcases the exceptional rate capability and long-term cyclability of the 50 nm LTO/2 nm γ -Al₂O₃/Si(111). This thin LTO stack was successfully cycled between 1V and 2.5 V vs. Li⁺/Li at rates from 25C to 1,000C (**Figure 5a-b**). Until 200C, the specific (dis)charge capacity exceeds the 175 mAh g⁻¹ theoretical value for LTO. Note that this previously reported phenomenon arises from surface-based contributions depending on the film morphology including overlithiation of surface facets compared to the bulk.^{32, 33} A reversible capacity of 136 mAh g⁻¹ is achieved at an extreme C-rate of 350C rate (1.05 mA cm⁻²) while 59 mAh g⁻¹ is attained at 1,000C (3 mA cm⁻²). **Figure 5b** exhibits the corresponding voltage profiles for rates up to 1,000C, where the overpotential consistently increases with higher C-rates. The excellent rate capability and reversible operation at high current densities (up to 3 mA cm⁻²) suggests enhanced Li-ion kinetics compared to the thicker (90 nm) LTO stack. Due to the rapid (de)lithiation processes occurring at such high C-rates, additional rate tests were performed for the 50 nm LTO stack (**Figure 5c**) where the Li reservoir was replenished (lithiated) at lower rates (10C) before delithiated at high rates (up to 5,000C). In this case, the achievable specific capacities upon delithiation are significantly increased, where nearly the same specific capacity reported at 1,000C can be achieved at an excessive C-rate of 5,000C (15 mA cm⁻²). Notably, the theoretical capacity of LTO (175 mAh g⁻¹) can still be achieved upon delithiation at 600C or 1.8 mA cm⁻² with a constant 10C lithiation. The limitations during the lithiation process can be explained by the low electronic

conductivity of the non-lithiated LTO compared to the lithiated compound ($\text{Li}_7\text{Ti}_5\text{O}_{12}$) leading to high polarization at high cycling rates. Specifically, Young *et al.* has reported, even at less than 5% lithiation, a dramatic increase in the bulk electronic conductivity of LTO from approximately 10^{-7} to 10^{-1} S cm^{-1} .²³ To determine long-term cyclability, the 50 nm LTO stack was immediately cycled at 100C ($300 \mu\text{A cm}^{-2}$) after the aforementioned rate tests. **Figure 5d** shows the exceptionally stable cycling of the 50 nm LTO stack for 5,000 cycles with a capacity retention of 91.2%. Thus, thinner LTO films deposited on 2 nm $\gamma\text{-Al}_2\text{O}_3/\text{Si}(111)$ outperform thicker films in terms of achievable capacity and retention at higher C-rates with reduced overpotentials.

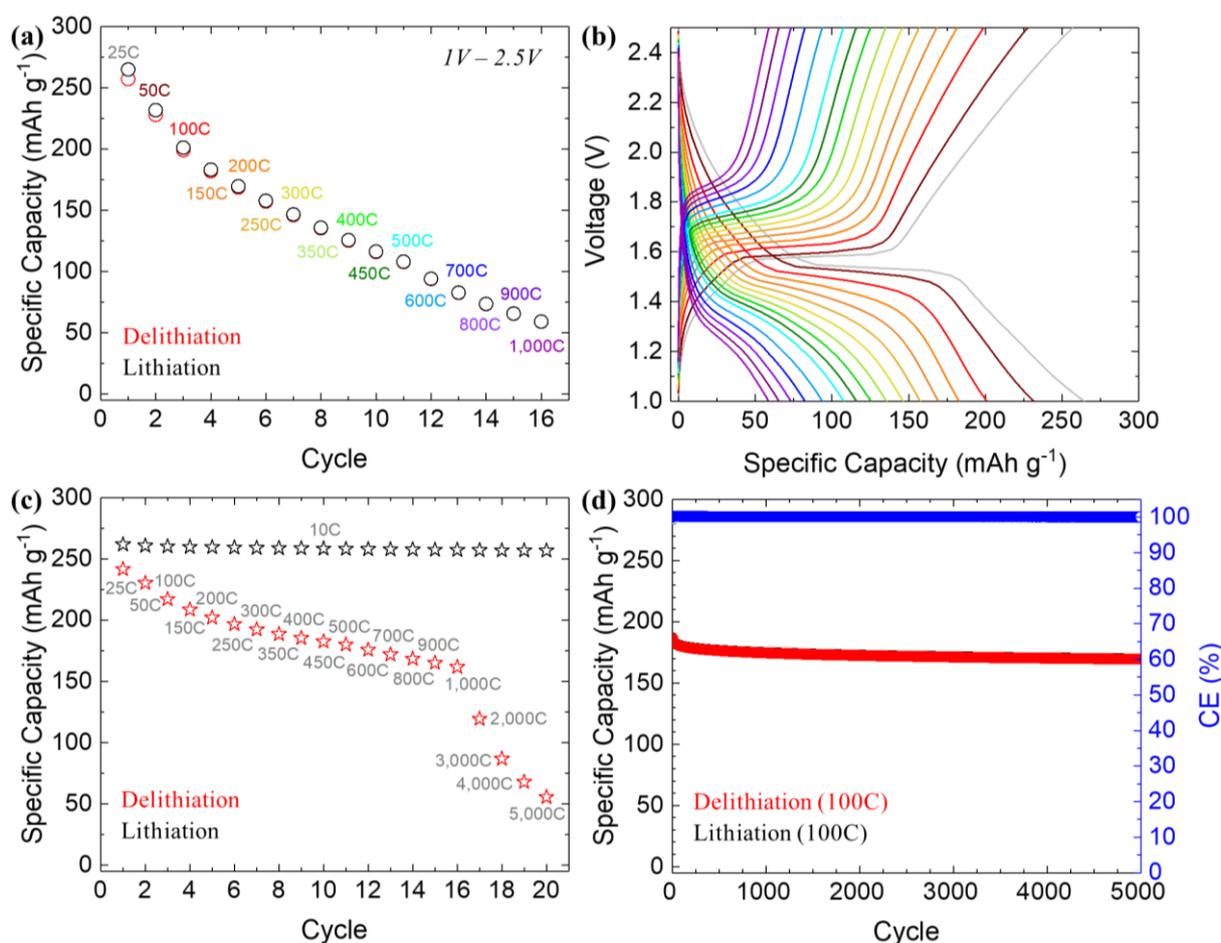


Figure 5. (a) Extended rate capability of the 50 nm LTO/2 nm $\gamma\text{-Al}_2\text{O}_3/\text{Si}(111)$ stack cycled within a wide voltage window (1-2.5 V vs. Li^+/Li) from 25C to 1,000C and (b) the corresponding voltage profiles, with associated colors up to 1,000C. (c) Special condition rate capability test, where the lithiation process remains at 10C (black stars) yet the delithiation

rates are varied from 25C to 5,000C (red stars). (d) Long-term galvanostatic cycling at a rate of 100C between 1 V and 2.5 V vs. Li^+/Li .

To emphasize the potential of thin LTO films for resistive memory devices where fast switching timescales (μs - ms) are required,^{4,7} sub-millisecond pulse tests (1,000C or 3 mA cm^{-2} , 0.2 ms pulse, 5 s rest) on 50 nm LTO/2 nm $\gamma\text{-Al}_2\text{O}_3/\text{As-doped Si(111)}$ stacks were conducted within a 1.4-1.7 V voltage window. **Figure 6** shows that Li can be successfully extracted with such short pulses as confirmed by the obtained delithiation plateau at ~ 1.55 V vs. Li^+/Li . The calculated Li-ion diffusion coefficients are 10^{-11} – mid $10^{-10} \text{ cm}^2 \text{ s}^{-1}$, which is relatively higher than the typical range (10^{-12} – $10^{-11} \text{ cm}^2 \text{ s}^{-1}$) reported for bulk LTO particles.³⁴

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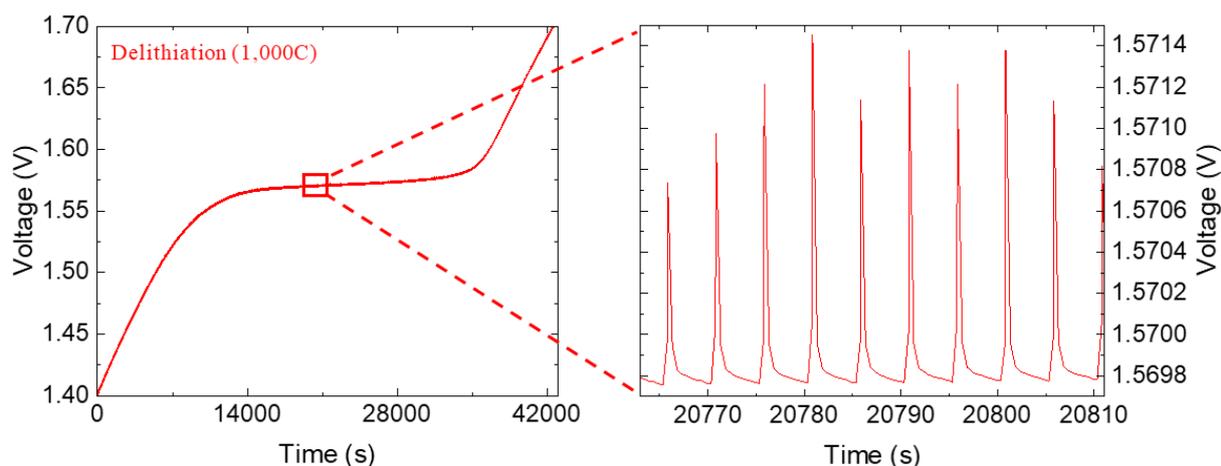


Figure 6. Sub-millisecond current pulse test (1,000C or 3 mA cm^{-2} , 0.2 ms pulse, 5 s rest) during delithiation of the 50 nm LTO/2 nm $\gamma\text{-Al}_2\text{O}_3/\text{Si(111)}$ stack. The zoom-in area shows the pulse response at the delithiation plateau.

By depositing even thinner LTO films (<50 nm) on the proposed $\gamma\text{-Al}_2\text{O}_3/\text{Si(111)}$ substrates, we envision further improvements regarding the growth quality of the oxide (e.g. epitaxial, single crystal) and the film's ionic transport characteristics. With the aforementioned 50 nm LTO film, these initial high C-rate and pulse tests in liquid electrolyte likely yield an upper diffusion limit that we should be mindful of when fabricating and testing all-solid-state device architectures. For instance, an ideal solid-state design is as follows: a Li-

ion synaptic transistor using LTO or chemically lithiated LTO as the channel, lithium phosphorus oxynitride (LiPON) as the solid electrolyte,³⁶ and (lithiated) silicon as the gate. Since our surface modified Si(111) substrate with 2 nm γ -Al₂O₃ has improved the growth quality of Li-containing oxides, future studies will explore this all-solid-state device architecture and similar component designs, such as growing Li ceramics on industrially relevant Si(001) with an γ -Al₂O₃ buffer layer, for neuromorphic applications and beyond. Note that γ -Al₂O₃ grown on Si(001) has been previously verified to have the same structural quality and out-of-plane orientation as Si(111) substrates.^{14, 37}

3. Conclusion

In summary, a high quality LTO film can be grown on silicon substrates by applying an ultrathin (2 nm) γ -Al₂O₃ buffer layer. This alumina layer enables highly crystalline LTO films to be deposited by PLD at low temperature (500 °C) while mitigating the formation of undesirable species such as silicates and SiO₂ on the surface of the silicon substrate. From in-depth structural characterization, the PLD process results in columnar growth of LTO(111) bidomains with two grain orientations rotated by 180° along the [111] growth axis. HRTEM and elemental maps acquired after 1,000 cycles at 3C also confirmed the sharp interfaces between Si-Al₂O₃-LTO, which showcases the overall crystalline quality of the Li-containing oxide film.

The electrochemical performance of the LTO thin film stacks was verified in liquid-based half-cells using the surface modified γ -Al₂O₃/Si(111) substrate directly as a current collector. Long-term galvanostatic cycling measurements of 90 nm and 50 nm LTO stacks were conducted at 3C with 96.5% capacity retention after 1,000 cycles and 100C (300 μ A cm⁻²) with 91.2% capacity retention after 5,000 cycles, respectively. A multitude of rate capability tests were performed using different voltage ranges (1.4-1.7 V vs. 1-2.5 V vs Li⁺/Li) and special conditions such as 10C lithiation steps while varying the delithiation C-

rates up to 5,000C. For the latter test, the 50 nm LTO/2 nm γ -Al₂O₃/Si(111) stack cycled with a charge capacity of 55.5 mAh g⁻¹ at an extreme rate of 5,000C (15 mA cm⁻²). Additionally, the stack retained more than 80% of LTO's theoretical capacity until a C-rate of 350C (1.05 mA cm⁻²). Furthermore, to showcase rapid (de)intercalation of the LTO thin film, sub-millisecond current pulses (0.2 ms pulse at 1,000C or 3 mA cm⁻²) were successfully applied to the 50 nm LTO/2 nm γ -Al₂O₃/Si(111) stack confirming the fast Li-ion diffusion promising the possibility of fast switching timescales in resistive memory devices.

This work highlights the feasibility to integrate oxide-based Li-ion conducting thin films on Si-based chips through interface engineering via a 2 nm alumina buffer layer to promote further developments in solid-state lithionic devices such as microbatteries, memristive memories or gas sensor technologies.

4. Experimental Section/Methods

Thin film depositions: Commercial n-type silicon wafers (As-doped, <111> orientation, 0.001-0.005 Ohm-cm, 100 mm diameter, 500 μ m thick) were purchased from University Wafer Inc. The silicon wafers were treated with HF and flushed at 750 °C in order to remove undesirable species, such as native SiO₂, from the surface. Next, an ultrathin (2 nm) γ -Al₂O₃ layer was grown onto 4 inch Si wafers by MBE (Riber 2300 reactor) at 750 °C under a 10⁻⁵ Torr oxygen partial pressure. Note that full procedural details have been previously reported.¹⁴ A 30 kV RHEED system is attached to the Riber 2300 MBE reactor in order to monitor the film growth characteristics. The resulting γ -Al₂O₃/Si(111) wafer was then laser cut into 9 × 9 mm substrates for subsequent growth of Li-containing oxides. Specifically, Li₄Ti₅O₁₂ (LTO) layers were grown by PLD at 500 °C on both the as-received commercial n-type Si(111) and the surface modified Si(111) substrates with 2 nm γ -Al₂O₃ using a stainless steel mask with Pt paste as thermal backing. The sintered LTO target was placed 4 cm away from the substrate during the PLD growth and had a Li-rich composition (Li/Ti = 1.03) due to

the addition of Li₂O powder. The following deposition parameters were used: repetition rate of 5 Hz, 1.6 J cm⁻², 10⁻² mbar oxygen pressure and mid 10⁻⁵ mbar background pressure, where the deposition and cooling pressure values match. **Note that the Pt paste was mechanically removed directly after PLD growth.**

Surface characterization: *ex-situ* XPS measurements were conducted in-house on a VG ESCALAB 220iXL spectrometer (Thermo Fisher Scientific) with the following parameters: base pressure of $\sim 2 \times 10^{-9}$ mbar, $\sim 500 \mu\text{m}^2$ beam size with focused monochromatized Al K α radiation (1486.6 eV), and spectra recorded with 50 ms dwell time in steps of 0.05 eV with a 30 eV pass energy. The spectrometer was calibrated on a clean silver surface by measuring the Ag3d_{5/2} peak at a binding energy of 368.25 eV with a full width at half maximum (FWHM) of 0.78 eV. No charge effect has been observed on the different samples since the adventitious carbon component in the C1s core level is always detected at 285.85 eV, which has similar values to our previous study (i.e. Si thin films deposited on Cu).³⁸

Bulk and interface characterization: **A combination of in-house (Bruker AXS D8) and in- and out-of-plane XRD measurements were performed.** To prepare the TEM lamella, the galvanostatically cycled LTO on Al₂O₃/Si(111) stacks were first extracted from the liquid half-cells in an Ar-filled glovebox and thoroughly rinsed with DMC to remove any residual salts and other electrolyte components from the surface. The cleaned specimen was then transferred to the FIB tool (Zeiss Nvision 40) for TEM preparation to achieve a 50-200 nm thick lamella. Carbon and platinum capping layers were deposited on the thin film stack first by electron deposition followed by Ga-deposition to maintain sample integrity during Ga-ion milling. The final polishing step was done with a Ga-ion beam of 100 pA and 3 keV acceleration voltage. In the TEM (probe corrected JEOL JEM-ARM200F with EDS detector), the specimen was tilted to be illuminated along the Si[110] direction. Note that electron diffraction patterns taken from larger areas were complemented with Fourier transforms of

small HRTEM image areas of 100-200 nm diameter in order to determine the local crystal structure and crystallographic orientation.

Electrochemical testing: Custom half-cells were assembled in a 2-electrode configuration in an Ar-filled glovebox using LC30 electrolyte [1M LiClO₄ salt in a mixture of 1:1 w/w of ethylene carbonate (EC) and dimethyl carbonate (DMC), Gotion], a glass fiber separator, and metallic Li as the counter/reference electrode. All cells were placed in a temperature-controlled chamber set at 25 °C during the electrochemical measurements. Galvanostatic cycling tests were carried out on a VMP3 potentiostat (BioLogic) with different cutoff potentials (1.4-1.7 V and 1-2.5 V vs. Li⁺/Li) and applied C-rate currents calculated based on the following parameters: theoretical density of LTO (3.43 g cm⁻³), LTO film thickness (90 or 50 nm), the lateral dimensions of the sample (≤9 mm × ≤9 mm), and the theoretical capacity of LTO (175 mAh g⁻¹). Upon cell assembly, the LTO stacks were initially discharged (lithiated) to the lower cutoff potential so each cycle ends on the delithiation process. Electrochemical characterization began with rate capability tests (C-rates from C/2 up to 5,000C) followed by long-term galvanostatic cycling at the desired C-rate (3C or 100C for 90 nm and 50 nm LTO stacks, respectively). Additional current pulsing tests (0.2 ms pulse with 5 s rest) were performed on the 50 nm LTO stack in a shallow operating window (1.4-1.7 V vs. Li⁺/Li) at a high C-rate of 1,000C to determine diffusivity values and potential limitations regarding Li (de)insertion.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgements

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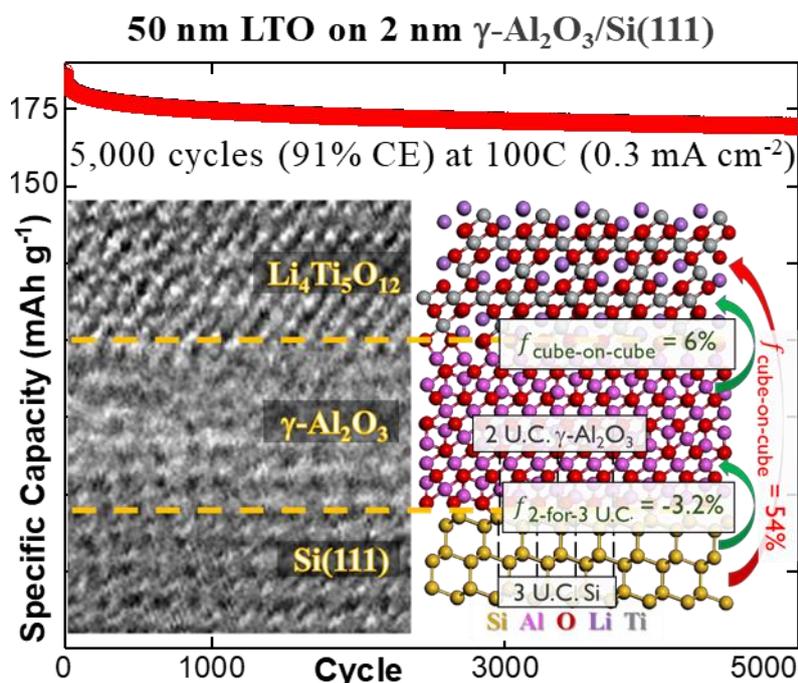
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TOC

Integration of $\text{Li}_4\text{Ti}_5\text{O}_{12}$ Crystalline Films on Silicon towards High-Rate Performance Lithionic Devices

Steven D. Lacey^{1*}, Elisa Gilardi², Elisabeth Müller³, Clement Merckling⁴, Guillaume Saint-Girons⁵, Claude Botella⁵, Romain Bachelet⁵, Daniele Pergolesi², and Mario El Kazzi^{1*}



The growth of high quality Li-containing oxides on silicon is a challenging task. Herein, on-chip lithionic devices become feasible through interface engineering with an ultrathin (2 nm alumina) buffer layer. 50 nm lithium titanate layers grown on alumina/silicon substrates exhibit exceptional electrochemical performance in half-cells, where reversible cycling is possible even at extreme C-rates up to 5,000C (15 mA cm^{-2}).

Supporting Information

Integration of $\text{Li}_4\text{Ti}_5\text{O}_{12}$ Crystalline Films on Silicon towards High-Rate Performance Lithionic Devices

Steven D. Lacey^{1*}, *Elisa Gilardi*², *Elisabeth Müller*³, *Clement Merckling*⁴, *Guillaume Saint-Girons*⁵, *Claude Botella*⁵, *Romain Bachelet*⁵, *Daniele Pergolesi*², and *Mario El Kazzi*^{1*}

Dr. S. D. Lacey, Dr. M. El Kazzi
Electrochemistry Laboratory, Paul Scherrer Institut, CH-5232 Villigen PSI, Switzerland
E-mail: steven.lacey@psi.ch ; mario.el-kazzi@psi.ch

Dr. E. Gilardi, Dr. D. Pergolesi
Multiscale Materials Experiments Laboratory, Paul Scherrer Institut, CH-5232 Villigen PSI, Switzerland

Dr. E. Müller
Electron Microscopy Facility, Paul Scherrer Institut, CH-5232 Villigen PSI, Switzerland

Prof. Dr. C. Merckling
Imec, Kapeldreef 75, Leuven 3001, Belgium

Dr. G. Saint-Girons, Dr. C. Botella, Dr. R. Bachelet
Institut des Nanotechnologies de Lyon (INL-CNRS UMR 5270), Université de Lyon, Ecole Centrale de Lyon, Ecully Cedex 69134, France

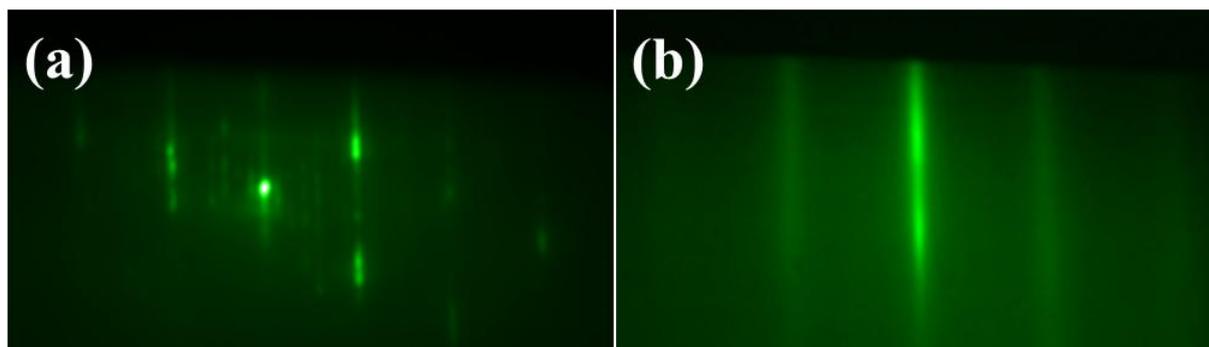


Figure S1. RHEED patterns along the [11-2] azimuthal direction of the (a) Si(111) (7×7) reconstructed surface and (b) after growth of the 2 nm thick $\gamma\text{-Al}_2\text{O}_3$ film.

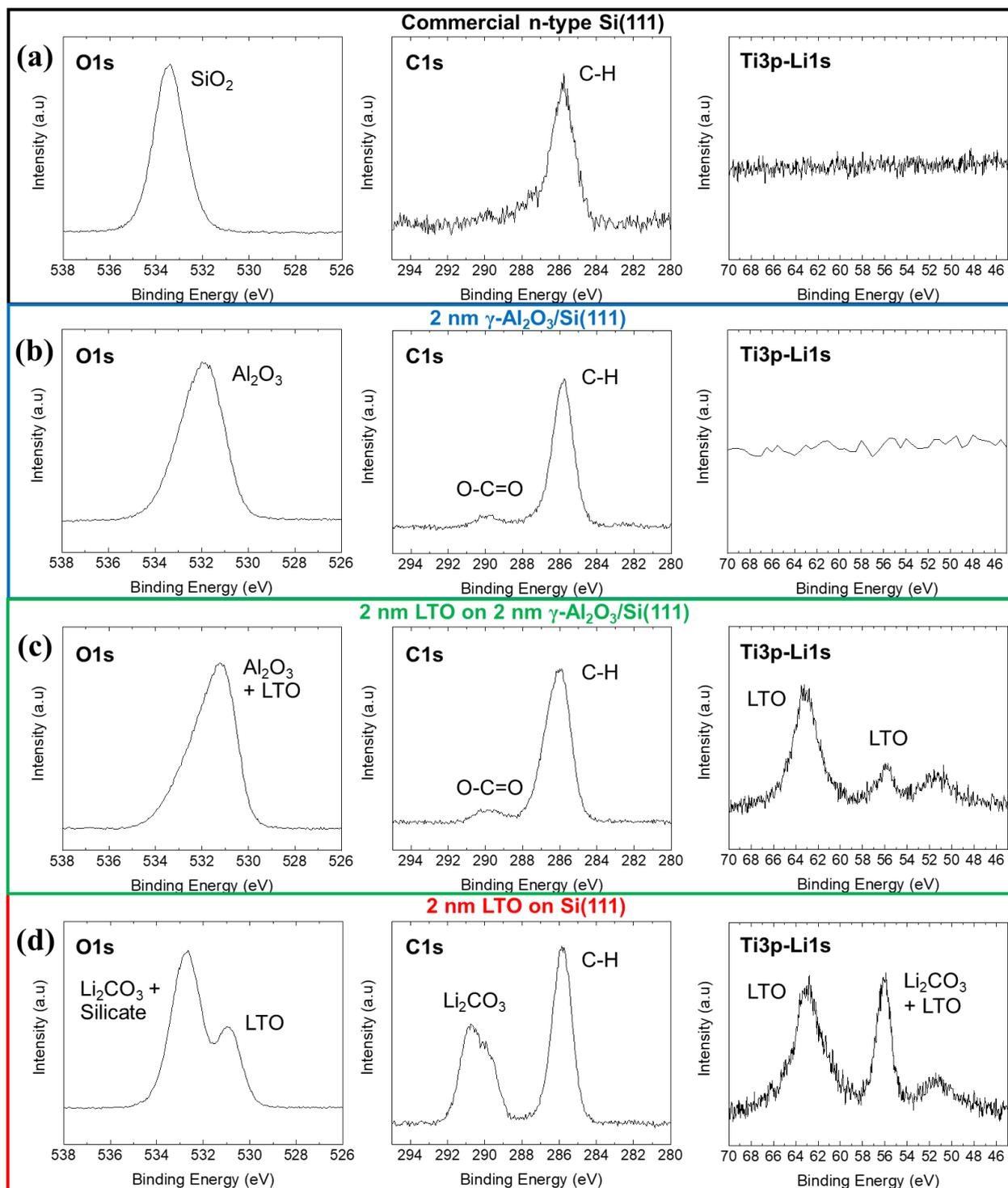


Figure S2. XPS O1s, C1s, and Ti3p-Li1s core levels acquired on: (a) the as-received As-doped Si(111) substrate; (b) 2 nm $\gamma\text{-Al}_2\text{O}_3/\text{Si}(111)$; (c) 2 nm LTO on 2 nm $\gamma\text{-Al}_2\text{O}_3/\text{Si}(111)$ and (d) 2 nm LTO on Si(111). Without an Al_2O_3 buffer layer, there is a significant amount of undesirable species (Li_2CO_3 , silicates) formed during the PLD-grown LTO directly on silicon.

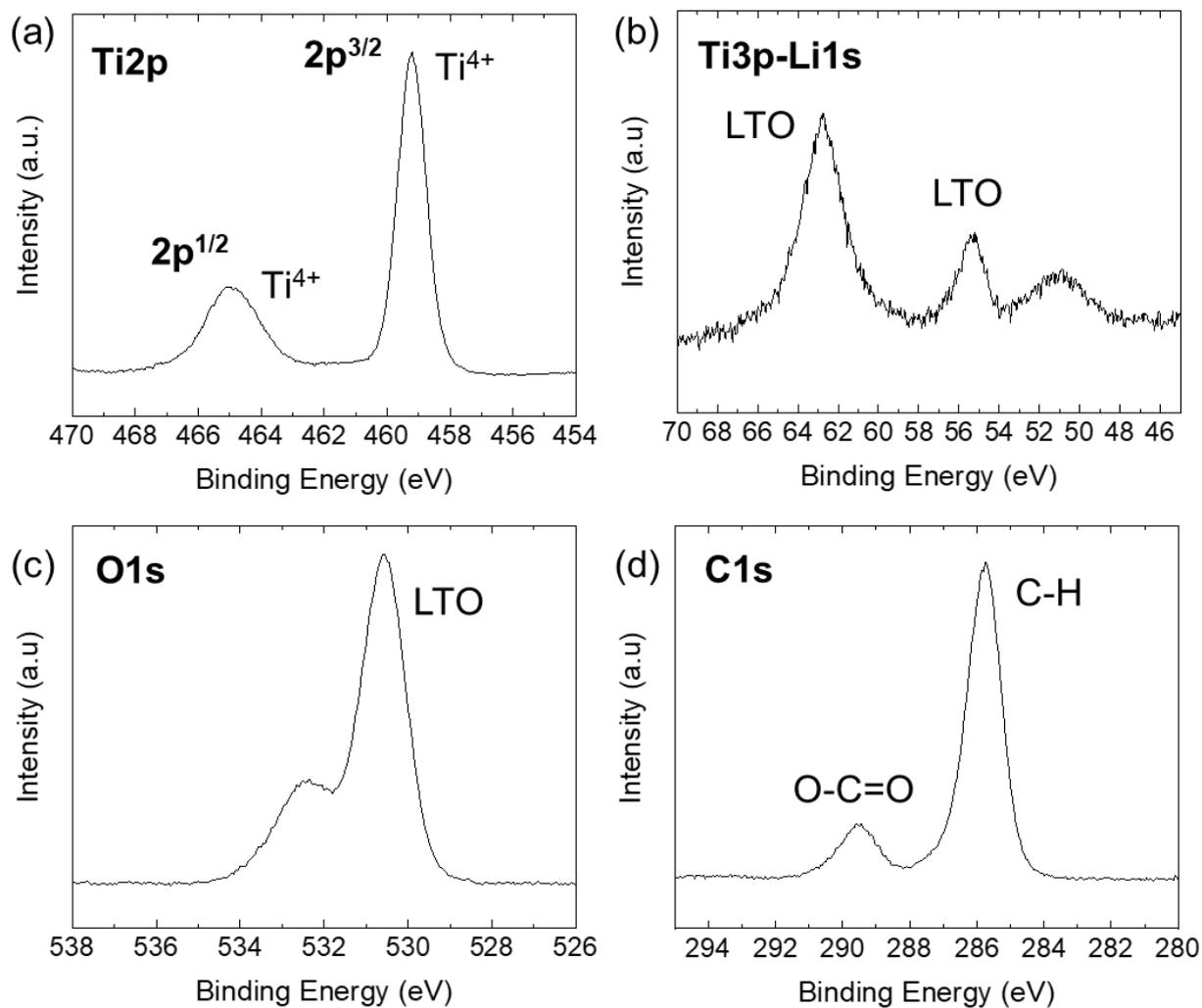


Figure S3. XPS (a) Ti2p, (b) Ti3p-Li1s, (c) O1s and (d) C1s core levels acquired on 90 nm LTO/2 nm γ -Al₂O₃/Si(111) stack.

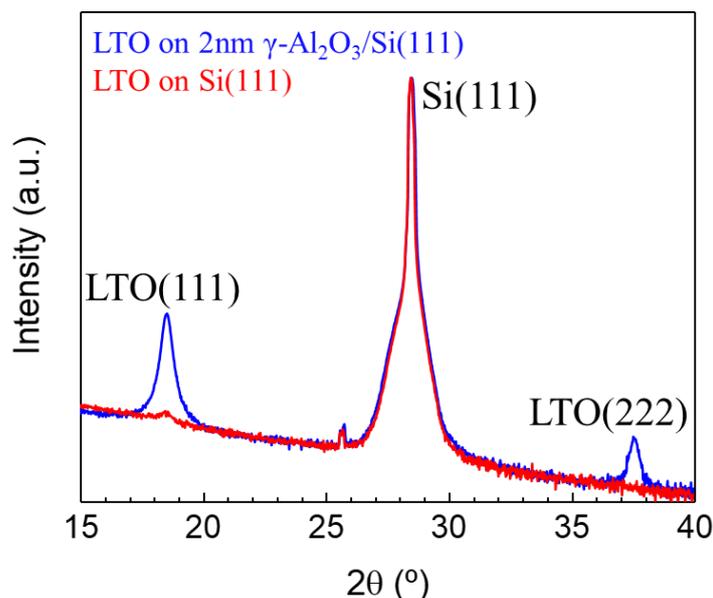


Figure S4. Out-of-plane XRD scan on 90 nm LTO films grown on bare Si(111) and on 2 nm γ -Al₂O₃/Si(111) substrates in red and blue, respectively. LTO is (111)-oriented, matching the underlying γ -Al₂O₃(111) and Si(111) substrate. However, the crystal quality improves greatly with the addition of the 2 nm γ -Al₂O₃ buffer layer. The small peak between 25-26° is a spurious contribution (i.e. an artifact) likely arising from removal of the Bruker's monochromator.

Table S1. Calculated lattice mismatches between LTO/ γ -Al₂O₃/Si(111) stack components.

Thin Film Stack	Lattice mismatch "cube-on-cube"	Lattice mismatch "2-for-3 U.C."
γ -Al ₂ O ₃ /Si(111)	45,2 %	-3,2 %
Li ₄ Ti ₅ O ₁₂ /Si(111)	54 %	2,6 %
Li ₄ Ti ₅ O ₁₂ / γ -Al ₂ O ₃ /Si(111)	6 %	/

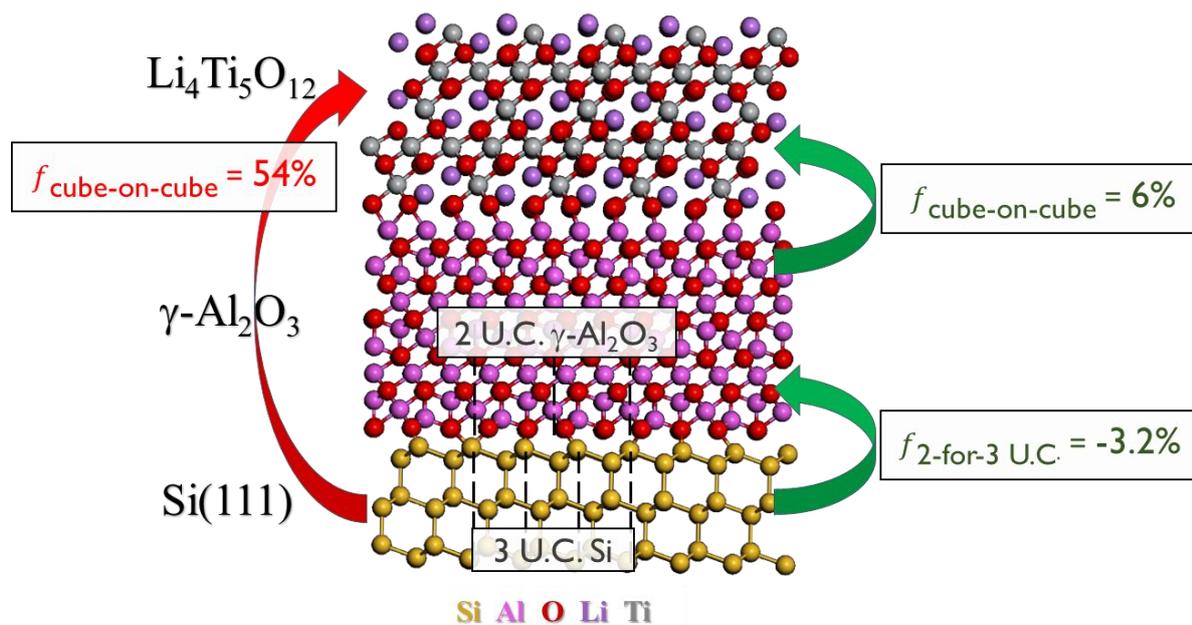


Figure S5. Schematic of the LTO/ $\gamma\text{-Al}_2\text{O}_3$ /Si(111) stack with calculated lattice mismatches.

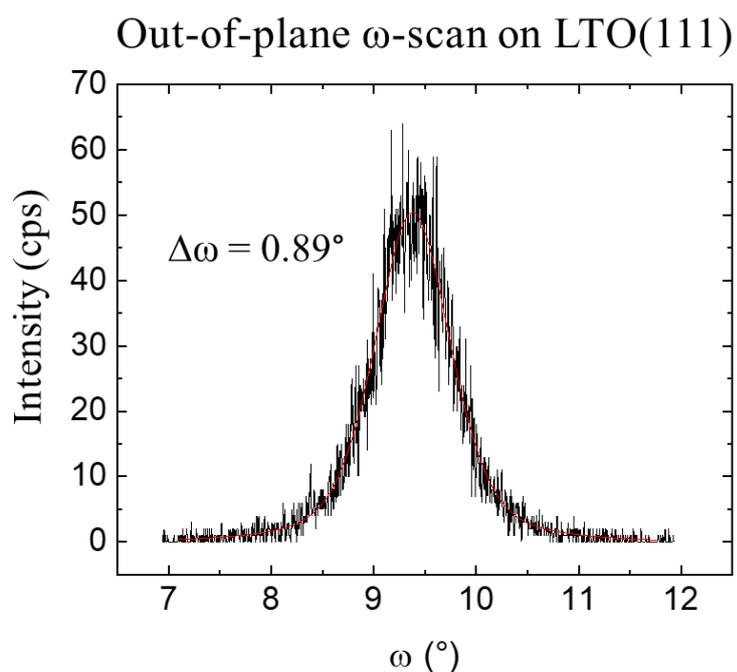


Figure S6. Out-of-plane XRD analysis to determine the mosaicity of the LTO/2 nm $\gamma\text{-Al}_2\text{O}_3$ /Si(111) stack.

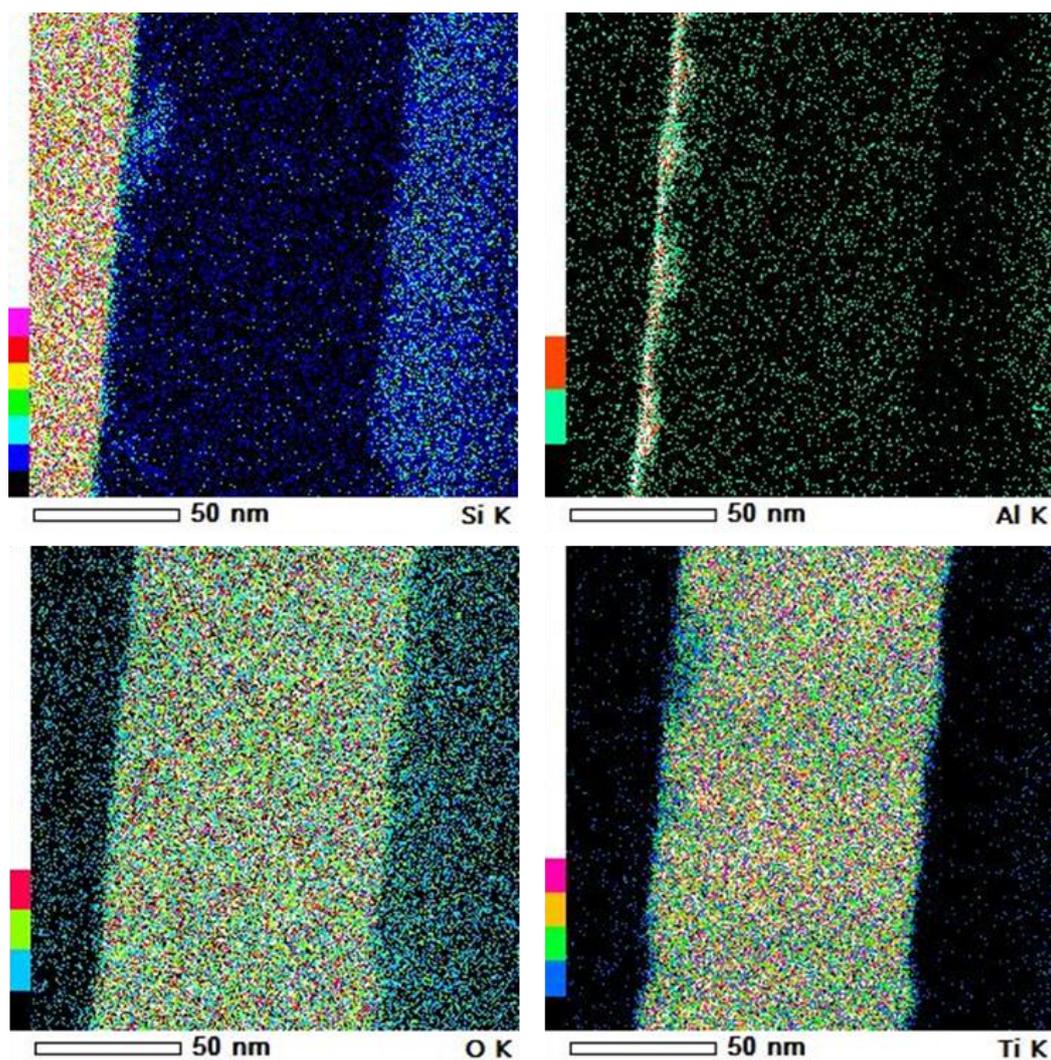


Figure S7. Individual EDX maps (Si, Al, O, Ti) performed on the 90 nm LTO/2 nm γ -Al₂O₃/Si(111) stack after long-term cycling (1,000 cycles at 3C). A distinct stripe of Al separates the Si(111) substrate from the PLD-grown LTO film.

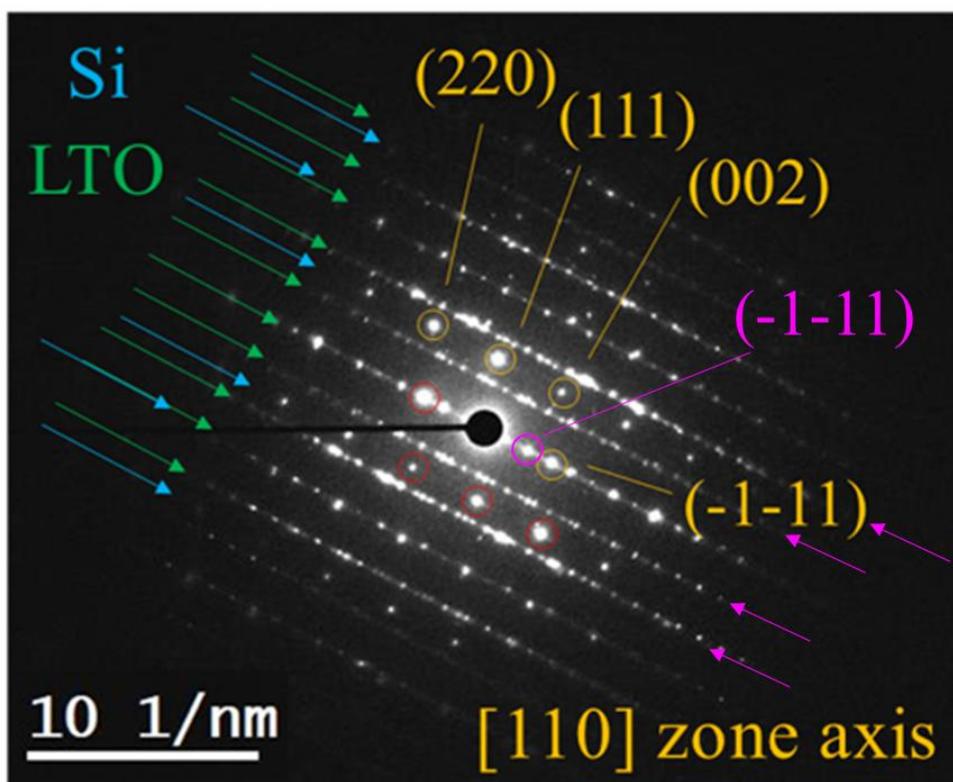


Figure S8. Electron diffraction pattern of the 90 nm LTO/2 nm γ -Al₂O₃/Si(111) stack, where the additional spots correspond to the two grain orientations of the LTO film along the [111]. Note that the majority of LTO(111) is oriented parallel to Si(111). Si reflections are indexed in yellow while pink arrows are complicated overlap LTO reflections due to stacking faults. Note that the (-1-11) spot of LTO (pink) nicely aligns with the Si(-1-11).

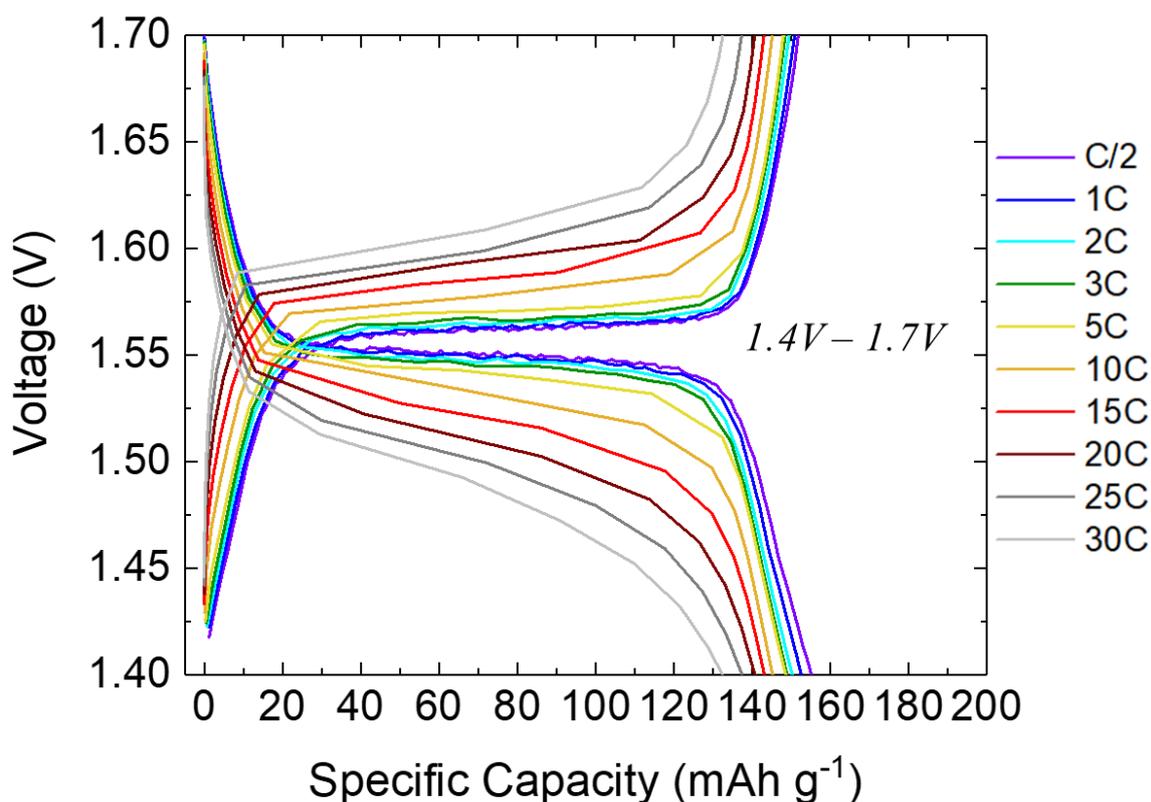


Figure S9. Polarization curves (C/2 to 30C) for the 90 nm LTO/2 nm γ -Al₂O₃/Si(111) stack operating within a small voltage window (1.4 V to 1.7 V vs Li⁺/Li). Upon higher C-rates such as 10C and above, significant overpotentials can be observed, which limits the achievable capacity due to shallow cutoff voltages.

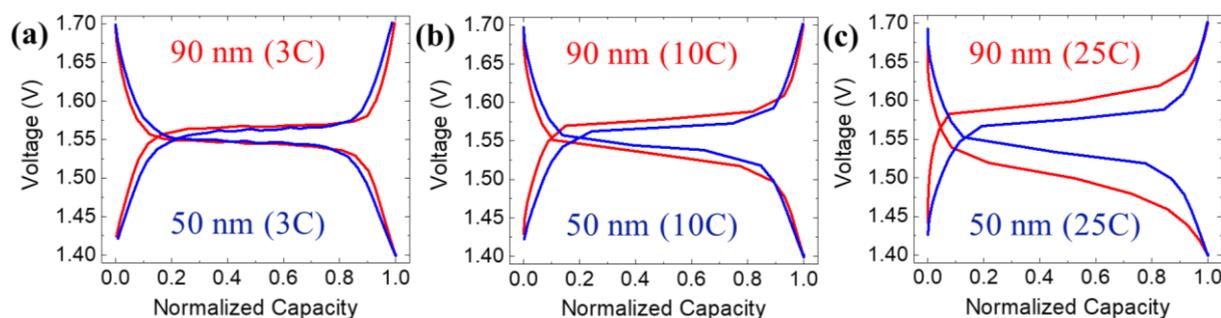


Figure S10. Normalized voltage profile comparison between thick (90 nm) and thin (50 nm) LTO/2 nm γ -Al₂O₃/Si(111) stacks cycled within 1.4-1.7 V vs. Li⁺/Li at different C-rates: (a) 3C, (b) 10C, and (c) 25C. The thinner (50 nm) LTO film showcases lower overpotentials, especially at rates from 10C and beyond.