Asymmetric DC-DC Converter for HVDC Heterogeneous Interconnections

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***Abstract*—Dc-dc converters are an important element for the future development of high voltage direct current (HVDC) grids. This paper presents a new dc-dc converter for the interconnection between different grid topologies. In particular, one elementary converter can interconnect an asymmetric monopole with a symmetric monopole. The use of two elementary converters allows the interconnection between a bipole and a symmetric monopole keeping the inherent redundancy of the bipole in case of a fault on that line. The converter is analyzed and sized for a proposed a case study. The converter is simulated in a Simulink-Matlab environment. The results prove the adequate performance of the control strategy during the power exchanges between the lines. A fault on the bipole is simulated showing the uninterrupted power transfer between the healthy pole and the symmetric monopole line bipole redundancy).**

***Index Terms*—Dc-dc converter, HVDC, modular, line topologies, non-isolated converter.**

I. Introduction

HIGH voltage direct current (HVDC) transmission lines are being currently used for different applications such as point-to-point interconnections, remote offshore applications and multi-terminal schemes [1]–[5]. In the future, the development of HVDC grids is expected [6], [7] based on the ac-dc and dc-dc converters [8], [9].

Multiple dc-dc converters for HVDC applications have been proposed in the literature and categorized in [10]–[12]. The dc-dc converters can improve the multi-terminal or HVDC grids by adding auxiliary services such as power control, voltage control, fault blocking capability, and system reconfiguration. The fault blocking capability (FBC) is the capacity to stop the fault currents, normally achieved with full-bridge sub-modules (FBSMs) or dc circuit breakers (DCCBs). A converter with FBC can enhance the so-called firewall capacity (protecting the healthy zones from an external fault event).

The dc-dc converters are usually compared to the ac transformer as they can interconnect systems with different voltages. However, dc-dc converters can be also used to interconnect systems with different technologies or different line topologies (grounding scheme). In a step-wise development of a dc system, the dc-dc converters can be used to interconnect the already installed lines into multi-terminal or meshed grids with different voltage levels or grounding schemes. Based on the already installed HVDC projects, four line topologies are identified: the asymmetric monopole (AM), the symmetric monopole (SyM), the rigid bipole (RB), and the bipole (B) [13], [14].

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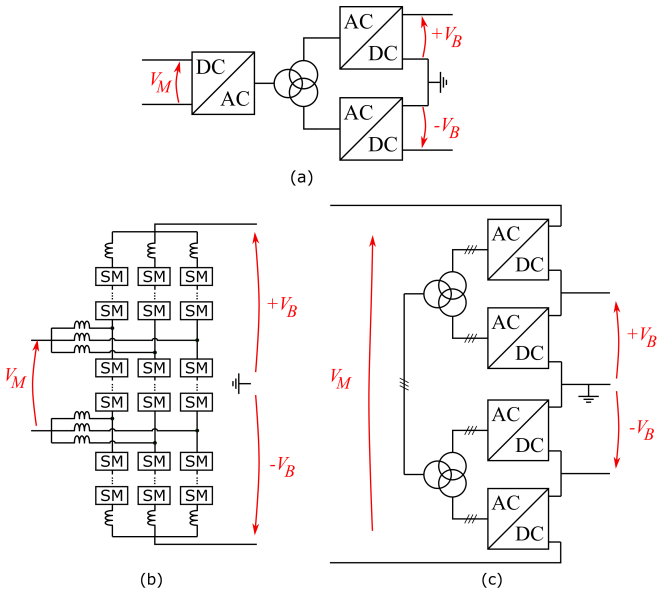

Fig. 1. Converters proposed for the interconnection between a SyM and a B line. (a) F2F. (b) Flexible dc-MMC. (c) Auto-transformer.

The main characteristic of the bipolar lines (either RB or B) is their natural redundancy after a fault in one pole. The RB provides interrupted redundancy, i.e. the line stops the power transfer to isolate the faulted section then, the system is restored with the healthy pole. On the other hand, B lines have immediate redundancy, i.e. after a fault on one pole, the healthy one continues uninterruptedly. Interconnecting a bipole with another line topology should not jeopardize its natural redundancy. The dc-dc converters interconnecting bipoles should allow the reconfiguration (for the RB lines) or immediate redundancy (for the B lines) after a fault in a pole.

Some publications have presented dc-dc converters for HVDC interconnections between different line topologies, specially the interconnection between B or RB and a SyM line [14]–[18] because these are more widely used topologies. The converter topology proposed in [15] is a front-to-front modular multi-level converter (F2F-MMC) with an arrangement of transformers to interconnect a SyM with a B, as presented in Fig. 1a. The F2F structure requires an intermediary ac stage with a full rated ac transformer to adapt the voltage difference. The ac transformer is a voluminous element that could increase the total cost of the dc-dc converter. To

reduce the volume of the ac transformer an arrangement of auto-transformers (AT) is proposed in [16], see Fig. 1c. The AT has a partial power transfer through the ac side reducing the power rating of the converters and transformers [16], [19]–[21]. However, the ac transformer represent anyway a considerable portion of the total volume and cost of the dc-dc converter solution. To eliminate the need of the ac transformer, different configurations of a non-isolated converter are presented in [17]. Nevertheless, the converter requires series connection of switches to withstand the typical voltages in HVDC applications, reducing the industrial interest in this solution. To avoid the use of transformers while reducing the semiconductor requirements, the dc-MMC has been proposed for the B-SyM interconnection [22]–[24]. However, the fault and post-fault has not been studied in those publications. The analysis and operation of a dc-MMC-based structure [9], [11], [22], [23], [25]–[29] after a fault on the B side has been explored by the authors in [14], [18]. The converter is called flexible dc-MMC and it allows the interconnection between dc systems with a single converter, as sketched in Fig. 1b. The converter does not use transformers and its modularity eliminate the need of series connection of switches.

The first two solutions, F2F and AT, provide immediate redundancy while the dc-MMC and flexible dc-MMC require the power flow interruption to reconfigure (suitable for RB lines). The redundancy of the non-isolated converter presented in [17] is unclear and has not been studied.

To the knowledge of the authors, there are no studies for non-isolated HVDC dc-dc converters interconnecting a B with a SyM allowing immediate redundancy. The lack of studies and proposals in the literature, for this interconnection and service, is the main motivation of this paper. The original contribution of this paper is the study of a new modular, non-isolated converter that does not stops the power exchange between the healthy pole of the B and the SyM during and after a fault on the B line. The three-leg version of the new converter is presented in Fig. 2a. It can be noticed that the input and output terminals are not symmetrically distributed, the reason why this converter is called an asymmetric dc-dc converter or ADCC. Different from the modular, non-isolated converters found in the state of the art, the ADCC is designed for the interconnection between AM and SyM (see Fig. 2). Using two ADDCs, one per pole on the B side (see Fig. 3), the B-SyM interconnection can be achieved. In case of a fault in one of the poles of the B, the faulted pole is isolated by the ADCC connected to that pole. The B redundancy is respected with the ADCC connected to the healthy pole.

The new ADCC is analyzed and introduced in Section II. A control strategy is proposed in Section III. The ADCC is implemented in a simulation model including cables and ad-dc converters. The simulation hypotheses and results are presented in Section IV. The conclusions and perspectives are presented in Section V.

II. Asymmetric dc-dc Converter

The ADCC has N_{legs} legs composed of three arms (upper, middle, and lower). If $N_{legs} = 1$, additional filters are needed

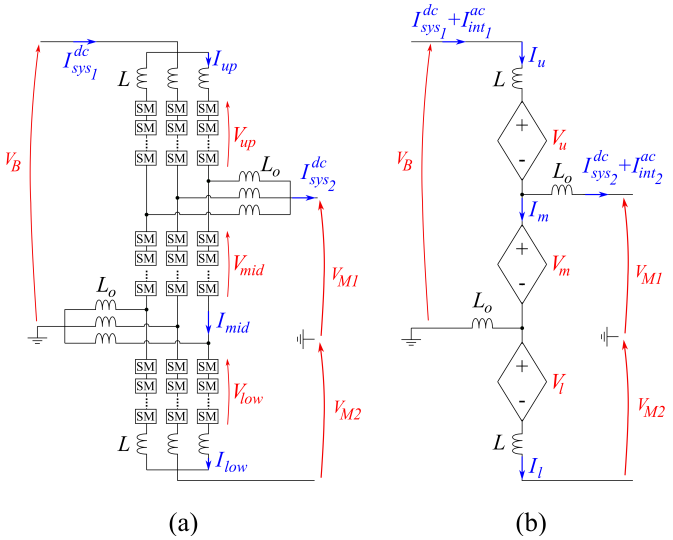

Fig. 2. Asymmetric dc-dc converter. (a) Three leg diagram. (b) Simplified single leg diagram.

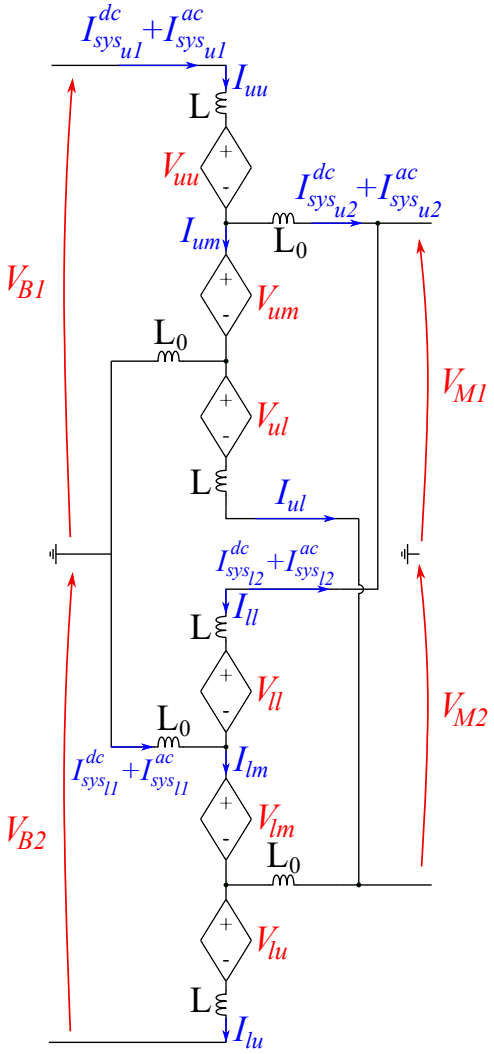

Fig. 3. Simplified, single leg diagram of two asymmetric dc-dc converters interconnecting a bipole (left side) with a SyM (right side).

$$-V_B + V_u + L\frac{d}{dt}I_u + R\,I_u + L_o\frac{d}{dt}\left(I_u - I_m\right) + R_o\left(I_u - I_m\right) + V_{M1} = 0 \tag{1}$$

$$-L_o\frac{d}{dt}\left(I_m - I_l\right) - R_o\left(I_m - I_l\right) + V_l + L\frac{d}{dt}I_l + R\,I_l - V_{M2} = 0 \tag{2}$$

$$V_m + V_l + L\frac{d}{dt}I_l + R\,I_l - V_{M1} - V_{M2} - L_o\frac{d}{dt}\left(I_u - I_m\right) - R_o\left(I_u - I_m\right) = 0 \tag{3}$$

$$\begin{bmatrix} L+L_o & -L_o & 0 \\ 0 & -L_o & L+L_o \\ -L_o & L_o & L \end{bmatrix}\begin{bmatrix} \dot{I}_u \\ \dot{I}_m \\ \dot{I}_l \end{bmatrix} = \begin{bmatrix} -\left(R+R_o\right) & R_o & 0 \\ 0 & R_o & -\left(R+R_o\right) \\ R_o & -R_o & -R \end{bmatrix}\begin{bmatrix} I_u \\ I_m \\ I_l \end{bmatrix} + \begin{bmatrix} -1 & 0 & 0 \\ 0 & 0 & -1 \\ 0 & -1 & -1 \end{bmatrix}\begin{bmatrix} V_u \\ V_m \\ V_l \end{bmatrix} + \begin{bmatrix} 1 & -1 & 0 \\ 0 & 0 & -1 \\ 0 & 1 & 1 \end{bmatrix}\begin{bmatrix} V_B \\ V_{M1} \\ V_{M2} \end{bmatrix} \tag{4}$$

to avoid ac components on the dc systems. For $N_{legs} > 1$ the ac components of currents are phase-shifted to have an internal balanced ac system avoiding currents on the dc side, i.e. $\sum_i^{N_{legs}} I_{leg_i} = 0$. Each arm is a series connection of SM and, for the upper and lower arm, an arm inductor (L). The SMs can be half bridge (HB) or full bridge (FB) depending on the system requirements (especially the need for fault blocking capability, see Section II-D). The three arms are connected sequentially. The ADCC exchanges dc power between the interconnected HVDC lines without an intermediary ac stage. However, this power exchange unbalances the energies in the arms, i.e. changing or discharging the capacitors in the SMs. To keep the converter balanced, an internal ac circulating power is generated to exchange power between the arms and legs, similar to the approaches used for the dc-MMC [22], [28], [30]. Thus, superposed to the dc voltages, the arm generates an ac component. Between the middle and external arms (upper and lower), two passive filters (L_o) connect the converter to the input (V_B) and output ($V_{M1,2}$) dc sides. These passive filters are used to exchange power between the converter legs avoiding ac components on the dc systems. The three-leg ADCC is presented in Fig. 2a and a simplified, single-leg diagram is presented in Fig. 2b.

Fig. 3 shows the single leg connection B-SyM. The ADCCs are connected in series on the bipole side (on the left), while a parallel connection is used on the SyM side (on the right). The ADCC connected to V_{B_1} is equal to the one presented in Fig. 2b, whilst the ADCC connected to V_{B_2} needs to inverse the polarity of the SMs to withstand the reversed voltage. Assuming that the poles on the SyM are balanced, the converter connected to the negative pole follows the same sizing, control strategy, and references calculated for the positive ADCC. Therefore, only the positive ADCC is studied in this paper. However, the results can be extended directly to the negative ADCC.

A. Mathematical Model

To analyze the ADCC, the following hypotheses have been used:

1) The converter has N_{legs} balanced legs.
2) The harmonic distortion is neglected due to a large number of installed SMs on each of the arms.
3) A balancing control algorithm keeps the average voltage in the SM capacitors unchanged.
4) Only the first harmonic is considered.
5) Independent voltage sources are considered for each of the pole in the SyM (V_{M1} and V_{M2}). These voltages are balanced in steady stated operation, i.e., $V_{M1} = V_{M2}$.
6) The converter losses are neglected for the mathematical analysys, i.e. $P_{in} = P_{out}$. Nevertheless resistances are considered for dynamic models and control design.

Based in the model presented in Fig. 2b, the circuit equations (1)-(3) are found. Where L and R are the arm inductance and resistance. L_o and R_o are the inductance and resistance of the passive filters. The subscripts u, m, l represent the upper, middle, and lower variables respectively. The equations are organized in the matrix from in (4) which is the mathematical model describing the ADCC.

B. Steady State Analysis

As mentioned before, the ADCC has ac and dc currents. The arm voltage and currents can be generalized as follows:

$$V_i = V_i^{dc} + V_i^{ac} \cdot \cos\left(wt + \theta_{Vi}\right) \tag{5}$$

$$I_i = I_i^{dc} + I_i^{ac} \cdot \cos\left(wt + \theta_{Ii}\right) \tag{6}$$

where $i \in u, m, l$.

The dc components of (5) and (6) can be expressed in terms of the interconnected dc systems, the transmitted power (P_{dc}), and the number of legs (N_{legs}) as follows.

$$V_u^{dc} = V_B - V_{M1} \tag{7}$$

$$V_m^{dc} = V_{M1} \tag{8}$$

$$V_l^{dc} = V_{M2} \tag{9}$$

$$I_u^{dc} \approx \frac{I_{sys_1}}{N_{legs}} \approx \frac{1}{V_B}\frac{P_{dc}}{N_{legs}} \tag{10}$$

$$I_m^{dc} \approx \frac{I_{sys_1} - I_{sys_2}}{N_{legs}} \approx \left(\frac{1}{V_B} - \frac{1}{V_{M1}+V_{M2}}\right)\frac{P_{dc}}{N_{legs}} \tag{11}$$

$$I_l^{dc} \approx -I_{sys_2} \approx -\frac{1}{V_{M1}+V_{M2}}\frac{P_{dc}}{N_{legs}} \tag{12}$$

The energy equilibrium is achieved if the total power exchanged by each arm is zero (i.e., $P_i^{ac} + P_i^{dc} = 0$). From the

estimated dc values presented in (7)-(12), the active ac power per arm can be obtained.

$$P_u^{ac} = -P_u^{dc} \approx -\frac{V_B - V_{M1}}{V_B}\frac{P_{dc}}{N_{legs}} \tag{13}$$

$$P_m^{ac} = -P_m^{dc} \approx -\left(\frac{V_{M1}}{V_B} - \frac{V_{M1}}{V_{M1}+V_{M2}}\right)\frac{P_{dc}}{N_{legs}} \tag{14}$$

$$P_l^{ac} = -P_l^{dc} \approx \frac{V_{M2}}{V_{M1}+V_{M2}}\frac{P_{dc}}{N_{legs}} \tag{15}$$

As the losses in the converter are neglected at this stage, the sum of the arm dc powers is zero ($P_u^{dc} + P_m^{dc} + P_l^{dc} = 0$). The converter energy balance, in steady-state, can be achieved using an ac circulating power.

C. Internal ac steady-state

As discussed above, dc references can be established from the dc voltages of the interconnected systems, the transmitted power, and the number of legs. Based on the dc power, the active ac power can be found as presented in (13)-(15). The ac power depends on the magnitude and phases of the arm voltages and currents, i.e. 12 variables. Mathematically, the ac power is restricted by the circuit equations (1)-(3) and the dc power per arm, i.e. nine restrictions if the circuit equations are separated in their real and imaginary part. As the system described is an underdetermined problem, i.e. more degrees of freedom than equations, an optimization problem is proposed to obtain the ac references numerically. The optimization problem used in this paper aims to reduce the conduction losses of the converter. The optimization is only used to find the ac references and not to improve the converter behaviour.

The objective function is presented in (16), where N_{SM_i} is the number of HBSMs plus twice the number of FBSMs in the arm i ($i \in u, m, l$). N_{SM_i} acts as a weight factor prioritizing the arm with a greater number of SMs. I_i^{RMS} is the calculated RMS current in the arm i. The objective function is proportional to the losses in the arm ($R \cdot {I_{RMS}}^2$) if all arm resistances are equal.

$$\begin{aligned}\min f(x) =& N_{SM_u} \cdot I_u^{RMS^2} + N_{SM_m} \cdot I_m^{RMS^2} \\ &+ N_{SM_l} \cdot I_l^{RMS^2}\end{aligned} \tag{16}$$

The ac currents and voltages are collected in a vector x as follows:

$$x^T = \left[V_u^d, V_u^q, V_m, V_l^d, V_l^q, I_u^d, I_u^q, I_m^d, I_m^q, I_l^d, I_l^q\right] \tag{17}$$

where the real parts of the variables are denoted with the subscript d and the imaginary parts with the subscript q. The middle arm voltage is the reference for all the variables (i.e., $V_m^q = \theta_{Vm} = 0$).

As mentioned above the optimization problem is subject to the circuit equations and the arm power. Additional inequality constraints limit the results to the physical limits of the semiconductors (rated current) and the maximum installed voltage (number of SMs).

$$\begin{aligned} I_i^{RMS} &\leq I_{rated} \\ V_i^{dc} + |V_i^{ac\,peak}| &\leq V_{max}\end{aligned} \tag{18}$$

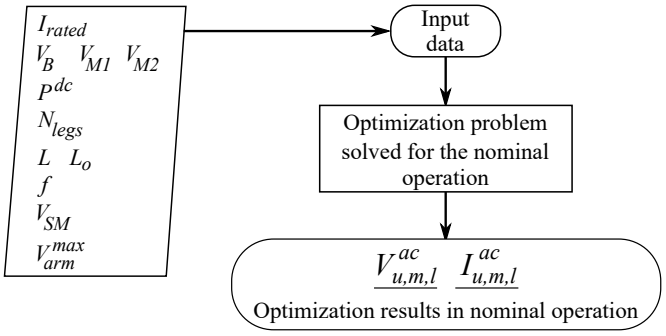

Fig. 4. Simplified flowchart representing the process to calculate the ac steady-state solution of an ADCC.

where I_i^{RMS} can be found as follows:

$$I_i^{RMS} = \sqrt{\left(I_i^d\right)^2 + \left(I_i^q\right)^2}. \tag{19}$$

The current I_{rated} depends on the considered valve, for this study an IGBT 3.3 kV and 1.8 kA is considered. The maximum arm voltage V_{max} must comply with the fault blocking requirements (described in subsection II-D).

The optimization problem is solved computationally using the *fmincon* function in Matlab, as non-linear restrictions are used. The general flowchart is presented in Fig. 4. The optimization is performed offline for the nominal operation. The solution depend on the rated current of semiconductor switches considered; the system dc voltages; the nominal power; the number of legs; the circuit inductances; the operating frequency; the voltage per SM; and the maximum voltage allowed per arm as presented in the inputs of Fig. 4. The ac currents and voltages obtained are used in the control strategy (see Section III). The control adjusts these references depending on the operation point of the converter.

D. Fault requirements

The ADCC is a converter with four terminals, three of which are connected to high voltage poles: V_B, V_{M1}, and V_{M2} (see Fig. 2). These high voltage poles influence the dc arm voltages as presented in (7)-(9). In case of a fault in the left side i.e., $V_B = 0$, the upper arm will need to withstand $-V_{M1}$, which requires FBSMs. In case of a fault in the positive pole of the SyM i.e., $V_{M1} = 0$, the upper arm must sustain $+V_B$. A fault in V_{M2} does not lead to additional requirements as the converter should be sized to withstand V_{M1}. Therefore, the ADCC can achieve fault blocking capability if enough FBSMs are installed in the upper arm, e.g. the FBSMs in the upper arm needs to withstand $-V_{M1}$. The middle and lower arms do not require FBSMs and the faults on both sides of the ADCC can be managed with the HBSMs installed in those arms.

E. Passive components sizing

The main characteristics of the ADCC (number of SMs, the capacitance per SMs, and the arm and output inductors) can be defined based on the dc and ac steady-state analysis.

The number of SMs is calculated using the dc and ac steady-state solutions and the fault requirements. The steady-state conditions can set the minimum voltage required per

arm V_i^{arm}, which is the maximum voltage generated per arm, usually $V_i^{dc} + \left|V_i^{ac\,peak}\right|$. The fault conditions set the voltage requirements in case of dc faults, e.g. FBSMs are required in the upper arm to withstand faults on the V_B side. Then, the number of SMs can be found with the voltage required and the average voltage per SMs:

$$N_{SMs_i} = \left\lceil V_i^{required}/V_{SM} \right\rceil . \tag{20}$$

The capacitance per SM can be sized using the approach proposed in [31]–[33]. The calculation uses the energy variation in the arm and the maximum allowed ripple to calculate the required equivalent capacitance. In this paper 10% of voltage ripple is considered, and the energy variation is calculated using the steady-state arm voltages and currents.

The ADCC has two sets of inductors, the arm inductor (L), and the output filter (L_0). Each set is composed of N_{legs} inductors. The inductors can be sized to limit the maximum current di/dt in case of a fault pole-to-pole [34] with expression (21).

$$L_{eq} \geq \frac{V_{eq}^{dc}}{di/dt} \tag{21}$$

A fault on the AM (or B) side is protected by the upper arm inductors and the set of L_o connected to that dc system. Similarly, the converter is protected from faults on the SyM side by the lower arm inductors and the L_o set connected to the monopole side. In this paper, the middle arm inductor is not considered. However, it can be used to reduce the size of the other inductances (L and L_o).

III. Control Structure

Based on the mathematical model found in (4) a simplified control strategy is proposed. The control has two cascaded stages. A slow energy control and a fast current control. The details are presented in the following subsections.

A. System Diagonalization

It can be evidenced that the currents in (1)-(3) are coupled, i.e. changing the current in one arm disturbs the other two. To simplify the current control, the diagonalization of the mathematical model (4) is proposed. The diagonalization decouples the currents into new independent, equivalent currents. The new currents are a linear combination of the initial variables. The new currents can be controlled with independent equivalent voltages facilitating the control design, i.e. using simple proportional-integral controllers. The change of variables used to diagonalize the model are:

$$\boldsymbol{I_{uml}} = \boldsymbol{P}\,\boldsymbol{I_{123}}; \qquad \boldsymbol{I_{123}} = \boldsymbol{P^{-1}}\,\boldsymbol{I_{uml}} \tag{22}$$

$$\boldsymbol{V_{uml}} = \boldsymbol{T}\,\boldsymbol{V_{123}}; \quad \boldsymbol{V_{123}} = \boldsymbol{T^{-1}}\,\boldsymbol{V_{uml}} \tag{23}$$

where uml refers to the currents and voltages in the upper, middle, and lower arms, and 123 refers to the new currents and voltages variables after the transformations. The transformation matrices are detailed below:

$$\boldsymbol{P} = \begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \\ -1 & 1 & 0 \end{bmatrix}; \boldsymbol{P^{-1}} = \begin{bmatrix} 1/2 & 0 & -1/2 \\ 1/2 & 0 & 1/2 \\ -1/2 & 1 & -1/2 \end{bmatrix} \tag{24}$$

$$\boldsymbol{T} = \begin{bmatrix} -1 & -1 & 1 \\ 0 & 0 & -2 \\ 1 & -1 & 1 \end{bmatrix}; \boldsymbol{T^{-1}} = \begin{bmatrix} -\frac{1}{2} & 0 & \frac{1}{2} \\ -\frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{1}{2} & 0 \end{bmatrix} \tag{25}$$

The diagonalized system is presented in (26). Similar to the uml variables, the new variables I_{123} and V_{132} have ac and dc components. It can be evidenced that each of the currents depends only on themselves, one voltage equivalent voltage (V_1, V_2 or V_3), and the dc voltages of the interconnected systems.

The new currents can be represented in three equivalent circuits, presented in Fig. 5. The circuits represent each of the lines of the diagonilized model (26). The ac currents are contained inside the converter and do not interact with the dc system, i.e. balanced system (first hypothesis of the mathematical model).

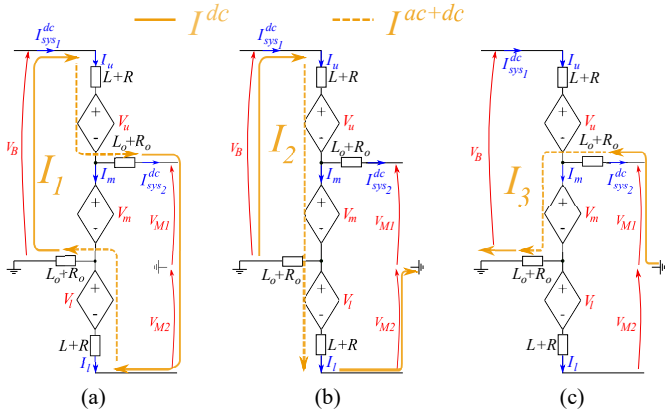

Fig. 5. Equivalent circuits of the decoupled currents. (a) I_1. (b) I_2. (c) I_3. The ac balanced currents circulate inside the converter only.

B. Energy controllers

The energy controllers are designed to keep the energy balanced throughout the operation of the converter. These controllers have a constant input reference. The output is the

$$\begin{bmatrix} \dot{I}_1 \\ \dot{I}_2 \\ \dot{I}_3 \end{bmatrix} = \begin{bmatrix} -\frac{R+R_o}{L+L_o} & 0 & 0 \\ 0 & -\frac{R}{L} & 0 \\ 0 & 0 & -\frac{R_o}{L_o} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} + \frac{1}{2} \begin{bmatrix} \frac{1}{L_o+L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L_o} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \end{bmatrix} + \frac{1}{2} \begin{bmatrix} \frac{1}{L+L_o} & -\frac{1}{L+L_o} & -\frac{1}{L+L_o} \\ \frac{1}{L} & 0 & \frac{1}{L} \\ 0 & \frac{1}{L_o} & 0 \end{bmatrix} \begin{bmatrix} V_B \\ V_{M1} \\ V_{M2} \end{bmatrix} \tag{26}$$

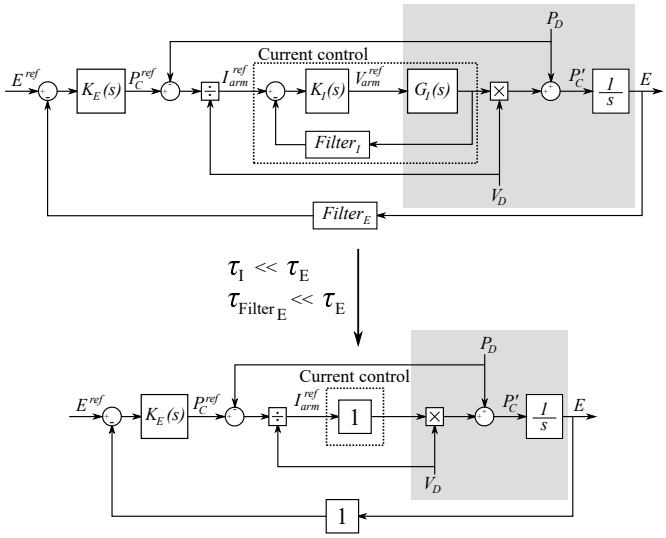

Fig. 6. General scheme of energy and current control (top). Simplified energy control (bottom). The colored blocks are the estimated converter plant. P_D and V_D are power and voltage disturbances due to the change of operating point of the converter.

reference of the internal current control. The control proposed governs the energy per leg, thus it can be extended to n legs.

The energy controllers implemented are proportional-integral (PI) controllers, with the structure presented in (27). Assuming that the converter plant for the energy control is an integrator (as presented at the bottom of Fig. 6, the energy controllers can be tuned to follow a second-order system response in a closed loop as the one presented in (28). The damping factor ζ is set to 0.7. The natural frequency ω_{nW} is presented in (29), where τ_{energy} is chosen to be a factor ($K_W = 7$) of a notch filter time constant, as presented in (30). The factor K_W is selected to neglect the impact of the notch filter on the energy control design. Thus, K_W should have a value of at least 5.

$$K_E(s) = K_p + \frac{K_i}{s} \tag{27}$$

$$G_{CL}(s) = \frac{1}{s^2 + 2 \cdot \zeta \cdot \omega_{nW} + \omega_{nW}^2} \tag{28}$$

$$\omega_{nW} = \frac{1}{\tau_{energy}} \tag{29}$$

$$\tau_{energy} = K_W \cdot \tau_{Notch} \; ; \quad \tau_{Notch} = \frac{Q}{\omega_n} \tag{30}$$

The notch filter is implemented to damp the first and second harmonics in the energy measurements. The notch structure is presented below.

$$N(s) = \frac{s^2 + \omega_n^2}{s^2 + 2\omega_n s/Q + \omega_n^2} \cdot \frac{s^2 + 4\omega_n^2}{s^2 + 4\omega_n s/Q + 4\omega_n^2} \tag{31}$$

where ω_n is the operation frequency of the converter and Q is the quality factor, set to 3 [28], [35].

C. Current References

As presented in Fig. 6, the current references are given by the energy controllers. These references are in the 123 frame to take advantage of the diagonalized model. Similar to the energy controllers, the current control is designed per leg, therefore the control strategy can be expanded to n balanced legs. The arm energies can be coupled by the arm currents either in uml or 123 frame. To have a simplified control strategy three energy controllers are proposed, the total energy (W_Σ), the total difference ($W_{\Delta T}$), and the difference between the upper and lower arms (W_{u-l}), which are a linear combination of the arm energies.

1) Total energy (W_Σ): the total energy is the sum of the energy in the three arms:

$$W_\Sigma = W_u + W_m + W_l \tag{32}$$

The dynamics of the energy can be expressed as the power in each arm:

$$\dot{E}_\Sigma = P_u + P_m + P_l \tag{33}$$

Equation (33) can be expressed in terms of the new variables 123, as follows:

$$\dot{E}_\Sigma = -2\left(V_1 I_1 + V_2 I_2 + V_3 I_3\right) \tag{34}$$

The energy controller follows and acts over the average value of the energy. Expression (34) needs to be expressed in its equivalent average value. The average value of a product between two variables, both composed of an ac (only first harmonic) and a dc part can be found with the following expression:

$$\overline{V_j \cdot I_k} = |V_j^{ac}||I_k^{ac}|\frac{cos(\theta_{Vj} - \theta_{Ik})}{2} + V_j^{dc} I_k^{dc} \tag{35}$$

where V_j is a voltage and I_k is a current, for $j, k \in 1, 2, 3$.

From the diagonalized system presented in (26) and assuming that the resistance is negligible with respect to the inductance impedance, the system can be simplified to inductive circuits. Using (35) is noticeable that the product between voltage and currents with $j = k$ have near zero values (inductive current in quadrature to the voltage).

Following the previous analysis, the expression (34) has only dc components, as the voltages, V_j and currents I_k are in quadrature when $j = k$. Therefore this energy cannot be controlled with an ac component. From Fig. 5, it is observed that the only current that affects all three arms is I_2^{dc}. The expression relating the total energy dynamic and I_2^{dc} is:

$$I_2^{dc} = \frac{\dot{E}_\Sigma + 2V_1^{dc} I_1^{dc} + 2V_3^{dc} I_3^{dc}}{-2V_2^{dc}}$$

replacing the variables to depend on the system voltages and transmitted power using (7)-(9), (24), and (25), e.g. $V_2^{dc} = -0.5(Vu + Vm + Vl) = -0.5(V_B + V_{M2})$:

$$I_2^{dc\,ref} = \frac{P_{E_\Sigma}^{ref} + \overbrace{\frac{V_{M2}^2 + V_{M1}V_{M2} + V_B V_{M1} - V_B^2}{V_B\left(V_{M1} + V_{M2}\right)}\frac{P_{dc}}{2\,N_{legs}}}^{P_{FF}^{dc}}}{V_B + V_{M2}} \tag{36}$$

where $P_{E_\Sigma}^{ref}$ is the output of the total energy controller (see fig. 6).

2) Total energy difference ($W_{\Delta T}$): this energy is the difference between the three energies:

$$\dot{E}_{\Delta T} = P_u - P_m + P_l \tag{37}$$

$$\dot{E}_{\Delta T} = 2\left(-V_1 I_2 - V_2 I_2 + 2V_3 I_2 + V_3 I_3\right) \tag{38}$$

Similar to the total energy, the dynamic of the total difference is expressed in the 123 frame in (38). In this case, the ac component of I_2 is used to control this energy:

$$I_2^{ac\,ref} = \frac{P_{E_{\Delta T}}^{ref} + \overbrace{\frac{V_{M1}V_{M2} + V_{M1}^2 - V_B V_{M1}}{V_B\left(V_{M1}+V_{M2}\right)}\frac{2P_{dc}}{N_{legs}}}^{P_{FF_{\Delta T}}^{dc}}}{\underbrace{2V_3^{ac}\cos\left(\theta_{V_3} - \theta_{I_2}\right)}_{V_{D_{\Delta T}}}} \tag{39}$$

where $P_{E_{\Delta T}}^{ref}$ is the output of the total difference energy controller (see fig. 6). θ_{V3} and θ_{I2} are the phases of the voltage V_3 and the current I_2 respectively.

3) Difference up-low (W_{u-l}): this controller keeps the energy balance between the upper and lower arms. The energy dynamic in 123 frame is presented below:

$$\dot{E}_{u-l} = 2\left(-V_1 I2 - V_2 I_1 + V_3 I_1\right) \tag{40}$$

This energy is controlled with I_1^{ac}, which links the upper and lower arm (see Fig. 5a). Equation (42) presents the I_1^{ac} reference, where P_{Eu-l}^{ref} is the output of the W_{u-l} energy controller, as presented in fig. 6.

D. Power reference

The power reference is used to calculate the dc component of I_1, as follows:

$$I_1^{dc\,ref} = \left(\frac{1}{V_B} + \frac{1}{V_{M1}+V_{M2}}\right)\frac{P_{dc}}{2N_{legs}} \tag{41}$$

For this model, the power is not controlled in a closed loop. To avoid oscillations, a low-pass filter can be used to damp the power response.

E. Pole balancing

From the equivalent currents presented in Fig. 5 it can be evidenced that the current I_3^{dc} can be used to charge/discharge the positive pole of the SyM (V_{M1}). Assuming that the pole-to-pole voltage on the SyM is controlled by the ac-dc converters in the system, the ADCC can be used to balance the poles. The pole balancing controller depends on the equivalent capacitance of the line and is presented in Fig. 9.

The current I_2^{dc} could incude an asymmetric disturbance on the negative pole of the monopole (V_{M2}). To avoid the unbalance, I_3^{dc} can be prepositioned to the dc value of I_2^{ref} reducing the control effort to keep the voltages balanced.

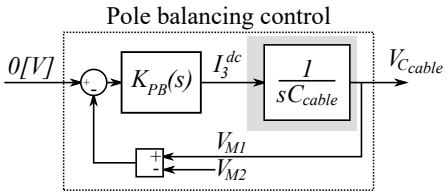

Fig. 9. Closed loop estimation for the pole balancing controller.

F. Current control

As the new equivalent currents ($I_{1,2,3}$) have dc and ac components, a PIR controller is used. Three PIR controllers are designed using the diagonal model found in (26) and the transfer function proposed in [39] (see (43)), where the term ω_r is the resonant frequency set equal to the frequency of ac currents and voltages. K_{PIR} is the controller gain, which depends on the equivalent circuit of each current (I_{123}). It is calculated as presented in (44).

$$G_{PIR}(s) = K_{PIR}\frac{\left(s+\alpha_{PIR}\right)^3}{s\left(s^2+w_r^2\right)} \tag{43}$$

$$K_{PIR} = \frac{\left(\omega_c^2 - \omega_r^2\right)\sqrt{\omega_c^2 L_{eq123}^2 + R_{eq123}^2}}{\omega_c} \tag{44}$$

Where ω_c is the crossover frequency, with the desired phase margin (φ_{PM}) and the time delay T_d as follows:

$$\omega_c = \frac{\pi/2 - \varphi_{PM}}{T_d} \tag{45}$$

and α_{PIR} can be calculated with:

$$\alpha_{PIR} = \frac{\omega_c}{10} \tag{46}$$

The equivalent inductance and resistance, extracted from (26) are:

$$L_{eq1} = L + L_o; \quad R_{eq1} = R + R_o \tag{47}$$

$$L_{eq2} = L; \quad R_{eq2} = R \tag{48}$$

$$L_{eq3} = L_o; \quad R_{eq3} = R_o \tag{49}$$

The complete control strategy implementation is presented in Fig. 7. The optimization results are used to fix the angles of $I_{1,2,3}^{ac}$ and the magnitude of I_3^{ac}. The matrix M_k is a matrix proposed in [40] to assure the balance between legs. The summary of the current components and their use in the control strategy is presented in Table I.

$$I_1^{ac} = \frac{P_{E_{u-l}}^{ref} + \overbrace{\frac{V_{M2}^2 + V_{M1}V_{M2} - V_B V_{M1} + V_B^2}{V_B\left(V_{M1}+V_{M2}\right)}\frac{P_{dc}}{N_{legs}}}^{P_{FF}^{dc}} + \overbrace{|V_1^{ac}||I_2^{ac}|\cos\left(\theta_{V1} - \theta_{I2}\right)}^{P_{FF}^{ac}}}{\underbrace{-|V_2^{ac}|\cos\left(\theta_{V2} - \theta_{I1}\right) + |V_3^{ac}|\cos\left(\theta_{V3} - \theta_{I1}\right)}_{V_{D_{u-l}}}} \tag{42}$$

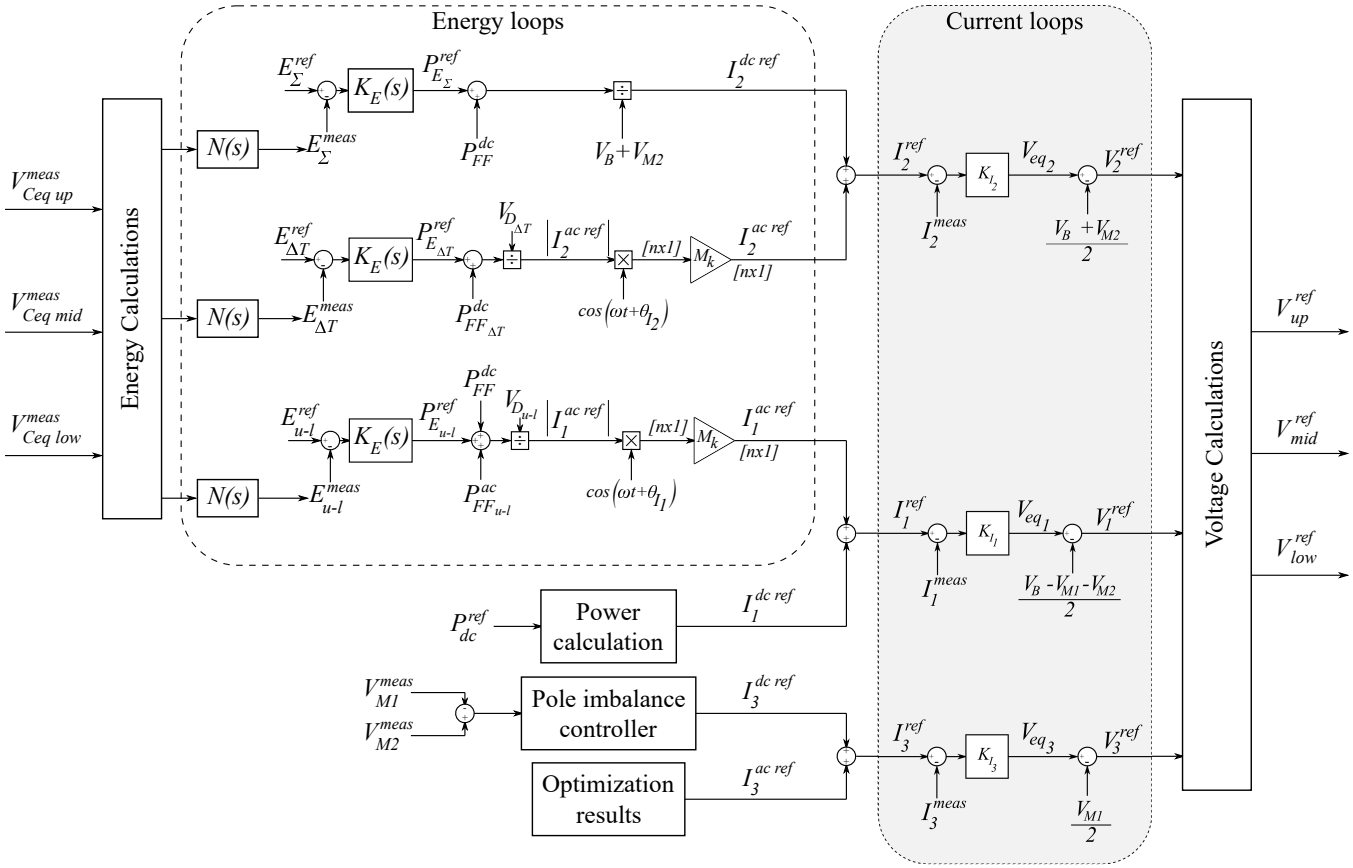

Fig. 7. Control strategy implemented to test the ADCC.

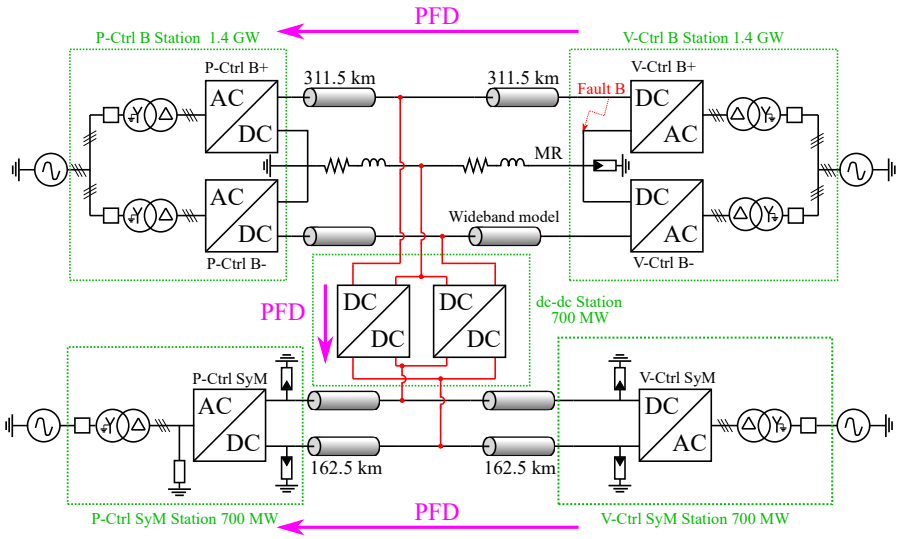

Fig. 8. Simulated system interconnecting a bipole (on the top) and a symmetric monopole (bottom). The magenta lines show the positive convention for the power flow direction (PFD). For this interconnection two ADCCs are used, one per pole. The B line is grounded on the P-Ctrl station, at the V-Ctrl station is floating to avoid ground currents. The SyM is grounded on the ac side with a star point reactor as the one used in [36]–[38].

TABLE I
CURRENTS COMPONENTS AND THEIR USE IN THE CONTROL STRATEGY

Current	Control Use
I_1^{dc}	Dc power
I_1^{ac}	Energy u-l (E_{u-l})
I_2^{dc}	Energy total (E_Σ)
I_2^{ac}	Energy difference total ($E_{\Delta T}$)
I_3^{dc}	Pole balancing
I_3^{ac}	Optimized reference

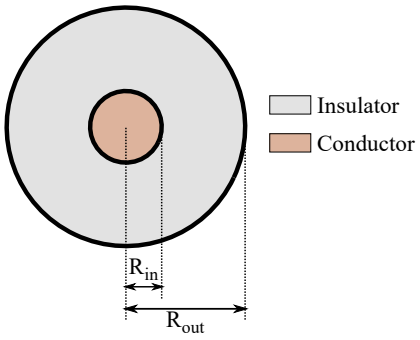

Fig. 10. General geometry used for the ULM from [41].

IV. SIMULATION AND RESULTS

To test the control strategy and ADCC behavior, the system presented in Fig. 8 is implemented in a Matlab/Simulink model. The case study and its details are presented in the following section.

A. Case Study

The dc-dc converter is tested for the interconnection between a B and a SyM. The B line is rated to ± 525 kV, 1400 MW, and a total length of 623 km. The SyM is operating at ± 320 kV, 700 MW, with a total length of 325 km, and an estimated cable equivalent capacitance $C_{cable\,SyM} \approx 21.3\,\mu$F (used in balancing control). The dc-dc converters are connected in the middle of both lines.

The dc cables are modeled with the universal line model (ULM) developed in the Best Paths project [41]. This model uses the geometrical parameters of the cable (radius of the conductor and insulator as shown in Fig. 10) and its layout (e.g. ground resistance, how deep is buried) to calculate the electrical parameters depending on the frequency. This model allows to have a representative dynamic of the cable during transients. Additional information can be found in Table II.

TABLE II
CABLE PARAMETERS

Section	Cable 320kV [42]	Cable 525kV
Length	325 km 2 sections of 162.5 km	623 km 2 sections of 311.5 km
Core (R_{in})	R_{in} = 25.1 mm $\rho = 1.7e^{-8}\ \Omega$ m	R_{in} = 25.95 mm $\rho = 1.7e^{-8}\ \Omega$ m
Insulator (R_{out})	R_{out} = 74 mm $\epsilon_r = 2.5$ $\mu_r = 1$	R_{out} = 73.5 mm $\epsilon_r = 2.5$ $\mu_r = 1$

The ac-dc converters are MMCs implementing the energy-based control presented in [43]. The modular HVDC converters, i.e. the MMCs and ADCCs are modelled using the average arm model including the blocked state for HBSMs [44] and FBSMs [45]. These models allow to simulate the general behaviour during fault transients.

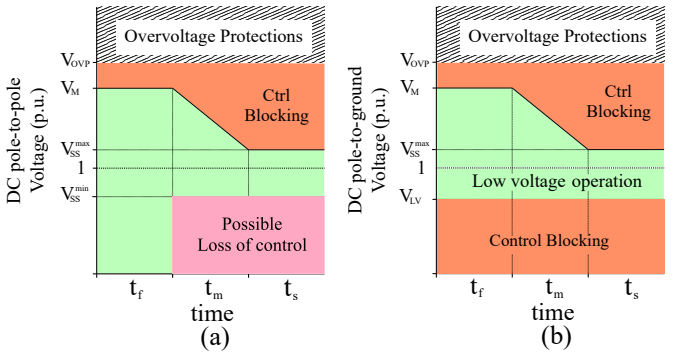

Fig. 11. Proposed operating zones, where $t_f = 1$ms, $t_m = 4$ms, and $t_s = 200$ms. (a) ac-dc converters, with $V_M = 1.2$ p.u., $V_{SS}^{min} = 0.85$ p.u., and $V_{SS}^{max} = 1.05$ p.u. (b) ADCCs, with $V_M = 1.2$ p.u., $V_{LV} = 0.6$ p.u., and $V_{SS}^{max} = 1.05$ p.u.

TABLE III
ADCC PARAMETERS

Arm	N_{HBSMs}	N_{FBSMs}	Rated voltage	$N_{switches}$
Upper	129	200	952.2 kV	1058
Middle	400	0	720 kV	800
Lower	339	0	610.2 kV	678

The ac-dc converters have a fault detection algorithm measuring the arm currents, the ac currents, and the dc voltages at the terminals of the converters. The arm currents are compared to two fault detection thresholds: the overcurrent (set to 3 kA), and the rate of change (set to 6.4 A/µs). The ac currents have an overcurrent threshold set to 5 kA. The acceptable range of operation for the dc voltage is defined by the operation zones presented in Fig. 11a. If any of the thresholds are reached, the ac-dc converter is blocked and the ac circuit breaker is opened.

The dc-dc converter solution is rated to 700 MW, i.e., each ADCC is rated to 350 MW. The ADCCs are designed to operate at 150 Hz.

The output filter has been designed to limit the current di/dt under 6.4 A/µs. The equivalent dc voltage on the B side is $V_B = 525$ kV, and on the SyM side is $V_{M1} + V_{M2} = 640$ kV. In both sides the equivalent inductance is $L + L_0$. Using expression (21), the minimum value for the equivalent inductance is 82 mH and 100 mH for the B and SyM sides respectively. The output filters have been increased to 200 mH to ensure the di/dt requirements while reducing the ac circulating power inside the converter, as suggested in [28]. The arm inductances are sized to keep the control with a minimal value of 15 mH. It should be noticed that sizing the inductors is independent of the operating frequency.

The ac voltage and currents found with the optimization problem are presented in Fig. 12. The values presented in the figure are the nominal voltages and currents. The number of SMs per arm is presented in Table III. The arm rated voltage and current is depend on the switches ratings (here assumed 1.8 kV and 1.8 kA). It can be noticed that the current in the upper arm (red arrow) is smaller than the other two. This is because the optimization problem aims to reduce the current

Fig. 12. Graphical representation of the arm voltages and currents found with the optimization problem for the nominal operation of the ADCC. Red, blue, and green, represent the values of the upper, middle, and lower arm respectively, in kV and kA.

in the arm containing more switches in the conduction path. The upper arm is the only arm composed by FBSMs, which implies twice the number of switches in the conduction path compared to the HBSMs.

The SM capacitance per arm are 1.1 mF, 2.9 mF, and 2.6 mF for the upper, middle and lower arms respectively. As the operating frequency has been set to 150 Hz, the size of ccapacitances can be significantly reduced compared to the 50 Hz applications.

Similar to the ac-dc converters the ADCCs have a fault detection algorithm based on the arm currents and dc voltage measurements. The ADCCs use the same arm current thresholds and the dc voltage operating zone is presented in Fig. 11b.

B. Simulation results

Two simulations are performed to test the converter and proposed control strategy: nominal operation, where the power direction is changed, and fault simulation.

1) Nominal operation: The nominal operation is presented in Fig. 13-15. Fig. 13 presents the power exchanged by ADCC and the total power exchanged between the B and SyM. The ADCCs are set to exchange 350 MW in both directions, following a ramp of 5 p.u/s. It can be noticed that the dc exchanged power has no visible ripple meaning that the ac circulating power is kept inside the ADCCs.

Figure 14 presents the arm voltages of phase A for the nominal operation. It also highlights the dc components of voltages. It can be noticed that the dc and ac values respect the theoretical values found with (7)-(9) and the optimization problem results presented in Fig. 11a. For example $V_u^{dc} = V_B - V_{M1} = 205$ kV. The ac component can be appreciated on the zoom at the rigth of Fig. 14 (blue curve) which presents an oscillating voltage with amplitude around 200 kV. For the complete length of the simulation the arm voltages are controlled and adjusted for the requested power reference. Some transients can be evidenced every time that the power reference change (see Fig. 13). Similar analysis can be done for the arm currents presented in Fig. 15. The currents are controlled during the complete simulation and the currents are adjusted depending on the power reference. The dc and ac components respect the theoretical analysis and can be validated using (10)-(12), and Fig. 11b.

2) Fault simulation: For the fault simulation the power direction has been changed in all three systems: the B line, the dc-dc converter, and the SyM line simulating the fault on the B. The worst case is found when the B line is set to send 900 MW from the P-Ctrl to the V-Ctrl station, the dc-dc converters

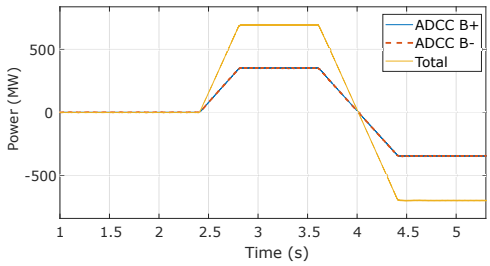

Fig. 13. Power exchange in nominal operation.

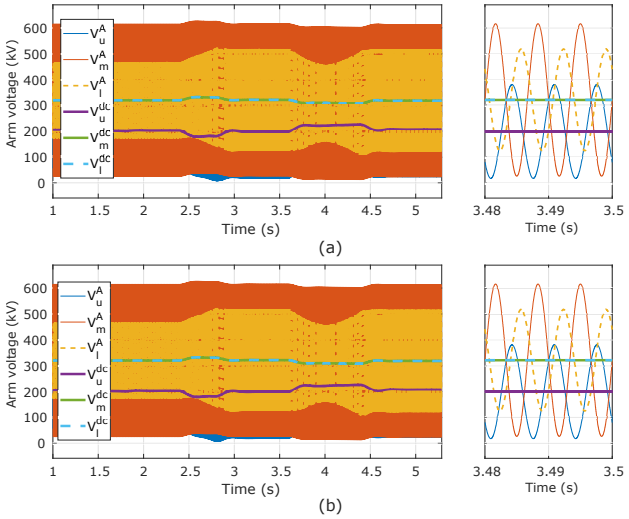

Fig. 14. Arm voltages for nominal operation. (a) connected to the positive pole of the bipole, and (b) connected to the negative pole of the bipole.

are set to send power towards the B line (500 MW), and the SyM is sending 200 MW from the P-Ctrl to the V-Ctrl station. All power directions are in negative convention concerning the directions presented in Fig 8.

The fault simulation is divided into three stages. The first is the normal operation, where the line exchanges dc power through the ADCCs (between 0 and 3.6 s). The second is where a fault pole-to-metallic return is simulated in one of the

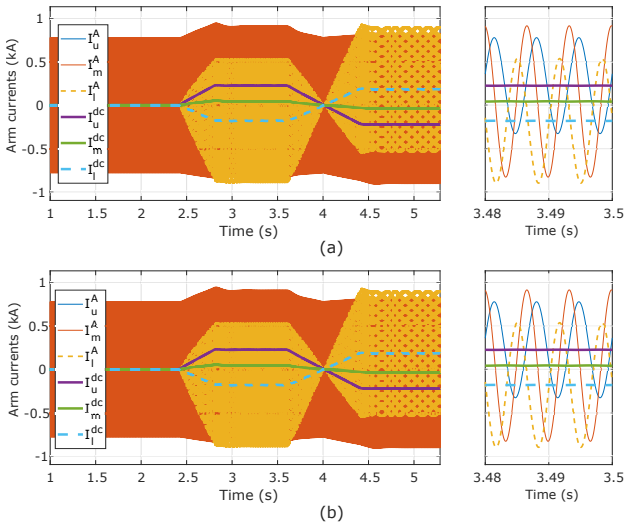

Fig. 15. Arm currents for nominal operation. (a) connected to the positive pole of the bipole, and (b) connected to the negative pole of the bipole.

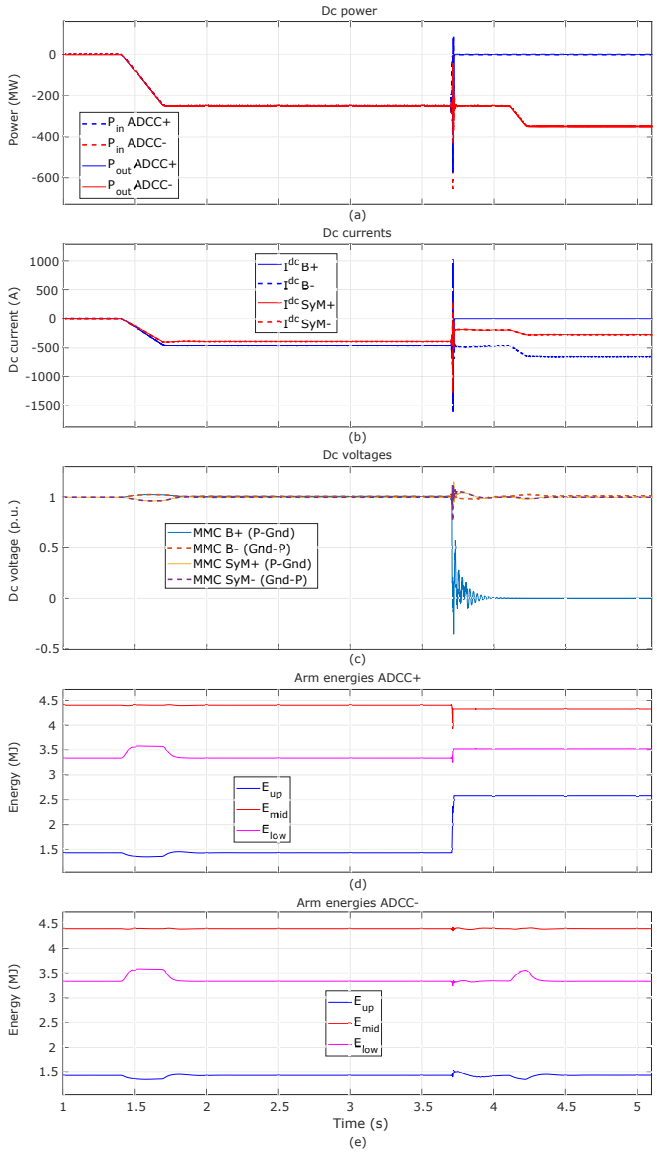

Fig. 16. Simulation results of the ADCCs. At 1.4 s the ADCCs start to exchange power from the SyM to the B. At 3.7 s a fault on the positive pole of the B line is simulated. At 4.2 s the power reference of the healthy ADCC is increased from 250 MW to 350 MW (rated power).

poles of the bipole (see Fig. 8). The last stage is the degraded mode, where the healthy components of the system continue to operate exchanging power through the dc-dc converter. The simulation results are presented in Fig. 16 and Fig. 17.

The results presented in Fig. 16a show that the ADCCs can exchange power between the B and SyM. Fig. 16b present the dc currents which are not affected by the internal ac currents of the ADCCs. The dc voltage is presented in Fig. 16c, it can be noticed that at the time of changing the power, there is a small disturbance, but the steady-state conditions are regained rapidly. Fig. 16d, e present the energy per arm of each ADCC. similar to the dc voltages, the energy is disturbed during the power changes. However, the control is capable to recover steady-state conditions.

At the time of the fault (around 3.7 s), the ADCC+ is blocked to stop the fault current with the FBSMs in the upper arm. It can be observed that the energy E_{up} in Fig. 16d

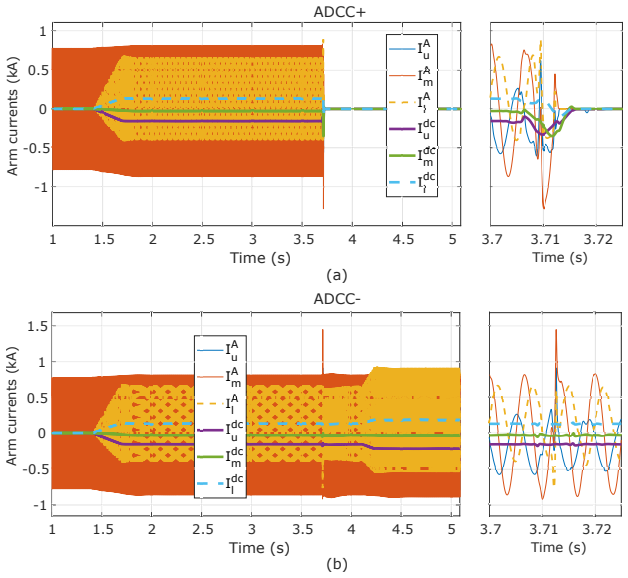

Fig. 17. Arm currents of one leg for the fault simulation . (a) ADCC connected to the positive pole of the bipole. (b) ADCC connected to the negative pole of the bipole.

increase as the FBSMs charge with the fault current. After the fault, the healthy equipment, i.e. B-, ADCC-, and SyM continue normal operation with small disturbances. At 4.2 s the power through the ADCC- increases from 250 MW to 350 MW to supply its rated power to partially compensate for the loss of B+.

The arm currents are presented in Fig. 17. The ADCC+ is blocked as the dc voltages drop below 0.6 p.u. (detection around 3.71 s). It can be noticed that the arm currents are stopped under 10 ms (see Fig. 17a), thanks to the FBSMs. The arm currents of ADCC- are presented in Fig. 17b. It is noticeable that a small disturbance is present at the time of the fault between 3.7 s and 3.715 s. After blocking the ADCC-, the healthy ADCC+ continues normal operation.

V. Conclusion

Due to the lack of non-isolated dc-dc converters proposed in the literature to provide immediate redundancy, a new modular converter, the asymmetrical dc-dc converter (ADCC) is proposed in this paper. The ADCC is proposed for the interconnections between a bipole and a symmetrical monopole. The redundancy is achieved using one converter per pole of the bipole. The converter was tested in a simulation model implemented in Matlab/Simulink for two scenarios: the nominal operation and fault event. The results suggest that the control strategy is able to keep the converter energy stable after transients, following the power reference. During the fault event, the ADCC solution allows to have continuous operation with the healthy equipment of the system, i.e. healthy pole of the bipole and monopole line.

Further studies should be carried out to optimize the inductors in the circuit. Experimental implementation should be performed to validate the control strategy in real applications.

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