A RISC-V Instruction Set Extension for Flexible Hardware/Software Protection of Cryptosystems Masked at High Orders

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Table of Contents

Table of Contents

Introduction

Side channel attacks (SCAs) [KJJ99]

Exploit correlations between measured physical values and operations and operands processed in the circuit

Masking countermeasure [Cha+99; GP99]

Randomize all intermediate sensitive variables

Instruction set extensions (ISEs)

New masked instruction to accelerate masking and increase security

Contribution

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Table of Contents

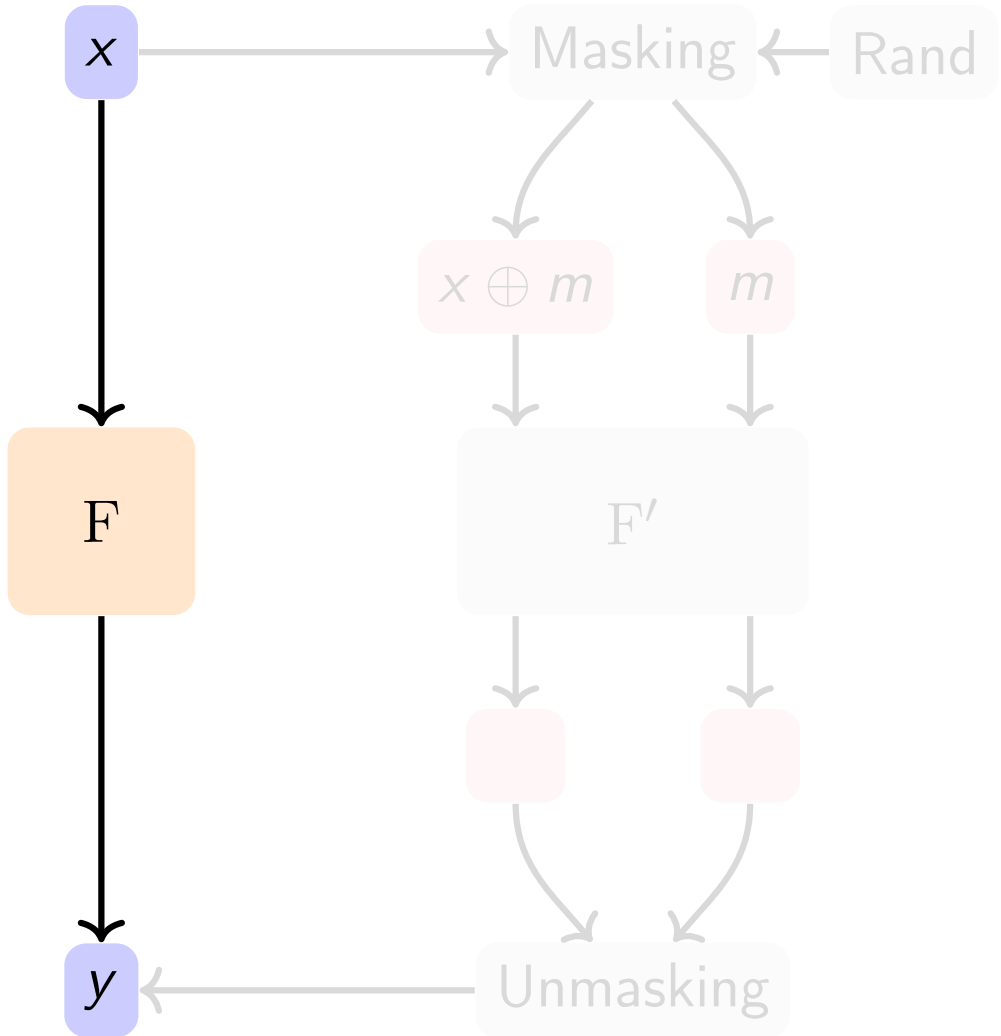
Masking Countermeasure

Masking

- Mask x into $(x \oplus m, m)$ with m a random mask
- Apply a masked function F'
- Unmask to get y

Software masking

- Computation time increases as $O(d^2)$
- Micro-architectural leakage



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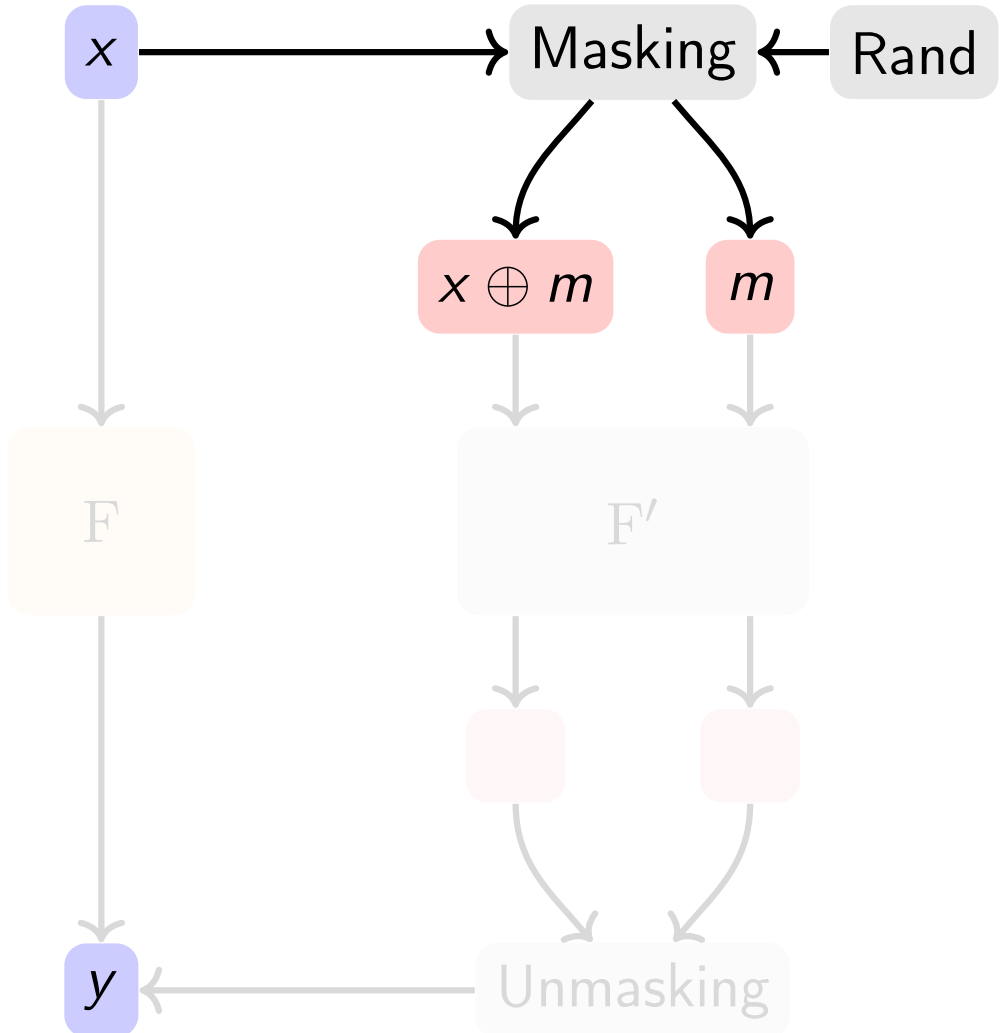

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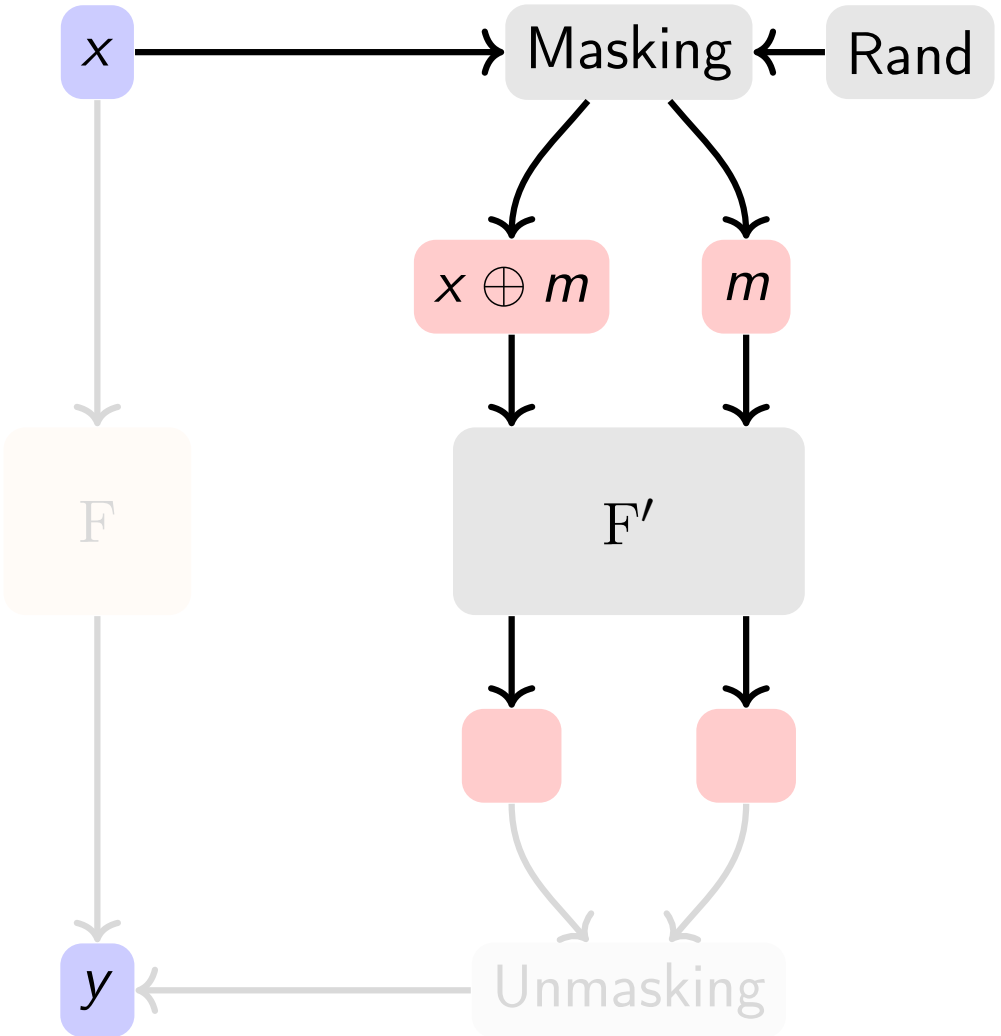

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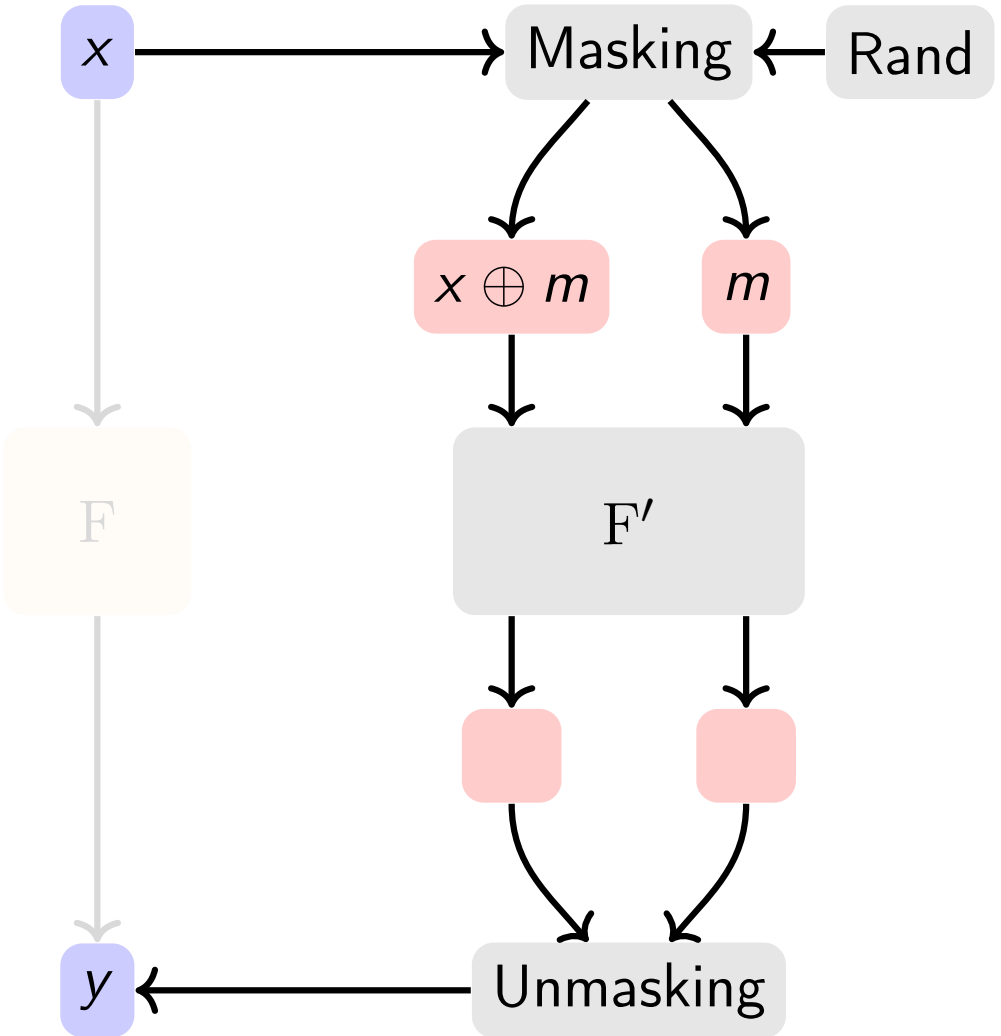

Masking Countermeasure

2-order masking

- Mask x into $(x \oplus m_1 \oplus m_2, m_1, m_2)$ with m_1, m_2 random masks
- Apply a masked function F'
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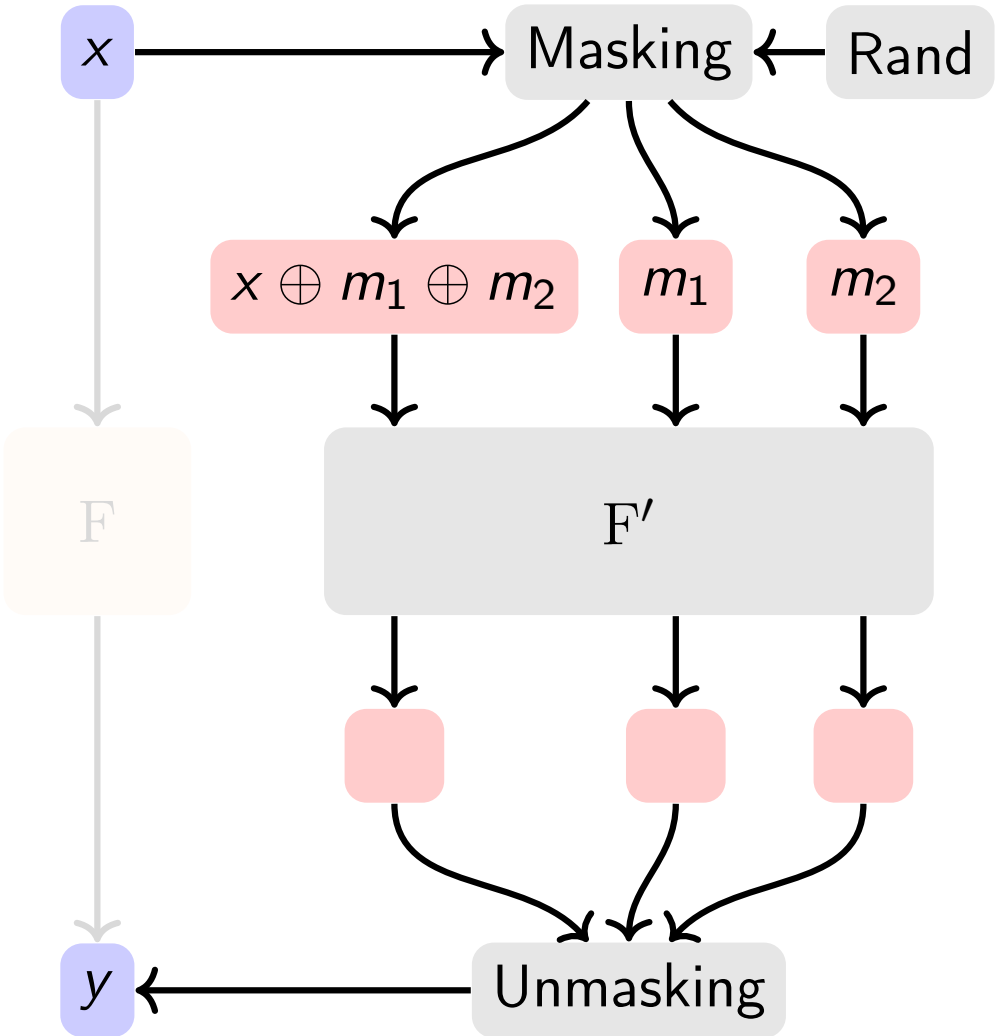

Masking Countermeasure

d-order masking

- Mask x into

  $(x \oplus m_1 \oplus \cdots \oplus m_d, m_1, \cdots, m_d)$

  with $m_1, \cdots, m_d$ random masks
- Apply a masked function F'
- Unmask to get y

Software masking

- Computation time increases as $O(d^2)$
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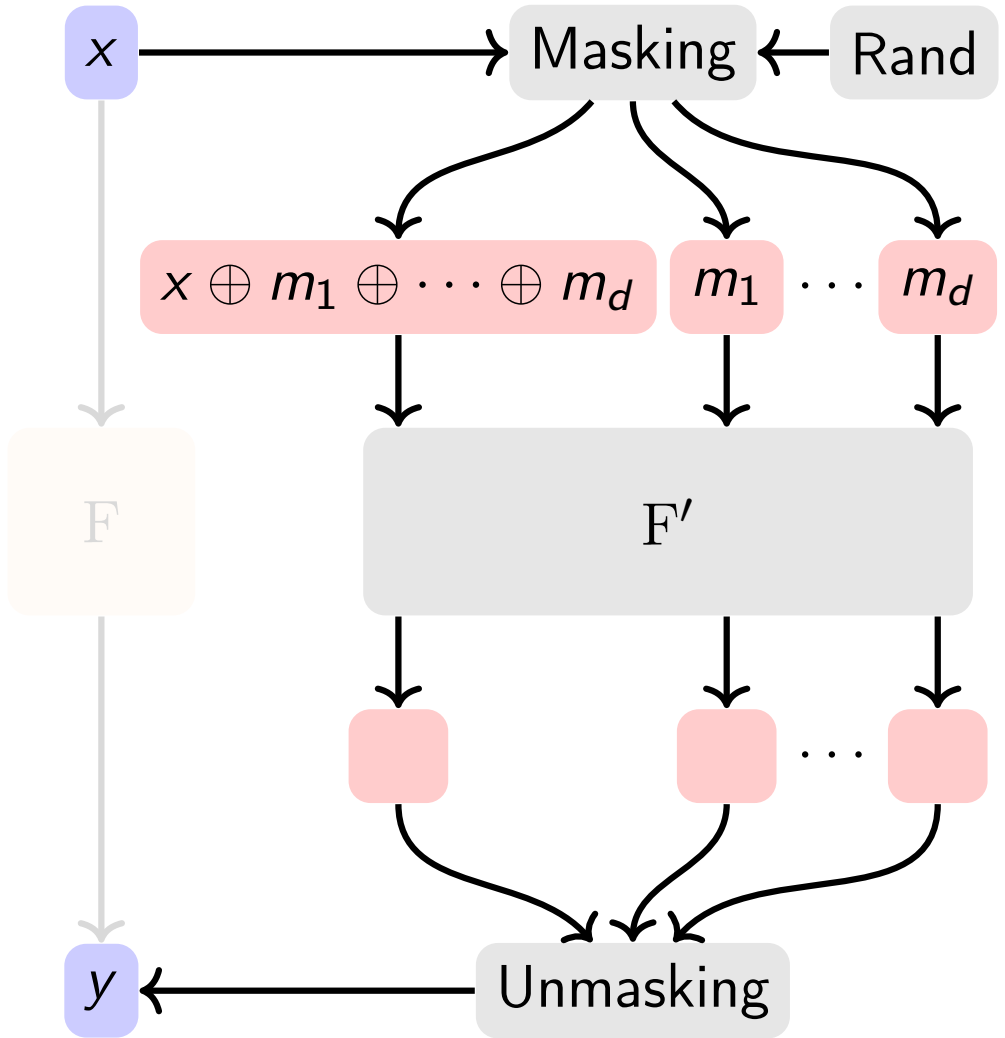

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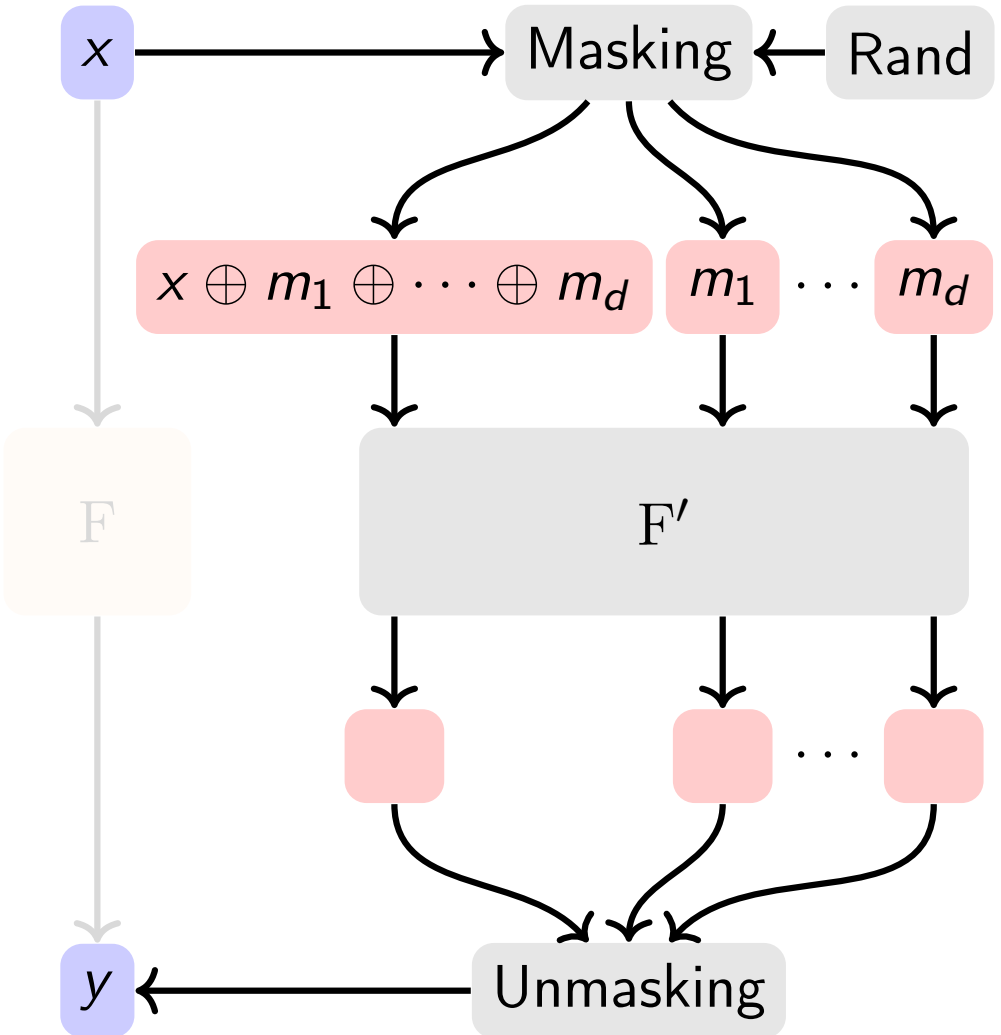


Instruction Set Extensions for Masking

Reference	RV	Masking order	Flexbility at design time	Flexbility at run time
[Gro+16]	✓	$\{1, 2, 3, 4\}$	✓	✗
[DGH19]	✓	1	✗	✗
[Gao+21]	✓	1	✗	✗
SKIVA [Kia+21]	✗	$\{1, 3\}$	✗	✓
SME [MP21]	✓	$\{1, 2, 3\}$	✓	✗
Our ISE	✓	$\{1, \cdots, 31\}$	✓	✓

Table of Contents

Our Hardware/Software Masking Solution

A hardware masked ISE

Masked ISE with order d_{H} fixed at synthesis time

Software usage of our hardware masking ISE

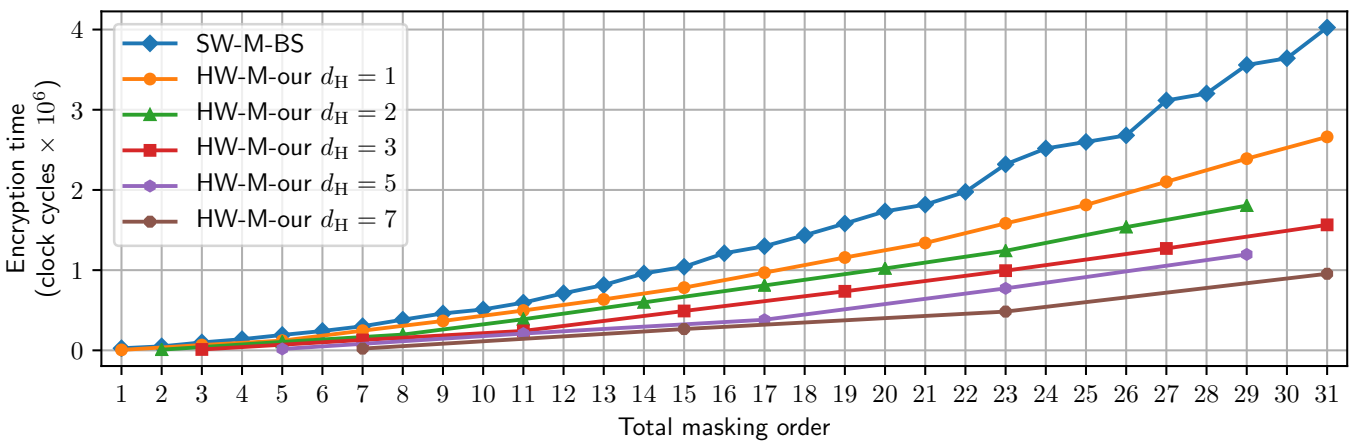
Secure composition over the masked instructions to mask at order:

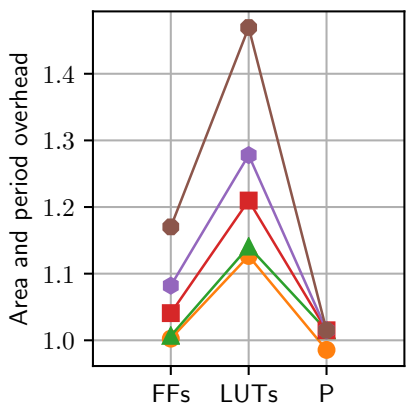
$$d = s(d_{\mathrm{H}} + 1) - 1,$$

where s is a software multiplicative factor fixed at run time

Implementation results

Masked ISE at orders $d_{\mathrm{H}} \in \{1, 2, 3, 5, 7\}$ and various total orders





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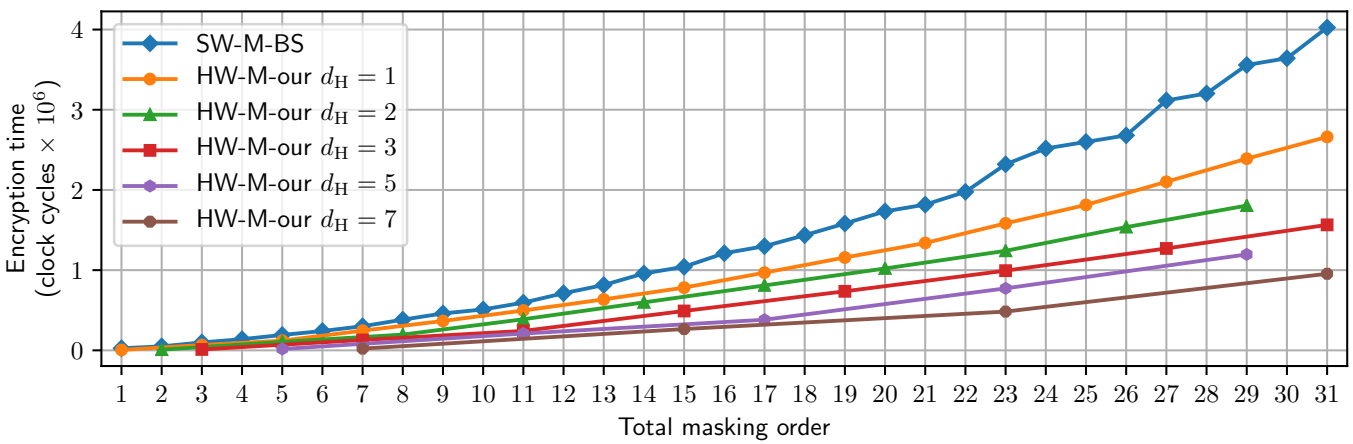

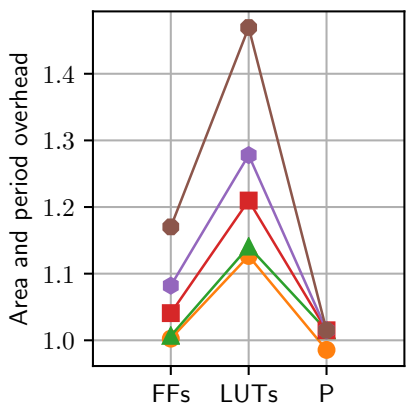

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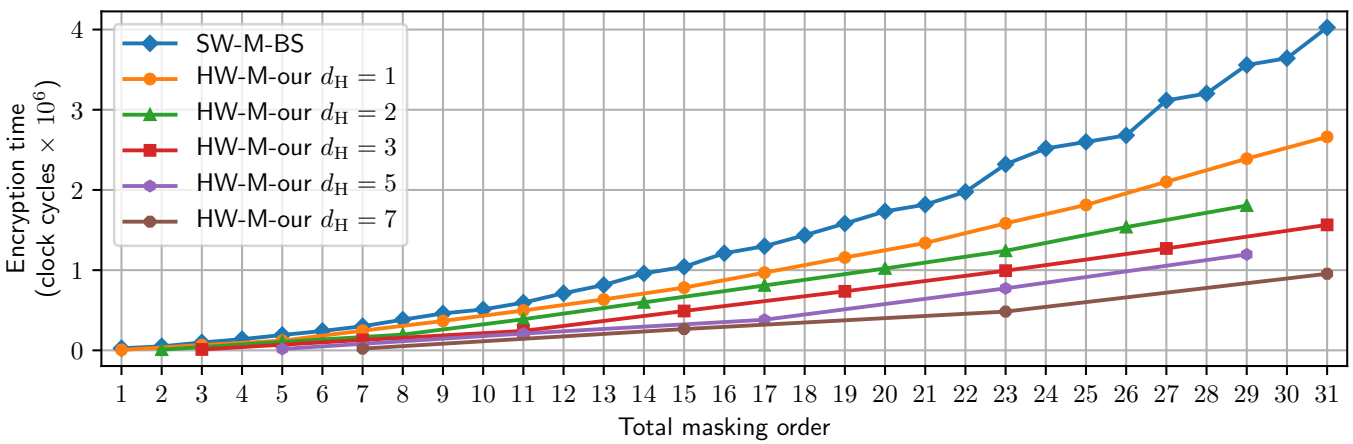
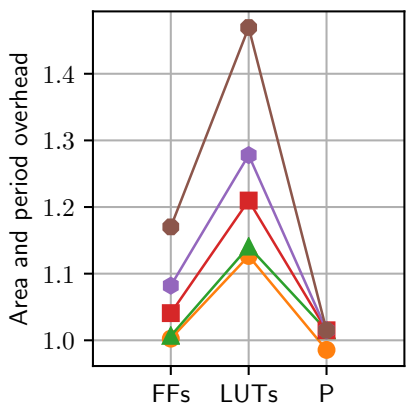




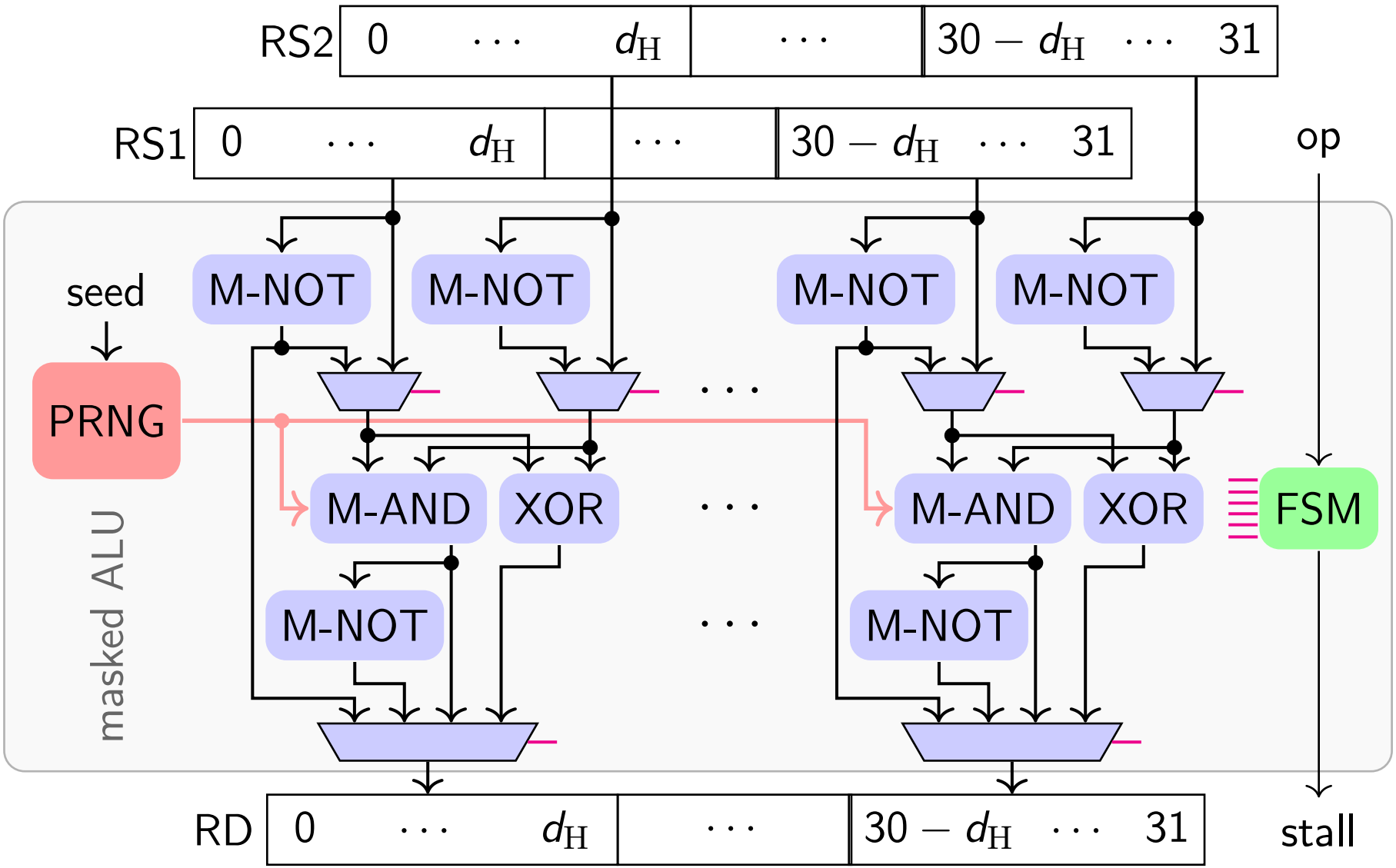
Our masked ISE

Masked Instructions

- Use share slicing representation (see [JS17])
- Verify PINI composability property (see [CS20])
- Easy masking of bit slicing implementations using USUBA (see [MD19])

Instruction	Format	Latency	Random bits
masked AND	`m.and rd, rs1, rs2`	2	$32(d_{\mathrm{H}}-2)$
masked OR	`m.or rd, rs1, rs2`	2	$32(d_{\mathrm{H}}-2)$
masked NOT	`m.not rd, rs1, rs2`	1	0
masked XOR	`m.xor rd, rs1, rs2`	1	0

Unit for Masking



Integration into the CV32E40P Core

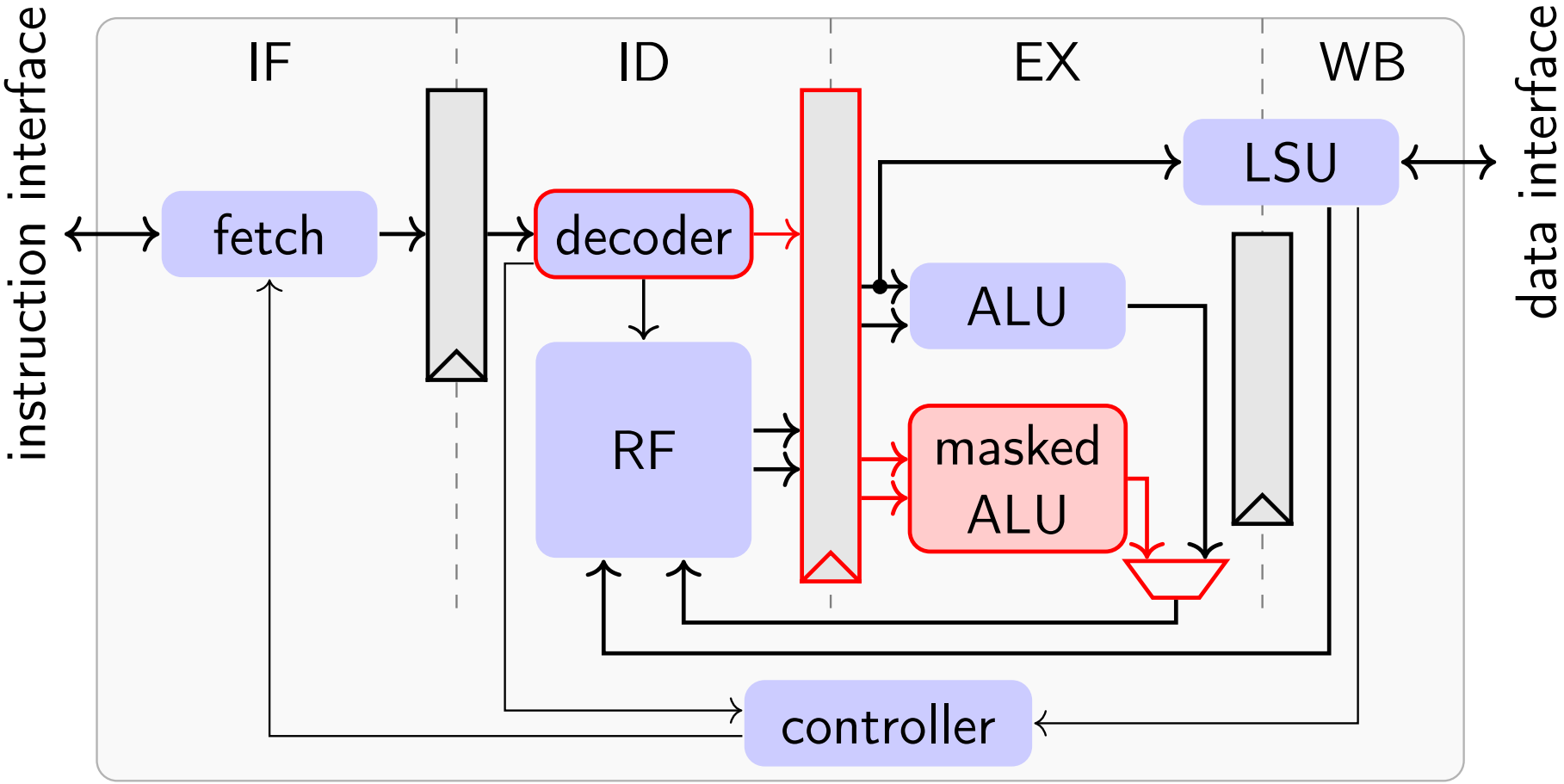
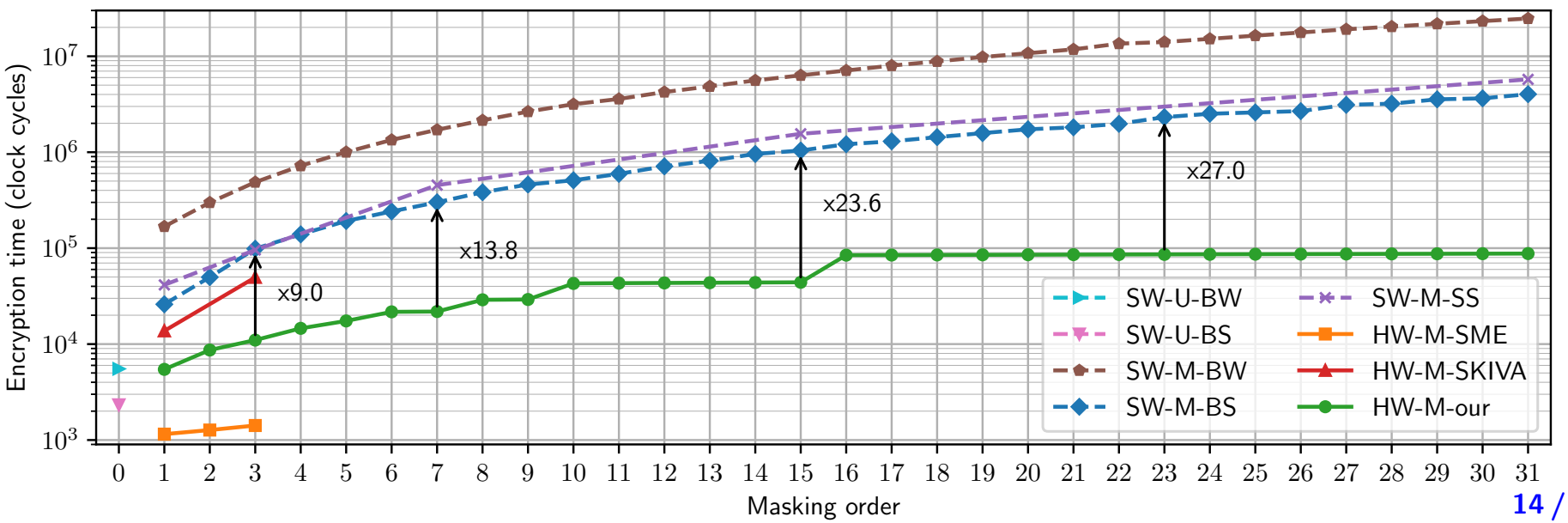


Table of Contents

Comparison to Previous Solutions

Encryption times in **log scale** for one AES block:

- SW-U-BW is unmasked and byte-wise
- SW-U-SW is unmasked and bit-sliced [MD19]
- SW-M-BW is masked and byte-wise [Cor+14]
- SW-M-BS is masked and bit-sliced [Bel+20]
- SW-M-SS is masked and uses share-slicing [JS17]
- HW-M-SKIVA is masked with SKIVA [Kia+21]
- HW-M-SME is masked with SME [MP21]
- HW-M-our is masked with our ISE



Comparison to Previous Solutions

Area/frequency results on a Digilent Arty A7 FPGA board of the CV32E40P with our and the various state-of-the-art ISEs

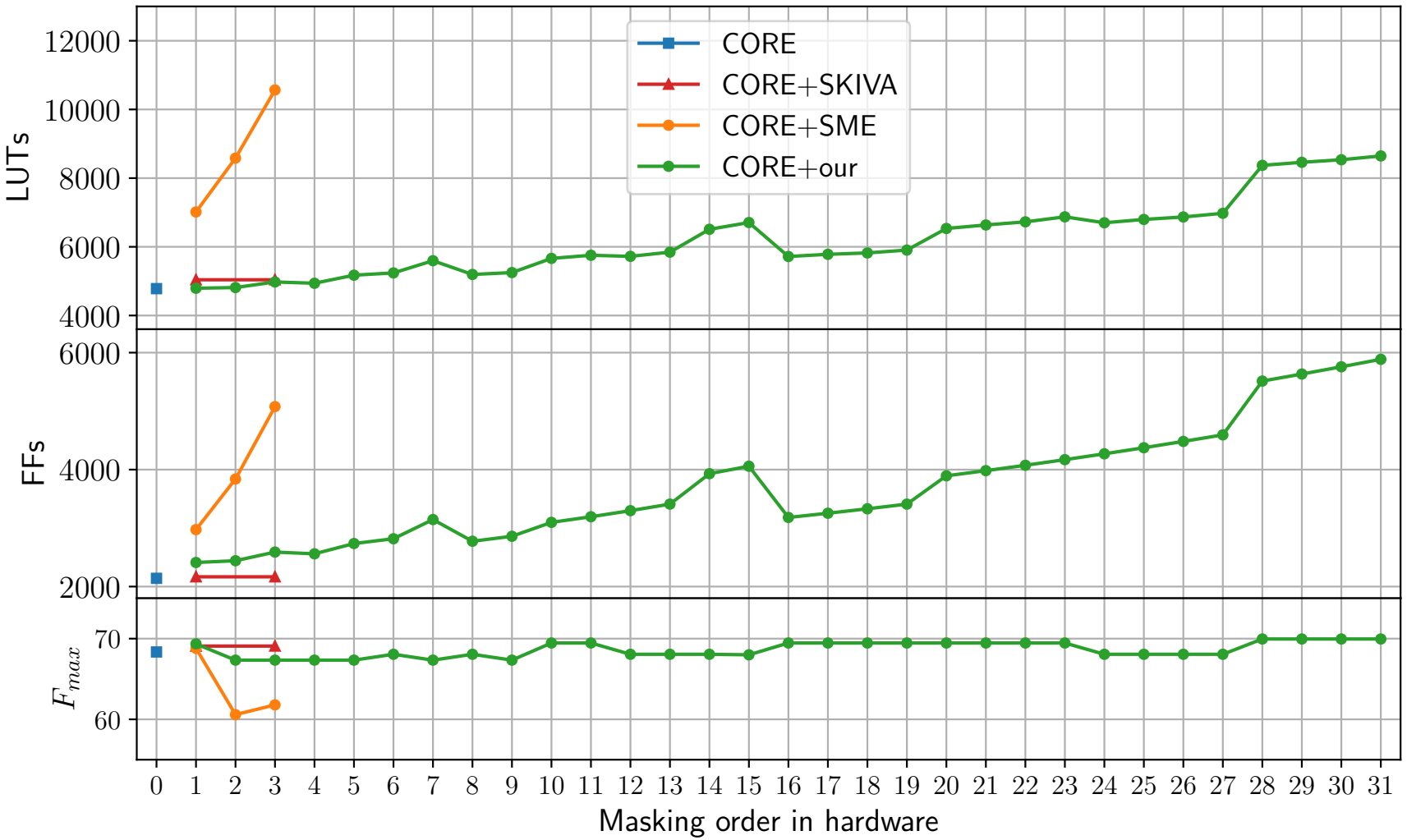


Table of Contents

Conclusion and Future Prospects

Our hardware/software masking solution

- Flexibility at design time and run time
- Speeds up masking with a small silicon cost
- Allow higher order masking
- Apply to various cryptosystems

Future Works

- Security evaluation using physical attacks
- Masked ISE optimized for AES and post-quantum cryptography

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End of Presentation

Thank you for your attention

Do you have any questions?

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Attack by Side Channel Observation

Available data

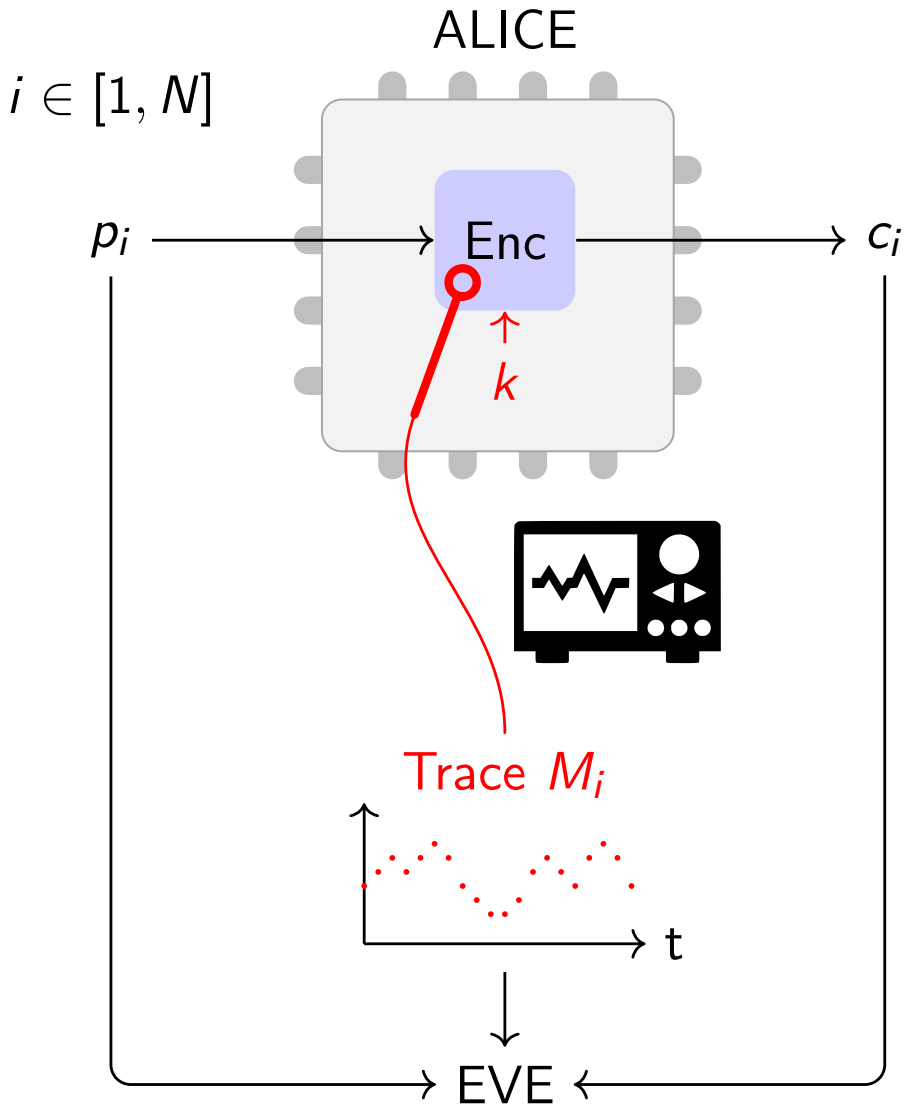
- Plaintexts and/or ciphertexts
- Physical measurements during each encryption

Measured physical quantities

- Power consumption [KJJ99]
- Electromagnetic radiation [QS01]
- ...

Good book

Power Analysis Attacks: Revealing the Secrets of Smart Cards [MOP07].



Bit Slicing

	Bloc 0	Bloc 1	$\cdots$	Bloc 31
R_0	b_0^0	b_0^1	$\cdots$	b_0^{31}
R_1	b_1^0	b_1^1	$\cdots$	b_1^{31}
$\vdots$	$\vdots$	$\vdots$	$\vdots$	$\vdots$
R_{127}	b_{127}^0	b_{127}^1	$\cdots$	b_{127}^{31}

Principle

- Transposes k input blocks of l bits into l registers of k bits
- Express algorithms in terms of elementary boolean gates (e.g. AND, XOR, OR, NOT)

Advantages

- High throughput
- Constant time implementation

Masked Bit Slicing

First solution

Shares of one bit are placed into different registers [JS17; Bel+20]

Second solution: share slicing

Shares of one bit are placed into one slice of a physical register [JS17; GR17]

- Avoids intermediate recombinations of shares
- Requires less memory words

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Overhead Comparison of Hardware Masking ISEs

d_H	ISE	Time		Area & period overhead		
		Cycles	Ov.	FFs	LUTs	P
1	SME	1142	n.a.	1.5	1.6	1.6
	Our SME	1152	0.5	1.4	1.5	1.0
	Skiva	2816	4.0	n.a.	n.a.	n.a.
	Our Skiva	13730	4.8	1.0	1.1	1.0
	Our	5452	2.3	1.1	1.0	1.0
2	SME	1333	n.a.	1.9	1.9	1.7
	Our SME	1271	0.5	1.8	1.8	1.1
	Our	8673	3.7	1.1	1.0	1.0
3	SME	1524	n.a.	2.6	2.2	1.7
	Our SME	1417	0.6	2.4	2.2	1.1
	Skiva	9264	13.2	n.a.	n.a.	n.a.
	Our Skiva	24787	17.0	1.0	1.1	1.0
	Our	11010	4.7	1.2	1.0	1.0