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III-V Semicondutor Nanostructures And Iontronics: InAs Nanowire-based Electric Double Layer Field Effect Transistors

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Abstract. In the emerging interdisciplinary field of *iontronics*, ionic motion and arrangement in electrolyte media are exploited to control the properties and functionalities of electronic devices. This approach encompasses a wide range of applications across engineering and physical sciences including solid-state physics, electronics and energy storage. We briefly discuss the use of approaches and techniques characteristic of iontronics in nanoscale devices based on III-V semiconductor nanostructures, a versatile and promising platform for nanoscience and nanotechnology applications. Then, we report and discuss the operation of InAs nanowire-based electrolyte-gated transistors implemented using ionic liquids. We show that the ionic liquid gating outperforms the conventional solid-state back gate, and we compare the current modulation achieved in the same InAs NW using the ionic liquid gate or the back-gate. Finally, we highlight the capability of the liquid electrolyte to drastically change the resistance dependence on temperature in the nanowire. Our results suggest promising strategies toward the advanced field effect control of innovative III-V semiconductor nanowire-based devices for information and communication technologies at large.

INTRODUCTION

Iontronics is an emerging discipline which addresses the use of ionic motion in electrolytes to operate electronic and optoelectronic devices [1–4]. In recent years, it found a plethora of applications in different fields such as solid-state physics [5], biology [6], electrochemistry [7], green chemistry [8],sensing [9] and energy management and storage [10]. When it comes to exploiting the features of iontronics in solid-state devices, the first wave of investigations focused on functional devices based on Van der Waals materials, the modulation of the electrical [11] and optoelectronical properties [3, 4] was demonstrated. From the fundamental point of view, the main feature of iontronics i.e. the occurrence of ultra-high electric fields inducing high charge carrier density was exploited to explore new regimes of carrier densities [12] as well as transitions from insulating to superconducting states in oxide thin films [13–15]. Besides, a bunch of very recent and intriguing works report iontronic devices based on nanowires of group IV and II-VI semiconductor compounds [16][9, 17–20] as well as oxide nanowires [21, 22].

Nanowires made with III-V semiconductors such as InAs and GaAs represent an important material platform for applications spanning from thermoelectrics [23–27], nanoelectronics [28] to optoelectronics [29] and photonics [30] and encompassing also sensing [31], quantum information [32–35] and spintronics [36]. Recently these systems were made object of investigation aimed at developing novel strategies for electrostatic gating, for instance by exploiting soft-matter systems typically used in organic electronics e.g. polymers and polymeric gels. In this context, modulation of zero-dimensional states in self-assembled InAs quantum dots has been demonstrated [37] exploiting ionic liquids. Polymeric electrolytes have been used to demonstrate the possibility to set the threshold voltage in InAs nanowires with perspectives for thermoelectrical applications [38] and to tune the Rashba spin-orbit interaction in InAs nanowires [36]. Furthermore, hygroscopic polymeric electrolytes have been used on n-type InAs and p-type

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GaAs nanowires in order to demonstrate logical operations in devices having implications in transducing protonic biological-like signals to electrical signals involved in inorganic circuitry [39]. Moreover, polymer electrolites have been used in combination with highly doped GaAs nanowires and effective charge modulation has been demonstrated in a doping regime in which any conventional solid state gate has no effect [40]. However, even if the use of polymeric electrolytes is auspicable for applications in which the patterning of the gate dielectric is needed (i.e. devices needing for non-trivial gate geometries), this material system features a limited ionic mobility, resulting in a limited gate efficiency and ac response. As a matter of fact, for devices needing a global gate acting on the entire nanostructure, the use of ionic liquids is more auspicable with respect to polymers, as briefly mentioned in [40].

In this work, after having briefly discussed the relevance of III-V semiconductor nanowire-based devices in the context of iontronics, we experimentally investigate the applicability of EDL gating using ionic liquids as the electrolyte to achieve field-effect control of InAs semiconductor nanowires. In particular, we used the room temperature ionic liquid 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide ([Emim][Tf_2N] - represented in Fig. 1(b)(c)) to operate our nanowire-based field-effect transistors. We report an impressive efficiency of this gating technique, revealing its potential for NW-based technology in low voltage applications and comparing it with the conventional solid-state gate. We also report a dramatic change of the temperature dependence of the electrical resistance in NWs, induced by the strong electric fields (exceeding 10 MV/cm [15]) accessible by mean of EDL gating.

RESULTS AND DISCUSSION

Even if solid state iontronic devices comprise very different material platforms and used to explore a plethora of phenomena (electric conduction, photon emission, phase transitions to name a few), there is a common aspect to every iontronic device. As a matter of fact, what allows to modulate the optical and transport properties of materials using electrolytes is the formation of an electric double layer (EDL) at the interface between the electrolyte and the material used as active channel (building block) in the device. The principle of the formation of EDLs is pictorially represented in the system depicted in Fig. 1. The system consists of 700 Emim and 700 Tf_2N molecules enclosed between two Au(111) with an area of 5.6x5.6 nm^2 positioned at a distance of 9.4 nm from each other. The gold slab is modeled with GolP force field [41] (GolP-FF), which yielded reasonable results in previous applications [42–44], whereas the ionic liquid is modeled with the OPLS-based ionic liquid FF recently developed by Doherty et al [45]. In Fig. 1(a) the electrolyte (ionically conductive but electronically insulating) is enclosed between two (electronically conductive) surfaces: one of them (referred to as the electrode) is set to a voltage V_{liquid}, while the other is electrically floating. In this configuration, ions having a determined charge in the electrolyte (positive for $V_{\text{liquid}} < 0$ or negative if $V_{\text{liquid}} > 0$) will tend to accumulate at the interface between the electrolyte and the electrode. Consequently, due to the electrical overall neutrality of the electrolyte, ions having the opposite charge with respect to the accumulation layer on the electrode will tend to reorganize far from the area in which the potential V_{liquid} is applied. This will create a second charge layer at the interface with the second conductive surface. The effect of this charge layer is to induce a second charge layer (hence the term electric ”double” layer) in the second electrode.

Here, it is worth thinking about the second electrode as the one playing the role of the active channel in a field-effect transistor configuration. The ability to manage the density of ionic redistribution in the electrolyte by means of an applied voltage on the electrode, consequently to modulating the density of charges in a material used as an active channel, is what makes EDL gating a functional technique to operate devices. The redistribution of ions when a voltage is applied to an electrode is shown in the computed curve in Fig. 1(d), representing the molecular distribution of Emim and Tf_2N molecules in the direction perpendicular to the conductive surfaces. The direct experimental imaging of the EDL formation at the interface between solids and ionic liquids represents an extremely challenging task that has not been accomplished yet. However, indirect measurements exploiting x-ray reflectivity have allowed to identify the double layer at the electrodes [46]; furthermore, the effects of the double layer formation on the electrode morphology have been addressed, revealing the surface reconstruction of Au(100) and Au(111) surfaces [47]. Despite the simplicity of the physical nature of this phenomenon, this technique to modulate the carrier density in materials has been found to be incredibly efficient, particularly when it comes to nanodevices in which a solid-state backgate is commonly used [48]. In this context, several works were devoted to the study of ionic layers in EDL transistors (EDLTs) [46, 49, 50]. Moreover, the conformal nature of the EDL gating achieved with ionic liquids can be used allows to operate devices in which the backgate has little or even no effect on the active channel, as for instance in the case of suspended nanowire-based devices [26]. The core of the devices used in this work is constituted by wurtzite n-type InAs NWs grown on a (111)B InAs substrate by means of gold nanoparticle assisted chemical beam epitaxy [51, 52]. As grown NWs are detached from the growth substrate by means of sonication in isopropyl alcohol (IPA) and are

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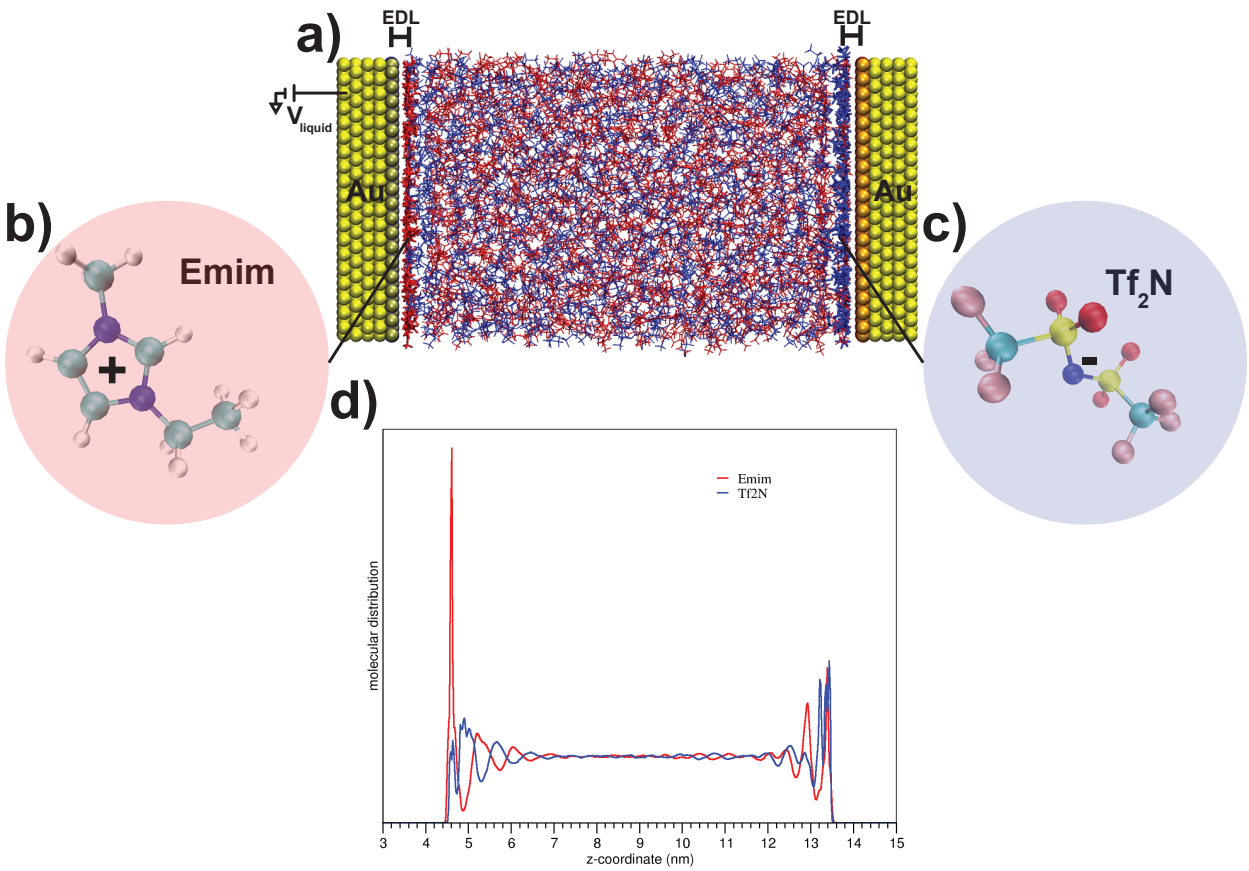

Figure 1. (a)Pictorial representation of the electric double layers forming at the interface between an electrolyte medium enclosed between two conductive electrodes. One of the electrodes is set to the potential V_{liquid}, while the other one is floating. The applied potential modifies the ionic landscape of the electrolyte, causing an accumulation layer of ions at the interface with the charged conductor. Due to the charge neutrality of the electrolyte, a second accumulation layer of ions having the opposite charge occurs at the interface with the second electrode, yielding very high electric fields and thus generating an accumulation layer of charges in the material. The EDL gate realized in this way is able to strongly modulate charge densities in several types of materials, as discussed in the text. (b)-(c) Molecules composing the room temperature ionic liquid 1-ethyl-3-methylimidazolium bis(trifluoromethylsulfonyl)imide ([Emim][Tf_2N]) used in this and many other works as electrolyte for EDL gating. The cation is Emim (b) while the anion is Tf_2N (c). (d) Computed molecular distribution of the ions in the configuration represented in panel (a): an accumulation layer of positive ions is visible at the interface with the negatively charged electrode. Negative ions assets themselves accordingly due to the overall charge neutrality of the liquid, causing a second accumulation layer of the opposite charge sign on the second electrode.

stored in IPA solution until being dropcasted on a Si++/SiO2 substrate. The devices consist in a comb of 100 nm wide electrodes defining ohmic contacts with the semiconductor, as well as a 100 μm x 100 μm square used as gate electrode to polarize the liquid. These structures are defined by means of standard electron beam lithography techniques. The ohmic contact between the gold electrodes and the semiconductor is assured by passivating the surface of the NW by means of a $(NH_4)_2S_x$ solution followed by metal evaporation (10/100 nm Ti/Au layers). An optical micrograph of a sample device is shown in Fig. 2, together with a scanning electron micrograph zoomed on the device as well as micrographs reporting top and side view of InAs nanowires showing the hexagonal cross section.

The devices used in this work are provided with both a conventional solid-state backgate (the Si++/SiO2 substrate) and the ionic liquid gate (ionic liquid droplet and counter-electrode). In this way, we are able to explore the operation of the same device by means of both techniques, allowing a direct comparison between their gating effectiveness. The main features of the two gates are pictorially represented in Fig. 2(c) and (d). When a gate voltage V_{backgate} is applied to the Si++ layer underneath the 285 nm SiO2 layer band bending occurs and the charge carrier

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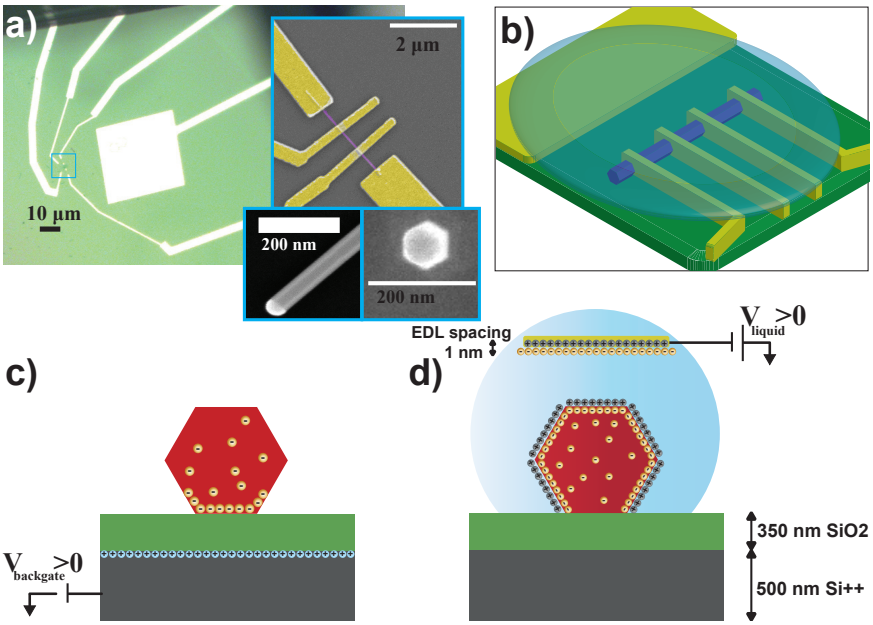

Figure 2. (a) Optical micrograph of one of the measured devices. The comb of contact electrodes is visible, as well as the 100 μm x 100 μm liquid gate counter-electrode used to modify the ionic landscape and perform gating on the semiconductor NW. The upper part of the onset reports a false-colored scanning electron micrograph zoomed on the nanowire, which is the core of the device: yellow color is used for gold, while purple indicates the semiconductor nanowire. The lower part of the onset reports scanning electron micrographs of InAs nanowire: left panel reports the side view of a nanowire, while the right panel reports the top view. In both cases it is possible to appreciate the hexagonal cross-section of the nanostructure.(b) Pictorial representation of the zoomed area defined by the black rectangle in Fig. 2(a). The NW is represented in blue, while the contact electrodes and the counter-electrodes are represented in yellow. The Si++/SiO2 substrate is represented in green. (c)-(d) Naive representation of the impact of device operation on the carrier distribution in the nanowire, for (c) the conventional solid-state backgate and (d) the liquid gate. Due to the geometrical characteristic of the conventional solid-state backgate, it effectively modulates mainly the charge carrier density in one of the six facets of the NW, while the conformal nature of the ionic liquid gating provides effective gating on five out of six facets of the NW in a dropcasted device configuration. This ideally makes it possible to control the carrier density in every facet in devices featuring a suspended nanowire architecture.

density can be modulated. Due to the geometrical conformation of this kind of gate, only the lower facet of the NW is involved so that a charge accumulation layer can be induced only on a single facet among the six defining the NW. On the other hand, the application of a voltage V_{liquid} on the liquid gate counter-electrode has a significantly different effect: the ionic landscape in the ionic liquid is modified to that and EDL is formed on the entire surface of the NW, thus involving five of the six facets. Furthermore, another fundamental aspect characterizing the liquid gating and making it more effective with respective to the conventional solid state gate is the characteristic length separating the accumulation layer in the semiconductor and the one inducing it: while the solid-state backgate relies on ~ 285 nm thick SiO2 layer, the typical thickness of the EDL is ~ 1 nm [1]. These naive but effective geometrical arguments were invoked for instance to quantitatively explain the huge performance difference between the conventional gating and the ionic liquid based EDL gating, as reported in several works [12, 48, 53] .

A typical device operation is reported in Fig. 3. Here, panel (a) reports the operation of the device as a EDL transistor (EDLT), reporting the measured current flowing through the active channel (represented by the color) in the parameter space defined by the applied liquid-gate voltage V_{liquid} and applied bias voltage V_{ds}. Panel (d) reports the operation of the same device as a conventional field effect transistor (FET) using the solid-state backgate and follows the same representation as the previously described panel, with the only difference of reporting the applied back-gate voltage V_{bg} on the x-axis. Strikingly, the full modulation of the active channel conductance is achieved with the liquid gate by applying gate voltage in a much lower range with respect to h the Si++/SiO2 gate. As a matter of fact, current flowing across the active channel of the transistor is found to be modulated nearly one order of magnitude higher with respect to current flowing through the channel in a conventionally-operated FET, at a fixed applied bias voltage value.

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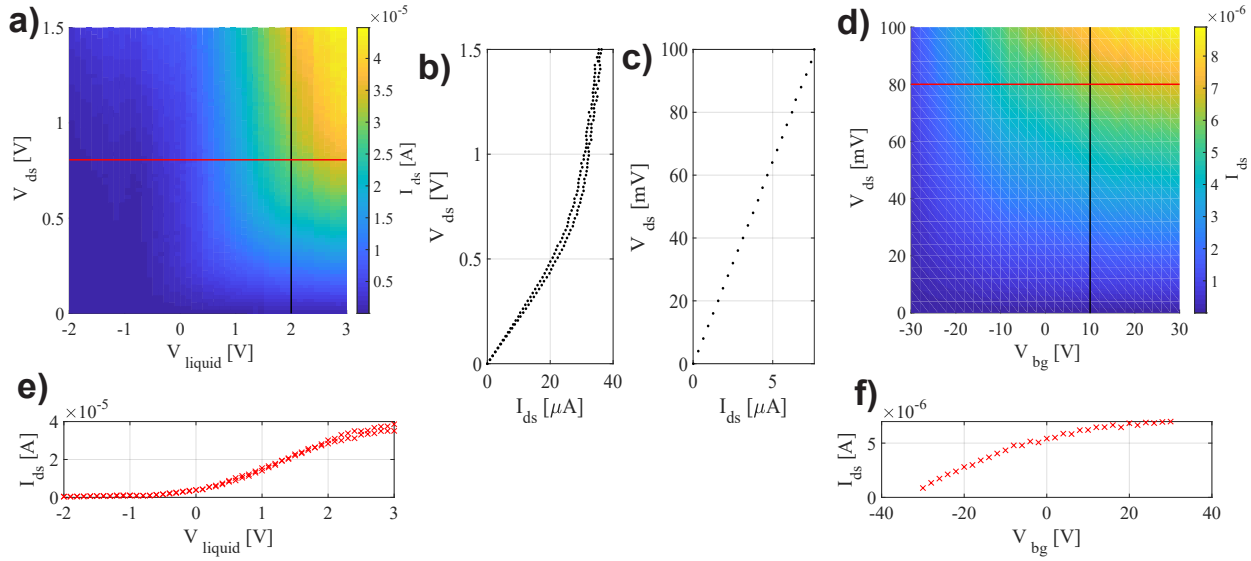

Figure 3. Device operation using the liquid (a) and solid (d) gate. The figures show the measured current (color scale) as function of the applied gate voltage (x direction) and applied source-drain bias voltage in the field effect transistor (y direction). A direct comparison between the two measurements allows to estimate the outstanding effectiveness of the liquid gate: the device is operated from a complete pinch-off regime (i.e. no current flowing across the nanowire) to the saturation regime in a voltage range which is 10 times smaller with respect to the similar operation exploiting the solid-state backgate. Fig.3(b)-(e) report current measurement for a fixed value of $V_{\text{liquid}}(V_{\text{DS}})$, varying $V_{\text{DS}}(V_{\text{liquid}})$. Fig.3(c)-(f) report similar measurements using the backgate. Results consistent with the current maps reported in the figure were typically achieved in the temperature range from slightly below room temperature to 250 K.

This effect is ascribable to the higher gate coupling of the liquid gate - taking advantage of the lower geometrical distance between the charge layers in the induced electric double layer - compared with the conventional solid-state gate, quantified as a ratio $C_{\text{liquid}}/C_{\text{bg}} \sim 30$ in a previous work [48], which allows to manipulate all the charge carriers injected by the dopants in the nanowire. Moreover, the required voltage range in order to achieve the full modulation of the conductivity of the channel is found to be ±3 V, while applied back-gate voltage values from -30 V to +30 V are required to operate the device. Typical characteristic curves are reported in panels (b)(e) for the liquid gate and (c)(f) for the back gate. The reported curves are obtained by extracting current measurements from the respective current maps (panels (a) and (d) for liquid gate and back-gate respectively). Fig. 3-(e) reports the current flowing through the device driven by the liquid gate with fixed applied bias voltage and varying the applied liquid gate voltage, showing the modulation of the semiconductor nanowire from the pinch-off to the saturation regime; Fig. 3-(b) report the current measurement of the same device, fixing the applied liquid gate voltage and varying the applied bias voltage. Equivalent current measurements are reported in Figs. 3-(c)(f) with the device driven by the solid state back-gate. A direct comparison of the measurements reported in Fig. 3(b)(liquid gate)-(e)(liquid gate) and Fig. 3(c)(solid gate)-(f)(solid gate) allows to further appreciate the outstanding performance of the liquid gate: while this completely tunes the conduction from zero current flowing through the NW to a saturated current value (Fig. 3(b)(liquid gate)-(e)(liquid gate), a well less performing operation is achieved using the solid-state backgate (Fig. 3(c)(solid gate)-(f)(solid gate) even for higher applied gate voltage values, showing that no proper pinch-off is obtained (ref. panel (f)(solid gate) with the conventional gating technique.

As a further analysis on the effect of the EDL gating using ionic liquids on InAs NWs, we studied the dependence of the resistance in the NW on temperature, for different gating regimes. To this aim, we apply a fixed gate voltage V_{liquid} and measure the conductance of the NW while cooling the system down from 250 K to 4.2 K. The result for two characteristic regimes (i.e. negative and positive applied gate voltage) are reported in Fig. 4(a). Here, the blue points refer to conductance measurements taken at positive applied voltage (+4 V), while the orange ones are measurements taken at a negative voltage value (-1 V). Because of the n-type doping of the NWs under analysis, the case of positive applied gate voltage corresponds to the active channel being populated by the liquid gate that tunes

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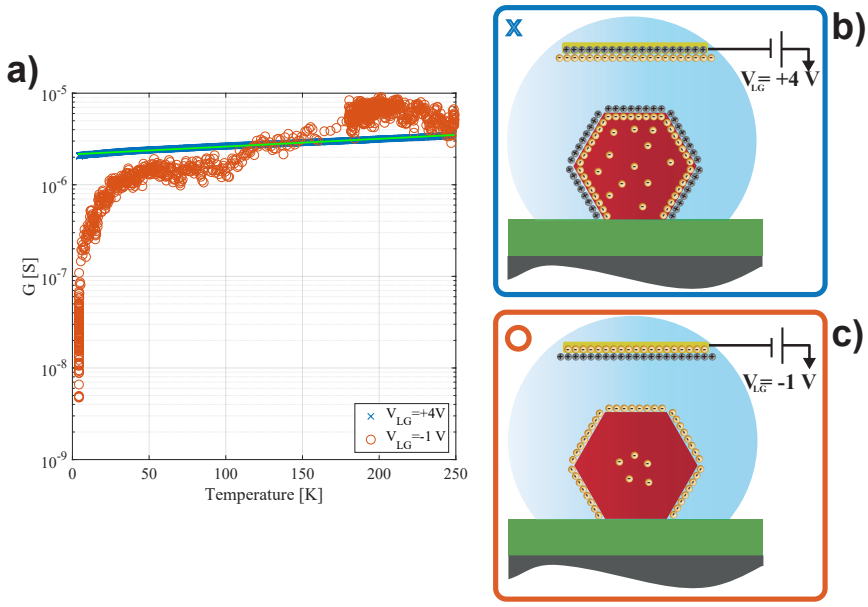

Figure 4. (a) Temperature dependence of the conductance in the NW, when different values of V_{liquid} are applied. When a positive voltage is applied to the counter-electrode driving the ions in the electrolyte, an EDL is formed at the interface between the (n-type) semiconductor and the liquid. In this way, charge carriers density is increased and the NW shows the typical semiconductor behavior in the dependence of its resistance on temperature. This configuration, corresponding to the blue points in Fig. 4(a), is schematically depicted in Fig. 4(b). The green line represents a best fit of the experimental data obtained with an exponential function $R(T) = ae^{bT}$, expected for semiconductors. On the other side, when a negative voltage is applied to the counter-electrode, a layer made of negative ions covers the surface of the NW (Fig. 4(c)). In this configuration, corresponding to the orange experimental points reported in Fig. 4(a), the majority charge carriers in the semiconductor are scattered away by the electric field induced by the ionic layer. This is reflected non-trivially in the conductance dependence on temperature, which in fact does not show the usual semiconductor behavior in this voltage configuration: a best fit with an exponential function is not possible.

the charge carriers density, increasing it (as represented in Fig. 4(b)). The corresponding experimental data in Fig. 4(a) basically suggest the expected conductance dependence on temperature in a semiconductor. As a further confirm of this, we performed a best fit (green line) of the experimental points using an exponential function: $R(T) = ae^{bT}$. This behavior, which is known from theory, is justified by the fact that temperature has the effect of exciting charge carriers from the valence band to the conduction band in the semiconductor. In this frame, increasing the temperature of a semiconductor corresponds to reducing its resistance and the exponential law readily comes from the thermodynamic nature of the phenomenon. Nonetheless, the behavior of the InAs NW resistance with respect to temperature variation does not follow the expected law when a negative voltage is applied to the counterelectrode driving the liquid gate (orange points in Fig. 4(a)). In this configuration, corresponding to Fig. 4(c), the channel is severely depleted of charge carriers. That said, the depletion of the conduction channel does not simply reflect in an increased resistance, but also its dependence on temperature does not correspond to the expected exponential law typical in semiconductor. This intriguing feature is likely due to the high coupling of the liquid gate with the nanostructure, strong enough to induce uncharted charge densities regimes.

The possibility to achieve a clear change in the material properties by field effect has been observed on several material platforms [13–15] and this perspective on III-V semiconductor nanowires is very promising for fields in which these materials are of great interest such as spintronics and quantum technologies [32–35]. As a matter of fact, the liquid gate provides a strong and reversible tool to severely modify the doping in the nanowire [48]. By fixing a doping regime by applying a liquid gate voltage and then by cooling the system until the liquid is frozen (i.e. below 220 K in our specific case) it is possible to fix the charge carriers density in the semiconductor nanowire even if the liquid gate voltage is removed, due to the ions being frozen at their positions. In this way, the doping of the wire becomes a new and promising parameter to be tuned in order to explore physical phenomena such as spin-orbit interaction in configuration which were inaccessible with previous technologies.

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CONCLUSIONS

In this work we have pointed out the promising combination of III-V semiconductor, an election material for applications regarding transport and photonics, with the soft-matter of ionic liquids, exploited as gate medium for field effect devices. As a test-bed of iontronic with III-Vs, we fabricated InAs nanowire-based electric-double layer transistors and demonstrated full modulation of the electrical conduction from pinch-off to saturation in few volts range of applied liquid gate voltage. Our devices comprised both the liquid gate and the conventional solid-state gate, allowing a direct comparison between the performances of the two methods. Owing to the intrinsic advantages of the ionic liquid gate with respect to the conventional gate, we find that the operation of the former out-stands the latter almost two orders of magnitude when it comes to voltages needed for device operation. Moreover, we find that the high electric fields induced by the ionic layer at the interface between the ionic liquid and the semiconductor are able to drastically change the temperature dependence of characteristic properties of the material such as the electrical resistance, suggesting the onset of a field effect-induced transition. Further investigations are needed to clarify this peculiar phenomenon.

This work sheds some light onto a technique - ionic liquid gating - able to unveil new and uncharted regimes of electrical conduction in III-V semiconductor nanowires, that represent the election material for several applications in spintronics and quantum information technologies, owing to the high spin-orbit coupling characterizing them. By using the liquid gate in the so-called set-and-freeze mode, i.e. by setting the ionic landscape of the liquid and then freezing it, it is possible to fix a determined charge carriers density in the semiconductor nanowire. In this way, it is possible to finely and reversibly tune the doping of the semiconductor under analysis, allowing to have a new and useful tuning parameter to exploit both for fundamental and applicative purposes.

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