



HAL
open science

CMOS Gate Driver with Integrated Ultra-Accurate and Fast Gate Charge Sensor for Robust and Ultra-Fast Short Circuit Detection of SiC power modules

Anas El Boubkari, Nicolas Rouger, Frédéric Richardeau, Marc Cousineau, Thierry Sicard, Pierre Calmes, Matthew Bacchi

► To cite this version:

Anas El Boubkari, Nicolas Rouger, Frédéric Richardeau, Marc Cousineau, Thierry Sicard, et al.. CMOS Gate Driver with Integrated Ultra-Accurate and Fast Gate Charge Sensor for Robust and Ultra-Fast Short Circuit Detection of SiC power modules. 2023 IEEE 35th International Symposium on Power Semiconductor Devices and ICs (IEEE ISPSD), Hong Kong University of Science and Technology (HKUST), May 2023, Hong Kong, France. pp.68-71, 10.1109/ispsd57135.2023.10147567 . hal-04132615

HAL Id: hal-04132615

<https://hal.science/hal-04132615>

Submitted on 19 Jun 2023

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

CMOS Gate Driver with Integrated Ultra-Accurate and Fast Gate Charge Sensor for Robust and Ultra-Fast Short Circuit Detection of SiC power modules

Anas El Boubkari
NXP SEMICONDUCTORS,
LAPLACE, Université de Toulouse,
CNRS, INPT, UPS
Toulouse, France
anas.elboubkari_2@nxp.com

Nicolas Rouger, Frédéric Richardeau,
Marc Cousineau
LAPLACE, Université de Toulouse,
CNRS, INPT, UPS
Toulouse, France
nicolas.rouger@laplace.univ-tlse.fr,
richard@laplace.univ-tlse.fr,
cousineau@laplace.univ-tlse.fr

Thierry Sicard, Pierre Calmes,
Matthew Bacchi
NXP SEMICONDUCTORS
Toulouse, France
thsicard5@gmail.com,
pierre.calmes@nxp.com,
matthew.bacchi@nxp.com

Abstract— This paper presents an innovative architecture for gate-drivers, offering new solutions to short-circuit issues commonly faced by SiC MOSFET power transistors. Due to their fast switching, SiC power devices require much faster short-circuit detection times than those used for Si MOSFET and IGBTs. A gate driver IC with an integrated ultra-fast and accurate gate current sensor for short-circuit detection is presented. First experimental results demonstrates a low gate current copy error (<1%) with a response time that does not exceed 40ns and a reliable fast short-circuit detection for power modules, within 370ns. This IC is fabricated using NXP Semiconductors' high-voltage SMARTMOS10 130nm CMOS SOI technology.

Keywords— SiC MOSFET; CMOS; Gate Driver; Current sensing; Short-Circuit; Detection

I. INTRODUCTION

As SiC MOSFETs have gained major interest in the silicon power devices market, gate drivers (GD) have a more challenging specification regarding SiC MOSFETs protection and short-circuit (SC) detection time (<1 μ s). There are various detection methods such as the improved desaturation method with an adaptive blanking time [1]. However, the method requires an external high-voltage diode which introduces cross-talk phenomena between the power circuit and the GD. Recent detection methods propose gate signals monitoring using the gate-source signal (V_{gs}) and the gate charge image (V_{Qg}) [2 - 4]. Nevertheless, V_{Qg} is not integrated in the GD which compromises the system's speed, accuracy and noise immunity. To overcome these issues, we propose a novel GD architecture generating internally an ultra-accurate and fast gate current copy (I_{gcopy}) with a response time shorter than 40ns used in a 2-dimensional (2D) SC detection method for Hard Switch Faults (HSF). Furthermore, this integrated current processing approach reinforces the GD's immunity, speed and robustness compared to a voltage processing approach using external discrete components.

II. BENEFITS AND CHALLENGES OF THE GATE CHARGE APPROACH FOR SHORT-CIRCUIT DETECTION

The presented 2D diagnosis short-circuit detection (Fig. 1) consists on monitoring low voltage signals. The primary signal is V_{Qg} that permits the system to distinguish SC events from normal operation modes. The HSF fault initiates before turning on the Low-Side SiC MOSFET. Unlike the cases for Active and Passive Normal Turn On (ANTO, PNTO), the HSF case shows an absence of Miller Plateau caused by the non-variation of the SiC MOSFET's drain-source voltage (V_{DS}), as shown in Fig. 1(b). Moreover, the SiC MOSFET's

V_{gs} and the gate current (I_g) time constant (τ) depends on the switching case, as illustrated in Fig. 2(a). These different case conditions highly impact the final gate charge value. In terms of quantitative comparison, the HSF has the lowest final gate charge value and the ANTO has the highest ($Q_{HSF} < Q_{PNTO} < Q_{ANTO}$). To evaluate the gate charge values at fixed conditions, a secondary trigger signal can be derived from either I_g or V_{gs} . These signals will be respectively compared to a current reference (I_{Ref}) or a voltage reference (V_{Ref}) to initiate the gate charge value examination. To increase the gate charge distinction between Q_{HSF} and Q_{ANTO} & Q_{PNTO} , I_{Ref} must be lower than the Miller Plateau current ($I_{gMiller}$) and V_{Ref} must be higher than the Miller Plateau voltage ($V_{gsMiller}$). These conditions help to avoid false short circuit detections.

When $I_g(t)$ reaches I_{Ref} (or alternatively, when $V_{gs}(t)$ reaches V_{Ref}) the system will examine $V_{Qg}(t)$. The SC flag transitions on the condition that the gate charge image reference (Q_{Ref}) is above the examined $V_{Qg}(t)$ otherwise it is considered a normal switching event, as mentioned in Fig. 2(b). In spite of the simplicity of this 2D SC detection method, it is necessary to have a fast and accurate gate charge estimation to establish rapid and robust system reaction.

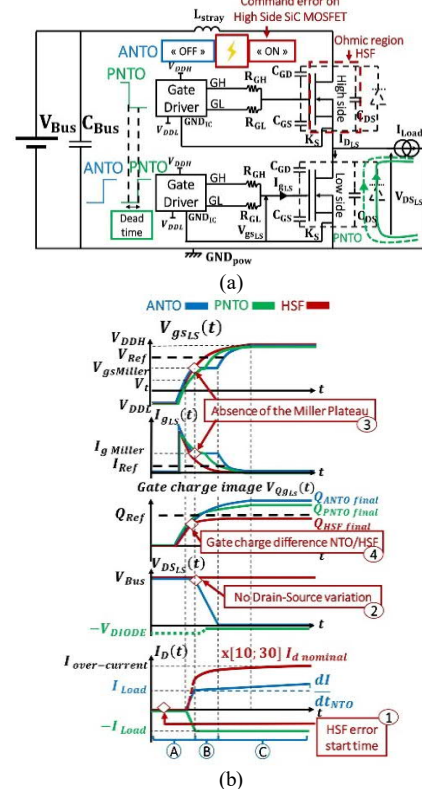


Fig. 1. (a) Half-Bridge circuit, (b) Qualitative Low-Side SiC MOSFET signals in ANTO, PNTO & HSF cases.

Switching cases	V_{gs} & I_g time constant (τ)			State
	A	B	C	
ANTO	$R_G \cdot C_{issmin}$	Miller Plateau	$R_G \cdot C_{issmax}$	When $V_{gs}(t)$ or $I_g(t)$ reaches V_{qref} (on the rising edge) or I_{qref} (on the falling edge) if $V_{qg}(t) > V_{qref}$
PNT0	$R_G \cdot C_{issmax}$			
HSF	$R_G \cdot C_{issmin}$			if $V_{qg}(t) < V_{qref}$

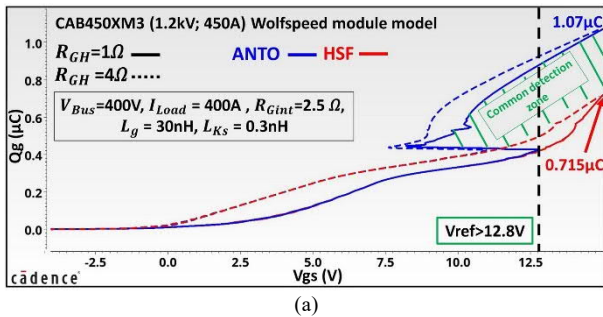
Fig. 2. (a) Time constant table relative to switching cases, (b) HSF diagnostic table.

A. Gate charge robustness

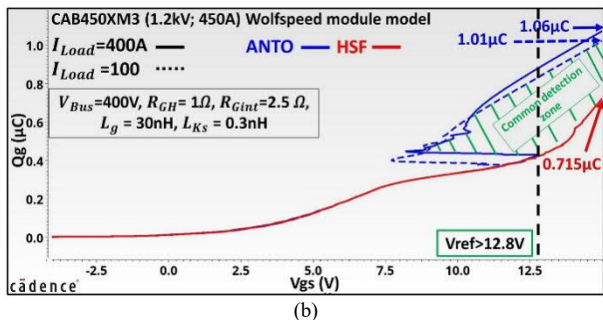
A short-circuit detection method must take into consideration the dispersion of all the parameters in a Half-Bridge circuit to ensure safe and robust SC detections. Unfortunately, these parameters are often neglected in the literature when it comes to proposing SC detection methods while they can potentially cause false detections. These parameters can be classified into two categories:

- The operating point parameters: external gate resistance (R_{GH}), internal gate resistance (R_{Gint}), bus voltage (V_{Bus}), current load (I_{Load})
- Parasitic inductances: gate stray inductance (L_g), common source stray inductances (L_{Ks})

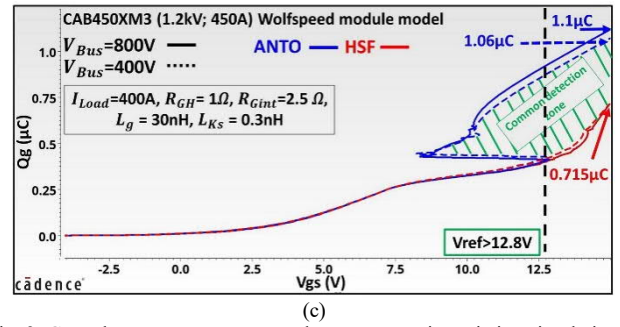
The operating point parameters are mainly determined by the application specification. On the other hand, the stray inductances can, but not always, be optimized accordingly. Fig. 3&4 shows the CadenceTM simulated gate charge signals versus the internal gate-source voltage using a CREE Wolfspeed SiC MOSFET module model (CAB450XM3, 1.2kV, 450A) while varying the operating point and the stray inductances parameters. Simulations demonstrate the high selectivity of the common detection zone (dashed in green). These results confirm the robustness of the gate charge approach and the necessity of an adjustable V_{Ref} to avoid false short-circuit detections. The SiC MOSFET's internal elements (such as R_{Gint} and L_g , illustrated in Fig. 6) will complicate the thresholding on V_{gs} (as demonstrated in Fig. 5) and therefore the interest of using the gate current as a trigger signal that will give us a more reliable information on the SiC MOSFET's input capacitance's state.



(a)

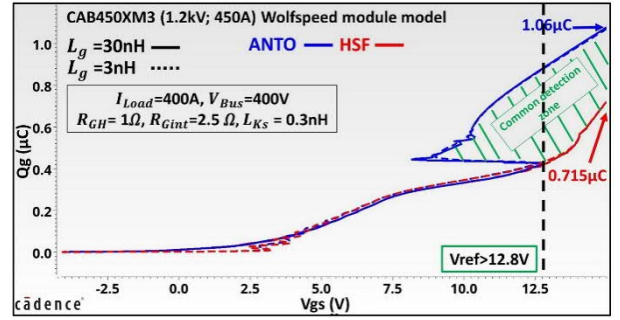


(b)

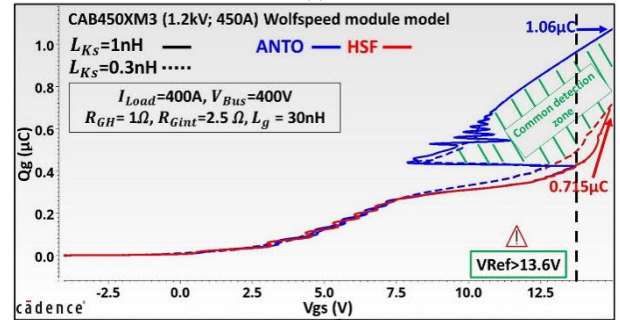


(c)

Fig. 3. Gate charge vs gate-source voltage parametric variation simulation of the operating point, (a) R_{GH} variation, (b) I_{Load} variation, (c) V_{Bus} variation.



(a)



(b)

Fig. 4. Gate charge (Q_g) vs gate-source voltage parametric variation simulation of the stray inductances, (a) L_g variation, (b) L_{Ks} variation.

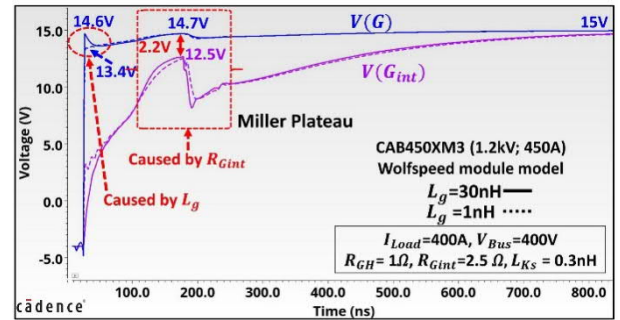


Fig. 5. External and internal gate voltage parametric variation simulation.

III. NOVEL GATE DRIVER ARCHITECTURE WITH AN ACCURATE, FAST AND INTEGRATED GATE CHARGE ESTIMATOR

A. Gate driver architecture

The proposed design aims to present a fast, stable and accurate copy of the gate current (with a possible 15A peak current within 40ns) before the beginning of the Miller Plateau and preserves its accuracy till the end of the gate charging. Due to the high voltage level at the output buffer (e.g. -4V/15V) the design uses both high and low voltage CMOS transistors. To clearly explain the concept behind this

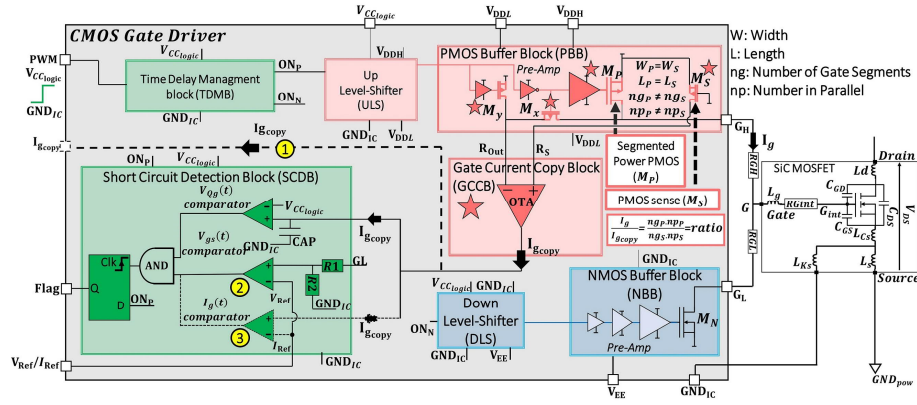


Fig. 6. Designed Gate Driver architecture,

(1) Variant evaluating I_{gcopy} , (2) Variant using $V_{QG} - V_{gs}$ for SC detection, (3) Variant using V_{QG} and I_g for SC detection.

accurate and fast I_{gcopy} , we will describe the block diagram of the proposed GD architecture presented in Fig. 6. Guaranteeing a reliable, accurate and ultra-fast sensing of the I_g current requires an on-chip current sensor consisting of an Operational Transconductance Amplifier (OTA) and a PMOS senseFET (M_s) that is matched with a segmented PMOS power switch (M_p). The SiC MOSFET power transistor is driven by the GD's output stage transistors M_p and M_n that are controlled by the Pulse Width Modulated (PWM) input signal. When PWM is high M_p is ON and M_n is OFF and reciprocally. During the SiC gate charging phase (PWM is high), the current sensor senses and generates internally a ratioed copy of I_g (I_{gcopy}). A high voltage transistor (M_x) is used to isolate the gate current copy system from the PMOS's high voltage output. To ensure an accurate current copy, M_p and M_s present the same source to gate voltage (V_{sg}), with M_s always turned ON. The OTA and the state of the switching transistors M_x and M_y will guarantee the same drain voltage for M_p and M_s . The transistors M_p and M_x are controlled by the same signal unlike M_y which is controlled by the complementary one. When M_p is ON, M_x is also ON ensuring that the potential $V(GH)$ is connected to the potential $V(Rout)$ and subsequently the OTA will make sure that the potential $V(Rs)$ is following $V(Rout)$. Transistors M_p , M_s , M_x and M_y are matched by width and length. The current copy ratio I_{gcopy}/I_g is determined by the ratio $(ng_p \times np_p)/(ng_s \times np_s)$, with ng_x the number of gate segment of an elementary transistor and np_x the number of transistors connected in parallel. M_y is used to set $V(Rout)$ and $V(Rs)$ at the same potential and to eliminate offsets when PWM is low. I_{gcopy} will be integrated internally in the Short Circuit Detection Block (SCDB) to generate an accurate gate charge estimation of the SiC MOSFET. This precise information will be interpreted with a downscaled SiC MOSFET's gate to source voltage or I_{gcopy} to detect the short circuit type I (HSF).

B. Current sensor functionality validation

A dedicated IC pin (number 1, circled in yellow Fig. 6) of the designed GD (packaged in SOIC-14 and soldered on a designed Evaluation Board, Fig. 7) is used to validate the accuracy and the speed of the current sensor. For this first validation phase, a fixed 50nF capacitive load (C_L) is used in place of the SiC MOSFET's input capacitance (C_{iss}). Fig. 8(a) shows the experimental result of the superimposed I_{gcopy} generated internally by the GD and the I_g measured externally by a 1 GHz optical probe (voltage drop across the external

gate resistor R_{GH}). I_{gcopy} 's response time is equal to 34ns and the error is negligible (<1%) after this initial delay correlating with simulation results presented in Fig. 8(b). This validates the reliability of the gate charge estimation.

In simulation, we ensured I_{gcopy} functionality's robustness over PVT (Process, Voltage and Temperature) variations thanks to the exhaustive tools available at NXP Semiconductors.

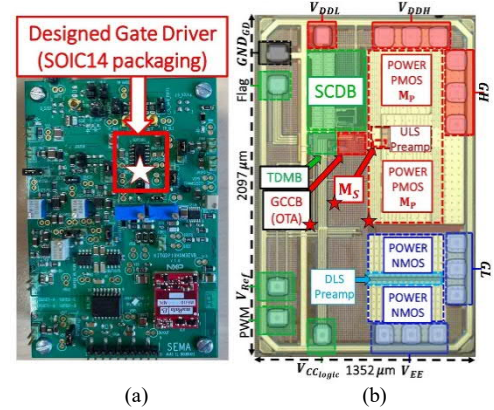


Fig. 7. (a) Gate Driver Evaluation Board (EVB), (b) Gate Driver bare die microscopic photo (version using V_{QG} and V_{gs} for SC detection, 2097 μm x 1352 μm).

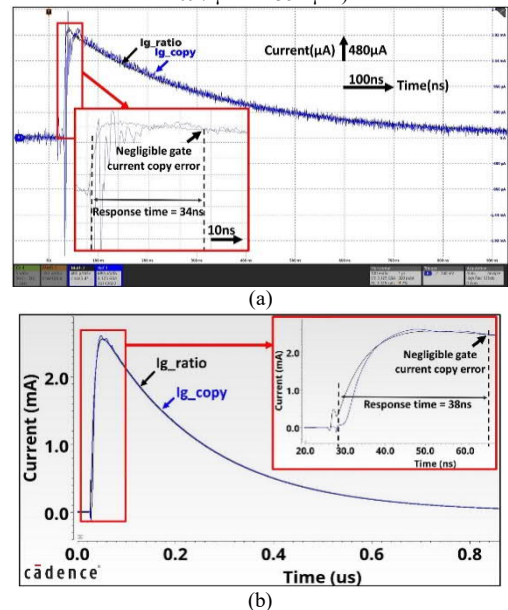


Fig. 8. (a) Experiment, (b) Simulation
Superimposed results of the I_{gcopy}/I_g ratio: $V_{DDH}=15\text{V}$, $V_{DDL}=10\text{V}$, $V_{CClog1c}=1.5\text{V}$, $V_{EE}=-4\text{V}$, $R_{GH}=5.4\Omega$, $R_{GL}=1\Omega$, $C_L=50\text{nF}$.

IV. 2-D SHORT-CIRCUIT DETECTION FUNCTIONALITY VALIDATION USING A SiC HALF-BRIDGE MODULE

To validate the concept and the robustness of the short-circuit detection block the second IC pin (number 2, circled in yellow Fig. 6) is measured on the EVB_{designed} connected to a SiC Half-Bridge power module (CAB450XM3: 1200V, 450A) driven by a CREE Wolfspeed Double Pulse Test kit (KIT-CRD-CIL12N-XM3), as shown in Fig. 9. Fig. 10(a) shows a normal switching event (Double Pulse Test), without any SC detection (flag stays low). The High-Side SiC MOSFET is driven at -4V for V_{GS} , representing a typical hard switching test for the transistor and its body diode. For the case of a HSF SC event, the High-Side SiC MOSFET is driven at a constant voltage +18V for V_{GS} with an external isolated power supply. For both experiments, the Low-Side SiC MOSFET is also driven by the designed CMOS GD. Under HSF, Fig. 10(b). shows a detection time of 369ns (flag is high), corresponding to a SC SiC drain current of 1.2kA at the detection time which is much lower than the channel saturation current ($>7kA$). This guarantees a fast SC protection compared to the 450A nominal rated current of the SiC MOSFET power module. For safety reasons, the DC bus voltage is reduced in the experiments to 150V and V_{DDH} to 12V without limiting the circuit validation. The detection flag is not looped back and the PWM signal is intended to be cleared after the rising of the flag. The soft shut down is realized by the integrated NMOS (Mn) at the CMOS GD's output stage, driven by the FPGA which generates the PWM signal. These results demonstrate the speed of the SC-detection method without the need of an external DSAT high voltage diode, using an integrated and accurate I_{gcopy} and gate charge sensing method, which is inherently robust.

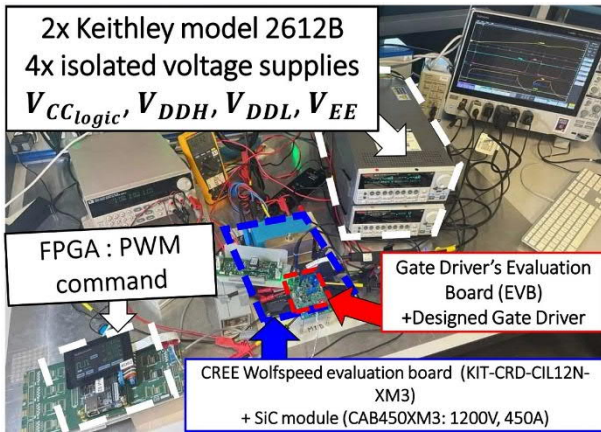
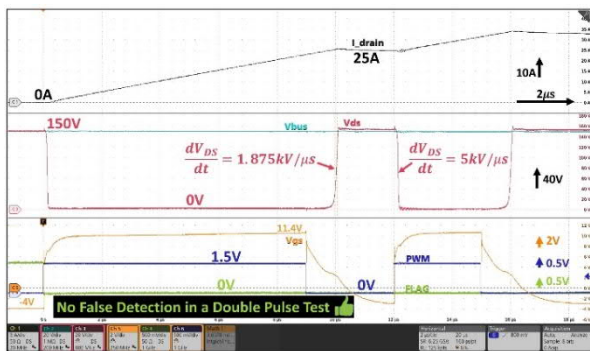
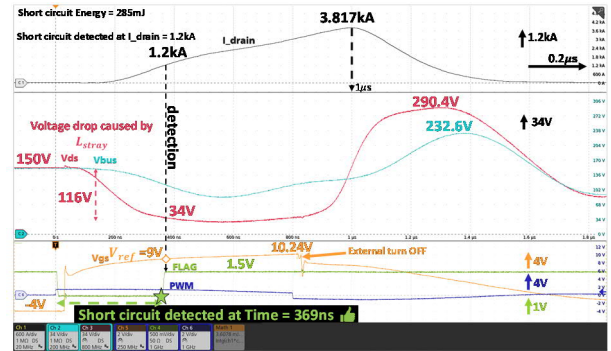


Fig. 9. Double Pulse Test and HSF Test bench.



(a)



(b)

Fig. 10. CREE SiC module experiments(CAB450XM3: 1.2kV, 450A), (a) ANTO, (b) HSF. $V_{Bus} = 150V$, $R_{GH} = 1\Omega$, $R_{GL} = 12\Omega$, $V_{Ref} = 9V$, $V_{DDH} = 12V$, $V_{DDL} = 10V$, $V_{CClogic} = 1.5V$.

V. CONCLUSION & FUTURE WORK

An integrated gate charge estimator, which is the ideal candidate for a fully integrated solution for Hard Switch Fault event detection is presented. This robust and time independent technique estimates the external SiC MOSFET gate charge at a specific trigger point. The integrated current sensor has been validated both by simulations and silicon measurements, showing a fast transient response (34ns) and a high accuracy (error $<1\%$). The on-chip gate charge estimator and SC detection system is validated while driving an automotive 1200V 450A SiC power module: the SC detection time is 369ns without any extra external components, limiting the SC current to less than three times the rated nominal current, finally avoiding the use of a dedicated and costly sense-FET-current SiC die. The CMOS circuit has been also validated under normal switching conditions, showing no false detection.

This proposed system can be further extended to the detection of the Fault Under Load (FUL) [5] short-circuit, giving the GD the advantage of being fully independent and qualified to ensure the protection of both High and Low-Side SiC MOSFETs in a half bridge power module.

ACKNOWLEDGMENT

The authors would like to thank NXP Semiconductors and LAPLACE laboratory for generously providing the technical guidance, fabrication resources and support to carry out the study.

REFERENCES

- [1] Jiawei Li, Cheng Qian, Zhiqiang (Jack) Wang, Yong Kang, "An Improved Desaturation Protection Method with Self-Adaptive Blanking-Time for Silicon Carbide (SiC) Power MOSFETs," 2021 IEEE (WiPDA) Asia.
- [2] Y. Barazi, N. Rouger and F. Richardeau, "CMOS Gate Driver with fast short circuit protection for SiC MOSFETs," 2020 32nd International Symposium on Power Semiconductor Devices and ICs (ISPSD), Vienna, Austria, 2020, pp. 94-97, doi: 10.1109/ISPSD46842.2020.9170164.
- [3] Shinya Yano, Yusuke Nakamatsu, Takeshi Horiguchi and Shinnosuke Soda, "Development and Verification of Protection Circuit for Hard Switching Fault of SiC MOSFET by Using Gate-Source Voltage and Gate Charge," 2019 IEEE (ECCE), United States.
- [4] Y. Barazi, F. Richardeau, N. Rouger and J.-M. Blaquiere, "Robustness study of a fast protection method based on the gate-charge dedicated for SiC MOSFETs power device," Microelectronics Reliability, Elsevier, 2021, pp.114246.
- [5] Eric Velander et al., "Analysis of Short Circuit type II and III of High Voltage SiC MOSFETs with Fast Current Source Gate Drive Principle", 2016 IEEE IPEMC-ECCE, Asia.