



HAL
open science

Fuse on PiN Silicon Diode Monolithic Integration for New Fail-Safe Power Converters Topologies

Amirouche Oumaziz, Frédéric Richardeau, Abdelhakim Bourennane,
Emmanuel Sarraute, Éric Imbernon, Ayad Ghannam

► To cite this version:

Amirouche Oumaziz, Frédéric Richardeau, Abdelhakim Bourennane, Emmanuel Sarraute, Éric Imbernon, et al.. Fuse on PiN Silicon Diode Monolithic Integration for New Fail-Safe Power Converters Topologies. *ELECTRIMACS 2022*, 993, Springer International Publishing, pp.289-303, 2023, Lecture Notes in Electrical Engineering, 978-3-031-24836-8. 10.1007/978-3-031-24837-5_22. hal-04132175v2

HAL Id: hal-04132175

<https://hal.science/hal-04132175v2>

Submitted on 18 Jun 2023

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Fuse on PiN silicon diode monolithic integration for new fail-safe power converters topologies

Amirouche Oumaziz^(1,2,3) · Frédéric Richardeau^(1,3) · Abdelhakim Bourennane⁽²⁾ · Emmanuel Sarraute^(1,3) · Eric Imbernon⁽²⁾ · Ayad Ghannam⁽⁴⁾

Abstract In this paper, a first concept of monolithic integration of a fuse on a silicon PiN diode is realized and experimentally characterized. An integrated fuse on PiN diode allows fast cut-off, with low I^2T (less than $2 \text{ A}^2\text{s}$) and short pre-arcing times (4 to 6 μs). These fuse-on-diode components are intended for fail-safe topologies power converter, aiming for more compact and reliable applications. The fuses were electrothermally designed using Comsol Multiphysics™ and TCAD Sentaurus™ simulations were carried out to study their integration on PiN diodes. Characterization and experimental tests were carried out after components realization.

1 Introduction

Fuses are simple, passive and inexpensive components, able to isolate faulty circuits paths in case of excessive current flow due to a failure. They allow in some fault-tolerant power converters topologies [1]–[3] to avoid spreading failure by separating failed circuit parts, thus enabling the continuous operation of the system. In Fig. 1 [4] a representation of a fault-tolerant topology is presented.

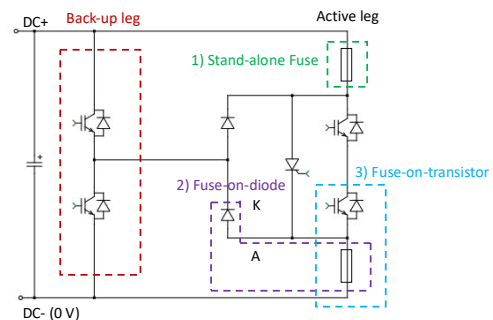


Fig. 1 Fail-safe topology based on dual-fuse (high-side and low-side fuse) and a crowbar switch (thyristor), with a back-up leg [4].

In case of internal short-circuit occurrence, the faulty leg is disconnected using the dual-fuse and the auxiliary crowbar switch, then a back-up leg (Fig. 1, red dashed box) is spontaneously connected, allowing continuity of operation. In order to improve the systems reliability and compactness, the used fuses could be integrated monolithically on power semiconductor [5], [6] components (IGBTs, MOSFETs, etc), as presented in Fig. 1 (Fuse-on-transistor, blue dashed box). The integration of the fuses on power the semiconductor component is carried out in two steps. First, fuses, called “Stand-alone fuses” (Fig. 1, green dashed box), made of thin copper layer (18 μm) electrodeposited on a silicon substrate have been realized in order to study the thermal and electrical behaviour of the components.

A. Oumaziz^{1,2,3} · F. Richardeau^{1,3} · A. Bourennane² · E. Sarraute^{1,3} · E. Imbernon² · A. Ghannam⁴

E-mail: frederic.richardeau@laplace.univ-tlse.fr

¹ University of Toulouse, INP, UPS, LAPLACE ENSEIHT, France

² LAAS-CNRS, University of Toulouse, CNRS, UPS

³ CNRS, LAPLACE, F-31071 Toulouse, France

2 rue Camichel, BP 7122, F-31071 Toulouse cedex 7, France

⁴ 3DiS Technologies, Miniparc, 478 rue de la découverte, 31670 Labège, France.

Table 1 : Summary of the fuse designs integration characteristics, advantages and drawbacks

Design Comparatives	Stand-alone Fuse	Fuse-on-diode	Fuse-on-transistor
Purpose of use and flexibility	Modular, could be placed in any part of the circuit Maximum protection Non-intrusive regarding the components	Fuse could be integrated either on anode or cathode side Fuse/component thermomechanical interaction during the arcing process	Fuse could be integrated only on the source side. The Drain side will require a Stand-alone fuse Fuse/component thermomechanical interaction during the arcing process
Integration issues	Easy	Medium	Complex
Lifetime	Expanded lifetime, thanks to the fuse integration	Diodes dissipate less power, so the lifetime could be expanded	More constraints, because transistors dissipate more power
Parasitic	+++ (more parasitic inductance)	+	+
Occupied area in the circuit	+++	++	+ (most compact)

Finite elements simulations using Comsol™ were carried out and experimental results allowed to validate the on-state operation of the components. Fast cut-off fuses with very low pre-arcing times (4 to 6 μ s) under 200 V_{DC} bus voltage have been reported, with low leakage currents ensuring high post-arc isolating resistance (up to 8 M Ω) [7], [8]. Then, the fuses were integrated on silicon PiN diodes (Fig. 1, Fuse-on-diode, purple dashed box), which is the work presented in this paper.

Table 1 gives a comparative overview between the monolithic fuse integration solutions, where several parameters are reported and compared.

The clean room process based on electrolytic growth of copper, provides micrometer resolution, which is better than classical fuses, resulting in less dispersive I²T values. In a previous work [8], the phase-leg dual-fuse function has been investigated in order to study the “Stand-alone” fuses symmetrical operation during a short-circuit. The characterization results showed well balanced post-arc voltages distribution between low-side and high-side fuses.

The paper is organized as follows: first, the 3D structure of the “Fuse-on-diode” components, thermal and electrical requirements used to design the components are discussed in section 2. Section 3 is dedicated to the monolithic integration of the fuses on silicon PiN diodes. To that end, TCAD Sentaurus™ simulations were carried out to study this integration in different cases. In section 4, the components realization detailing the main technological process steps is presented. Section 5 is devoted to experimental and characterization results.

2 Components design procedure

2.1. Fuse characteristics and design

The “Stand-alone” fuses [7] (Fig. 2) are made of a thin layer of copper (18 μ m) to form the fuses constrictions and pads, electrodeposited on an insulated silicon wafer (500 μ m), using a thin nitride (200 nm) layer to prevent leakage currents once the constrictions are evaporated. The fuses constrictions are deposited on an insulating epoxy layer (25 μ m). The purpose of this epoxy, with its low thermal conductivity (1.16 W.m⁻¹.K⁻¹), is to provide a thermal insulation to the constrictions from the substrate (high thermal conductivity: ~130 W.m⁻¹.K⁻¹) and concentrate the thermal energy during a short-circuit occurrence on this constrained area, thus improving the cut-off process. The epoxy

layer also provides a mechanical protection to the substrate or the active area below during the cut-off process. Its thickness has been improved through simulations using Comsol Multiphysics™, where 25 μ m thickness is enough to induce a thermal decoupling between the constrictions and the silicon substrate.

The fuses have been designed for 10 A nominal current, allowing a maximum temperature of 115 °C at the constrictions center, while operating at an ambient temperature of 85 °C.

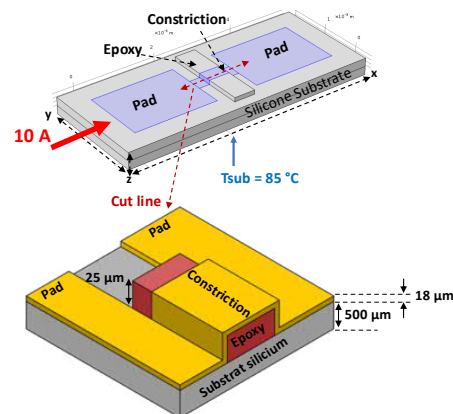


Fig. 2 Stand-alone fuse designed by the authors and presented in [7] with a cutline along the constriction.

In the previous work [7], four prototypes of the “Stand-alone” fuses were designed, according to the number of the constrictions number and configurations (series/parallel). Table 2 summarizes the main electrical and geometrical parameters obtained from the electrothermal simulations based on Comsol™. When a short-circuit occurs, the fuse’s current increases through the circuit’s stray inductance to reach a maximum value, in a time duration called Tp (pre-arcing time), that results in fuse melting. The required normalized energy to evaporate the fuse constrictions is defined by the I²T ([A².s]) parameter.

Table 2 Comparison between designed stand-alone fuses prototypes

Design	I ² Tp (A ² .s)		Tp (μ s)	Area (mm ²)
	Theo.	Exp.		
Ns=Np=1	1.53	1.93	4.9	2.52
Ns=1 Np=2	1.45	1.71	2.8	1.84
Ns=2 Np=1	1.01	0.7	3.1	2.95
Ns=Np=2	0.47	0.55	1.9	1.46

Ns: number of constrictions in series. Np: number of constrictions in parallel. $[I^2Tp]$: normalized energy to evaporate fuse. Tp: pre-arcing time.

From Table 2, we can notice that the fuses I^2Tp parameter are very low and the difference between the theoretical and experimental values is very acceptable and some assumptions explaining the origin of this difference are explained in a previous work [7]. The pre-arcing times (Tp) are very short, making the fuses very fast in case of a short circuit occurrence. It has also been shown in [8] a reduction in the area of the fuse by a ration ratio of about five, and therefore in its compactness, as compared to the best commercially available SMD fuses.

2.2. Fuse-on-Diode design approach

Once the “Stand-alone fuses” operation is validated, the technological process has been integrated within a vertical PiN silicon diode. Fig. 3 shows a 2D representation of the “Fuse-on-diode” integration.

Thanks to this PiN diode vertical architecture and its top-side aluminum electrode (anode here), the lateral fuse is realized through several materials depositions. One of the fuse’s pads is the diode’s electrode (anode), the second one must be fully isolated from the P⁺ region to withstand the full voltage after constrictions evaporation, therefore, avoiding leakage current flow between the pads. The electrical insulation is achieved using a thin nitride layer with optimized thickness. The pads thickness is about 43 μm . After depositing a first layer of copper (18 μm) to form the pads and the constrictions, the pads are thickened by compensating the epoxy thickness (25 μm) to obtain planar layers which is easier to make technologically.

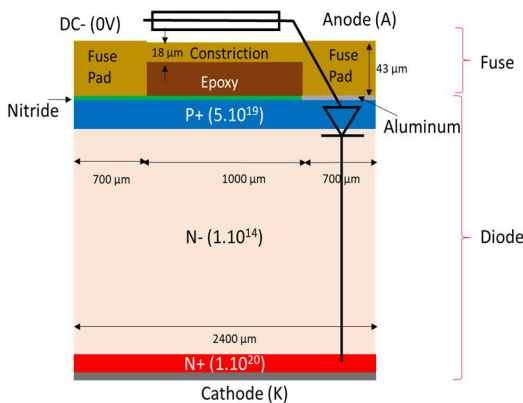


Fig. 3 First fuse-on-diode design approach.

3 Simulations results

according to the circuit’s operating modes presented in Fig. 1, the “Fuse-on-diode” could be in three different states, either the fuse is conducting or not, the diode could be in off or on-state. Using 2D TCAD Sentaurus™ simulations, the different operating states have been studied in order to validate the feasibility of this integration. The PiN diode physical and geometrical parameters were those imposed by the IGBT process of the LAAS-CNRS micro and nanotechnology platform [9]. In these simulations, the Junction Termination Extension (JTE) has not been included since the process has already been validated during a previous work through several simulations and experiments [12].

3.1. Case 1- fuse conductive and diode off-state

The most common case deals with the fuse conducting the nominal current through the active leg (Fig. 1), while the back-up leg is in off-state. The auxiliary diode leg used during the back-up operation is as well in off-state, since no fault has occurred. Fig. 4 shows the simulated circuit to validate this case.

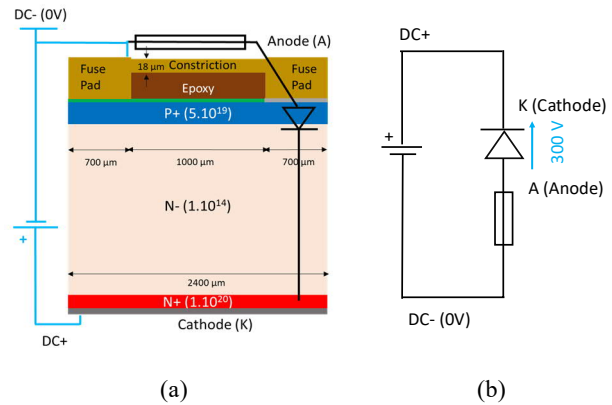


Fig. 4 Simulated circuit for case 1: Fuse is in on-state and diode in off-state.

Fig. 5 presents the electrostatic potential and the electric field distributions when 300 V_{DC} were applied at the DC+ bus.

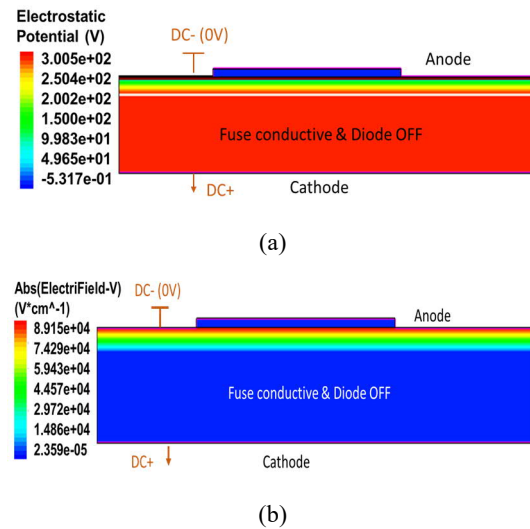


Fig. 5 Electrostatic potential (a) and electric field distribution (b) for case 1 (fuse normally on-state and diode off-state) where a DC bus voltage of 300 V is applied on the diode’s cathode.

In this case, the simulations allowed to validate that reverse biased diode sustains the rated DC voltage (300 V, Fig. 5.a) with low leakage currents (8.5 μA). The simulated structure shows an electric field distribution around $8.9 \cdot 10^4$ V/cm (Fig. 5.b), for the rated voltage (300 V_{DC}), which is under the silicon critical electric field ($\sim 2 \cdot 10^5$ V/cm).

3.2. Case 2- fuse open and diode on-state

In case of a short-circuit occurrence, the fuse’s current increases, therefore, the constrictions evaporated when the required melting energy is reached (I^2Tp). In this case, the diode could be in on-state

with the back-up leg. Fig. 6 shows the simulated circuit used to validate the components operation in this case.

The current density lines distribution when the diode is in on-state conducting 100 A/cm² current density is presented in Fig. 7.

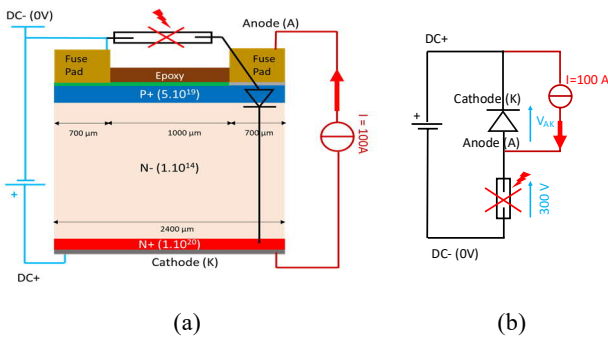


Fig. 6 Simulated circuit for case 2: Fuse open and diode in on-state.

Fig. 7.a shows a current density mostly focused on the diode section (right side), with a voltage drop of 0,78 V (Fig. 7.b). Once the constrictions are evaporated and the diode is in on-state, the fuse pads sustain the rated voltage (300 V_{DC}) thanks to the insulating nitride layer, ensuring negligible leakage current (~9 nA). Given the nitride breakdown voltage (~10 MV/cm) and the components rated voltage (300 V), 350 nm nitride thickness has been designed using TCAD Sentaurus™ simulations.

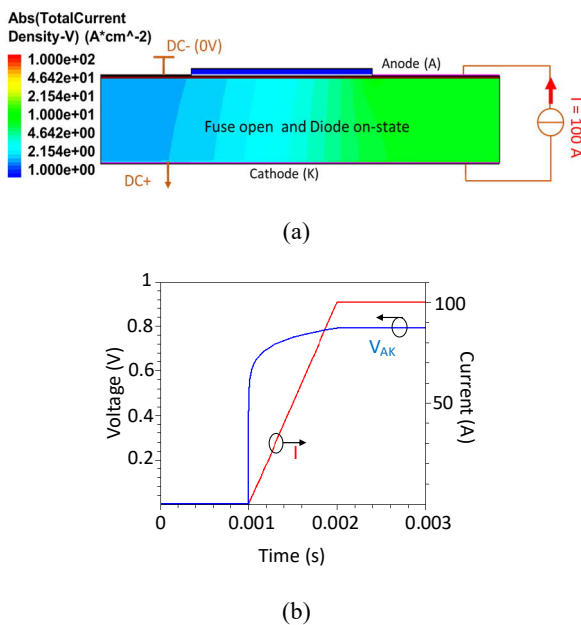


Fig. 7 Current density distribution (a) and diode's on-state voltage drop while conducting 100 A/cm² (b) for case 2 (fuse open and diode on-state).

3.3. Case 3- fuse open and diode off-state

The last studied case takes into account a blown-up fuse and the diode in off-state, because the back-up leg's high-side RC-IGBT is in on-state. In this case, the diode is reverse biased and supports few volts (simulated with 5 V_{DC}) due to the thyristor and IGBT on-state voltage drops, while the fuse supports almost the DC bus voltage (295 V_{DC}).

Fig. 8 shows the simulated electrical circuit for this case, where the fuse is open and the diode is in off-state. The simulations results presenting the simulated structure current density and electric field distribution are shown in Fig. 9.

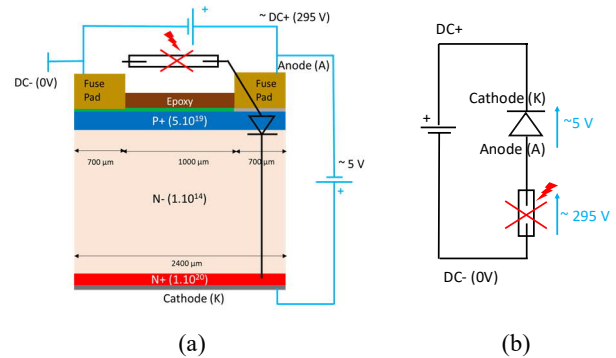


Fig. 8 Simulated circuit for case 3: Fuse open and diode in off-state.

The leakage currents (Fig. 9) are mostly concentrated around the pads, but in steady state, very small values have been reported (~1μA) between the pads. The electric field is higher around the nitride (Fig. 9.b-c) sustaining the rated voltage between the pads, but still lower (8.55.10⁶ V/cm) than the breakdown value (~10 MV/cm).

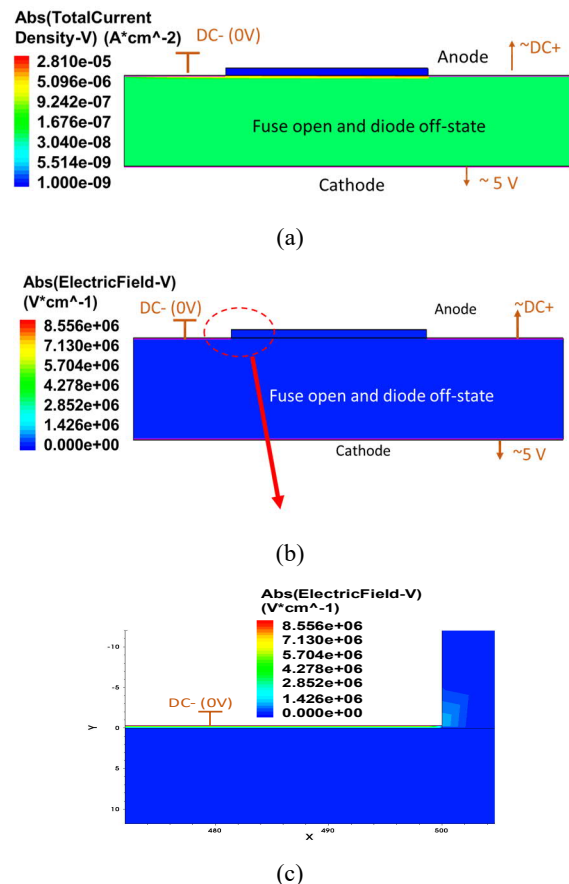


Fig. 9 Current density (a) and electric field distribution (b-c) for case 3 (fuse open and diode off-state) where a DC bus voltage of 300 V is applied.

Fig. 10.a and Fig. 10.b show respectively the current density and lattice temperature distributions when the constrictions are

evaporated. The boundary conditions consider a back-side temperature applied to the diode's cathode of 85 °C. Thus, simulated component's temperature evolves following the physical models, which are temperature dependent.

As presented in Fig. 3, the designed component comprises an anode contact covering partially the front side P⁺ region. This geometrical disposition causes a non-uniform current density distribution (Fig. 10.a), concentrated at the diode side (right side). As a consequence, the component shows a slightly higher temperature (Fig. 10.b) and mostly focused in the components front-side, where the current density is higher.

On-going study focuses the work on an improved design where the front side P⁺ region could be fully exploited in order to obtain a homogenous current density distribution and thus improve components cooling.

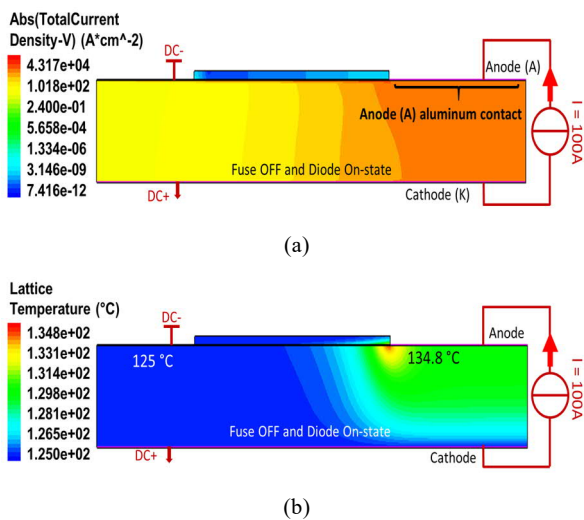


Fig. 10 Current density distribution (a) and lattice temperature distribution (b) when the constrictions are evaporated and the diode is conducting 100 A.

The component realization comprises two technological processes. First, the diode is realized using the LAAS-CNRS micro and nanotechnology platform. Then the fuse is realized by the company 3DiS technologiesTM [10].

4 Experiments and results

In order to validate the components operation under a short circuit occurrence, the electrical test circuit presented in Fig. 11 has been used. It is composed of a current-limited voltage source, four parallel capacitors of 470 μ F each and crowbar thyristor, used to induce a short-circuit. A 700 nH snubber inductance is added in order to limit the energy and the current variation (di/dt), avoiding the damaging of the thyristor. A freewheeling diode is added in parallel with the inductance. The diode prevents the fuse from having to dissipate all the energy stored in the snubber inductance. Only the energy stored in the stray inductance (\sim 50 nH) will be dissipated in the fuse as in a real switching cell.

Once the thyristor is triggered, the stored energy in the capacitors is partially discharged through the fuse, causing the fuse voltage and current to increase until the required constrictions melting

point energy is reached. The initiated electrical arc persists until the current reaches zero. No current restrike should be observed.

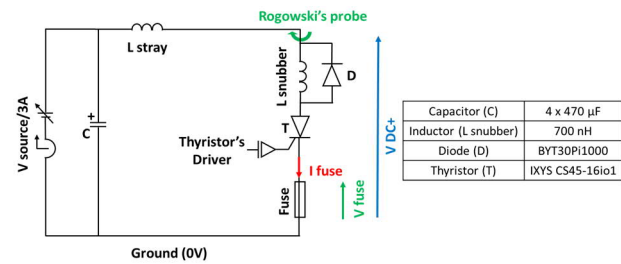
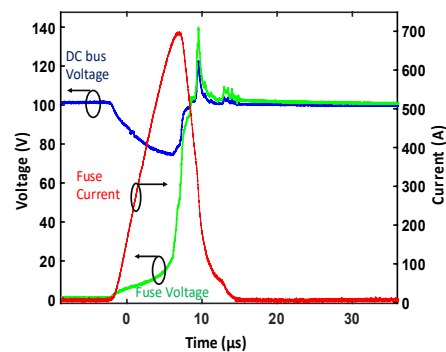


Fig. 11 Electrical test circuit used to validate the operation of the components.

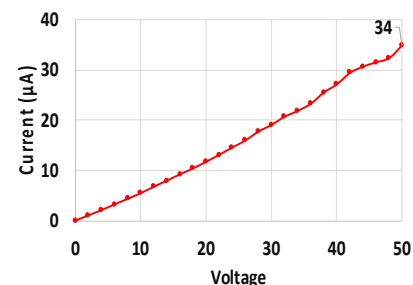
4.1. Cut-off tests

Several cut-off tests have been conducted on the realized components during a short-circuit occurrence using the presented electrical test circuit (Fig. 11). Fig. 12 shows some test results on a "Fuse-on-diode" component under a DC bus voltage of 100 V_{DC}.

When the short-circuit is initiated, the fuse current and voltage increase (Fig. 12.a) to reach a maximum value, corresponding to the moment when the constrictions melting energy is reached, this after a pre-arcing time of \sim 7 μ s. Once the current is cancelled, no current restrike was observed. The associated leakage current is very low (Fig. 12.b), about 35 μ A, leaving a very high post-arc isolation resistance (\sim 3 M Ω).



(a)



(b)

Fig. 12 Electrical cut-off test results (a) with the associated leakage current (b).

Fig. 13 shows a three parallel constriction "Fuse-on-diode" component before cut-off test (Fig. 13.a) and the distribution of the constraints around the constrictions right after the cut-off test (Fig. 13.b), where the released particles are trapped in the passivating silicone gel. The results (Fig. 13.b) may suggest a good current distribution over the three constrictions, thanks to a well-managed technological process.

Using an impedance analyzer (HP4294A), the parasitic inductance (ESL) brought by the integration of the fuse on this silicon PiN diode has been estimated. A measured value of 2.23 nH has been reported, which is very acceptable.

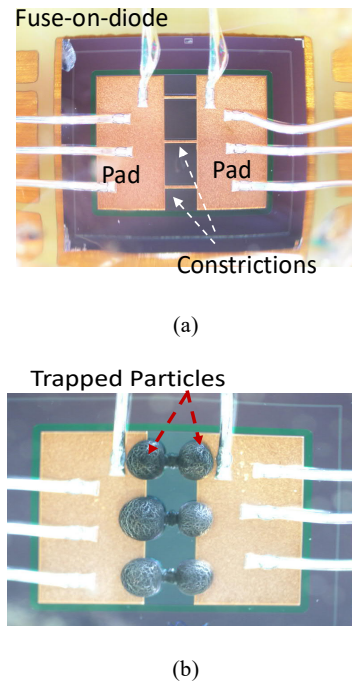


Fig. 13 Pictures of the component before (a) and after (b) the cut-off test encapsulated in a silicone gel.

Unfortunately, this 100 V_{DC} was the maximum cut-off voltage obtained with these components. On-going components analysis suggest that the insulating nitride layer has to be optimized to sustain higher breakdown voltages. Rugosity of the deposited aluminum to form the diodes electrodes impacts the nitride layer thickness and causes non-uniform deposition, which weakens the nitride at some points.

5 Conclusion

In this paper, a new concept of vertical PiN diodes integrating monolithically lateral fuses are realized and experimentally tested. The devices are able to perform very fast cut-off ($\sim 7 \mu\text{s}$) under a DC bus voltage of 100 V_{DC}, with very low I²T energies (1.35-1.55 A².s). The insulating post-arc resistances are very high ($\sim 3 \text{ M}\Omega$) ensuring very low leakage currents. The passivating silicone gel improved the cut-off by absorbing the excess of energy and avoiding its spreading towards the pads, thus avoiding any damage. Although, the cut-off voltage needs to be improved in order to cut-off higher voltages (around 200 V_{DC}) and fit commercial required applications. These good results suggest that

design of more compact and reliable power converters combining these integrated fuses is possible. Future work will focus on the improvement of the components to support higher voltages and study their monolithic integration on power semiconductor transistors (IGBT, MOSFETs, etc).

Acknowledgements Thanks to Céline Combettes and Vincent Bley for their participation in the fuses passivation process using the 3DPhi platform.

References

- [1] W. Zhang, D. Xu, P. N. Enjeti, H. Li, J. T. Hawke, and H. S. Krishnamoorthy, "Survey on fault-tolerant techniques for power electronic converters," *IEEE Transactions on Power Electronics*, vol. 29, no. 12, pp. 6319–6331, 2014, doi: 10.1109/TPEL.2014.2304561.
- [2] M. Gleissner and M. M. Bakran, "Fault-tolerant B6-B4 inverter reconfiguration with fuses and ideal short-on failure IGBT modules," *PCIM Europe 2016; International Exhibition and Conference for Power Electronics, Intelligent Motion, Renewable Energy and Energy Management*, no. May, pp. 683–690, 2016.
- [3] F. Richardeau, Z. Dou, J. M. Blaquiere, E. Sarraute, D. Flumian, and F. Mosser, "Complete short-circuit failure mode properties and comparison based on IGBT standard packaging. Application to new fault-tolerant inverter and interleaved chopper with reduced parts count," *Proceedings of the 2011 14th European Conference on Power Electronics and Applications, EPE 2011*, pp. 1–9, 2011.
- [4] Z. Dou, "Sûreté de fonctionnement des convertisseurs. Nouvelles structures de redondances pour onduleurs sécurisés à tolérance de pannes," Ph.D Dissertation, Toulouse INP, University of Toulouse, 2011.
- [5] S. E. Berberich, M. März, A. J. Bauer, S. K. Beuer, and H. Ryssel, "Active fuse," *Proceedings of the International Symposium on Power Semiconductor Devices and ICs*, vol. 2006, pp. 0–3, 2006, doi: 10.1109/ispsd.2006.1666088.
- [6] J. vom Dorp, S. E. Berberich, A. J. Bauer, and H. Ryssel, "DC-arc behavior of a novel active fuse," *ESSDERC 2008 - Proceedings of the 38th European Solid-State Device Research Conference*, pp. 67–70, 2008, doi: 10.1109/ESSDERC.2008.4681700.
- [7] A. Oumaziz *et al.*, "Fast cut-off, low I²T and high temperature monolithic on-chip fuse on silicon substrate for new fail-safe embedded power switch," *Microelectronics Reliability*, p. 114240, Oct. 2021, doi: 10.1016/j.microrel.2021.114240.
- [8] A. Oumaziz, Amirouche, Sarraute, Emmanuel, Richardeau, Frédéric, Bourennane, "Fail-safe switching-cells architectures based on monolithic on-chip fuse Keywords Fail-safe topologies using single-fuse or dual-fuse function," in *European Conference on Power Electronics and Applications (EPE 2020 ECCE Europe)*, 2020, p. 10.
- [9] É. Imbernon *et al.*, "International Semiconductor Conference (CAS'2001)," 2001. [Online]. Available: <https://hal.laas.fr/hal-01867591>
- [10] A. Ghannam, "3Dis technologies." <https://www.3dis-tech.com/>