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# Memory Window in Si:HfO<sub>2</sub> FeRAM arrays: Performance Improvement and Extrapolation at Advanced Nodes

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**Abstract**—The Memory Window (MW) of BEOL-integrated Si:HfO<sub>2</sub>-based 16kbit 1T1C FeRAM arrays is shown to be significantly improved ( $\times 3$ ) by etching the ferroelectric (FE) film of the Ferroelectric CAPacitor (FeCAP). To estimate the MW evolution in larger arrays at advanced technology nodes, a Preisach current-based compact model is developed, calibrated on measured FeCAP electrical characteristics and validated at various operating voltages. Electrical simulations of an elementary 1T1C 16kbit FeRAM array-like structure using Siemens Eldo show that scaling the transistor (1T) at advanced technology nodes can be beneficial for the MW. FE film thickness reduction below 10nm will also be requested for low voltage applications.

**Index Terms**—non-volatile memory, FeRAM, etched FeCAP, compact model, advanced technology nodes

## I. INTRODUCTION

The development of PZT-based FeRAM has been limited to the 130nm technology node due to poor CMOS-compatibility and scalability [1]. Since the discovery of FE properties in CMOS-compatible HfO<sub>2</sub> thin films [2], research has been focused on non-volatile memory applications such as FeRAM (Ferroelectric Random Access Memory), FeFET (Ferroelectric Field Effect Transistor) and FTJ (Ferroelectric Tunnel Junction). 64kbit and 16kbit FeRAM arrays have been successfully integrated in the MOL [3] and BEOL [4] of 130nm CMOS process technologies respectively, and high endurance and writing speed have been reported. However, potential for scaling has yet to be fully demonstrated as reported operating voltages are too high for thinner gate oxide transistors on more aggressive nodes like 28FDSOI [5]. In this work, a step towards FeRAM arrays with increased MW is made with the etching of the HfO<sub>2</sub> layer. The development of a new, Preisach-inspired [6], FeCAP compact model and its calibration allow to simulate the projection of this technology at advanced transistor nodes and to make recommendations for improved MW.

## II. EXPERIMENT

### A. Devices

Scaled TiN/Si:HfO<sub>2</sub>/TiN capacitors were integrated in the Back-End Of Line (BEOL) of a 130nm CMOS technology (Fig. 1). Above M4, TiN Bottom Electrode (BE) was deposited by Physical Vapor Deposition (PVD). A 10nm-HfO<sub>2</sub> thin film was then deposited using Atomic Layer Deposition (ALD)

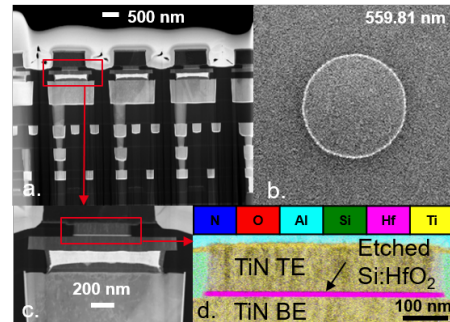


Fig. 1. (a) Cross-section HAADF-STEM imaging of TiN/Si:HfO<sub>2</sub>/TiN FeCAPs integrated in 130nm BEOL; (b) Top-down SEM measurement of FeCAP diameter in a 1T1C 16kbit FeRAM array. 1.8% variation from the designed 550nm is measured; (c) Close-up HAADF-STEM showing vertical etched walls on Si:HfO<sub>2</sub> layer; (d) EDX analysis of the FeCAP demonstrating uniformity of Si:HfO<sub>2</sub> layer

technique. To promote ferroelectricity, HfO<sub>2</sub> layer was Si-doped by ion implantation as reported in [7]. PVD-deposited TiN Top Electrode (TE) was patterned to define capacitors of critical diameters ranging from 300nm to 600nm. In some wafers top electrode etching stopped on the HfO<sub>2</sub> layer ('non-etched FeCAP') as in our previous work [4], whereas it continued down to the bottom electrode in other wafers, etching the HfO<sub>2</sub> layer ('etched FeCAP'). In both cases, a specific thermal annealing step was performed at the end of process at BEOL-compatible temperature. To assess the electrical response of thus processed capacitors, available test structures include capacitor fields made of 1290 FeCAPs routed in parallel and 16kbit 1T1C FeRAM arrays [4].

### B. Impact of FE layer etching on FeCAP performance

At single-cell level, current-voltage characteristics were measured on 550nm diameter non-etched and etched capacitor fields using Positive Up Negative Down method [8]. Fig. 2a. shows that both devices exhibit FE behavior after a wake-up phase consisting in  $10^4 \pm 4V$ -100kHz triangular pulses. The maximal FE current of the etched FeCAP is almost twice as high as that of the non-etched FeCAP. The remanent polarization ( $2.P_R$ ) integrated from the FE current peaks is

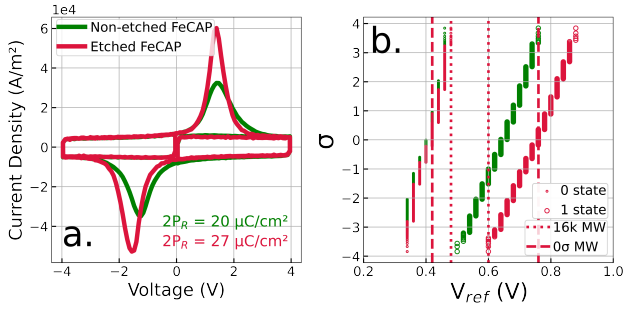


Fig. 2. Comparison of (a) normalized current from triangular PUND measurements at  $\pm 4\text{V}$ -10kHz on 550nm non-etched and etched capacitors after a wake-up phase of  $10^4$  triangular pulses at  $\pm 4\text{V}$ -100kHz; (b) '0' and '1' state distributions on a 16kbit 1T1C FeRAM array with 550nm non-etched and etched capacitors measured at 4.8V after a wake-up phase of  $10^4$  square pulses at 4.8V-2 $\mu\text{s}$ . Dotted vertical lines define 16kbit MW and 0 $\sigma$  MW.

20  $\mu\text{C}/\text{cm}^2$  and 27  $\mu\text{C}/\text{cm}^2$  for non-etched and etched FeCAP, respectively. This indicates that etching the HfO<sub>2</sub> layer does not inhibit the crystallization in the FE orthorhombic phase, nor degrades the FeCAP FE properties, but actually increases the remanent polarization. A possible explanation could be a more favorable and localized stress on the FE layer after etching that favors crystallization in the orthorhombic phase.

### C. Impact of FE layer etching at 16kbit array level

In 16kbit arrays, the FeCAP (1C) bottom electrode is connected to the transistor (1T) drain. Bitcells can be programmed in the '0' polarization state by applying a positive pulse on 1C top electrode (Plate Line, PL), or in the '1' polarization state by applying a positive pulse on 1T source (Bit Line, BL). The FeCAP polarization state is read by attempting to program a '0' and measuring the BL voltage elevation, which is defined as

$$V_{BL}^0 = \frac{C_{DE}}{C_{DE} + C_{BL}} \times V_{PL} \quad (1)$$

or

$$V_{BL}^1 = \frac{C_{DE}}{C_{DE} + C_{BL}} \times V_{PL} + \frac{2P_R \cdot S}{C_{DE} + C_{BL}} \quad (2)$$

when reading a '0' or '1' state, where  $C_{DE}$  is the dielectric (DE) capacitance and  $C_{BL}$  is the BL capacitance. A Sense Amplifier then compares BL voltage to a pre-defined reference voltage ( $V_{ref}$ ) and outputs a 0 or Vdd logic value. Experimentally sweeping  $V_{ref}$  enables to precisely extract  $V_{BL}^0$  and  $V_{BL}^1$  analog values for each bitcell. Hence, distributions centered on median values of  $V_{BL}$  and tilted according to bitcell to bitcell variability and design effects can be reported. The MW is either defined at product-like level across the 16kbit array (16k MW) or as the difference between median  $V_{BL}^1$  and  $V_{BL}^0$  (0 $\sigma$  MW). In the sense of Eqs. 1 and 2, MW is proportional to  $2P_R$ . Fig. 2b. compares '0' and '1' distributions for 16kbit arrays with 550nm diameter non-etched and etched capacitors at 4.8V programming and reading voltages. A 16kbit MW of 0.04V for the non-etched capacitors array is measured, which is similar to the 0.05V 16kbit MW reported in [4]. In the etched capacitors array,  $V_{BL}^1$  distribution is shifted

towards higher values and a 0.12V 16kbit MW is measured, demonstrating that etching the FE layer improves the MW in FeRAM arrays. In order to estimate the MW evolution in advanced structures, a compact model of FeCAP in circuit environment is needed.

## III. MODEL

### A. Definition and calibration

The compact model developed is based on the current variation measured when applying a PUND sequence to a FeCAP. The DE-induced current ( $I_{DE}$ ), FE switching current ( $I_{FE}$ ) and static leakage current ( $I_{leakage}$ ) contribute to the total current and are modelled by the following analytical equations:

$$I_{DE} = C_{DE} \frac{dV}{dt} \quad \text{with} \quad C_{DE} = \frac{\epsilon_0 \cdot \epsilon_R \cdot S}{t} \quad (3)$$

where  $\epsilon_0$  and  $\epsilon_R$  are the vacuum permittivity and HfO<sub>2</sub> layer relative permittivity, respectively, and  $S$  and  $t$  the capacitor area and thickness, respectively.

$$I_{FE} = S \frac{dP}{dE} \frac{dE}{dt} \quad (4)$$

where  $E = \frac{V_{app} - V_{off}}{t}$  is the electric field depending on applied voltage  $V_{app}$  and offset voltage  $V_{off}$  accounting for FeCAP coercive voltages asymmetry and fixed charges.  $\frac{dP}{dE}$  will be determined to match the measured FE current.

Poole-Frenkel effect is the considered conduction mechanism for static leakage simulation [9]:

$$I_{leakage} = S \cdot A_{leak} \cdot E^{B_{leak}} \quad (5)$$

where  $A_{leak}$  and  $B_{leak}$  are fitting parameters.

While Fig. 2 results were measured on a FeCAP after a wake-up with triangular pulses, the FeCAP considered for model calibration experienced 16kbit-like wake-up with square pulses. Based on Eq. 3, 4 and 5, the model is calibrated to match the total current measured at 4.8V-30 $\mu\text{s}$  on a 550nm diameter etched capacitor field of median behavior (Fig. 3).

Extracting  $\epsilon_R$  from the DE current measured during the U and D voltage pulses is challenging due to backswitching and leakage phenomena. C-f measurement at 0V using E4980A Precision LCR meter enables to determine a safe area for reliable  $\epsilon_R$  extraction (Fig. 3b. & inset).

As shown in Fig. 3a., a Lorentzian distribution allows a good fit of the FE current peaks so  $\frac{dP}{dE}^\pm$  can be defined as:

$$\frac{dP^\pm}{dE} = \frac{2 \cdot \frac{A^\pm}{\pi} \cdot w^\pm}{4 \cdot (E - E_c^\pm)^2 + w^{\pm 2}} \quad (6)$$

To accurately describe both positive (P-U) and negative (N-D) FE current peaks, three fitting parameters from Eq. 6 are adjusted to the experimental dots of Fig. 3a. through a non-linear least squares numerical method. Although Eq. 6 is not physically-based, these parameters can be approached as physical characteristics of the FeCAP:  $E_c$ , the coercive voltage,  $w$ , the full-width at one-fifth of the maximum and  $A$ , the peak area, or domains density.

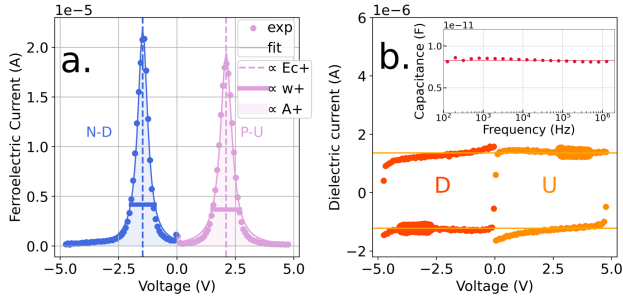


Fig. 3. On etched FeCAP of median behavior, experimental (a) FE current from P-U and N-D voltage pulses at 4.8V-30 $\mu$ s and Lorentzian distribution calibrated to fit  $I_{FE}$ ; (b) DE current from U and D voltage pulses at 4.8V-30 $\mu$ s. Inset: Capacitance measured over the 100Hz-2MHz frequency range at 0V. The relative permittivity extracted from C-f determines the DE current area of reliable  $\epsilon_R$ , highlighted on the graph.

TABLE I  
FITTING PARAMETERS VALUES AND FECAP DIMENSIONS

Ferroelectric						
$A(C/m^2)$		$E_c(V/nm)$		$w(V/nm)$		$V_{off}(V)$
$A^+$	$A^-$	$E_c^+$	$E_c^-$	$w^+$	$w^-$	
0.365	0.354	0.179	-0.179	0.058	0.050	0.32
Dielectric		Leakage		Dimensions		
$\epsilon_R(-)$	$A_{leak}$	$B_{leak}$	$S(\mu m^2)$	$t(nm)$		
29.7	0	0	306	10		

Table I lists the 12 fitting parameters extracted from the etched FeCAP experimental data presented in Fig. 3 and FeCAP dimensions to calibrate the model.

### B. Model validation

Automated and systematic parameters extraction from measured current is reliable and repeatable for different process options. The current simulated when applying a PUND signal to the FeCAP and the P-V loop extracted from the simulated I-V perfectly fit the measured data as shown in Fig. 4a. & b.

To assess the model accuracy beyond the calibration conditions, the simulated FeCAP is subjected to a wider range of voltage operation. The model takes into account history effects by relying on stored previous polarization states to compute the current [10] and so reproduces well the low voltage nested hysteretic subloops behavior of FeCAPs. The simulated  $2.P_R$  along programming voltage successfully follows the same decreasing trend as measured values (Fig. 5a.), validating the model accuracy at different voltages at the single-cell level.

To simulate the programming and capacitive reading mode implemented on 16kbit arrays, a 130nm 1T1C bitcell routed in an elementary circuit is simulated. A capacitance component emulating  $C_{BL}$  is fixed at 188fF and corresponds to the gate-source capacitance of the 128 selection transistors evaluated using 130nm 1T spice model, together with the parasitic capacitance coupling between metal lines extracted through a 16kbit circuit simulation. Programming and reading operations are simulated by modulating voltages applied to circuit ports. A simpler model that does not record history was used in

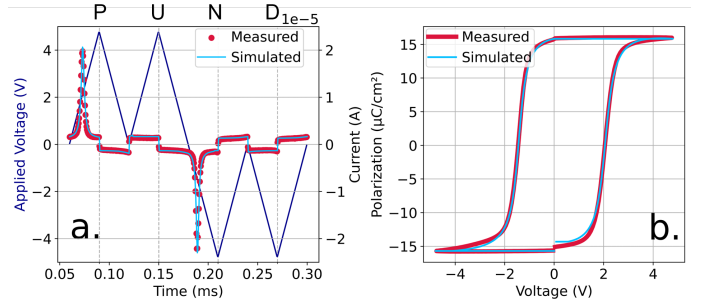


Fig. 4. On a 550nm diameter etched FeCAP of median behavior, (a) experimental I-t measured for a PUND sequence at 4.8V-30 $\mu$ s; simulated I-t using the developed current-based model; (b) experimental and simulated P-V numerically integrated from (a) are a close match, validating the calibration

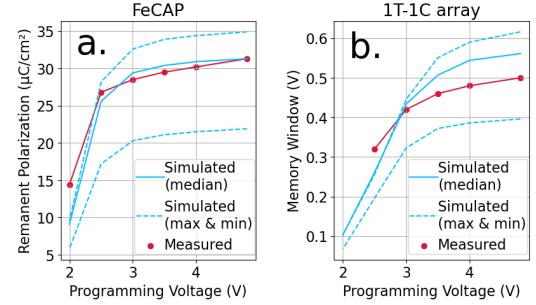


Fig. 5. (a) Remanent polarization values extracted from I-V subloops measured on 550nm diameter etched FeCAP of median behavior and simulated with the model calibrated on FeCAP I-V at 4.8V. Dashed lines result from simulations calibrated on measured FeCAP of maximal and minimal  $2.P_R$ ; (b)  $0\sigma$  MW values measured on a 16kbit structure and MW simulated on an elementary circuit emulating a 16kbit circuit, both with square 600nm etched capacitors

this circuit for convergence. Simulated MW follows the same trend along voltage as the  $0\sigma$  MW measured at 4.8V-2 $\mu$ s on 16kbit arrays with square 600nm etched capacitors (Fig. 5b.), validating the elementary circuit and proving that it can correctly simulate MW variation along voltage.

## IV. PROJECTION OF FERAM MW TOWARDS 28FDSOI NODE

This part focuses on  $0\sigma$  MW evolution with scaling and does not account for device or design induced variability.

Fig. 6 represents the  $2.P_R$  needed to maintain a constant 0.1V MW for a FeCAP of given diameter in an array of given  $C_{BL}$ , where  $2.P_R$  is computed from the MW defined as  $2.P_R \cdot S / (C_{DE} + C_{BL})$  (Eq. 1, 2). In 16kbit arrays with 130nm 1T,  $C_{BL}$  is 188fF (III-B). Increasing the array size equally in both directions (WL and BL) at the same technology node increases the total gate-source capacitance and thus  $C_{BL}$ ; larger capacitor diameters would be needed at constant  $2.P_R$  to maintain 0.1V MW (Fig. 6), in drastic opposition with scaling.

Considering 28FDSOI 1T in 16kbit arrays scales  $C_{BL}$  down to 89fF for thick gate oxide transistors (GO2) operating at voltages up to 2.5V. This represents roughly half the value obtained at the 130nm node and accounts for reduction in

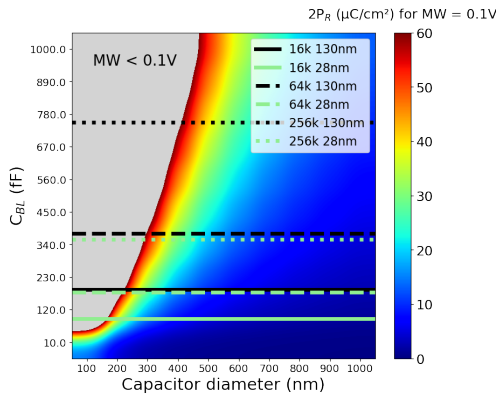


Fig. 6. Projection of the remanent polarization needed to maintain a 0.1V MW for decreasing capacitor diameter and increasing array size. Markers of  $C_{BL}$  values at different nodes and for different array sizes were computed with  $C_{BL}(16k, 130nm) = 188fF$  and  $C_{BL}(16k, 28FDSOI) = 89fF$

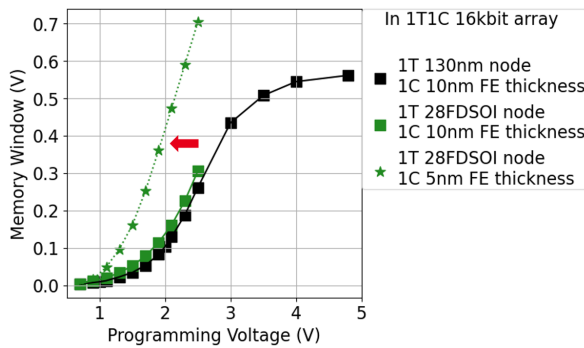


Fig. 7. MW simulated along voltage in an elementary circuit emulating a 16kbit 1T1C FeRAM array with square 600nm FeCAP and 1T at the 130nm and 28FDSOI technology nodes. At the 28FDSOI node, MW improvement at low voltage with a 5nm thick FeCAP is shown. The simulated 28FDSOI 1T gate length and gate width are 150nm and 160nm, respectively (GO2 type).

both the 1T dimensions (down to 10 times) and the parasitic capacitance (38%) in 16kbit circuit at advanced 1T nodes. The reduced  $C_{BL}$  in 28FDSOI arrays enhances FeCAP scaling capability and favors array size expansion compared to 130nm arrays: a 0.1V MW in 256k arrays of 300nm diameter FeCAPs with a realistic  $2.P_R$  is achievable at 28FDSOI node (Fig. 6).

However, advanced node 1T have a lower operating voltage than 130nm node 1T (2.5V instead of 4.8V for GO2 1T). As shown in Fig. 7, the MW simulated at 1.9V operating voltage in the elementary circuit at 130nm node ( $C_{BL} = 188fF$ ) is less than 0.1V. Scaling the 1T to the 28FDSOI node ( $C_{BL} = 89fF$ ) increases only slightly the simulated MW compared to the circuit with 130nm 1T. The reduced  $C_{BL}$  at advanced nodes does not compensate for a rapidly decreasing MW at low voltage due to the FeCAP subloops behavior (Fig. 5) with coercive voltages around 1.8V. Improving the FeCAP performances at operating voltages below 2.5V is therefore needed. FeCAP with 5nm  $HfO_2$  layer and unchanged  $2.P_R$  is simulated in the circuit with advanced 1T. The simulated MW is improved at low voltage compared to a 10nm  $HfO_2$  layer, thanks to decreased coercive voltages at constant coercive

fields [11]. Overcoming the challenge of making FE 5nm-Si:HfO<sub>2</sub> films at BEOL-compatible temperature with large  $2.P_R$  would lead to devices and arrays fully functioning at 2.5V and below with an increased MW.

3D capacitors as demonstrated in [12] are another option to boost  $2.P_R$  with no area penalty and would allow for an improvement of the MW with no increase of FeCAP footprint.

## V. CONCLUSION

We demonstrated that etching the FeCAP ferroelectric Si:HfO<sub>2</sub> film in a 16kbit Si:HfO<sub>2</sub>-based 1T1C FeRAM array at the 130nm node significantly improves the MW compared to the case where only the top electrode is etched. In order to predict the MW evolution for scaled 1T1C bitcells and increasing array sizes, a new current-based Preisach compact model for FeCAP is developed, calibrated and shown to accurately reproduce the FeCAP behavior at various operating voltages. Integrating the model to an elementary circuit emulating the 16kbit array enables to correctly predict the MW variation along voltage. The model allows to quantify the MW evolution at advanced technology nodes and therefore outlines the need to adopt advanced node 1T, reduce FeCAP FE layer thickness to lower coercive voltages and consider 3D capacitors to boost  $2.P_R$  with no footprint increase.

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