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# Thermal and statistical analysis of various AlN/GaN HEMT geometries for millimeter Wave applications

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**Abstract-** Downscaling HEMT devices is nowadays substantial to allow their operation in the millimeter wave frequency domain. In this work, the electrical parameters of three different AlN/GaN structures featuring various GaN channel thicknesses were compared. After a DC stabilization procedure, 96 HEMT devices under test exhibit a minor dispersion in DIBL and lag rates, which reflects an undeniable technological mastering and maturity. Evaluation of the sensitivity of devices with different geometries at temperatures of up to 200°C revealed that the gate-drain distance impacts  $R_{on}$  variation and not  $I_{dss}$  variation with temperature. We also showed that DIBL at moderate electrical field and the drain lags exhibit athermal behavior; unlike gate lag delays which can be thermally activated and exhibit a linear temperature dependence regardless of the size of the gate length.

**Keywords-** GaN, HEMT, on-resistance  $R_{on}$ , DIBL, traps,  $I_{dss}$

## I. INTRODUCTION

Modern telecommunication systems such as 5G, military wireless communication and radar amplifiers are applications that imply high power, high temperature and high frequency operation, with high level of confidence on the reliability. GaN technology is the optimal candidate to fulfill these requirements [1]. In order to increase the frequency range to mmWave and maintain a high power-added / output power density combination, downscaling the gate length ( $L_G$ ) in HEMT devices is crucial. Decreasing  $L_G$  should therefore be associated to epi-layer downscaling (e.g. channel thickness  $t_{ch}$ ) to ensure strong electron confinement and high electron density in the 2D-Electron-Gas (2DEG). The ultrathin AlN barrier on GaN channel meets these criteria [2-3]. However, a trade-off must be implemented to ensure high reliability of the active device considering the high junction temperature sensitivity, which could lead to transistor degradation, especially under high current and high voltage biasing. In this work, a statistical analysis of relevant electrical parameters of 3 different AlN/GaN structures featuring various  $t_{ch}$  for  $2 \times 100 \mu\text{m}$  gate width transistors was conducted in a safe operating area using DC and pulsed DC measurement setup. Thermal characterization was also carried out to monitor the main electrical parameters variation with temperature ( $T^\circ$ ).

## II. DEVICE FABRICATION

The AlN/GaN-on-SiC HEMT devices previously described in [4] were grown by metal organic chemical vapor deposition. Three different device structures A, B and C that have the same epitaxy but differ in their GaN  $t_{ch}$  (100nm, 150nm and 500nm respectively [Fig. 1]) were characterized. Transistors featuring different geometries ( $L_G$  [100nm, 150nm, 250nm, 500nm], gate-to-drain distances  $L_{GD}$  [1.5 $\mu\text{m}$  and 2.5 $\mu\text{m}$ ]) have been developed for each of these 3 technological processes.

## III. DATA/RESULTS AND DISCUSSION

**Electrical Characterization.** Before initiating an exhaustive and systematic statistical characterization procedure, having a stable operating device is mandatory. A dedicated measurement protocol has been developed to ensure the stability of the DC measurements throughout the characterization campaign. We

validated its efficiency through the reduction of the measurement dispersion, as illustrated for the output characteristics of 2 twin devices (Fig. 2). Drain Induced Barrier Lowering (DIBL) is extracted, as well as the transconductance profile with  $V_{GS}$  for different  $V_{DS}$  voltages (Fig. 3). DIBL values are weakly scattered, with no impact of  $L_{GD}$  as expected, but with an inverse sensitivity to  $L_G$ , which suggests a less important electron confinement (an effect that is less marked for small  $t_{ch}$  [Fig. 4]). The availability or functionality of devices of each  $t_{ch}$ , according to  $L_G$ , will be discussed in the final paper. In order to quantify lag rates at different quiescent voltages in pulsed DC measurements, we determine the power ratio variation [5] (data not shown). Lag values are less dispersed and mostly depend on  $t_{ch}$ , but not on  $L_G$  nor  $L_{GD}$  (Fig. 5). The activation of traps seems to significantly increase when  $t_{ch}$  decreases. This effect could arise from the proximity of the carbon-doped region with the 2DEG. Among the 3 studied structures, we find that structure A enables efficient device operation with an  $L_G=100\text{nm}$ , but not structure B which exhibits high DIBL, nor structure C that is not functional at this  $L_G$ . Nevertheless, trap activation is highly pronounced in structure A compared to structures B and C.

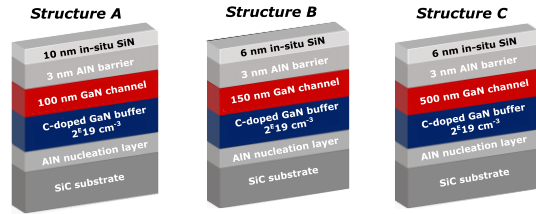
**Thermal analysis.** We focus the thermal analyses on the intermediate B structure as it encompasses all geometric variations for  $L_G$  and  $L_{GD}$ . The variation of DIBL,  $R_{on}$ ,  $I_{DSS}$  and lag rates with  $T^\circ$  are assessed. DIBL is not significantly changed after exposure to  $T^\circ$  of up to 150°C and maintains same levels compared to room  $T^\circ$  (Fig. 6). These results suggest a high thermal stability, even for devices featuring the smallest  $L_G=100\text{nm}$  (which usually exhibit a degraded electron confinement).  $I_{DSS}$  variation with  $T^\circ$  is independent of  $L_G$  and  $L_{GD}$  and twice greater in DC than in pulsed DC mode, due to the impact of the junction  $T^\circ$  on the electron mobility (Fig. 7). The relative variation of  $R_{ON}(T^\circ)$  in the two characterization modes is  $L_G$ -independent but  $L_{GD}$ -dependent. The variation of  $\sim 6.4 \text{ m}\Omega\cdot\text{mm}/^\circ\text{C}$  for  $L_{GD}=1.5\mu\text{m}$  and  $9.3 \text{ m}\Omega\cdot\text{mm}/^\circ\text{C}$  for  $L_{GD}=2.5\mu\text{m}$  is attributed to the access resistances  $T^\circ$  dependence (Fig. 7). Finally, Fig. 8 shows that as  $T^\circ$  reaches 200°C, only the drain lag rates remain constant. Gate lag rates increase with  $T^\circ$ , probably consequently to the positive shifting of threshold voltage with  $T^\circ$ . As the transistor is more pinched off, a greater activation of electron traps is involved at the AlN/GaN vicinity of the 2DEG under the gate [6].

## IV. CONCLUSIONS

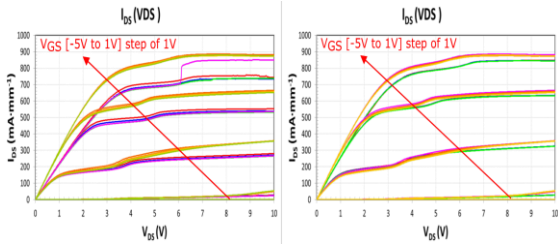
This study highlights the strengths and weaknesses of 3 low dispersed AlN/GaN topological structures featuring different  $t_{ch}$ . Adjusting  $t_{ch}$  allows transistor operation at high frequencies while controlling the impact of traps on its electrical behavior. The thermal characterization showed a negligible effect of  $T^\circ$  on the DIBL values. We also documented the impact of traps on gate lag, resulting from thermal and electrical activation, and drain lag  $T^\circ$  independency. This representative study will be completed with step stress tests to compare structures robustness and identify their safe operating area.

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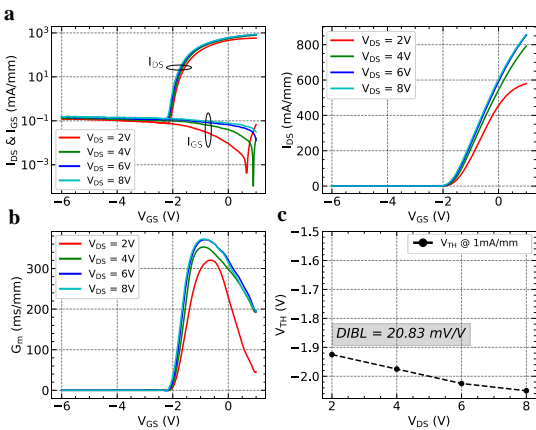
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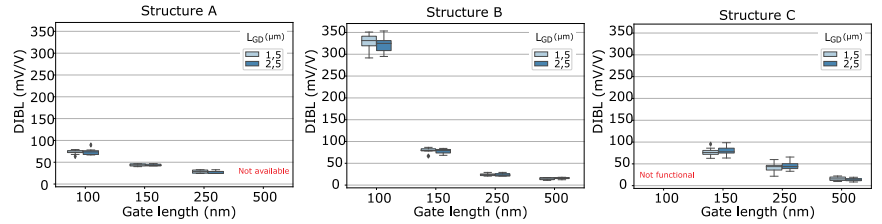
**Figure 1.** Schematic illustration of different stacked layers of AlN/GaN on SiC epi-taxial structures, all featuring  $2 \times 10^{19} \text{ cm}^{-3}$  Carbon-doped GaN buffer but with different channel thicknesses (A: 100nm, B: 150nm & C: 500nm).



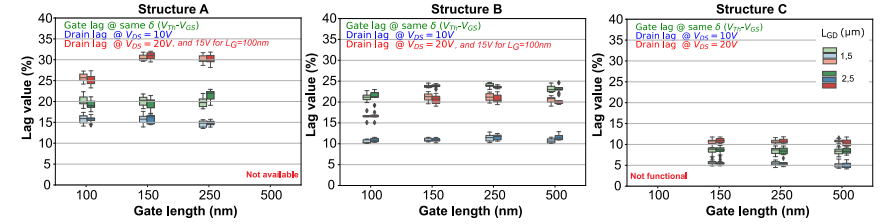
**Figure 2.** Output characteristics  $I_{DS}(V_{DS})$  in  $\text{mA} \cdot \text{mm}^{-1}$  of twin devices ( $2 \times 100 \mu\text{m}$ ,  $L_G = 500 \text{ nm}$   $L_{GD} = 2.5 \mu\text{m}$  of structure B) with  $V_{GS}$  swept from -5V to +1V with 1V step, before (left panel) and after stabilization (right panel).



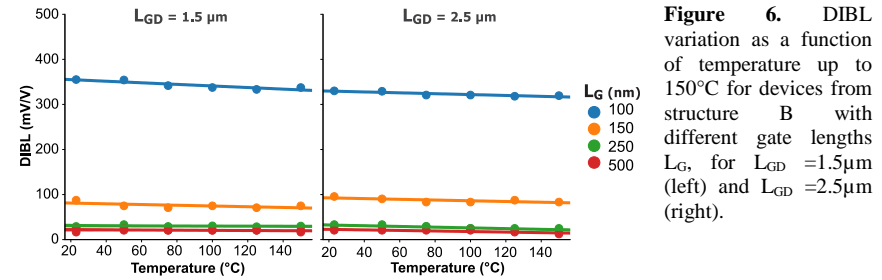
**Figure 3.** Transfer characteristics with  $V_{DS}$  sweep [2V to 8V] with a 2V-step, (a)  $I_{DS}$  and  $I_{GS}$  in logarithmic scales ( $\text{mA}/\text{mm}$ ) and in linear scale, (b) transconductance profile  $g_m(\text{ms}/\text{mm})$  and (c)  $\text{DIBL} = \frac{\Delta V_{TH}}{\Delta V_{DS}}$  ( $\text{mV}/\text{V}$ ).



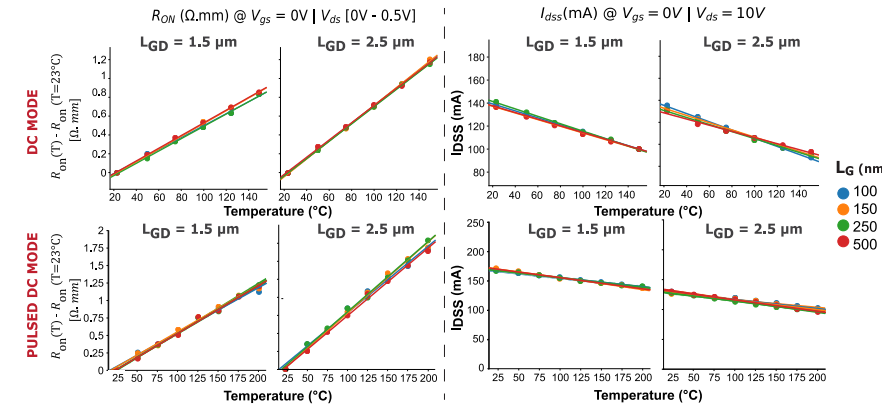
**Figure 4.** Statistical dispersion of DIBL values for the different structures as a function of gate length  $L_G$  and gate-to-drain distance  $L_{GD}$ .



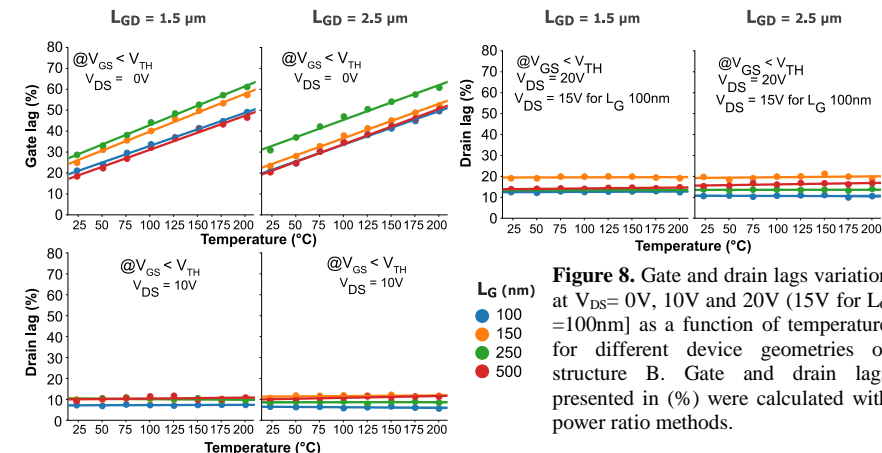
**Figure 5.** Statistical dispersion of gate and drain lag values at different quiescent voltages as a function of gate length  $L_G$  and gate-to-drain distance  $L_{GD}$ . Gate voltage is applied with respect to a negative constant of  $\delta(V_{GS} - V_{TH})$  for all devices (because  $V_{TH}$  changes with  $L_G$ ). Drain voltage  $V_{DS} = 0\text{V}$  for all gate lag measurements.



**Figure 6.** DIBL variation as a function of temperature up to  $150^\circ\text{C}$  for devices from structure B with different gate lengths  $L_G$ , for  $L_{GD} = 1.5 \mu\text{m}$  (left) and  $L_{GD} = 2.5 \mu\text{m}$  (right).



**Figure 7.** Relative variation of  $R_{on}$  and  $I_{DSS}$  for devices from structure B with different gate lengths  $L_G$  and gate-to-drain distances  $L_{GD}$ , as a function of temperature in DC mode (up to  $150^\circ\text{C}$ ) and in pulsed DC mode (up to  $200^\circ\text{C}$ ).



**Figure 8.** Gate and drain lags variation at  $V_{DS} = 0\text{V}$ ,  $10\text{V}$  and  $20\text{V}$  ( $15\text{V}$  for  $L_G = 100\text{nm}$ ) as a function of temperature for different device geometries of structure B. Gate and drain lags presented in (%) were calculated with power ratio methods.