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Device Reliability to Circuit Qualification: Insights and Challenges

(Invited Paper)

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Abstract— Aging phenomena are first evidenced at device level to cell level considering a precise knowledge of the leading degradation mechanisms and interactions useful for processing optimization focusing performance vs. reliability requirements. Digital to analog circuits are then studied for product qualification based on the former results that needs specific methodologies adapted case by case with mission profile and the correlation between sensing parameter, accelerating factors for lifetime margin. This represents huge challenges for operational lifetime determination, considering top down and bottom up consistencies for relevant product qualification.

Keywords: Wearout, Bias Temperature Instabilities, Hot carriers, Hard Breakdown, damage interaction, HTOL.

I. INTRODUCTION

Since the first developments of integrated circuit (IC) processing, CMOS technologies have shown tremendous ability for scaling dimensions (W_G/L_G) towards nanometer size, frequency (F_{CLK}) increase and consumption (P_{Tot}) reduction for low power (LP) applications [1, 2]. The huge investments in optimizing performances in speed, static (P_{DC}) and dynamic (P_{AC}) power, have faced the necessity to guaranty the reliability of devices and circuits targeting a supply voltage range (V_{DDmin} , V_{DDmax}) Fig.1, while increasing transistor density and the use of various operational functions for digital and analog applications [3, 4]. Even if V_{DD} has been reduced accordingly to the device size, the increase in temperature (Fig.1), electric field and current density have raised a great attention for reliability requirements with the need of a good electrostatic control and the strong reduction of equivalent oxide thickness (EOT) for the gate dielectric of Si-bulk to FDSOI planar transistors [1-3]. This consequently moved MOSFET architecture from 2D to 3D and multi-gate FinFETs where lattice temperature, design and contact quality [5] are known to strongly influence the performance and reliability risks [6, 7]. This led the manufacturers to develop front-end reliability tests in order to guaranty the robustness of ICs that need a complete examination of Wearout mechanisms at

device level, as hot-carrier damage (HCD), bias temperature instability (BTI) and soft to hard gate-oxide breakdown (SBD, HBD) [8] that may balance their contributions in the overall wearout. This leads to the big challenge of a proper modelling of

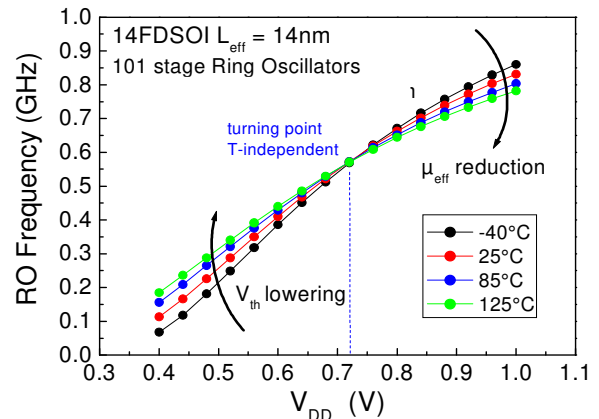


Fig. 1 : Ring Oscillator (RO) frequency dependence as a function of supply voltage V_{DD} for different temperatures. The main effects of V_{th} shift and mobility reduction (μ_{eff}) is distinguished as the performance criteria on switching speed for digital application in 14nm FDSOI (HKMG) CMOS node.

all mechanisms with the right acceleration factor that takes the lead in MOSFETs, Then, this must be transferred up to digital cells with interacting phenomena [9, 10], chained in the critical paths, forming elementary functions into the block (bottom up approach). However, this methodology which is valid for process optimization presents limitations at the circuit level with the increase in device/cell density and complexity [8, 9]. One can deal with this issue by an accurate analysis of circuit aging (top down approach) using high temperature operational lifetime (HTOL) tests with in-situ monitors that give a precise qualification of products [11].

In this paper, the main contribution of aging phenomena is studied in section II in different CMOS nodes coming from LP 28nm FDSOI (HKMG gate stack) and smart power extended drain (EDMOS with SiO₂ gate oxide). We restricted the work here to HCD, BTI mechanisms which may trigger HBD in some configurations [12]. Drain current reduction (ΔI_{DS}) is described by V_{Th} shift (ΔV_{Th}), mobility reduction ($\Delta \mu_{eff}$) and source-drain resistance increase (ΔR_{SD}) whereas each contribution depends on the leading damage mechanism (defect density and spread) and on drain to channel architecture. Section III deals with the challenge of device modelling considering the sense effects and temperature impacts [10] through interacting damage mechanisms in switched transistors between Off-mode and On-mode when channel carriers from different energy ranges are involved [12]. The last part (Section IV) gives insights in digital to analog circuits for a realistic reliability determination using HTOL in Ring Oscillators (RO), SRAM cell, Low Drop-Out regulator (LDO) and ADC circuit that illustrate the product reliability qualification.

II. AGING PHENOMENA IN PLANAR CMOS NODES

Hot-carrier damage, BTI and soft breakdown are known to be the first consequences of Wearout mechanisms in MOSFETs that may trigger HBD of gate-oxide [13] depending on the structure resistance and power level requirement [14]. A figure of merit for process quality is to determine the worst-case of aging in transistors using accelerated DC stressing that can be transferred to cycling transistors in digital cells with quasi-static modeling under medium frequency range [15]. Time to breakdown was recently reconsidered at high frequency in circuits (1GHz) where a net gain is observed [16]. The persistence of HCD with nominal supply voltage (V_{DD}) reduction and size scaling has moved the modeling from lateral field acceleration to an energy dependence paradigm [17, 18]. As supply voltage V_{DD} does not scale accordingly to gate-length (L_G) reduction due to performance requirements [19], the effective field in the channel strongly rises leading to mobility reduction (Fig.2a) that can be expressed as a function of the distinct scattering phenomena in the channel [20]. It is shown in Fig.2b that for a given HC mechanisms, here at $V_{GS} > V_{DS}$ (HC-M3) [15], the transistor parameter sensitivity is larger for R_{SD} increase (gate-drain region), then followed by μ_{eff} reduction (channel damage) and V_{Th} -shift (extension towards the source).

We have modelled the effective mobility μ_{eff} as a function of mobility attenuation factors ($\theta_1(t_s)$, $\theta_2(t_s)$) that can be related to source-drain resistance increase ($R_{SD}(t_s)$), using first [21] or second order modelling [22]-[23] that were used in fresh devices. The technique is based on the useful Y-function [24] that allows us to use a self-consistent extraction methodology for $R_{SD}(t_s)$ extraction during stressing at low-field measuring condition [23]. As the attenuation factor is $\theta_1(t_s) = \theta_{10} + K_0 R_{SD0}$, with the geometry factor $K_0 = \mu_{00} C_{ox} W_G / L_{eff}$, one can extract for a direct determination in Fig.3a θ_{10} (Y-intercept) and R_{SD0} (slope) in Extended Drain (EDMOS) and 28FD and do it subsequently as a function of stress time (t_s) in Fig.3b for 28nm FDSOI devices.

$$I_{DS} = \frac{K_{eff}(t_s) V_{GT}(t_s) V_{DS}}{1 + \theta_1(t_s) V_{GT}(t_s) + \theta_2(t_s) V_{GT}^2(t_s)} \quad (1)$$

$$K_{eff}(t_s) = \mu_{ot}(t_s) C_{ox} \frac{W}{L_{eff}}, \quad (2a)$$

$$\theta_1 = \theta_{1.0} + K_{eff}(t_s) * R_{SD}(t_s) \quad (2b)$$

$$\theta_2 = \theta_{2.0} + K_{eff}(t_s) \lambda(t_s) \quad (2c)$$

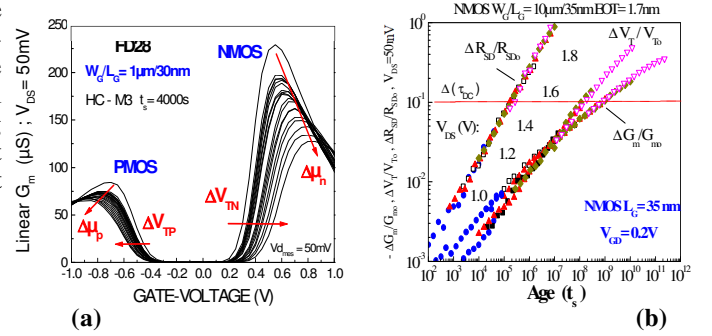


Fig. 2 : (a) Reduction in transconductance (G_m) due to mobility decrease and V_{Th} shift in N- and P- channel devices (28FD) under HC mode M3 ($V_{GS} > V_{DS}$). (b) Relationship of N-MOSFET degradation to the Age(t_s) function expressed as function of the acceleration factor in LP 28nm HKMG stack with equivalent oxide thickness EOT = 1.7nm.

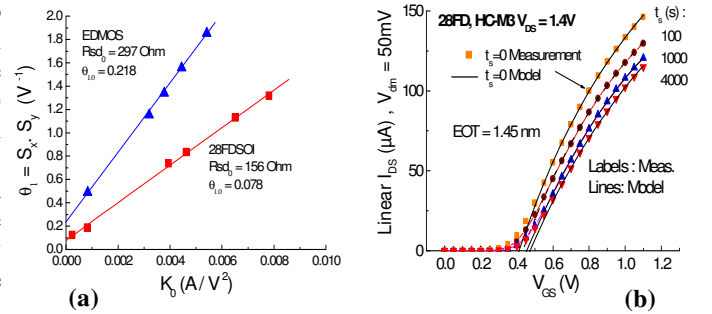


Fig.3: (a) Direct extraction of θ_{10} (Y-intercept) and R_{SD0} (slope) that is compared to the product of $Y = I_{DS}/G_m^{0.5}$ and $X = G_m^{-0.5}$ functions [22] in fresh 28FD and EDMOS devices. (b) Corresponding linear $I_{DS} - V_{GS}$ dependence in 28FD compared between models (lines) and measurements (labels) under HCD M3 mode ($V_{GS} > V_{DS}$).

Based on I_{DS} expressed with (1)-(2a-c) and the use of Y- and X- functions, this allows to obtain the $\theta_1(t_s)$ and $\theta_2(t_s)$ factors in Fig.3b that lead to $R_{SD}(t)$ extraction considering a fixed sensing V_{GT} range dedicated to θ_1 and θ_2 extraction [22, 23], and assuming constant (θ_{10} , θ_{20}) values with L_G variable in (2b)-(2c). Moreover, we have $K_{eff}(t_s)/K_0(0) = \mu_{ot} / \mu_{00} = G_m(t_s)/G_m(0)|_{max}$ giving the relationship to low-field peak mobility with time.

As EDMOS HCD structure is limited to R_{SD} increase in the drift zone [14], short channel FDSOI with $L_G = 35-14nm$ in Figs.1-3 is rather a combination of strong μ_{eff} reduction, ΔV_{TP} and ΔR_{SD} (Figs.2a,b) showing the phonon to surface roughness scatterings in conjunction to multi vibrational excitation (MVE)

of Si-H and Si-O bonds under HCD in the high V_{GS} range [19]. The persistence of HCD at low voltage was explained by a general thermal modeling depending on the local heat through self-heating (SH) contribution [5], the bond dissociation probability, dependent on the MVE properties through current driven modeling [15], the implication of a BTI (V_G only) effect into the HCD mechanism [25], or by a coupled modeling between bond dissociation and SH mechanism based on the description of the phonon transport equation [26]. Fig.4 shows that HCD under M3 mode ($V_{DS} = 1.4V$) is clearly more degrading the 28FD structure at room temperature than BTI

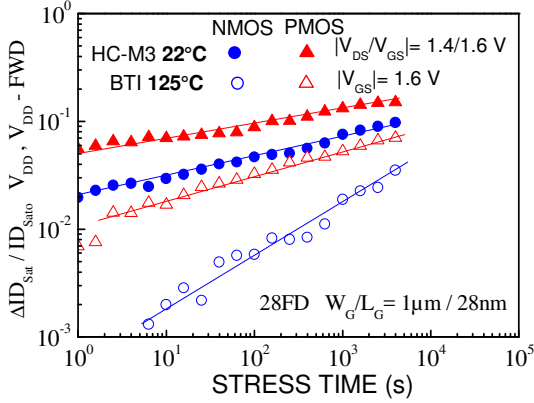


Figure 4: Reduction in drive current $\Delta I_{D_{Sat}}(V_{DD}, V_{DD})$ under BTI stress at 125°C and HC-M3 stress at 22°C in N- and P- channel FDSOI $W_G/L_G = 1\mu m / 28nm$ (Low- V_T , HKMG $HfO_2/SiON$) CMOS node.

stress carried out at 125°C. Furthermore, P-channel worsens HCD with channel holes compared to N-channel which is opposite to the classical HCD result. This may be explained by SH or NBTI contribution in P-channel under DC stressing. The distinction between each contribution requires to use alternating DC voltage stressing and AC stressing which is pulse shape dependent ($t_{r,f} / T_{AC}$, duty cycle), in order to identify the dominant behavior vs. time and frequency (t_s, f_{AC}). This becomes more complicated due to thermal implication whereas HCD increases with temperature [27] which is strongly dependent on the technology scaling, the thermal resistance of the structure and shapes [28], [29] *i.e.* on the property to maintain local heat (with effective temperature $T_{eff} > T_{Lat}$) or evacuate it by cooling energetic carriers [5]. We propose in the following to describe some examples developed in different CMOS nodes used to assess the role of the main degradation mechanisms.

III. CHALLENGES OF AGING DEVICE MODELING

The first attention to be paid under accelerating stressing condition is to determine the role of switching MOSFET between Off and On modes as distinct regions are submitted to distinct defect generations which may be related to HBD. Thus, the first subsection 3.A presents some ways to distinguish On to Off mode stressing, then followed by the study of sensing effects (subsection 3.B) with temperature in short channel LP CMOS technologies.

A. On and Off mode degradation

HCD in DC “On-state” mode is modelled through a simple model based on physical theories depending on carrier energy related to lateral electric field, and to carrier density related to vertical electric field. Then linear ΔI_{DS} modeling has included both contributions using a compact HCD model using (3a) with a balance between degradation and recovery (3b) where defect neutralization and field-assisted detrapping may occur.

$$\Delta I_{DLin_{on}}(t)_{DC} = A \cdot t^n \cdot e^{\beta \cdot V_{don}} \cdot (V_{g_{on}} - V_{th})^p \quad (3a)$$

$$\Delta I_{DLIN_{HL}}(t) = \Delta I_{DLIN_{LL}}(t) + \Delta I_{DLIN_{rec-off}} \quad (3b)$$

$$\Delta I_{DLIN_{rec-off}} = \frac{K_f}{F\alpha} \cdot V_{g_{on}}^\gamma \cdot e^{\delta \cdot V_{don}} \cdot \ln\left(1 + \frac{(t_{off} - t_0)\tau_e}{\tau_c}\right) \quad (3c)$$

$$\Delta I_{DLIN_{LL}}(t) = \frac{K_f}{F\alpha} \cdot \sum t_{on}^n \cdot e^{\beta \cdot V_{don}} \cdot (V_{g_{on}} - V_{th})^p \quad (3d)$$

where γ, δ parameters in (3c) are related to the accelerating recovery efficiency as a function of the vertical and lateral electric field, respectively. τ_c and τ_e are the trapping/detrapping time constant, K_f is the frequency damage generation rate and $t_0 = 50$ ns is a time characteristic for hole trapping [12]. Linear drain current degradation (ΔI_{Lin}) was extracted between 25 °C and 125 °C in Fig.5, in FDSOI N-FET ($L_G = 30nm$) under DC HCD On-state (modeling shown in lines) on one hand, and under DC Off-state on the other hand for fixed $V_{DS} = 1.5$ to 1.8V and $V_{GS} = -1$ up to 1.8V. We note that ΔI_{Lin} during HCD “On-state” mode above V_{TH} continuously increases (negatively) with V_{GS}

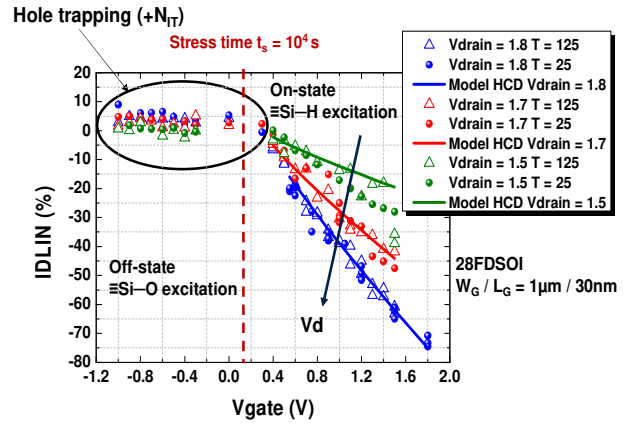


Fig.5: ΔI_{Lin} ($V_{DS} = 50$ mV) in 28FDSOI N-channel $L_G = 30$ nm extracted at $t_s = 10^4$ s. V_{GS} dependence of ΔI_{Lin} under HCD in On and Off modes with V_{GS} stress between -1 and 1.8 V with the modeling (lines) in On mode, between room temperature (25 °C) and $T = 125$ °C.

and V_{DS} and it follows a time power law reported as to be due to interface defects generation (ΔN_{IT}) related to $\equiv Si-H$ bonds breaking at Si/SiO_2 interface. Under HCD “Off-state” stress, ΔI_{Lin} measured under subthreshold regime is plotted (Fig.5) showing positive increase with time and following a logarithmic law dependence [30]. In this case the damage doesn’t exceed 10%, which might be related to $\equiv Si-O$ bonds excitation and breaking due to hole trapping.

Thin gate oxide breakdown is characterized under DC Off-state TDDB stress with different gate-length L_G and as a function of drain voltage V_{DS} and temperature [31]. Even without inversion layer build-up, the carriers can be injected from drain edge by impact ionization and favored by gate-induced drain leakage (GIDL) and band-to-band tunneling (BTBT) combination, which may create defects at the interface and into the volume gate-oxide until triggering dielectric HBD. **Figs.6a,b** show that Off-state TDDB increases with L_G without changing markedly Weibull slope β value for both N- and P- FET FDSOI devices, where in this latter one have much higher β value.

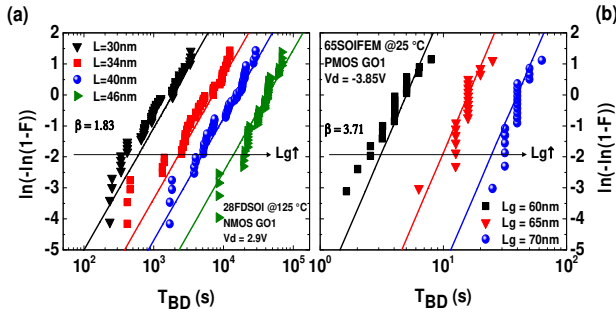


Fig.6: TDDB time to failure distribution for different FET gate lengths at fixed drain voltage (a) 28FDSOI NFETs $W = 1\mu\text{m}$ for $V_{DS} = 2.9\text{V}$ and (b) 65nm SOI PFETs $W_G = 10\mu\text{m}$ for $V_{DS} = -3.85\text{V}$. Breakdown occurs later for longer devices under same stressing voltages.

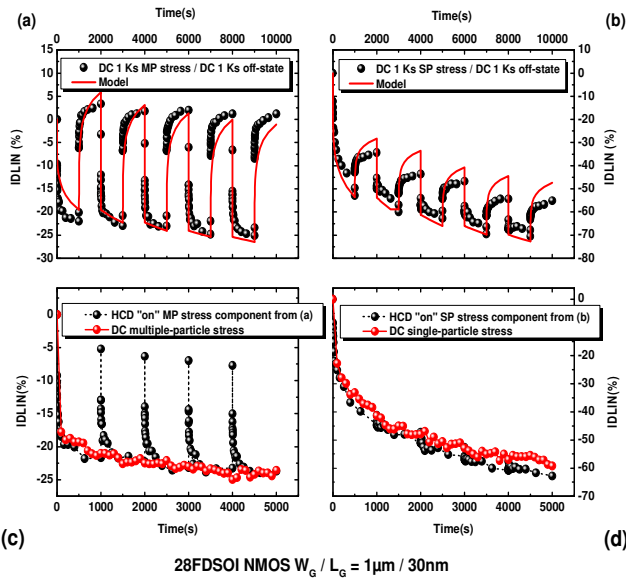


Fig.7: Alternating $t_s = 10^3\text{s}$ (DC) sequences performed in low frequency (LF) range compared to the corresponding modelling (red lines) in 28FDSOI NMOS $L_G = 30\text{nm}$. (a) HCD-MP at $V_{DS} = 0.9\text{V}$, $V_{GS} = 2.2\text{V}$ alternated to Off mode $V_{DS} = 1.8\text{V}$ and $V_{GS} = -1\text{V}$. (b) HCD-SP at $V_{DS} = 1.9\text{V}$, $V_{GS} = 1.4\text{V}$ alternated to Off-mode $V_{DS} = 1.8\text{V}$ and $V_{GS} = -1\text{V}$. Cumulative ΔId_{Lin} are extracted from HCD phases between alternating DC “On/Off” in (a) and (b) and compared to pure DC HCD only. Alternating (c) “MP/Off mode” to DC HCD MP and (d) “SP/Off mode” to DC HCD SP is shown with the corresponding stressing voltage condition.

In order to evidence potential interaction between On mode and Off mode, alternated DC (**Fig.7**) and AC (**Fig.8**) stress sequences have been done. In this manner, HCD with high energy carriers are involved at $V_{DS} = 1.9\text{V}$ and $V_{GS} = 1.4\text{V}$ under field driven where single particle (SP) leads to classical HCD [17], [18]. Low energy carriers are involved at $V_{DS} = 0.9\text{V}$ and $V_{GS} = 2.2\text{V}$ under current driven phenomenon where multiple particle (MP) mechanism leads to Si–H bond breaking [19], [27], while Off-state stressing is involved at bias $V_{DS} = 1.8$ and $V_{GS} = -1\text{V}$. We show the stressing alternance of DC MP to Off mode and from SP to Off mode in **Figs.7a,b** compared to the modeling (lines) giving relative good agreement with (3a)-(3d). We also compare the extracted HCD MP and SP phases in **Figs. 7c,d**. It is shown that Off mode does not introduce aggravation in the successive HCD parts that remain cumulative and matches the DC results only.

Low frequency (LF) with $F = 0.1\text{Hz}$ and high frequency (HF) with $F = 100\text{KHz}$ AC stressing have been compared in **Fig.8** to pure DC MP (10^4s) and to alternated phases using DC MP to Off-state measurements using 10^3s quasi-static sequences [12]. AC pulse trains are composed of successive “On” and “Off” mode stress with two kinds of sequences, either ending with “On mode” stage or else ending by “Off mode” stage. We show that the magnitude of ΔId_{Lin} measured at LF depends on the signal configuration, because AC pulses ending with Off-state characterizes the reached level of the degradation named here high level (HL). This has been calculated quasi-statically with (3b) with respect to the low level (LL), considering a net compensation in ΔId_{Lin} due to hot-hole trapping using expression (3c).

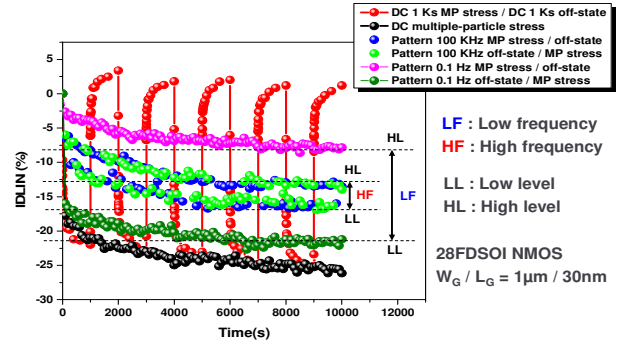


Fig.8: Several AC (DC) sequences between 0.1 Hz and 100 kHz, alternating HCD multiple particle (V_{GS} at high level) and Off-mode stressing (low level) and done in the reverse order, as a function of pulse duration and voltage level of the stressing pulses.

We show in **Fig.8** that when AC signals end with HCD in On-state, the generation of permanent defects become dominant inducing a larger effect on ΔId_{Lin} corresponding to LL dynamics with (3d). Moreover, a maximum of recovery occurs after alternating MP HCD (M3 mode) to “Off mode” with respect to SP HCD switched to Off-mode sequences. In the next subsection a straight method is presented to decouple stress and sensing temperature impact based on ΔId_{Lin} extraction.

B. Sensing effects in short channel LP MOSFETs

Another challenge in ageing device modeling is the effect of sensing temperature on the residual drift. As a general approach, MOS transistor parameter drift measured at various stress voltages is renormalized to a common junction temperature using an apparent activation energy (E_{App}). It comes out that such approach can induce significant errors since the sensing temperature itself can represent up to 50% of the apparent measured E_{App} value, as previously explained in [10]. For the sake of illustration, the I_{dLin} drift is reported in Fig. 9 versus the sensing temperature for N-channel MOSFETs with thick gate-oxide (GO2) obtained from LP 40 CMOS node.

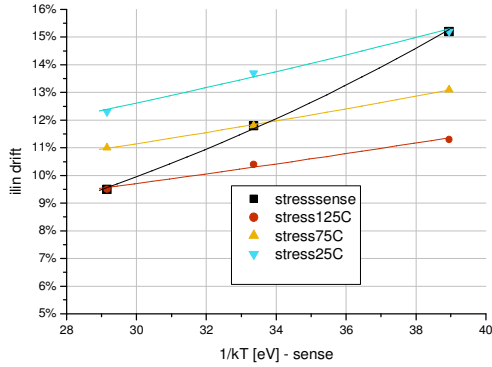


Fig.9: I_{dLin} drift vs. sensing Temperature for N-channel thick gate-oxide (GO2) Input/output devices LP 40nm node stressed between 25°C and 125°C.

It has been shown that in general, HCI drift is higher at low stress temperature for N-FET and at high temperature for P-FET. At the same time, I_{dLin} drift always increases with sensing temperature, while V_{Th} drift does not depend so much on sensing temperature for the same stressing type, due to the larger mobility variation with sensing temperature than V_{Th} [10].

IV. CIRCUIT RELIABILITY FOR PRODUCT QUALIFICATION

With the increasing requirement of low power SOC design without compromising performance, and vice versa, the need to support Dynamic Voltage Frequency Scaling (DVFS) Technique at SOC is growing. DVFS aims to improve Power-Delay product by adjusting the supply voltage (V_{DD}) and frequency (F_{AC}). It results the necessity to develop an accurate and predictive impact modeling of reliability for any design of components, and thus a dedicated qualification flow.

A. Digital and SRAM illustrations

This section intends to illustrate some examples of reliability effect at digital and SRAM circuit level. The aim is to highlight standard approach of qualification with discussing the current challenges.

The intrinsic reliability of digital logic function is usually guaranteed through consideration of timing margin (either dedicated corner or global derating factor). At cell level, the

adequation between model and measurement in aged state needs to be validated in any process, voltage, temperature (PVT) corners used in implementation. Illustration of this correlation is presented in Fig.10 for a logic cell drift at different V_{DD} , temperature and ageing time. The challenge is to consider in the device model all the possible stress and relaxation configurations (especially relaxation with positive V_{DS}) but also after implementation, the sign-off scenario of the worst-case for hold and setup timing violations.

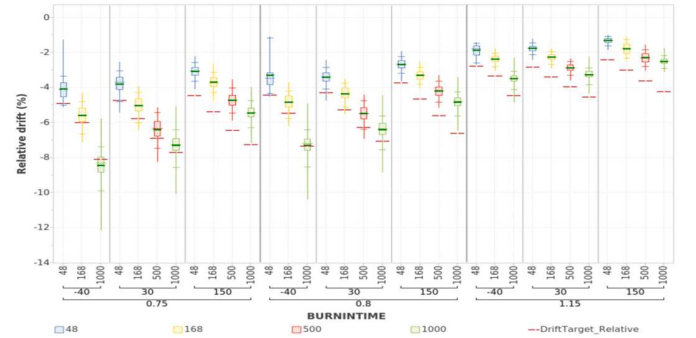


Fig.10: For a given logic cell, evolution of the measured drift (box plot) and ageing simulation for various supply voltage V_{DD} , temperature and time.

SRAM blocks represent nowadays a large portion of SOC applications. Applying DVFS means to reduce the supply voltage V_{DD} , but this tends to increase the risk of single bit fail due to degraded stability and writability. The degradation in stability and writability is also dependent on other factors like global, local variations, especially in temperature and ageing. Hence, it is important to analyze the distribution of minimum operational voltage (V_{min}) in SRAM and to determine the limitation of V_{min} in different stressing and sensing conditions. As shown in Fig.10, SRAM V_{min} can be limited by Dynamic Noise Margin (DNM) during read operation at hot ($T=140^\circ\text{C}$) or it can be limited due to Dynamic Write Margin (DWM) at cold (-40°C) or room temperature.

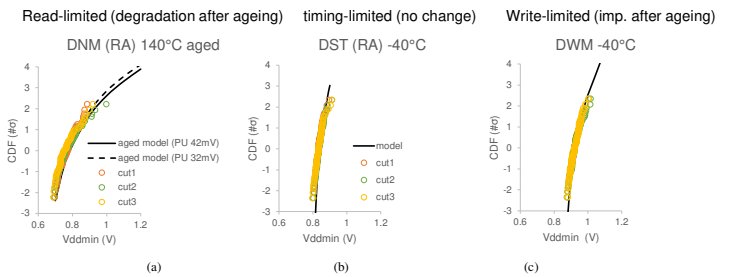


Fig.11: SRAM V_{min} distribution at hot can be predicted by the model, read limitation at hot (42mV degradation of pull-up after ageing) (a). With read assist, at cold, it can be self-timing limited (b) and write limited without assist (c).

The advantage of V_{min} distribution analysis can be multi-folded in case of a good correlation with silicon, where not only Spice modeling but also memory design & chip design can truly represent CAD behavior. As shown in Fig.11 in solid lines, using the modulation of some key Spice parameters and design, the silicon V_{min} distribution can be represented even at CAD level. Using this approach, the CAD V_{min} distribution can be predicted

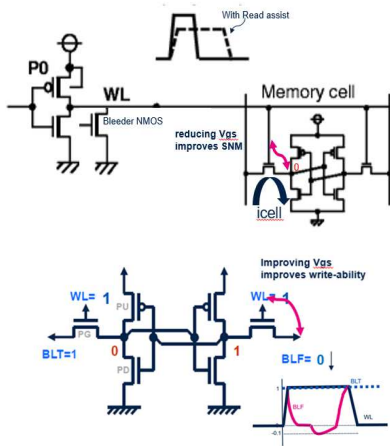


Fig.12: Schematics for the Read assist in memory design with WL lowering (top). Write assist with BL lowering (bottom).

for any mission profile, or it can be further explored to process changes, or design modifications like the usage of Read / Write Assist to improve V_{min} distribution. The usage of Read Assist is shown in **Fig.12** by reducing the Word Line (WL) Voltage level to improve the SBFs related to DNM, also by using write assist (BL Lowering). The bit cell can thus reach good writability at low voltage. For read-limitation V_{min} , read assist can be used to compensate ageing degradation while write-limited V_{min} tend to be improved after ageing.

B. Analog IP illustrations

Finally, the last illustration deals with analog circuit. In the context of the examination of analog IP reliability, stressing results are presented in Analog to Digital Converter (ADC). A burn-in is performed during 100h with a dynamic pattern on several samples on three ADCs, two 10 bits 1MSP/s and one 12 bits 5MSP/s ADCs with similar manufacturing processes. Stresses were used by increasing the supply voltage by 40% and 60% and the temperature was raised to 125°C. The subsequent drift was compared to reference samples in order to exclude any influence of the measurement setup. The 1MSP/s devices do not

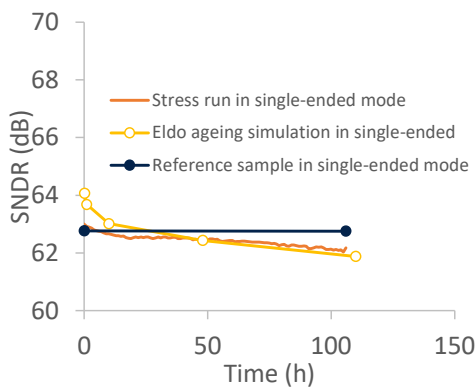


Fig.13: Evolution of SNDR during burn-in time, compared to simulation and to a reference part that remains un-stressed.

exhibit any drift to the stress condition whatsoever. Indeed, the stress was not sufficient to overcome the large design margins. However, the 5MSP/s ADC is showing a sensitivity on output dynamic parameters. Indeed, SNR is known to be sensitive to ageing [32]. A drift in single-ended mode was then observed in **Fig.13** and can be explained by the simulations. A deeper analysis shows that comparator noise is degraded during ageing and can affect resulting SNR.

We emphasize that care must be taken to obtain a good correlation with fresh device, to accurately assess both simulations and measurements corresponding variation. Any disparity - sampling, number of harmonics, supply voltage, saturation margins - may easily bring some discrepancies. To help in bridging any offset between measurement and simulation, a noise model was implemented which highlighted a 20% drift in the comparator noise over a period of one month. Although its contribution was overshadowed by quantization noise, it is one of the factors inducing a shift in the ADC performance that will motivate comparator design improvement for the future.

In a similar context, reliability of a regulator for power management is now investigated with an industrial qualification standard. With dedicated analog burning board, 1000h OLT was done in **Fig.14** at 125°C on Low Drop Out (LDO) circuit with static current load and supplied overvoltage. It results in a slight variation of output regulated voltage, which is accurately reproduced by simulation as well.

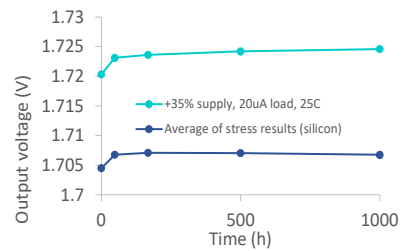


Fig.14: Evolution of output voltage in LDO circuit during 1000 h stress time, comparison is done between measurements versus simulations.

Interestingly, Operational Lifetime Test (OLT) conditions were chosen to induce the strongest possible stress effect that the models would allow, and then related to the drift caused by a differential pair where both transistors were degrading at different speeds, causing an offset, which was then amplified by the closed loop circuit. This explanation is consistent with simulated degradation at device level which matches the output variation, enabling the computation of the end of life for the circuit. As a conclusion, OLT conditions must be carefully chosen to represent a realistic stimulus, and to be confident with the fact that the observed degradation is related to the real stress condition and not triggered by abnormal stressing behaviors.

V. CONCLUSION

Last CMOS nodes fabricated with various drain architectures on LP Si-bulk and FDSOI HKMG, have been compared about

aging phenomena under main Wearout mechanisms, represented by BTI, HCD and HBD issues. Accelerated stressing have been presented from DC, alternating DC in MOSFETs, till AC degradation, to decouple the main degradation mechanisms. Cares have been taken to distinguish the sensing effect, neutralization and/or compensation effects for the damage, when these are involved depending on the variation of the stressing signal patterns, or temperature for sensing and stressing. Challenges both at device and circuit level modeling have been enlightened through some examples, that have been discussed using operational lifetime tests for IP qualification based on advanced CMOS nodes for digital and analog applications.

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