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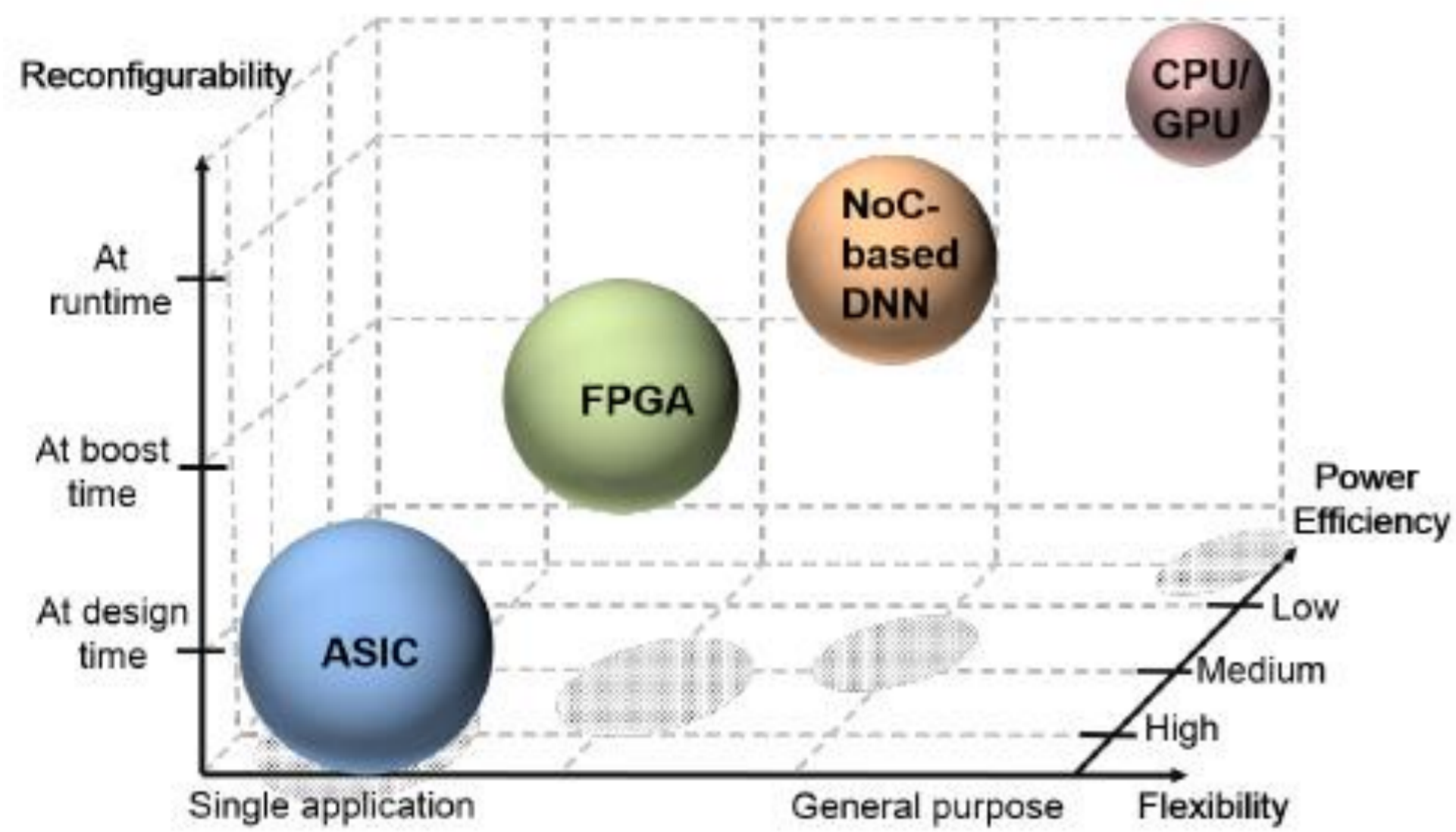
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Motivation

NoC-based AI accelerators

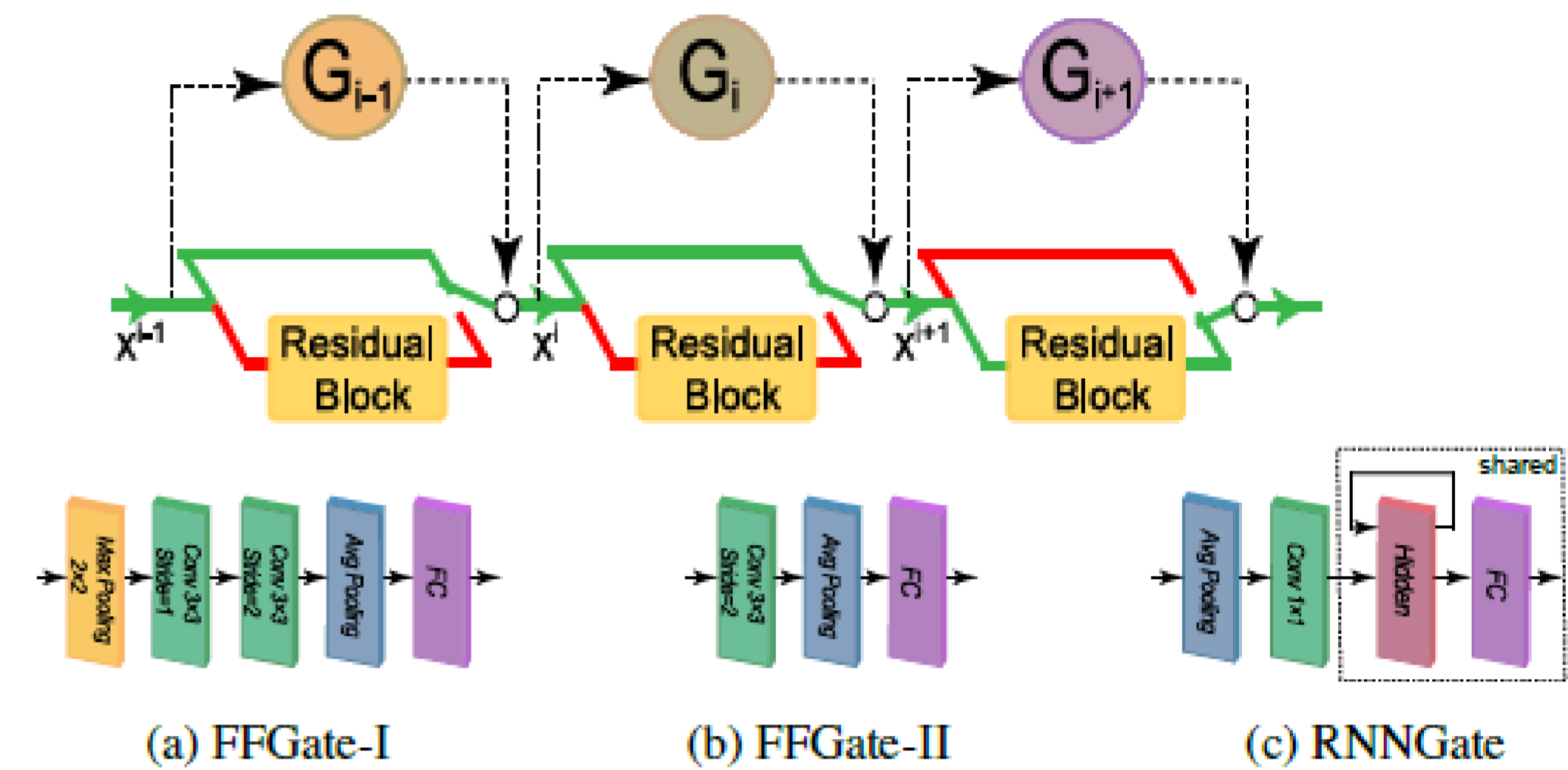
- Rise of AI and dedicated hardware architectures
- NoC-based AI accelerators decouple communication from computation for more flexibility and energy efficiency [1]



Flexibility and reconfigurability of current DNN accelerator design paradigms [1]

Dynamic Neural Network

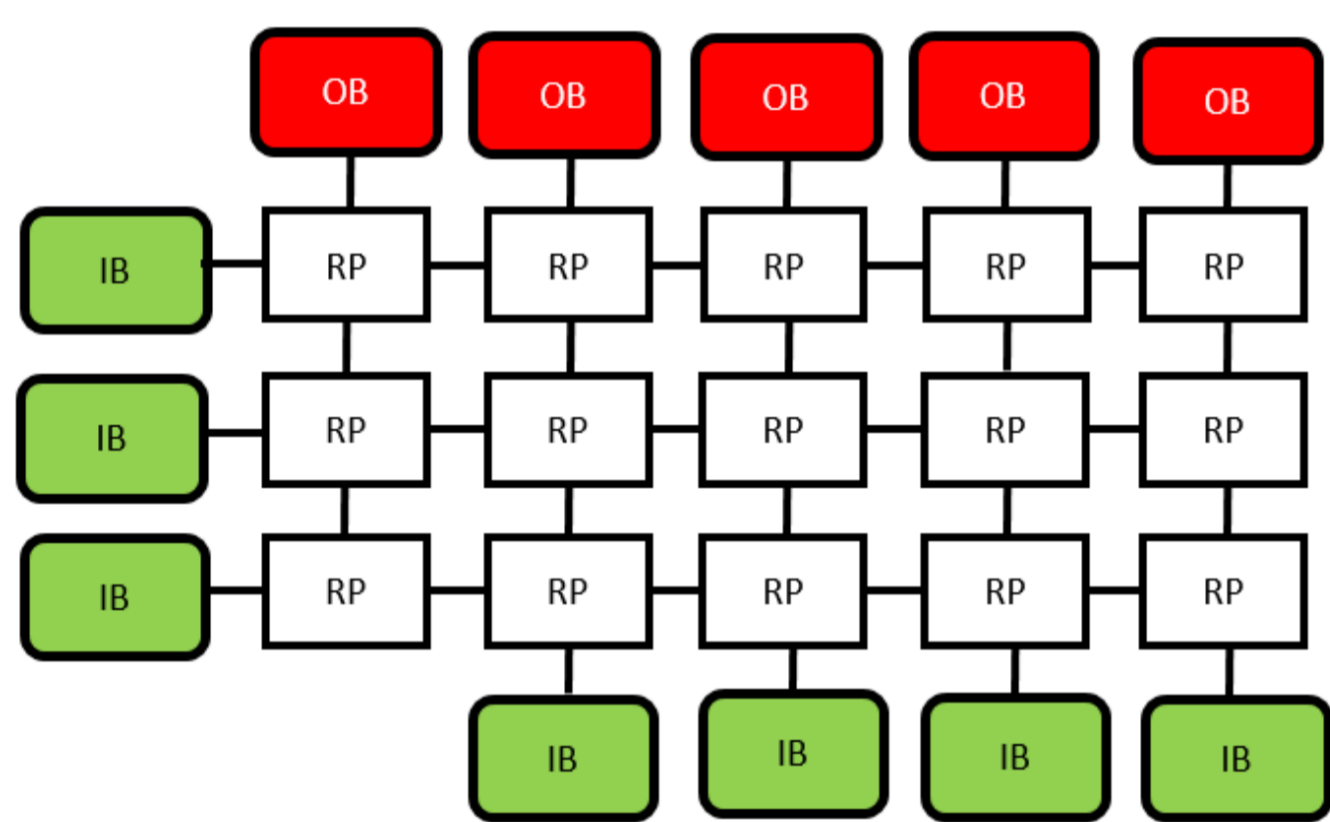
- Dynamic Neural Network : Computational graph or parameters depend on the input [2]
- SkipNet [3] : Layer skipping mechanism



Gating mechanism and Gates design in SkipNet [3]

Modeling

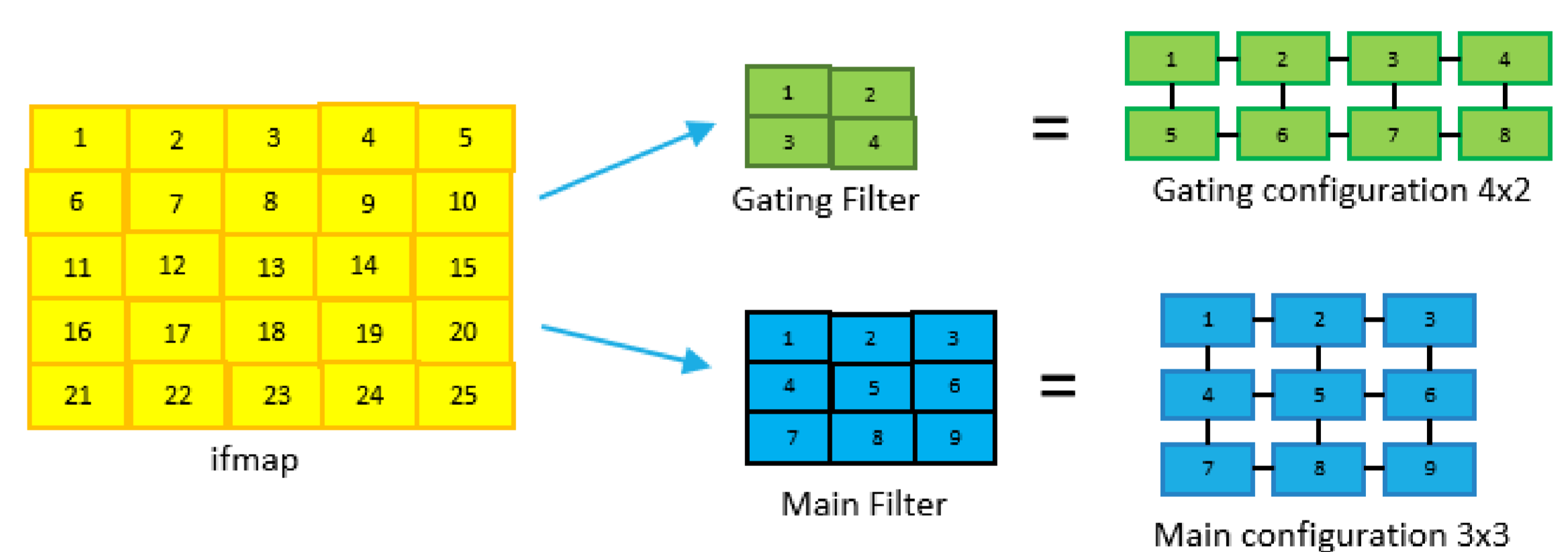
AINoC based architecture



5x3 configuration of AINoC

- AINoC[4]: reconfigurable NoC
- Row stationary dataflow [5]:
 - Filters: horizontal multicast
 - Input feature map: diagonal multicast
 - Output feature map: vertical accumulation

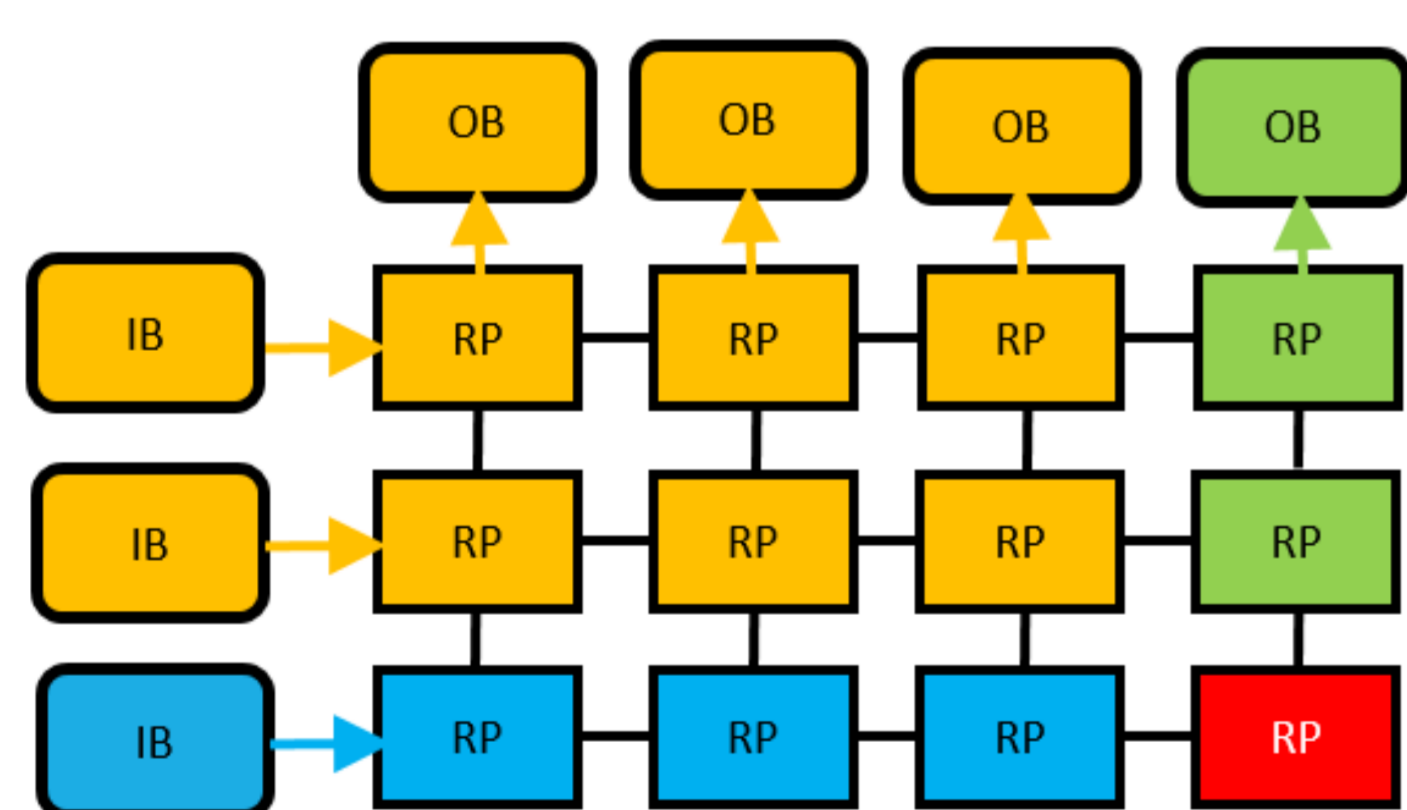
SkipNet Mapping on the architecture



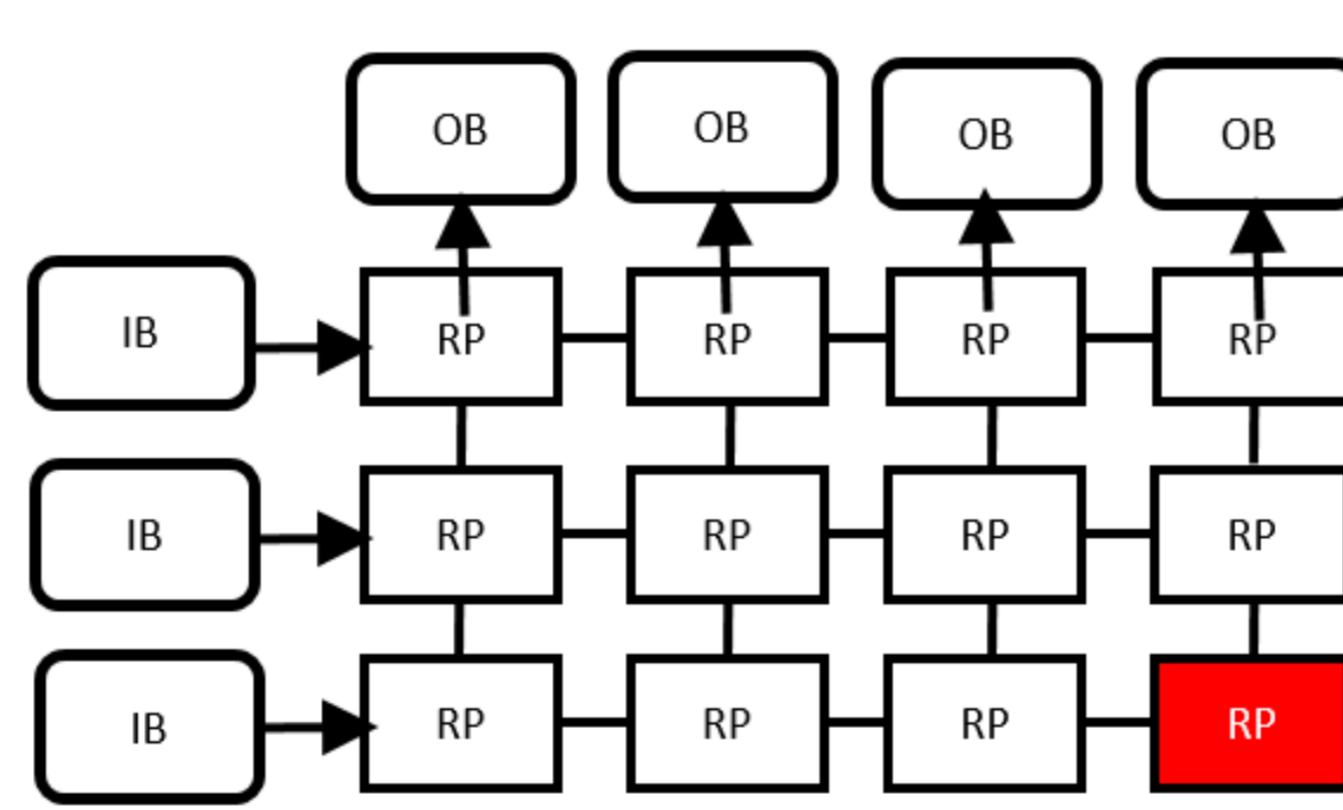
Mapping example of SkipNet over the architecture

Comparative study

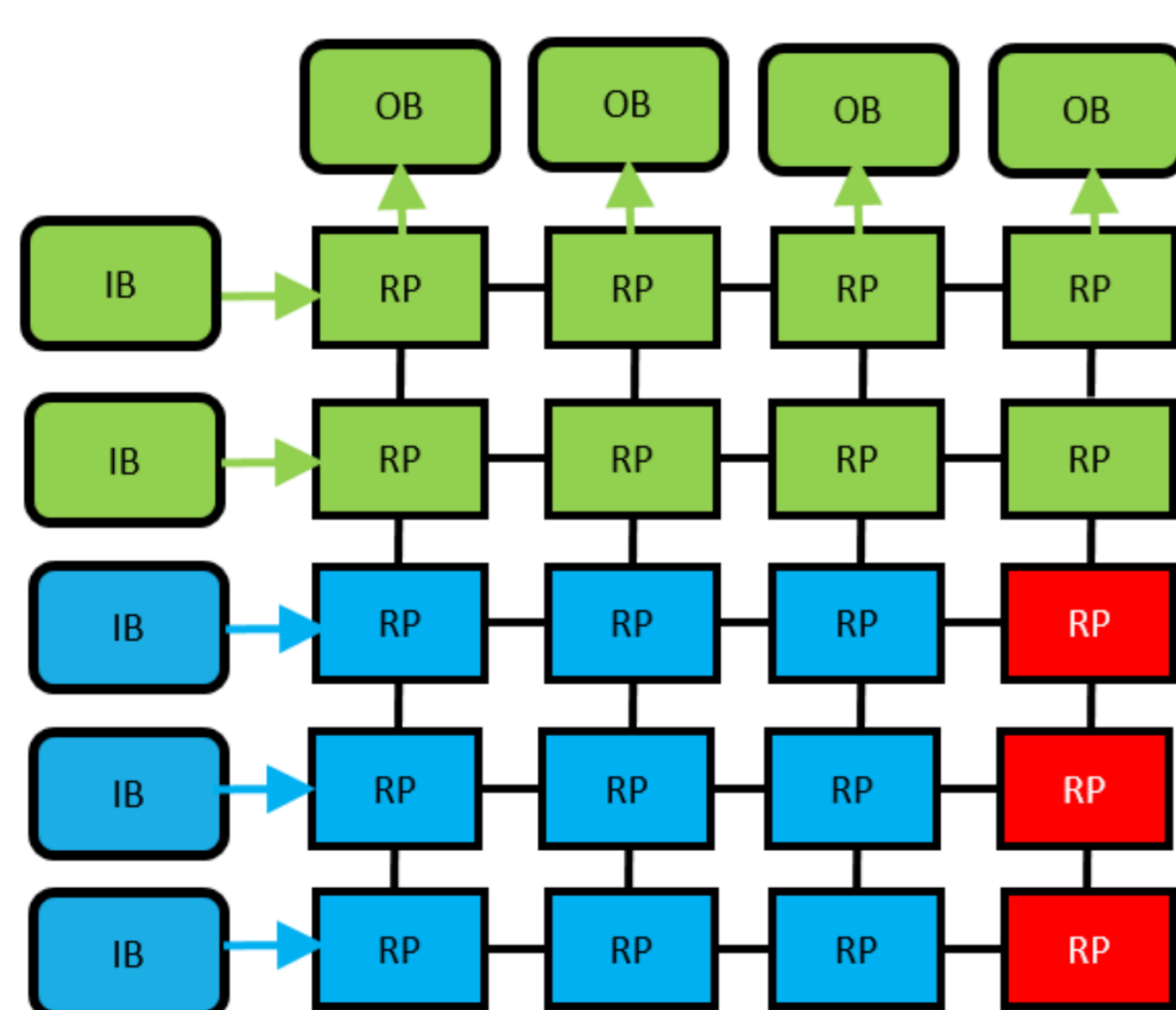
Mapping techniques



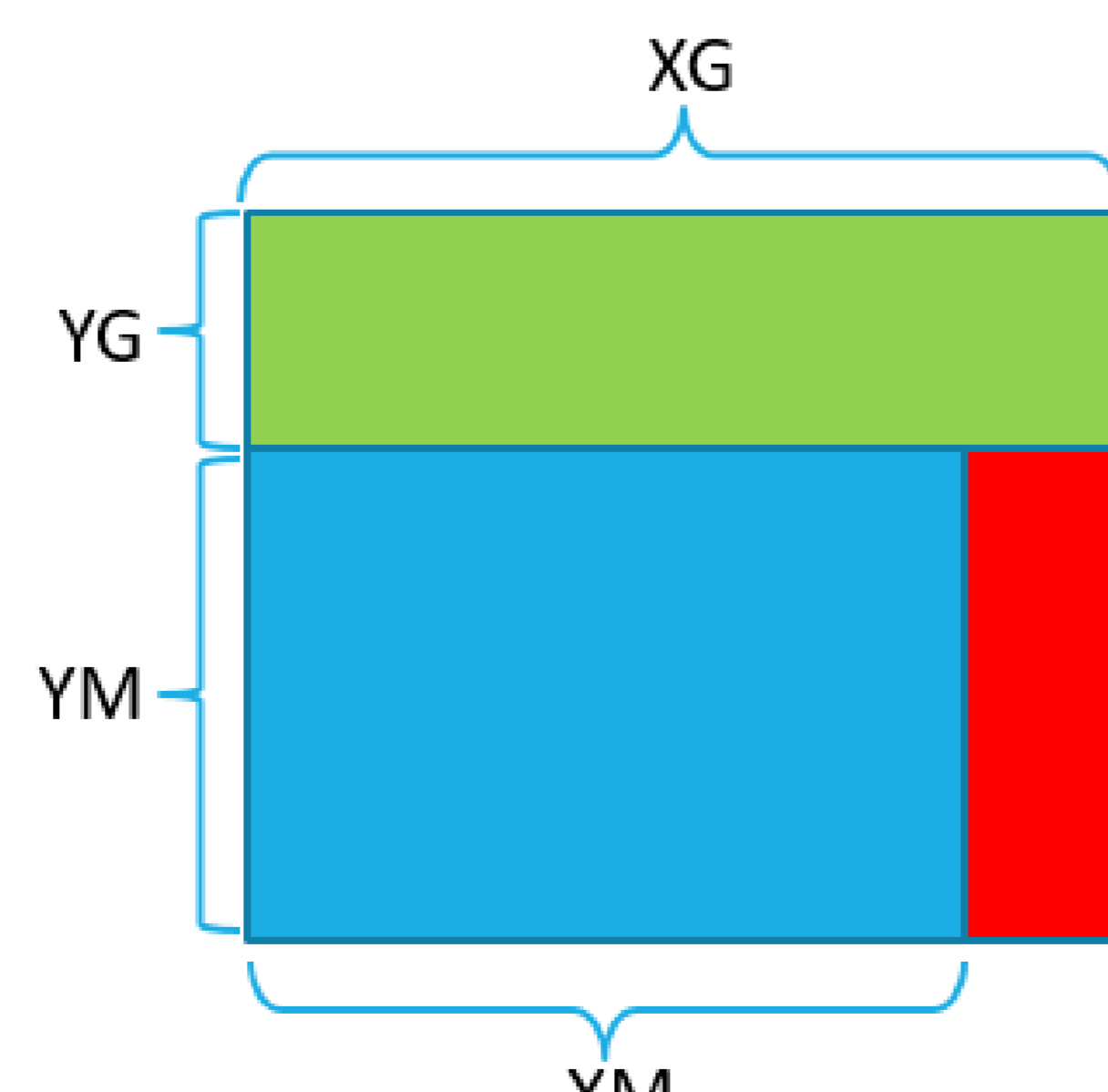
Shared resource + parallel execution



Shared resource + sequential execution



Clustering



Clustering method analysis

■ Gating convolution only ■ Main convolution only ■ Simultaneous gating and main convolutions ■ Non used component

Latency analysis

	KO	OK
Clustering	XG+YG+XM	YG+max(XM+YM,XG)
Shared parallel	XG+YG+XM	max(XG+YG,XM+YM)
Shared sequential	XG+YG	XG+YG+XM+YM

Resource analysis

	Non used PE %	Resource size
Clustering	High	Small
Shared parallel	Low	Large
Shared sequential	Low	Small

References

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