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p-GaN HEMT Hard Switching Fault Type Short-Circuit Detection Based on the Gate Schottky-Barrier Leakage Current and Using a Dual-Channel Segmented CMOS buffer Gate-Driver

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Abstract— This article presents an alternative solution to the short circuit challenges commonly faced by ultra-fast power transistors. Specially 650V p-GaN HEMTs, where the short-circuit timing capability is very critical, and the presence of thermal run-aways is very sensitive. In response to this issue, a dedicated approach to detect the short-circuit inserting an on-line monitoring gate-resistor through a dual-channel segmented CMOS Gate Driver is proposed. The short-circuit indicator under Hard Switch Fault is based on the Gate-Schottky-Barrier leakage current, which is translated on a voltage drop at the gate-source voltage. The detection circuit can be fully integrated in the IC with a low monitoring voltage. A dual-buffer IC prototype including impedance state and monitoring integrated circuit using XFAB XT018 0.18um CMOS SOI technology was performed. Parametric results show a robust and quick detection propagation delay around 580ns under $V_{DS} = 400V$ and $V_{GS} = 5V$.

Keywords—Active Gate Driver, p-GaN HEMT, CMOS, Short-Circuit, Hard Switching Fault, Detection, Thermal run-away, On-line monitoring.

I. INTRODUCTION

Technological process to develop GaN power devices are being actively explored [1] in different applications due to their lower conduction and switching losses, and small size and level of integration [2]. However, the switching frequencies are extremely high and with lower ON-State resistance and smaller intrinsic parasitic capacitance, the Short-Circuit Fault (SCF) detections using state of art methods start to be extremely difficult.

Under short-circuit fault, 650V p-GaN gate devices must be protected in less than 1 μ s when used at nominal drain-source voltages and even faster in the case where a high gate-voltage is applied [3]. Moreover, the devices must be quickly protected if several SCF cycles must be accepted without device ageing [4]. In this article, an original approach is proposed. It is based on the detection of an abnormally high gate Schottky-barrier leakage current from the metal/p-GaN AlGaIn/GaN stack region [5] and using a dual-channel segmented gate-driver. In [6, 7] A. Borghese *et al.* suggest to use the high gate-leakage temperature dependence to perform an interesting quasi-linear fast thermal detection for overload operation but SCF management was not fully explored and developed by authors. In [8] X. Zhang *et al.* take advantage of the gate-leakage effect on the gate voltage drop to detect SCF but using a SMD common one-channel gate driver which does

not allow a good trade-off between fast switching detection sensitivity and immunity to false failures.

In this article, a first gate-channel supports the switching while a second gate-channel monitors the leakage current by inserting a dedicated high value gate resistance (typically $\times 100$ the first channel's one) just after the end of the switching. A thresholding of the gate voltage drop allows to detect directly SCF in less than 600ns @ $V_{DS} = 400V$ using a 0.18 μ m SOI segmented CMOS buffer IC developed by the authors using XFAB™ technology. Compared to [8], this approach presents an interesting compromise between speed, immunity, adjustment flexibility with a high integration capacity of an essential function. Although IC segmented gate-driver has already been used in the past to optimize switching shape as proposed by J.S. Yu *et al.* in [9], such an architecture is here declined for the first time to manage powerfully SCF detection. The article is organized as follows: in section II.A. the gate-driver architecture and the IC prototype are described, in section II.B. the control signals configuration is depicted, finally section III. highlights the experimental validation.

II. PROPOSED ARCHITECTURE

A. Schematic and Circuit

In Fig. 1, the power circuit and the proposed dual-channel CMOS buffer architecture are detailed. The figure exhibits the switching High Side/ Low Side buffer-transistors pads, T_{HS-SW}/T_{LS-SW} , the monitoring buffer-transistor pad $T_{HS-Monitoring}$ and the Soft-Shut-Down pad, T_{LS-SSD} . DUT is an enhancement mode Schottky-type-gate 650V-25m Ω @ $T_{CASE} = 25^{\circ}C$ p-GaN Systems™ GS61516B device. D_{FW} is a free-wheeling SiC Schottky-barrier-diode, L_{DP} is a high bandwidth double-pulse inductor, and R_{SENSE} is a high bandwidth shunt current sensor for I_{DS} measurement. D1 symbolizes the physical metal/p-GaN Schottky-barrier-diode in series with D2 the p-AlGaIn barrier layer/GaN epi-layer PIN-type diode of the gate-stack [5]. $R_{G-ON/OFF-SW}$ (10 Ω) are the normal switching gate resistances used, $R_{G-Monitoring}$ (1k Ω) is the dedicated additional "sense" resistance, to detect the abnormally high gate leakage under SCF, and R_{G-SSD} (100 Ω) is the soft turn-off gate-resistance triggered only if a SCF is detected for a soft shut down (SSD). A discrete SMD comparator – opto-isolator set allows the monitoring of the gate voltage drop and feedbacks on the gate-driver IC as soon as the gate leakage appears. All control signals configuration, Hi-Z signal and flag detection are managed by a FPGA host as a first demonstration and for better

flexibility. Fig. 2 (a) and (b) show photos of the designed "easy-to-use modular plug-in" boards to experimentally evaluate the functionalities and performances of the proposed solution. Fig. 3 (a) shows a Cadence™ layout overview and Fig. 3 (b) an optical microscope photo of the dual-channel segmented ($\pm 2A$ and $\pm 1A$) CMOS buffer fabricated using $0.18\mu m$ SOI XFAB™ technology (XT018) with tri-state 40V max output stage, integrated level shifters and dead time management. The dedicated design can be found in Y. Barazi's *Ph.D.* manuscript [10].

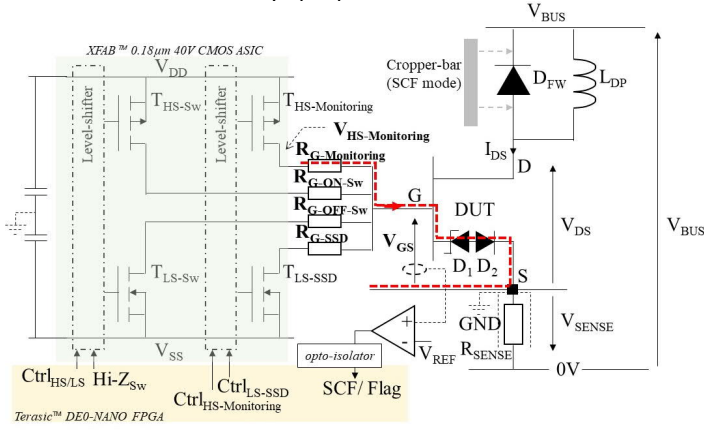


Fig. 1. Schematic diagram of test power circuit, p-GaN HEMT DUT and the proposed segmented gate-driver including $R_{G-Monitoring}$, exhibiting D_1 gate leakage detection (in red dotted line).

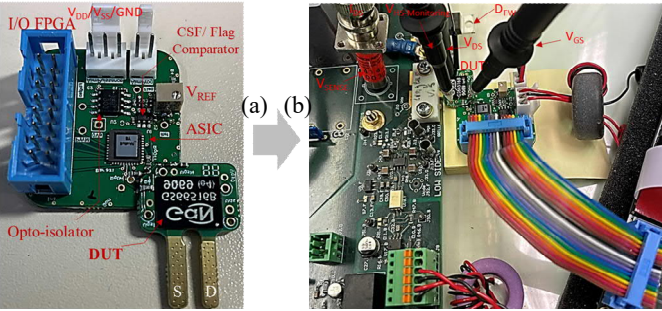


Fig. 2. (a) overview of the segmented gate-driver and p-GaN DUT modular (b) plug-in daughter-boards and test power circuit mother-board.

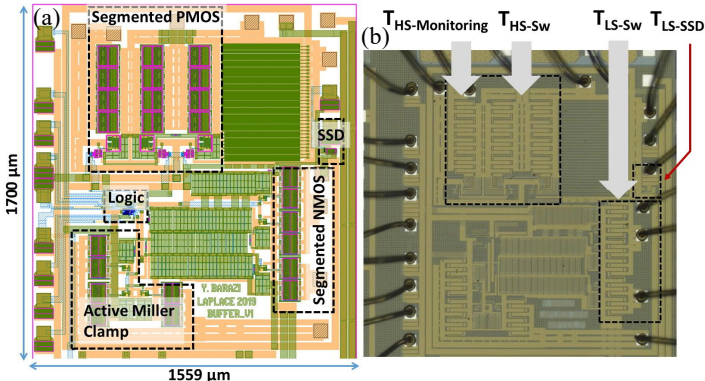


Fig. 3. (a) layout with selected layer-view under Cadence™ of the segmented CMOS gate-driver, (b) microscopic view of the fabricated chip.

B. Control signals management – Concept basic analysis

A complete timing diagram set is depicted in Fig. 4. The diagram timing selection is configured and automatized by the FPGA. Each case will be re-used and deeply experimentally analyzed in section III. Basically, for the switching, $R_{G-ON/OFF-Sw}$ will be the only gate resistors used. The approach we are proposing is different because the purpose is also to detect the continuous voltage drop in on-

state due to the Schottky-barrier gate leakage increase if a SCF occurs.

Fig. 4 (a) deals with the normal operation, which also includes the monitoring: the switching $R_{G-ON/OFF-Sw}$ is used on the turn-on and the turn-off for only a determined timing $\Delta T_{Sw-ON/OFF}$ using $Hi-Z_{Sw} = 0$. Afterwards, the monitoring resistor $R_{G-Monitoring}$ is inserted using $Hi-Z_{Sw} = 1$ to monitor the possible SCF event between the turn-on and turn-off without affecting switching speed and the normal operation due to a low gate leakage.

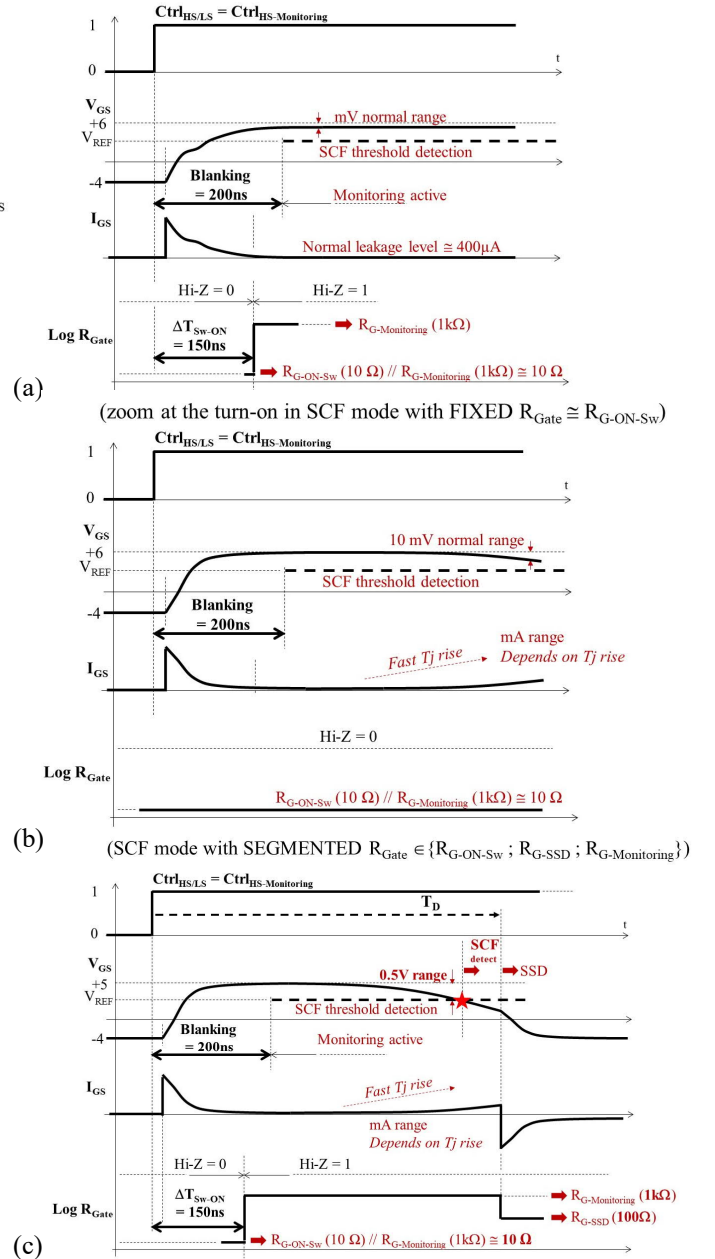


Fig. 4. Timing diagram set and selection (a) normal double pulse operation, (b) SCF monitoring with R_{G-Sw} ON, (c) SCF monitoring with $R_{G-Monitoring}$.

Fig. 4 (b) depicts a SCF operation using only switching $R_{G-ON-Sw}$ by a permanent $Hi-Z_{Sw} = 0$, which represents the classical driving approach: the voltage drop is not enough to cross the SCF threshold detection. It will not be detected or at best at the end of the on-state cycle but depending on the duty ratio and then a SSD will be lately activated. Clearly, this results in a much longer time to

protect the device from ageing effect. The optimal case in SCF operation is now depicted in Fig. 4 (c), which includes the proposed monitoring method: $R_{G\text{-Monitoring}}$ is inserted just after $\Delta T_{\text{Sw-ON/OFF}}$ as presented in Fig. 4 (a). The voltage drop will be now significantly higher, and the detection will be earlier.

III. EXPERIMENTAL VALIDATION

A dedicated power test bench illustrated in Fig. 2 (b) is used to experimentally validate the proposed gate-driver architecture. The DUT (Device Under Test) and the gate-driver daughter boards are plugged on the low side of a phase-leg power test bench. On the high side of the power test bench, a connection was made between the drain and source electrode of the upper device of the leg by using a copper strap to force the HSF short-circuit behavior.

A. Normal operation

Firstly, in Fig. 5, a double pulse testing is applied using the timing diagram depicted in Fig. 4 (a). At turn-on, $R_{G\text{-On-Sw}}$ is enabled only for $\Delta T_{\text{Sw-ON}} = 150\text{ns}$ to cover the whole gate voltage transient period, then the $R_{G\text{-Monitoring}}$ is enabled through the rest of the monitoring range. A 200ns FPGA blanking time is implemented in addition to allow a stable gate voltage monitoring and to avoid possible false SCF detection at turn-on. Due to a permanent gate Schottky-barrier leakage under the gate voltage bias ($\cong 400\mu\text{A}$ @ $V_{\text{GS}} = 6\text{V}$ at 25°C), a residual but low value continuous gate voltage drop ($\cong 400\text{mV}$) occurs through $R_{G\text{-Monitoring}}$. Then, the V_{REF} detection threshold must be adjusted to satisfy a practical immunity range to detect the gate voltage drop. The operation is safe and does not impact the control of the switching events.

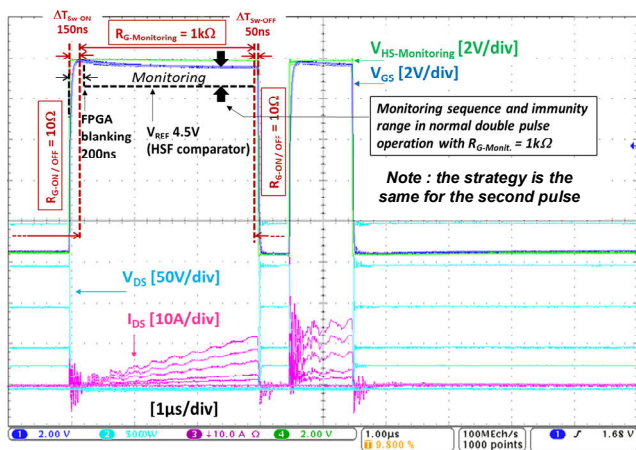


Fig. 5. Parametric normal double pulse operation tests exhibiting immunity range for monitoring sequence : $V_{\text{BUS}} = 200\text{V}$, $V_{\text{DD}} = 6\text{V}$, $\Delta T_{\text{Sw-ON}} = 150\text{ns}$, $\Delta T_{\text{Sw-OFF}} = 50\text{ns}$, $\text{FPGA}_{\text{Blanking Time}} = 200\text{ns}$, $V_{\text{REF}} = 4.5\text{V}$.

B. Short-circuit Fault Operation: using $R_{G\text{-On-Sw}}$

Fig. 6 shows a first SCF test using the timing diagram depicted in Fig. 4 (b) (classical setup). In this mode, $R_{G\text{-On-Sw}}$ (10Ω) is directly re-used to monitor the gate voltage drop after the turn-on. V_{GS} waveform clearly shows that such a small gate resistance is not able to produce a sufficient gate voltage drop to be quickly detected. The gate voltage drop may be significant and detectable but only with a high duty ratio leading the device under high temperature and with ageing effects, reducing the life-cycle of the device.

However, the slight drop gate voltage yields a I_{DS} reduction that increases the robustness under repetitive SCF cycles.

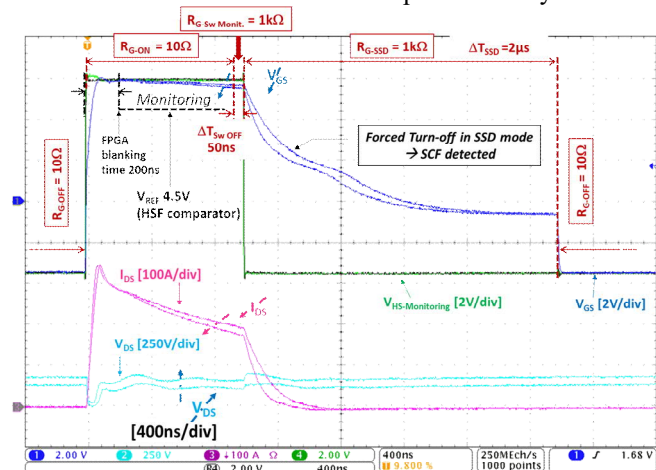


Fig. 6. Parametric SCF operation and monitoring with $R_{G\text{-On-Sw}}$, $V_{\text{DD}} = 6\text{V}$ @ $V_{\text{BUS}} = 150\text{V}$ and 200V , $\Delta T_{\text{Sw-ON}} = 150\text{ns}$, $\Delta T_{\text{Sw-OFF}} = 50\text{ns}$, $\text{FPGA}_{\text{Blanking Time}} = 200\text{ns}$, $V_{\text{REF}} = 4.5\text{V}$.

C. Short-circuit Fault Operation: using $R_{G\text{-Monitoring}}$

Fig. 7 shows a second SCF test using now the final timing diagram depicted in Fig. 4(c). Using a dedicated $R_{G\text{-Monitoring}}$ ($R_{G\text{-On-Sw}} \times 100$) a large and stable gate voltage drop occurs and can be easily and quickly detected by the comparator – opto-isolator set which send feedbacks at the input of the CMOS gate-driver. The Fig. 7 shows stacked experimental waveforms under different V_{BUS} values, starting from 100V to 350V with a 50V step. The black curve is used as a reference of the applied signal, and as one can see the green curve V_{GS} is turn-off hence the SCF is detected. With the increase of V_{BUS} , the power dissipated by the DUT is increasing, temperature and gate-leakage are increasing too, leading to an increase of the gate voltage drop and finally protecting the device and even faster.

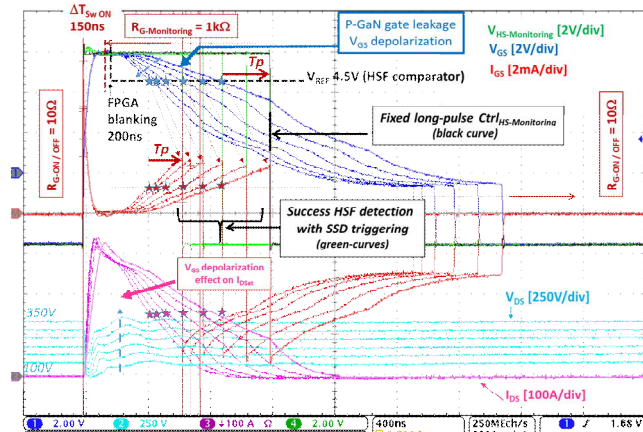


Fig. 7. Parametric SCF operation and monitoring with $R_{G\text{-Monitoring}}$ and success SSD triggering, Different V_{BUS} (100V - 350V), $V_{\text{DD}} = 6\text{V}$, $\Delta T_{\text{Sw-ON}} = 150\text{ns}$, $\Delta T_{\text{Sw-OFF}} = 50\text{ns}$, $\text{FPGA}_{\text{Blanking Time}} = 200\text{ns}$, $V_{\text{REF}} = 4.5\text{V}$.

It can be noted that due to an initially non-optimized hardware configuration a significant propagation time ($T_p \cong 300\text{ns}$, in Fig. 7) is visible between the $V_{\text{REF}} - V_{\text{GS}}$ after crossing and the Soft-Shut-Down triggering. This propagation time associated with a high gate voltage bias ($V_{\text{DD}} = 6\text{V}$ to optimize R_{DSON} in nominal on-state) leads the device to a very fast thermal runaway failure just at 320ns after the turn-on under $V_{\text{BUS}} = 400\text{V}$ as shown in Fig. 8.

Moreover, T_{LS-SSD} exhibits a great internal current limitation giving an ultra-soft-shut-down, as one can see in Fig. 7 and Fig. 8 (V_{GS} signal after SSD activation exhibits a very slow fall shape). This limitation is translated to $V_{GS} \cong -400\text{mV}$ instead of -4V in steady state, the value is due to the equivalent equation $V_{SS} + (R_{G-SSD} + R_{NMOS-SSD}) \times I_{GS-leakage-neg}$. To manage this limitation, the SSD command is bypassed by using the switching CMOS Low-side transistor T_{LS-sw} (off) after $\Delta T_{SSD} = 2\mu\text{s}$ using R_{G-OFF} .

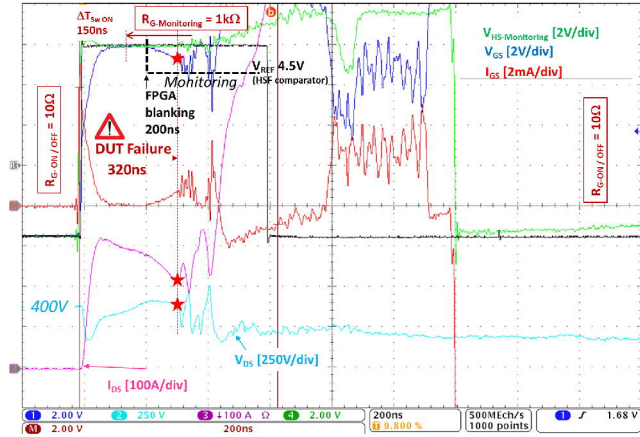


Fig. 8. SCF operation and monitoring with R_{G} -Monitoring, ultra-fast thermal runaway before SSD triggering, $V_{BUS} = 400\text{V}$, $V_{DD} = 6\text{V}$, $\Delta T_{Sw-ON} = 150\text{ns}$, $\Delta T_{Sw-OFF} = 50\text{ns}$, FPGA Blanking Time = 200ns , $V_{REF} = 4.5\text{V}$.

In Fig. 9, the gate bias is then reduced to $V_{DD} = 5\text{V}$ considering same V_{REF} but with a more optimized hardware sensing package, ΔT_p reduction $\cong 50\text{ns}$. This new gate-bias combined with the propagation time reduction helps to avoid such a failure and allow to reach the nominal drain – source voltage bias $V_{BUS} = 400\text{V}$ with only a total delay time of 576ns . One should note that the gate-source voltage drop is more significant at higher V_{BUS} , which makes the detections more robust and early.

Finally, in Tab. 1, the total delay time detection is measured in relation with V_{BUS} : higher the voltage, higher the temperature rise, giving a stronger gate leakage rate that is more quickly and significant to detect a SCF and keep the device in a safe mode.

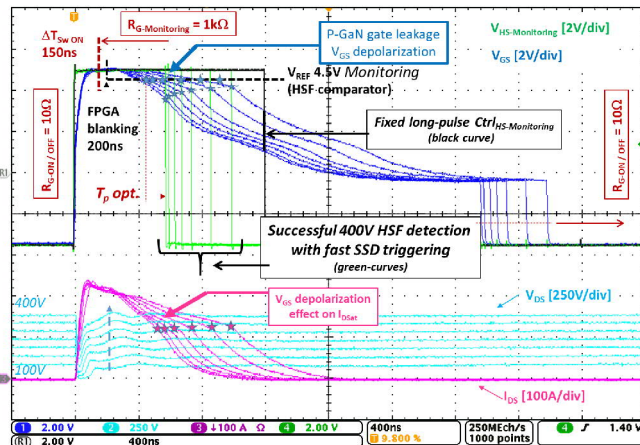


Fig. 9. Parametric SCF operation and monitoring with R_{G} -Monitoring, successful SSD triggering, V_{BUS} (100V-400V), $V_{DD} = 5\text{V}$ and optimized hardware detection (50ns T_p reduction), $\Delta T_{Sw-ON} = 150\text{ns}$, $\Delta T_{Sw-OFF} = 50\text{ns}$, FPGA Blanking Time = 200ns , $V_{REF} = 4.5\text{V}$.

TABLE I. TOTAL DELAY TIME (T_D) OF THE PROPOSED SCF DETECTION BETWEEN CTRL EDGE AND SSD TRIGGERING

V_{BUS} [V]	T_D [ns] ⁽¹⁾ $V_{DD} = 6\text{V}$, $V_{REF} = 4.5\text{V}$ Initial design Fig. 7	T_D [ns] ⁽¹⁾ $V_{DD} = 5\text{V}$, $V_{REF} = 4.5\text{V}$ Optimized design Fig. 9
100	1180	990
150	1070	864
200	884	740
250	752	680
300	692	636
350	640	596
400	Thermal run-away DUT failure @320ns	576ns

(1) Hardware detection includes comparator and opto-isolator between DUT and FPGA

IV. CONCLUSION

The proposed short-circuit detection based on a CMOS IC dual-channel gate driver has proven a fast and robust protection timing, around 580ns at $V_{DS} = 400\text{V}$ and $V_{GS} = 5\text{V}$ on a 650V HEMT p-GaN type device, without any impact of the control of normal switching transients. Thanks to the segmented architecture, a dedicated high value gate resistor can be inserted to on-line monitoring the Schottky-barrier gate-leakage current and the continuous drop gate-voltage to detect on an original way a hard short-circuit fault.

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