Integrated test circuit for off-state dynamic drain stress evaluation

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***Abstract*— Dynamic off-state stress for RF applications is investigated via integrated test circuits to enable GHz level testing. We have performed characterization of test circuits to ensure the dynamic stress signal waveform integrity, which is verified against model simulation data. We report a x2 gain on time-to-breakdown at 1GHz against DC TDDB off-state stress. Based on extraction of I_{Dlin} degradation, no frequency effect is observed from DC to 1GHz off-state stress conditions. Modeling of on-state and off-state interactions based on sum of degradations modes is then demonstrated and supported by experimental data.**

***Index Terms*-- Off-state reliability, Integrated test circuit, Dynamic stress, TDDB, Degradation modes.**

I. INTRODUCTION

Off-state leakage current (I_{off}) is becoming a critical reliability concern for both analog and digital circuits in deep sub-micron CMOS technologies. The downscaling of transistor dimensions has been necessary to accommodate the increasing chip density while enhancing the device's performance, precisely the on-current density I_{on}/W. The supply voltage V_{dd} and oxide thickness t_{ox} needs to be scaled accordingly to channel length and this incurs an increase in I_{off}. It has been reported in [1,2,3] that the off-state drain leakage current Id_{off} is dominated by band-to-band-tunneling (BTBT) current in the gate-to-drain overlap region when high gate-drain bias is applied to the device.

Static (DC) off-state stress has been investigated extensively in MOS and DeMOS devices [1,2,4], and in applications such as memory and logic gate circuits [5,6]. However, AC off-state degradation research is comparatively low and mainly limited to kHz and MHz frequencies, due to test signal integrity challenges caused by capacitive loading on the device input that influences high voltage periodic waveforms. For millimeter-wave (mmW) devices that drive high output power, i.e., power amplifiers (PA), drain voltage swings often exceed $2xV_{dd}$ when the gate-source voltage is below threshold voltage. This large gate-to-drain voltage V_{DG} bias can cause two reliability issues: parametric degradation (which impacts the RF performance) and device breakdown after long-term stress. Previous RF TDDB investigations of PA device in [7] has demonstrated RF TDDB at 1.8GHz under V_{DG} stress bias of x3 V_{DDNOM}, while no hard breakdown after 50ks of RF TDDB stress has been evidenced in [8] at 14GHz.

Based on our previous work in [9], we identified that the PA device is subjected to alternatively on-state and off-state stress when driven near to saturation output power at 28GHz, as shown in the PA mission profile in Fig. 1. In the case of on-state degradation due to hot-carrier injection (HCI), DC to RF degradations have been established via quasi-static approximations, enabling accurate estimations of RF aging models. On the other hand, accurate estimations of RF off-state degradations are more difficult to reproduce, given the lack of understanding on the frequency-dependent behavior of device parametric degradation at GHz level.

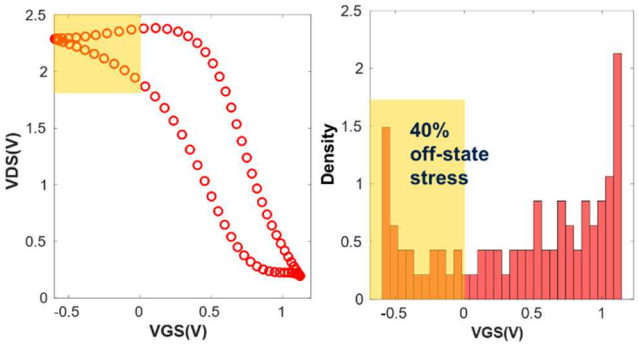

Figure 1: Mission profile of RF linear power amplifier (left) with off-state region at VG<=0 highlighted. The probability density function of this region (right) represents 40% of the total time in RF cycle.

The purpose of this paper is to investigate dynamic off-state stress at GHz frequency using a dedicated test structure featuring an integrated ring oscillator for pulsed waveform generation. Firstly, we perform DC and AC characterization of the test structure to demonstrate the validity of the generated stress waveform. Using this test structure, off-state AC TDDB data is provided in the form of Weibull distribution and parametric degradation of MOS transistor performance up to 1GHz will then be discussed. The interaction between on-state and DC/AC off-state degradations is then investigated experimentally and validated against reliability modeling strategies.

II. Test Structure Description

To overcome the limitations of conventional frequency generators of testing equipment at higher RF frequencies (>1MHz), on-chip frequency generators are necessary to reduce waveform distortion from propagation loss, i.e. attenuators (cables, probes, impedance mismatch) on the signal path to the device under test (DUT). The key interest of this integrated test structure is to generate a high pulsed voltage while maintaining the slew rate relatively high compared to the desired test frequency. This ensures a pulsed waveform with 50% duty cycle with minimum voltage overshoots.

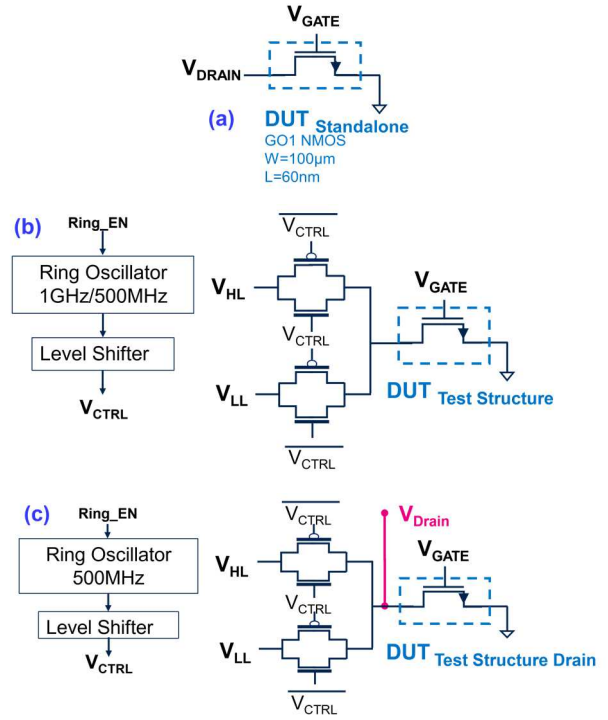

Figure 2: (a) Standalone DUT consisting of a body-contacted GO1 NMOS in 65nm PDSOI technology, RO test structures (b) without direct drain access (c) with direct drain access. DC and AC stress modes are applied to DUT drain terminal via transmission gates controlled by RO oscillation mode (Ring_EN).

The test structures, designed and fabricated in STMicroelectronics 65nm partially depleted (PD) SOI technology, are shown in Fig 2. The standalone DUT in Fig. 2(a) consists of a body contacted GO1 NMOS with gate width and length of W=100µm and L=60nm respectively. We propose a DUT with large W suitable for analog and RF applications, as well as to achieve device breakdown in a reasonable stress time frame for TDDB data in Section IV.A. Pulsed waveform up to a frequency of 100kHz can be applied directly to V_{Drain} via a pulsed unit generator (1GHz). The DUT test structures in Fig. 2(b) and Fig. 2(c) are designed for AC pulsed waveform stress on the drain terminal of the DUT (V_{Drain}) which are generated by GO1 ring oscillators (RO) with oscillation frequency of 500MHz and/or 1GHz. Since high stress voltages are applied on the V_{Drain}, a level shifter is used to prevent RO device degradation by keeping nominal V_{dd} operation of RO and providing $2xV_{dd}$ voltage level at V_{Drain} via transmission gates consisting of thick-oxide (GO2) transistors. DC and AC modes of these structures are controlled by the RO enable signal (Ring_EN). When Ring_EN ='0', DC mode is activated so that $V_{Drain} = V_{HL}$ while when Ring_EN='1', AC mode is activated so that V_{Drain} is oscillating between V_{HL} and V_{LL} at 500MHz or 1GHz with 50% duty cycle target. The same 500MHz test structure with direct drain access, $DUT_{Test\ Structure\ Drain}$, in Fig.2(c) is used for DUT characterization comparison purpose (discussed in Section III) and to monitor transmission gate degradation during off-state stress (discussed in Section IV.B).

III. DUT Characterization

Prior to off-state drain stress measurements, DC characterization was conducted on each test structure to ensure the signal integrity of the pulsed waveform at V_{Drain}. Firstly, linear I_DV_G DUT characterization is performed for the three structures at $V_{Drain} = V_{HL}$= 50mV, which is illustrated in Fig. 3 with good correlation to simulation data. The linear I_{VHL} of the DUT goes into saturation from V_{Gate}=0.3V onwards due to the

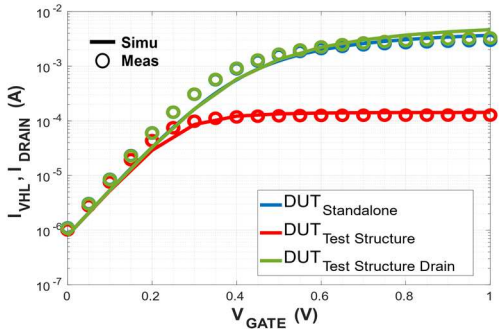

Figure 3: Linear I_DV_G DC characterization at V_{Drain}=V_{HL}=50mV. From V_{Gate}=0.3V onwards, saturation of linear I_{VHL} (red) is due to large Ron_{SW} in series with DUT (refer to Fig.4) Thus, linear I_{VHL} is extracted at V_{Gate}=0.1V and/or 0.3V for comparable I_{Dlin} degradation values.

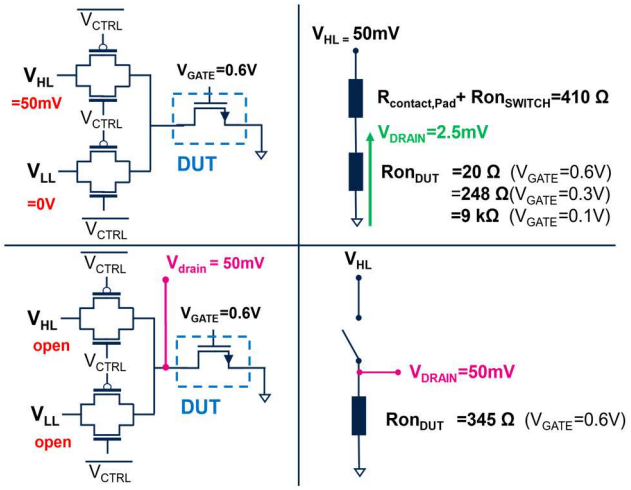

Figure 4: Equivalent schematic of DUT test structures with (bottom) and without (top) drain access for linear I_DV_G characterization. V_{Drain} of DUT test structure without drain access is reduced when Ron_{DUT} is smaller or equal to Ron_{Switch}.

significant on-state resistance of transmission gates (Ron_{Switch}) in series with the DUT. To explain this result, the equivalent schematic of test structures with and without direct drain access for linear I_DV_G characterization is illustrated in Fig. 4. The DUT on-state resistance (Ron_{DUT}) varies according to its

ratio against Ron_{Switch}. When Ron_{DUT} is smaller or equal compared to Ron_{Switch}, V_{Drain} is drastically reduced due to voltage dividing effect. As a result, it is not relevant to compare I_{Dlin} at V_{Gate} = 1V and V_{Drain} = 50mV across different structures, as per convention. In the following, I_{VHL} of DUT $_{Test\ Structure}$ is extracted at V_{Gate}= 0.3V for equivalent I_{Dlin} degradation (ΔI_{Dlin}) comparison with I_{Dlin} of DUT $_{Standalone}$.

Fig. 5 shows I_DV_D characterization of the test structures at V_{Gate}= -1V which corresponds to off-state stress conditions. In both measurement and simulation results of test structures in AC mode, we observe a higher average I_{VHL}(AC) which is attributed to large current peaks during transmission gate switching that is verified from simulation results in Fig.6. When these peak currents are neglected, the ratio of I_{VHL}(DC)/I_{VHL}(AC)=2.15, translating to duty cycle of 46.5%. In the case of test structure with drain access, V_{Drain}(t) AC waveform is altered due to capacitive loading of probes at drain access terminal, causing the average I_{VHL}(AC) to increase (supported by experimental results in Fig. 5). To summarize the characterization of different test structures, we demonstrate that the impact of Ron_{Switch} on V_{Drain} and I_{Drain} signal integrity is negligible during off-state DC and AC stress conditions, while during linear I_{Dlin} measurements, it is necessary to consider V_{Drain} drop caused by Ron_{Switch}.

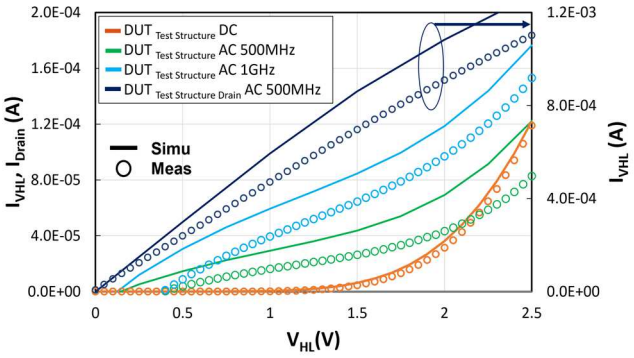

Figure 5: I_DV_D characterization at V_{Gate}= -1V, corresponding to off-state stress conditions. Higher I_{VHL} during AC mode is attributed to large current peaks during transmission gate switching (refer to Fig. 6). Measurement results show good correlation to simulation.

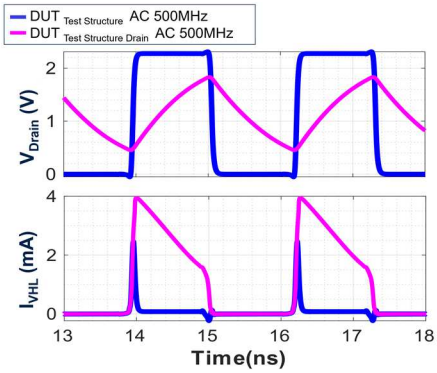

Figure 6: Simulation results of DUT drain voltage and current waveforms during AC mode (V_{Gate}=-1V, V_{Drain}=V_{HL}=2.3V) of test structure with (magenta) and without (blue) direct drain access. The current peaks during transmission gate switching, when neglected, gives ratio I_{VHL}(DC)/I_{VHL}(AC)=2.15. Due to capacitive loading at V_{Drain} of DUT$_{Test\ Structure\ Drain}$, average I_{VHL}(AC) is increased (also illustrated in Fig.5) and V_{Drain} waveform is subjected to distortion.

IV. Experimental: DC to AC Off-State Reliability

A. TDDB Off-state

Fig. 7 shows the breakdown voltages (BV) of each test structure which are determined by conducting fresh (T0) I_GV_D and I_DV_D characterization until device breakdown. The BV of DUT standalone is at V_{Drain} =2.7V while in the case of DUT$_{Test\ Structure}$ under DC mode the BV is at V_{HL}=3.2V due to voltage drop across Ron_{Switch} as I_{VHL} increases with V_{HL}. In AC mode, the BV of DUT $_{Test\ Structure}$ is higher at V_{HL}=3.75V due to the combined effects of Ron_{Switch} voltage drop and duty cycle. Therefore, the-TDDB off-state DC and AC drain bias stress

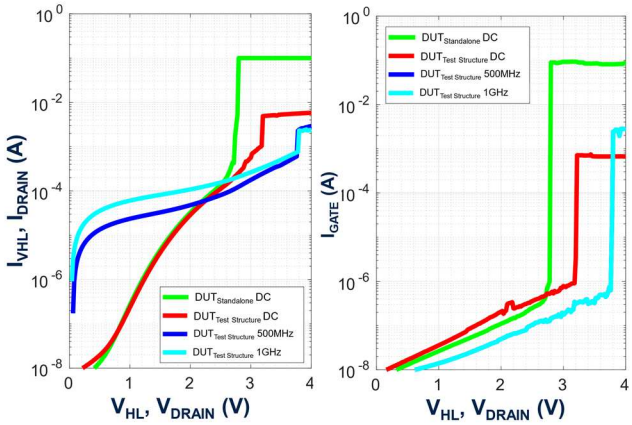

Figure 7: T0 characterization of breakdown voltage (BV) at V_{Gate}= -1V. The BV for DUT standalone is 2.7V. For test structures in AC mode, BV is almost twice that of DC mode.

condition is fixed at V_{Drain} = V_{HL} = 2.3V and gate bias stress V_{Gate} = -1V to obtain practical time-to-breakdown (TBD) for both DC and AC On-The-Fly stress measurements at T=125°C. The TBD of equivalent time stress at DC and AC frequencies by applying the duty cycle factor are plotted in the Weibull distribution illustrated in Fig.8. An increase in TBD is observed as off-state TDDB stress frequency is increased, while the Weibull slope β =1.27 remains constant at different stress frequencies up to 1GHz. A gain factor of 2.15 in TBD is observed at 1GHz stress compared to DC TBD. Assuming the on-state frequency TDDB analytical model in [10] which

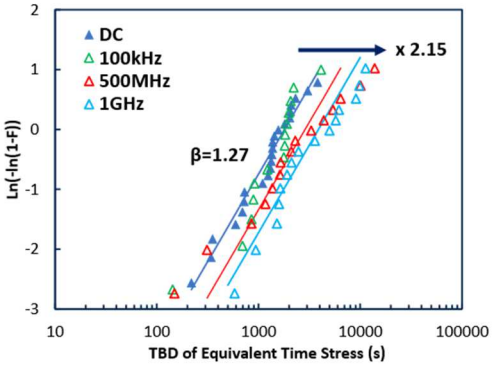

Figure 8: Weibull distribution of DUT standalone and DUT test structures at VD=2.3V for DC, 100kHz, 500MHz and 1GHz stress at T=125°C. The Weibull slope β=1.27 remains constant for both DC and AC stress frequencies. A gain factor of 2.15 in time-to-breakdown (TBD) is observed at 1GHz stress compared to DC stress.

follows a frequency power law dependence, the experimental TBD AC values are compared to this model (with exponent n=0.76 extracted from 500MHz and 1GHz experimental data) in Fig 9(a). Here, a TBD "plateau" for frequencies lower than 100kHz is observed, which is not covered by the proposed model. However, additional data is needed to confirm this assumption for 100kHz to 500MHz. Using this frequency model, the extrapolated TBD at 28GHz (operating frequency for mmW PA applications) is x25 larger than DC TBD, as shown in Fig. 9(b). As V_{Dmax} margins for RF PA design are usually fixed by TBD DC, TBD AC projections can relax V_{Dmax} overhead in design to optimize RF performance at higher frequencies.

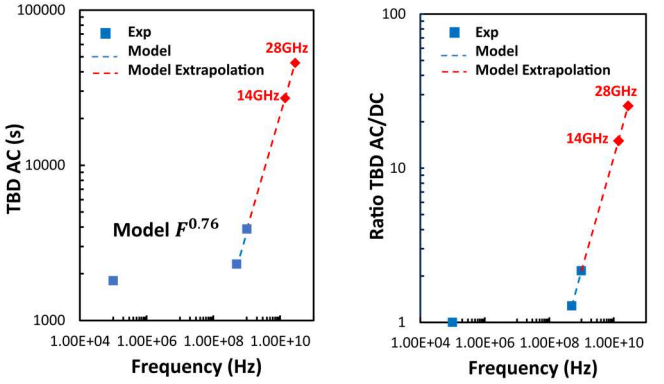

Figure 9: (a) TBD AC experimental data fitted to power law model with an exponent of n=0.76. (b) TBD AC Model extrapolation at 28GHz (mmW PA operating frequency) shows x25 estimated gain factor compared to TBD DC.

B. Effect of dynamic off-state stress on I_{Dlin} degradation

To conduct this study, a Stress-Measurement-Stress methodology is used: during stress phase, stress bias conditions V_{Gate}=-1V and V_{Drain}=V_{stress} or V_{HL}=V_{stress} are applied on DUT at DC or stress frequency, during measurement phase DC mode is activated to perform linear I_DV_G measurements to enable extraction of ΔI_{Dlin} at V_{Gate} =0.1V, 0.3V,0.6V or ΔI_{VHLlin} at V_{Gate}=0.3V. The total stress time is fixed depending on V_{stress} to avoid device breakdown during the experiment.

In Fig. 10, we show the evidence of off-state stress DC and AC 500MHz and 1GHz degradation of $DUT_{Test\ Structure}$ on linear I_DV_G characteristics: Increase in threshold voltage V_T (due to charging of interface traps), decrease in transconductance Gm (due to the increase in drain resistance caused by hot hole injection localized at gate-drain region), and an increase of subthreshold slope. We observed a pivot effect between V_{Gate} = 0.1V and 0.3V as I_{Dlin} is increased for V_{Gate}=0.1V (subthreshold current) while I_{Dlin} is decreased for V_{Gate} = 0.3V and 0.6V (weak inversion current). The pivot effect for off-state stress, as reported in [1,4], is due to the discharge of interface traps depending on bias measurement conditions of device, from depletion to weak inversion. In Fig. 11(a), (b) & (c), we have extracted ΔI_{Dlin} of $DUT_{Standalone}$ at various V_{Gate} characterization at V_{Drain}=50mV, for V_{stress}=V_{Drain}=2.2V. ΔI_{Dlin} is slightly higher for DC stress compared to AC 100kHz stress condition. However, ΔV_{Tlin} in Fig. 11(d) shows that there is no difference in AC stress

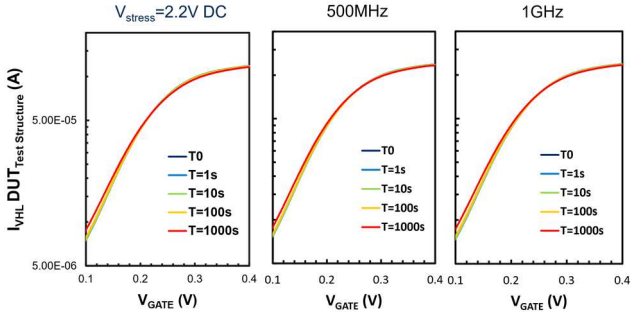

Figure 10: Off-state degradation on linear I_DV_G characteristics of DUT Test Structure for DC and AC stress at 2.2V. AC stress pivot point (similar for both 500MHz and 1GHz) is at higher V_{Gate} compared to DC stress pivot.

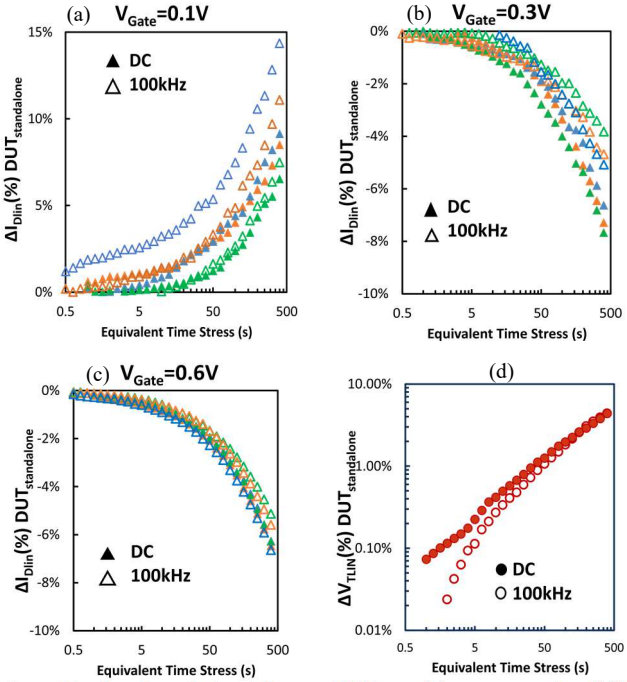

Figure 11: I_{Dlin} degradation (ΔI_{Dlin}) of DUT standalone extracted at different (a)V_{Gate}=0.1V, (b) V_{Gate}= 0.3V and (c) V_{Gate}=0.6V during measurement phase for V_{stress}=V_{Drain}=2.2V DC and 100kHz stress conditions. The pivot effect is located between measurement bias of V_{Gate}= 0.1V and 0.3V. (d) No significant difference is observed in V_{Tlin} degradation (ΔV_{Tlin}) of DUT standalone at DC and 100kHz stress.

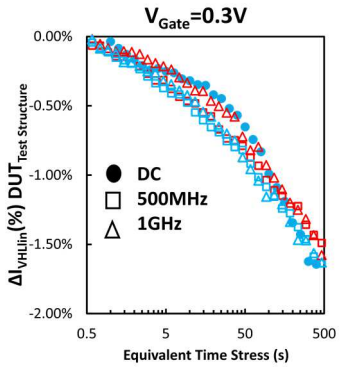

Figure 12: I_{VHLlin} degradation of $DUT_{Test\ Structure}$ (ΔI_{VHLlin}) extracted at V_{Gate}=0.3V during measurement phase for V_{stress}=V_{Drain}=2.2V at DC, 500MHz & 1GHz stress frequencies. ΔI_{VHLlin} of DC stress is similar to ΔI_{VHLlin} of AC stress while ΔI_{VHLlin} is lower than ΔI_{Dlin} due to Ron_{Switch} during measurement phase.

compared to DC stress. We are presuming from the plot of ΔV_{Tlin} in Fig. 11(d) that the the interface trap generation rate ΔN_{IT} is unaffected by the de-trapping AC stress conditions. Likewise, to observe the ΔI_{VHL} at DC, 500MHz and 1GHz, ΔI_{VHL} of $DUT_{Test\ Structure}$ is extracted at V_{Gate} =0.3V, as shown in Fig. 12. The frequency effect on ΔI_{VHL} is non-existent, despite that the magnitude of ΔI_{VHL} is smaller than that of ΔI_{Dlin} extracted at V_{Gate} =0.3V. The V_D dependence of ΔI_{VHLlin} is then discussed based on the experimental results in Fig. 13. The I_{VHLlin} degradation rate for V_{stress}=2.5V is slightly higher than V_{stress}=2.2V and 2V. This reflects the higher interface defect generation rate when the stress bias V_{GD} is increased. A saturation behavior for 500MHz and 1GHz stress conditions at higher V_{stress} is also observed but is not present for DC stress conditions. A possible explanation for this behavior is the different defect generation time dynamics between DC and AC off-state stress, as proposed in [11].

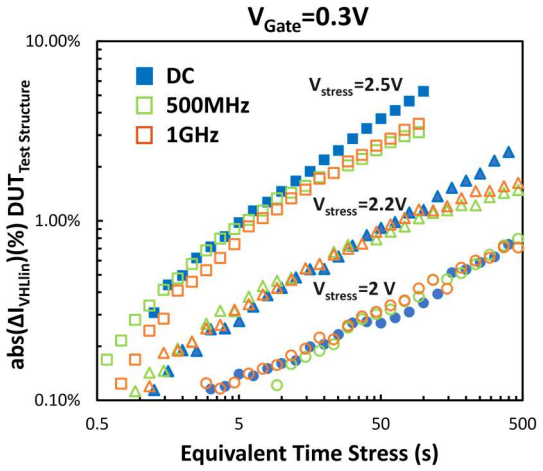

Figure 13: Comparison of abs(ΔI_{VHLlin}) during measurement phase for different V_{stress}=V_{Drain}=2V, 2.2V & 2.5V at DC and AC stress frequencies.

To confirm that ΔI_{VHLlin} is not influenced by degradation of transmission gate device (GO2), the comparison of Ron_{Switch} degradation for DC and AC 500MHz V_{stress}=2.2V condition extracted from $DUT_{Test\ Structure\ Drain}$ is shown in Fig. 14. No significant Ron_{Switch} degradation is observed during stress and measurement phase, which validates the test structure application.

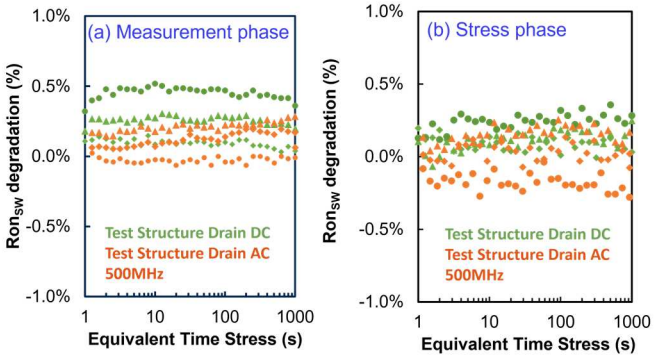

Figure 14: Comparison of Ron_{Switch} degradation under DC and AC 500MHz stress extracted during (a) measurement phase (V_{HL}=50mV) and (b) stress phase (V_{HL}=2.2V) by using $DUT_{Test\ Structure\ Drain}$. No significant degradation is observed on all the 3 samples tested for each condition.

C. *Interaction of on-state & off-state degradation modes*

To provide insight to off-state and on-state interactions, we have studied the history effect of a combination of stress sequences comprising of DC HCI on-state and DC/AC off-state stresses. In this study, the stress sequences are applied on $DUT_{Test\ Structure\ Drain}$ at V_{Gate}=V_{Drain}=1.8V for DC HCI on-state condition while off-state DC and AC 500MHz stress conditions V_{Gate}= -1V and V_{HL}=2.2V at T=125°C. By using a total equivalent time of 3.3ks for the stress sequences, ΔI_{Dlin} level is within acceptable range (<10%) without inducing device breakdown. ΔI_{Dlin} of each degradation mode is fitted to a time power law dependence with a saturation component Δ_{max} in the following model:

$$\Delta = \frac{1}{\frac{1}{\Delta max} + \frac{1}{A \cdot t^n}} \qquad (1)$$

with the following parameter values.

Degradation mode / Parameter	DC HCI ON	DC OFF	AC OFF
A	15.2E-4	4.2E-3	5.9E-3
n	0.71	0.31	0.55
Δ_{max}	0.16	1	0.015

From the model fit, we note that the off-state degradation has a smaller degradation rate in contrast to on-state degradation, given by the smaller exponent n. It is important to remind here that the exponent n of AC off-state is different than that of DC off-state due to the non-pulsed waveform stress (discussed in Section III).

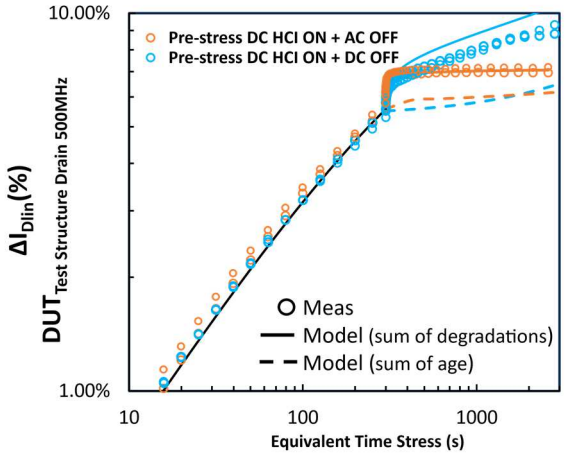

Figure 15: ΔI_{Dlin} of pre-stress DC HCI (V_{Gate}=V_{Drain}=1.8V 300s) followed by DC/AC off-state stress (V_{Gate}=-1V, V_{Drain}=2.2V 3ks). Total ΔI_{Dlin} of stress sequence is modeled by the sum of degradation of each mode.

Fig. 15 shows ΔI_{Dlin} for the sequence pre-stress DC HCI on-state for a duration of 300s followed by DC/AC off-state stress for 3ks. Experimental data is found to be well modeled by the sum of degradation of each mode, as opposed to the sum of age interaction model, indicating the absence of

interaction between these two mechanisms [11]. For comparison, Fig. 16 shows the inverse stress sequences of Fig.15, ΔI_{Dlin} with pre-stress DC/AC off-state stress for a duration of 3ks followed by DC HCI stress for 300s. Again, no history effect is observed after pre-stress. However, we observe in this case that both sum of degradation and sum of age modelling fit experimental data of this stress sequence. In addition, a series of alternating DC HCI on-state and DC/AC off-state stress sequences (30 cycles) are conducted to compare with the previous ΔI_{Dlin} results obtained in Fig. 15 & Fig. 16, as shown in Fig. 17. Interestingly, the total ΔI_{Dlin} is the same for DC HCI on-state to DC/AC off-state stress modes given the same stress duration of different stress sequences, thus validating the sum of degradation model for on and off-state interactions.

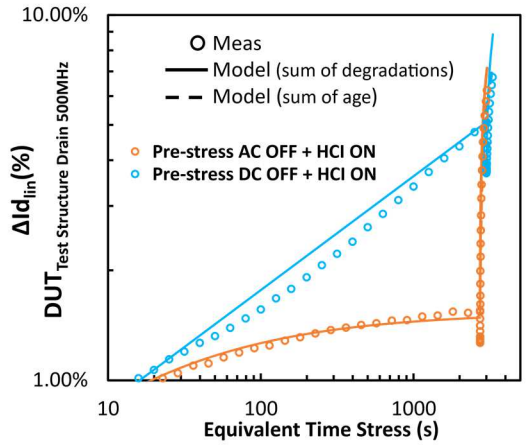

Figure 16: ΔI_{Dlin} of pre-stress DC/AC off-state stress (V_{Gate}=-1V, V_{Drain}=2.2V 3ks) followed by DC HCI (V_{Gate}=V_{Drain}=1.8V 300s). Both models sum of degradation and sum of age are in good agreement with experimental data. ΔI_{Dlin} of pre-stress AC off-state is different from DC off-state due to non-pulsed waveform stress pattern.

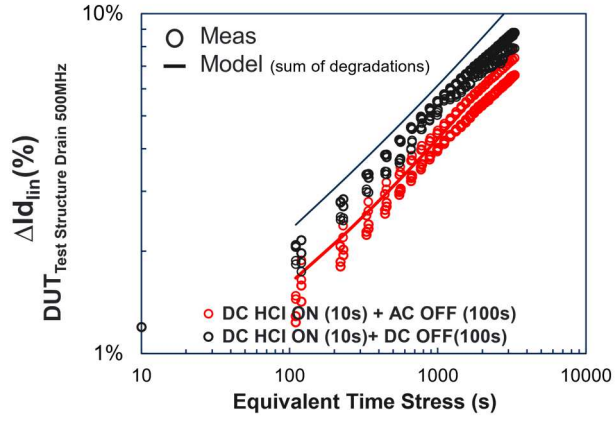

Figure 17: ΔI_{Dlin} of alternating DC on-state HCI and DC/AC off-state stress sequences with total stress duration of 3.3ks. Sum of degradation model shows good agreement with measurement data.

V. Conclusions

In-depth characterization of the test structures, presented by good model-to-hardware correlation (MHC) data has proven the integrity of the applied off-state pulsed voltage stress until 1GHz. Through experimental results using these integrated test structures, we have reported in TBD gain factor of 2 for 1GHz compared to DC off-state TDDB stress. In contrast, our off-state stress investigation on linear I_D parameter has evidenced no difference in degradation from DC to AC 1GHz stress. We have also experimentally proven the absence of interaction in DC & AC off-state vs DC on-state degradation modes, which allows them to be modeled independently in reliability models as the sum of degradation modes.

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