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Influence of DMC EMI Optimization on CMC EMI for DC-AC Isolated Power Converter Array.

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Abstract

This paper focuses on the EMC disturbances generated by converter networks (PCA). After recalling the interest of the interleaving for the reduction of the differential mode current (DMC), the impact of the interleaving strategy on the common mode current (CMC) is studied. For this purpose, a PCA model allowing the evaluation of the CMC is proposed. This model, confronted with measurements carried out on a prototype PCA, has shown its good accuracy. Based on this model, several interleaving strategies of the PCA converters are evaluated according to the conducted EMC disturbances they generate. The interleaved control strategies are therefore studied according to their induced CMC but also according to the impact they have on the DMC. The work is based on simulations and modelling of a multi-stage DC-AC converter. The modelling of the CMC sources as voltage hotspots exploited by the interleaved control strategy is developed. An analysis is performed to highlight the opportunity of common mode recycling at the multistage converter and ends with the presentation of a control strategy allowing CMC recycling inside the PCA.

1 Introduction

Initially used on high power, high voltage applications [1], modular converters are today considered in low-medium power (100W up to 100kW) low-medium voltage (10V up to 1kV) systems to increase converters performances, dynamics and densities [2]–[4]. Modular converters are made of vectors or matrices of identical conversion modules working together to answer conversion specifications. Many different topologies and architectures have been proposed in the literature [5], all based on the association in parallel and or in series of several, and even numerous conversion cells [6]. Among them, multicellular, multi-levels power converter arrays are gaining in interest [7]. In particular, these conversion architectures are helping sharing voltage and current constraints, distributing losses while offering potential benefits from their multi cell organization in terms of conducted EMI but also modularity, fault tolerance or efficiency [8]. A further step in modularity is related to the concept of power converter arrays [9], [10]. Power Converters Arrays (PCA) are made of Conversion Standard Cells (CSC) working together,

connected in series and or in parallel, to achieve the global conversion. The main difference is about the structure of the sub module. In PCA, each CSC is an individual isolated converter contributing to the overall conversion effort as illustrated in **Fig. 1**. By associating them in series and parallel, it is possible to accommodate the PCA to almost any range of conversion specifications, opening the opportunity to address a wide range of converter specifications with a limited variety of components, design and manufacturing options. Multicellular converters open up the opportunity to implement multi-levels which can be used to interleave voltage steps in series associations or current ripples in parallel associations, both leading to significant differential mode current (**DMC**) conducted EMI reductions [11]. If the literature is extensively investigating DMC in multicell converters, it is not focused on its impact on Common mode currents (**CMC**). CMC are parasites currents flowing from the converter through ground. They are also subjected to conducted EMI limitations [12] and must be carefully addressed in low and medium power levels. This paper is investigating how interleaved control strategies can also provide an interesting benefit from the CMC point of view.

The paper is organized as follows. First, DC to AC PCA converter architecture considered in this paper is recalled, since it is fundamental to address conducted EMI issues to clearly define it. Then the main benefits of interleaved control strategy optimization with respect to DMC are recalled. Its impact on CMC is then analyzed before considering the control strategy options that can be implemented to limit CMC levels. The analysis is carried out thanks to equivalent models and time domain simulations.

2 DC to AC, PCA inverter topology

The multicell inverter topology used in this work consists of an association of isolated DC-AC conversion standard cells (CSC) connected in parallel on the DC side and in series on the AC side. The CSCs shown in dashed green boxes on the **Fig. 1**, are made out of a Dual Active Bridge (DAB) DC/DC conversion stage with galvanic isolation, cascaded with an H bridge DC/AC conversion stage. Two inductors L_{DM} are placed on the AC side of this DC/AC conversion stage to filter out high frequency (HF) voltage patterns.

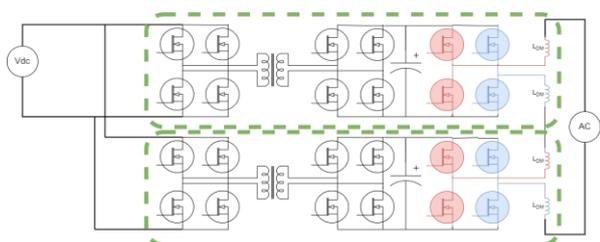


Fig. 1 DC/AC power Converter arrays implemented with two CSC.

Such a converter topology provides the opportunity to interleave the voltage steps of each full bridge through interleaved control signals, as illustrated in the **Fig. 2**. By reducing the amplitude of the HF voltage steps while multiplying the apparent frequency of the HF voltage pattern, the interleaving control offers a significant reduction in differential mode filtering needs as described in [13]–[15].

2.1 Experimental behavior

A prototype was designed in order to evaluate in practice the benefits of interleaving multicell converters. The DMC filter was designed accordingly to regulation compliance. The prototype displayed on **Fig. 3** is made out of 2 parallel converters of 6 CSCs in series. Table 1. Pro-

vides a few essential data related to the hardware implementation. The prototype was tested under conducted EMI measurement standard conditions. As it can be seen in **Fig. 4** where EMI normative measures are presented with DMC filter and without CMC filter, significant EMI levels are still preventing the prototype from regulation compliance. This is mainly due to CMC disturbances that are still very high and have to be filtered out.

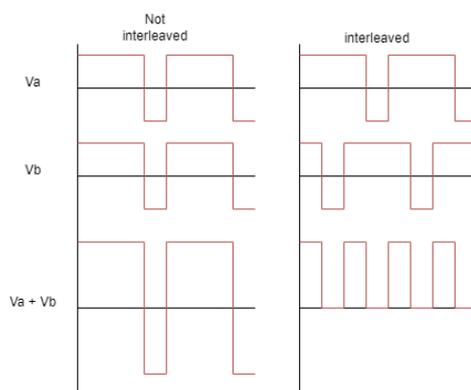


Fig. 2 Comparison between HF output voltage waveforms of a series non-interleaved and interleaved bipolar control strategy at 75% duty cycle



Fig. 3 PCA prototype with 12 CSCs (6 series of 2 cells parallels) used to characterize the impact of interleaving driving signals on conducted EMI disturbances.

Component	characteristic	Value
VDC		40 V
VAC		200 V
Switching frequencies	DC/DC stage	250 kHz
	DC/AC stage	100 kHz

Table 1 Converter main characteristics

Each H bridge is operating under 100 kHz switching frequency. With interleaved command, one could expect the disturbance spectrum to start from 600kHz, but unlike a parallel interleaved converter, here, each commutation cell

have a different effect on the common mode current due to the electrical series connections. The resulting conducted EMI harmonics are multiple of the switching frequency. This behavior will be detailed in **section 4**.

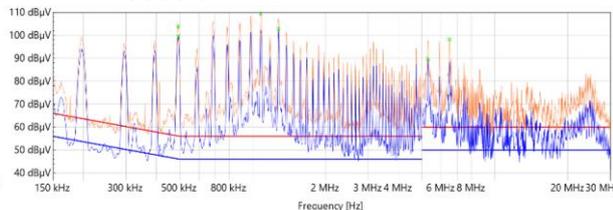


Fig. 4 Normative measure of the conducted EMI from the PCA converter prototype (including DMC filter and no CMC filter)

The very flat envelop for conducted EMI levels is characteristic of conducted CMC. It shows that traditional interleaved control strategies, if effective on DMC, is not effective on CMC, at least for multicell series associations. It is therefore interesting to investigate further, how interleaved control signals could be considered in order to limit as well CMC disturbances. For this purpose, the following section is introducing an original modeling of PCA converters in order to study and analyze its CMC EMI signature.

3 Common mode equivalent model

In order to represent the behavior of each CSC in terms of CMC conducted EMI source, CSCs are simplified as illustrated in **Fig. 5**. In this equivalent model, the DC/DC converter stage is totally neglected from the modeling effort. This is made possible since the switching frequency of the DC/DC converter stage is different from the H Bridges and its corresponding CMC EMI can be discriminated. As a result, the DC/DC conversion stage is represented as a perfect voltage source V_{DC} connected to the DC link. To account for the parasitic propagation paths offered by the DC stage to CMC, two parasitic capacitances (B_1 & B_2) are added to the equivalent circuit, both connected to ground on one side and each to a terminal of the DC link as illustrated in **Fig. 5**. The H bridge is still represented with its four switches plus two common mode capacitances between each middle point and ground (A and C).

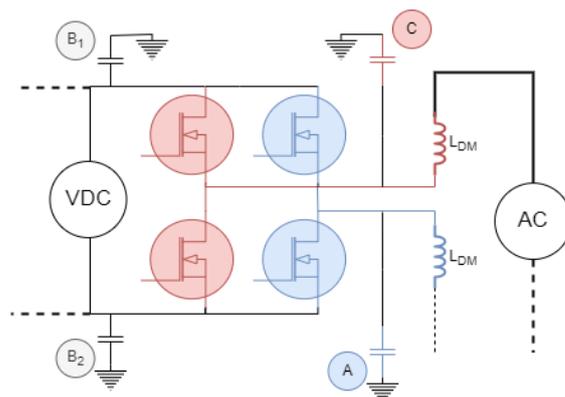


Fig. 5 Individual H bridge inverter with parasitic common mode capacitors

An additional modeling stage proposed in [15] is introduced in **Fig. 6** in order to consider only HF signals. The H bridge switches and the DC link voltage source are substituted then by two voltage sources representing the HF voltage patterns of each H bridge middle point as illustrated in **Fig. 6**. Each voltage source V_A and V_C is a two level HF square wave with the magnitude of the DC link voltage source V_{DC} . In this equivalent model, the two parasitic capacitors (B_1 & B_2) have been summed up in HF to a single named (B). In the analysis parasitic capacitance C_B of B, is expected to be significantly larger than capacitances C_A and C_C of capacitors A and C. Also the AC side loop is connected to a resistor that represents the LISN HF equivalent model. This is necessary to close the common mode path loop. Please note the color code that has been used in **Fig. 5** and **6** in order to ease the comprehension.

The right side of **Fig. 6** represents the two stable states of an H bridge operated in bipolar control strategy. A stable state occurs between switching transitions, when no voltage variation is visible at the output of the H bridge. It is then possible to set the voltage across the various components of the HF equivalent circuit.

States “+” and “-” are used to name the two stable state in bipolar control strategy. In “+” state, the CSC adds V_{DC} to the output AC loop. When in “-” state, it adds $-V_{DC}$.

The measured CMC is the current flowing through R_{LISN} , and the Kirchoff laws show that the current flowing through this resistor is the sum of the current flowing through the parasitic capacitors.

Considering $C_A = C_C$, and the equivalence of the impedance of different current path, the CMC is equal I_{RLISN} in the following equation. The common mode current is always proportional to the sum of the voltage variation on A, B and C.

$$I_{RLISN} = C_{A\&C} \sum \frac{dv_{C_{A\&C}}}{dt} + C_B \sum \frac{dv_{C_B}}{dt} \quad (1)$$

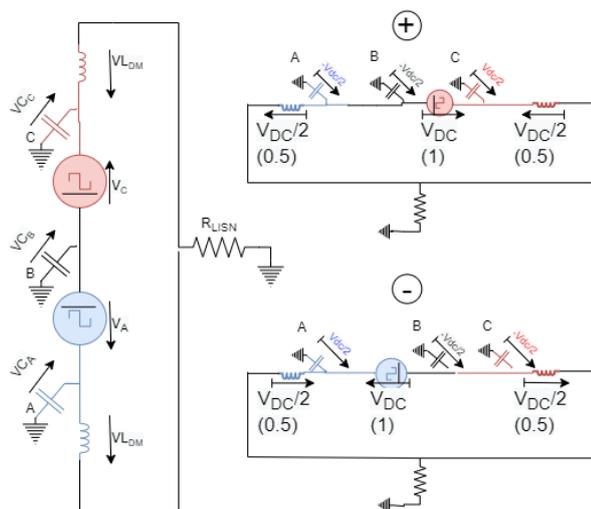


Fig. 6 HF equivalent model of a full bridge inverter and the two stable states voltage distribution for bipolar control strategy.

	State and transition [$k \cdot V_{DC}$]				
	+	->	-	->	+
C	-0.5	1	-0.5	-1	-0.5
B	-0.5	0	-0.5	0	-0.5
A	0.5	-1	-0.5	1	0.5
$\sum \Delta v_{C_{A\&C}}$		0		0	

Table 2 Stable states and magnitudes of A, B and C capacitor voltage steps in a single H bridge.

The **Table 2** presents the way the analysis is going to be carried out to analyze CMC generation across each parasitic capacitance A, B and C. The analysis approach is introduced here for a single H bridge operating in bipolar control strategy. Each switching cell has two stable states + and - and two transitions, represented in the **Fig. 6** by arrows and in the table by $k \cdot V_{DC}$. The grey columns account for the stable voltage states of the switching cells (between switching transitions) and the orange columns describes the voltage transition magnitude across each capacitance at each switching transition.

The last line of the table (dark grey) shows the sum voltage swing across C_A and C_C for each switching transition. If equal and opposite, the CMC cancelation is observed and no CMC current flows to the LISN [16].

With the use of this model, the next part will present the analysis of CMC generation when several CSC are associated in series on their AC sides.

4 Analysis of driving signal strategies on serial conversion interleaving conducted EMI.

4.1.1 Command strategies analyzed

As reminded in part 2, the interleaving of series connected PCA reduces the magnitude of the HF voltage steps, reducing the need of DM filtering. However, it produces high CMC. In this part this CMC is analyzed when an interleaved control strategy is used in a PCA converter with 4 CSC associated in series on the AC side. This analysis is carried out considering first a bipolar control strategy. Similar analysis can be carried out for unipolar control strategy and only main conclusion will be provided for that case.

Based on the analysis, a specific interleaving strategy for the driving signal will be proposed and analyzed to cancel out CMC disturbances in PCA converters. Please note that the analysis can be generalized to any number of CSCs, odd or even and any type of control strategy.

4.1.2 Effect on common mode generation

Fig. 7 introduces the equivalent HF model of the PCA with 4 DC/AC CSCs connected in series on their AC side. The control signal configuration displayed in **Fig. 7** corresponds to state "-+++" where the first CSC (on the left) is in Sate "-" and the 3 others are in the Sate "+". Similarly to **Table 1** **Table 2**, **Table 3** presents in orange columns, for each transition, the evolution of the voltage across each parasitic capacitor and, in grey columns, their fixed voltage for each stable state. The last line, in dark grey is the sum of the resulting CMC contribution for each capacitor type (A_x , B_x and C_x). One can see that in contrary with the analysis and results obtained in **Table 2**, here the sum of the CMC flowing through the parasitic capacitors is no more cancelled.

As previously introduced in **section 2**, each CSC is inducing a specific CMC current, avoiding the opportunity of CMC cancelation at PCA level. The CMC wave at PCA level will not be a unique signal generated at 4 times the switching frequency but a complex signal due to unequal contributions.

State and transition [$k \cdot V_{dc}$]

	++++	Cell 1	-+++	Cell 2	--++	Cell 3	---+	Cell 4	----
A1	-0.5	0.25	-0.25	0.25	0	0.25	0.25	0.25	0.5
B1	-0.5	-0.75	-1.25	0.25	-1	0.25	-0.75	0.25	-0.5
C1	0.5	-0.75	-1.25	0.25	-1	0.25	-0.75	0.25	-0.5
A2	-0.5	-1.25	-1.75	0.75	-1	0.75	-0.25	0.75	0.5
B2	-0.5	-1.25	-1.75	-0.25	-2	0.75	-1.25	0.75	-0.5
C2	0.5	-1.25	-0.75	-1.25	-2	0.75	-1.25	0.75	-0.5
A3	-0.5	-0.75	-1.25	-0.75	-2	1.25	-0.75	1.25	0.5
B3	-0.5	-0.75	-1.25	-0.75	-2	0.25	-1.75	1.25	-0.5
C3	0.5	-0.75	-0.25	-0.75	-1	-0.75	-1.75	1.25	-0.5
A4	-0.5	-0.25	-0.75	-0.25	-1	-0.25	-1.25	0.75	0.5
B4	-0.5	-0.25	-0.75	-0.25	-1	-0.25	-1.25	0.75	-0.5
C4	0.5	-0.25	0.25	-0.25	0	-0.25	-0.25	-0.25	-0.5
$\sum \Delta V_{CB}$		-3 Vdc		-1 Vdc		1 Vdc		3 Vdc	
$\sum \Delta V_{CA\&C}$		-5 Vdc		-2 Vdc		2 Vdc		5 Vdc	

Table 3 stable states and evolutions of the parasitic capacitors voltages in a 4 cells converter. A 4 CSC bipolar converter has **8** switching events per period.

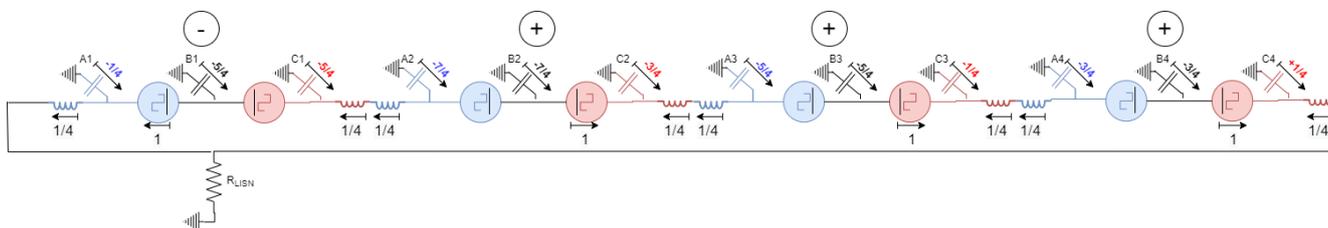


Fig. 7 HF equivalent model of the 4 CSCs for the stable State “-+++”

4.2 Symmetrical bipolar command

4.2.1 Common mode current recycling

Common mode current recycling is a method to cancel CMC outside the converter [16]. In single-phase H bridges, designed and operating with two symmetrical switching cells, the resulting parasitics may cancel each other. For PCA inverters with DC/AC stage associated in series, in addition to the symmetrisation of the physical hardware thanks to modular approach, it is necessary to symmetrize the control signals in order to provide CMC cancellation. This is analysed in the following section. It is shown that if the same

control signal are applied to two “electrically” symmetrical CSCs, the switching effect of one cell is cancelled by the other. By “electrically” symmetrical, one must understand opposite in the series association (top one and bottom one in the string for example or first one with fourth one and second one with third one in Fig. 7).

4.2.2 Effect on common mode current generation

In the following, CSCs 1 and 4 are supposed to be symmetrical due to their respective positions in the serial connexion. It is the same for CSCs

2 and 3. Let's consider that, cells 1 and 4 have opposite driving signals and it is the same for 2 and 3. With this approach at each switching transition during the period, CMC current flowing through B capacitors of a CSC is cancelled by the opposite CMC generated by the physically and electrically symmetrical CSC. Similarly, the CMC from capacitor C of one CSC is cancelled by the CMC through capacitor A of the symmetric CSC. This allows to expect a perfect recycling of the CMC into the PCA, equivalent to the natural recycling in a regular two levels H bridge voltage source inverter. This is outlined in Table 4 where stable states and evolutions of the hot spots voltages in a 4 cells PCA are described. 4 switching event per period are considered in bipolar control strategy. It is shown that with the symmetrization of driving signals at PCA level, it would lead to a perfect cancellation of the switching transitions.

4.3 Unipolar command

The same analyse can be done with a unipolar control strategy. It is known that using unipolar control in VSI allows reducing DM filtering effort by 4, it is also known that it also causes higher CMC emissions since it is less suitable for CMC cancelation [16].

However in the case of interleaved PCAs, the analyse shows the same opportunity of improvement as it is the case for bipolar control strategy. Also by using 180° shifted signals to drive physically and electrically symmetrical cells, the "symmetrised unipolar control strategy" has the same behaviour than "symmetrical bipolar command" having a possible perfect CMC recycling. For the lack of place, the illustration with a table is not depicted here but the reader can easily understand that it works as well for any type of driving signal strategy as long as two physically and electrically symmetrical switching cells are switched at the same time.

4.4 Effect on differential mode current

The proposed driving signal approach has an effect on the differential mode filtering need. For the symmetrization needs, it reduces the number of CSCs that can be interleaved by a factor of two. It is well known that interleaving N CSCs the output inductor value will be reduced by a N^2 factor, no matter the control strategy considered (bipolar or unipolar or other). Therefore, symmetrized driving signals at PCA level will induce a reduction of 4 in the benefits of interleaving, no matter the number of CSC considered. This may be the price to pay in order to reduce CMC levels.

	++++	1&4	---	2&3	----
A1	-0.5	0.5	0	0.5	0.5
B1	-0.5	-0.5	-1	0.5	-0.5
C1	0.5	-1.5	-1	0.5	-0.5
A2	-0.5	-0.5	-1	1.5	0.5
B2	-0.5	-0.5	-1	0.5	-0.5
C2	0.5	-0.5	0	-0.50	-0.5
A3	-0.5	0.5	0	0.5	0.5
B3	-0.5	0.5	0	-0.5	-0.5
C3	0.5	0.5	2	-1.5	-0.5
A4	-0.5	1.5	2	-0.5	0.5
B4	-0.5	0.5	0	-0.5	-0.5
C4	0.5	-0.5	0	-0.5	-0.25
$\sum \Delta V_{C_B}$		0		0	
$\sum \Delta V_{C_{A\&C}}$		0		0	

Table 4 stable states and evolutions of the hot spots voltages in a 4 cells PCA. 4 switching event per period are considered in bipolar control strategy.

The next section will present the spectrum analysis of a simulated PCA. This analysis will compare the CMC spectrum of the PCA according to the different interleaved control and driving signals strategies (bipolar, symmetrical bipolar, unipolar and symmetrical unipolar)

5 Time based simulation

5.1 Simulation parameters

The time domain simulation parameters must be set according to a realistic case study. For that purpose, the prototype depicted in **Section 2** is considered. The electrical and dynamic behaviour of the main components of the DC/AC stages are represented to account for switching times, as well as filtering effects. In these simulations the PCA is supposed made out 6 pairs of interleaved CSCs, 12 in total, as the prototype one. Bipolar control strategy is considered. The

switching events location are considered perfect (no dead time). Only the DCR of the filtering inductors and transistors are considered with the Coss and common mode (A B and C) capacitors. A and C capacitors are estimated equal to 10 pF, and B capacitors are estimated equal to 200 pF. The **Fig. 8** presents in blue the simulated CMC spectrum using the same bipolar command mode as in the prototype. The image of the produced CMC is observed looking at the voltage across the pair of 50 Ω resistors of the LISN model. The simulation result having the similar behaviour as the prototype (see **Fig. 4** Normative measure of the conducted EMI from the PCA converter prototype (including DMC filter and no CMC filter)), the model is considered representative of CMC generated by the PCA converter. One can compare the natural reduction of the 6th and 12th harmonic in both the simulation and measurement.

The red curve is the envelope of the spectrum. This envelop will be used in the following to compare the CMC spectrum generated by each control and driving signal strategy.

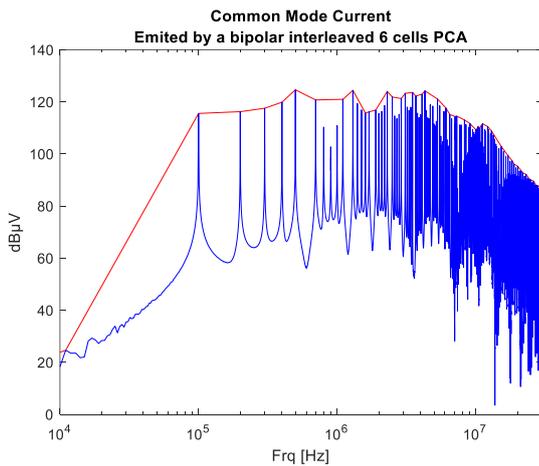


Fig. 8 Spectrum and envelop of the simulated CMC measured on standard LISN impedance (2X50 Ω)

5.2 Analysis of the common mode spectrum

The **Fig. 9** presents four envelops of CMC spectrums, the red one is the previously presented spectrum for the interleaved bipolar non symmetrized control strategy. The green one is the unipolar interleaved non-symmetrized spectrum. The dotted red and dotted green are respectively the spectrum generated by symmetrized bipolar and unipolar control strategies.

The level of these two last dotted spectrums are comparable with numerical calculation noises. These time domain simulation results demonstrate the great interest of symmetrized driving

signal at PCA level to cancel and to solve the CMC issue.

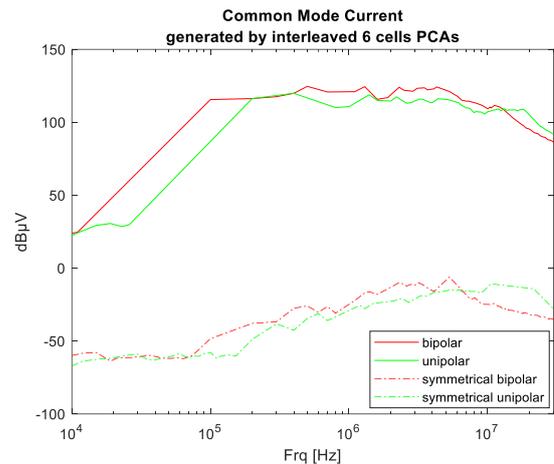


Fig. 9 Comparison of four CMC EMI spectrum envelops with respect to control strategy choices.

6 Sensibility to imperfection

One knows that without imperfections and dispersion, there would be no need of common mode filtering on regular VSI as discussed in [15-16]. However, the parasitics and component dispersions, associated with switching time location dispersion affect the perfect CMC recycling and cancelation. Taking into account all the imperfections is a complex task which should nevertheless be carried out if one wants to verify the effectiveness of the proposed symmetrical controls.

7 Conclusion

This work has exposed the incompatibility between standard interleaving control methods into series connected multinodular inverters and CMC conducted EMI mitigation. After a description of the CMC origin and causes into PCA topologies, a new symmetrized driving signal approach has been presented. It has been demonstrated the opportunity to cancel CMC. Considering components and parasitic dispersion, the time domain simulations of the PCA under symmetrized driving signal has shown significant benefits. This whole approach remains to be demonstrated in practice.

References

- [1] J. Rodriguez *et al.*, « Multilevel Converters: An Enabling Technology for High-Power Applications », *Proc. IEEE*, vol. 97, n° 11, p. 1786-1817, nov. 2009, doi: 10.1109/JPROC.2009.2030235.
- [2] J.-J. Jung, H.-J. Lee, et S.-K. Sul, « Control Strategy for Improved Dynamic Performance of Variable-Speed Drives With Modular Multilevel Converter », *IEEE J. Emerg. Sel. Top. Power Electron.*, vol. 3, n° 2, p. 371-380, juin 2015, doi: 10.1109/JESTPE.2014.2323955.
- [3] V. Mendes, G. Rezende, T. Ferreira, J. L. da Silva, J. Regnier, et T. Meynard, « Design Aspects for Achieving High Bandwidth Series and Parallel Multicell Converters », *IEEE Trans. Power Electron.*, vol. 37, n° 6, p. 6437-6449, juin 2022, doi: 10.1109/TPEL.2021.3136481.
- [4] D. Ronanki et S. S. Williamson, « Modular Multilevel Converters for Transportation Electrification: Challenges and Opportunities », *IEEE Trans. Transp. Electrification*, vol. 4, n° 2, p. 399-407, juin 2018, doi: 10.1109/TTE.2018.2792330.
- [5] M. A. Perez, S. Ceballos, G. Konstantinou, J. Pou, et R. P. Aguilera, « Modular Multilevel Converters: Recent Achievements and Challenges », *IEEE Open J. Ind. Electron. Soc.*, vol. 2, p. 224-239, 2021, doi: 10.1109/OJIES.2021.3060791.
- [6] J. W. Kolar, F. Schafmeister, S. D. Round, et H. Ertl, « Novel Three-Phase AC-AC Sparse Matrix Converters », *IEEE Trans. Power Electron.*, vol. 22, n° 5, p. 1649-1661, sept. 2007, doi: 10.1109/TPEL.2007.904178.
- [7] A. G. Andreta *et al.*, « A High Efficiency and Power Density, High Step-Up, Non-isolated DC-DC Converter Based on Multicell Approach », in *CIPS 2018; 10th International Conference on Integrated Power Electronics Systems*, mars 2018, p. 1-5.
- [8] J. W. Kolar, F. Krismer, Y. Lobsiger, J. Muhlethaler, T. Nussbaumer, et J. Minibock, « Extreme Efficiency Power Electronics ».
- [9] X. Huang, F. C. Lee, Q. Li, et W. Du, « High-Frequency High-Efficiency GaN-Based Interleaved CRM Bidirectional Buck/Boost Converter with Inverse Coupled Inductor », *IEEE Trans. Power Electron.*, vol. 31, n° 6, p. 4343-4352, juin 2016, doi: 10.1109/TPEL.2015.2476482.
- [10] M. Liserre *et al.*, « Power Routing: A New Paradigm for Maintenance Scheduling », *IEEE Ind. Electron. Mag.*, vol. 14, n° 3, p. 33-45, sept. 2020, doi: 10.1109/MIE.2020.2975049.
- [11] T. Lamorelle, Y. Lembeye, et J.-C. Crébier, « Handling Differential Mode Conducted EMC in Modular Converters », *IEEE Trans. Power Electron.*, vol. 35, n° 6, p. 5812-5819, juin 2020, doi: 10.1109/TPEL.2019.2947735.
- [12] X. Chen, W. Chen, Y. Han, Y. Sha, X. Yang, et X. Li, « Common-mode interference study of a auxiliary power supply based on the serialization of SiC MOSFETs for MMC-HVDC system », in *2016 IEEE 8th International Power Electronics and Motion Control Conference (IPEMC-ECCE Asia)*, mai 2016, p. 31-36. doi: 10.1109/IPEMC.2016.7512257.
- [13] J. Rodriguez, M. Rivera, J. W. Kolar, et P. W. Wheeler, « A Review of Control and Modulation Methods for Matrix Converters », *IEEE Trans. Ind. Electron.*, vol. 59, n° 1, p. 58-70, janv. 2012, doi: 10.1109/TIE.2011.2165310.
- [14] T. de Sa Ferreira *et al.*, « Novel Multirate Modulator for High-Bandwidth Multicell Converters », *IEEE Trans. Power Electron.*, vol. 36, n° 4, p. 4887-4900, avr. 2021, doi: 10.1109/TPEL.2020.3032118.
- [15] J.-C. Crebier *et al.*, « DC-AC Isolated Power Converter Array. Focus on Differential Mode Conducted EMI », *Electronics*, vol. 8, n° 9, Art. n° 9, sept. 2019, doi: 10.3390/electronics8090999.
- [16] J. C. Crebier, L. Jourdan, R. Popescu, et J. P. Ferrieux, « Common mode disturbance reduction of PFC full bridge rectifiers », in *2000 IEEE 31st Annual Power Electronics Specialists Conference. Conference Proceedings (Cat. No.00CH37018)*, juin 2000, vol. 2, p. 922-927 vol.2. doi: 10.1109/PESC.2000.879937.