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# Influence of different peripheral protections on the breakover voltage of a 4H-SiC GTO thyristor

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**Keywords:** 4H-SiC, thyristor, MESA, JTE, EGR

**Abstract :** 4H-SiC asymmetrical gate turn-off (GTO) thyristors have been developed using a PP-NP<sup>+</sup> epitaxial layer structure, where P<sup>-</sup> is a 35 μm thick p-type drift layer doped at 5×10<sup>14</sup> cm<sup>-3</sup>. The process sequence uses plasma etching steps (ECR and RIE) in order to expose inter-digitated devices with a recessed gate structure. Knowing the difficulty in reaching the theoretical forward blocking capability of V<sub>b</sub> = 6 kV, determined by numerical simulations using the finite element code MEDICI™, three different device terminations were realized. The first and simplest termination used is a MESA etched down to 12 μm depth into the drift layer. Better performances were expected by using a combination of MESA and Junction Termination Extension (JTE), where implantation and anneal have to be precisely adjusted. Finally, Etched Guard Ring (EGR) terminations were realized etching five 2 μm wide grooves around the device periphery through the n-base layer. The electrical characteristics of the devices with all the three terminations are presented and discussed. The highest breakover voltage measured for mesa terminated devices amounts to 3.9 kV.

## Introduction

Today, at French-German Research Institute of Saint-Louis (ISL) there are pulsed power applications under investigation which handle electric energies up to 10 MJ using sparc gaps or silicon based high power semiconductors as switching elements [1]. Since silicon based technology is reaching its physical limits concerning blocking and power handling capability, for compact future military pulsed power systems we are investigating GTO thyristors based on SiC [2, 3]. Like others we are motivated by some excellent results for Schottky diodes [4], thyristors [5] and bipolar diodes [6]. Reaching a breakdown voltage of 19 kV [6], the potential of SiC based devices appears to be very interesting. The goal of this article is to show the electrical characteristics of 3 different terminations for the same component.

## Simulations

The goal of this work is to develop a 4H-SiC thyristor with a blocking voltage equals to 5kV and a current density of 2 kA.cm<sup>-2</sup>. Simulations were made in order to determine the electrical characteristics in blocking and in conduction state. The structure of the thyristor is described by the figure n°1. An asymmetrical thyristor has been developed because the thickness of the P<sup>-</sup> epilayer is three times smaller than the classical structure (without P buffer layer, doped at

$4 \times 10^{17} \text{ cm}^{-3}$ ). The junction  $J_2$  is in charge of the blocking voltage. The SCR (Space Charge Region) extends in the P<sup>-</sup> layer. So, this region has got a lower doping level and a larger thickness. To obtain a 5 kV breakdown, the thickness must be superior to 30  $\mu\text{m}$  and the doping inferior to  $10^{15} \text{ cm}^{-3}$ . With a safety margin, a 35  $\mu\text{m}$  thickness doped at  $10^{15} \text{ cm}^{-3}$  is sufficient for the thyristor. These simulation results, shown in Fig. 2, are obtained by MEDICI<sup>TM</sup>. The parameters and the equations used by the software are described in [7].

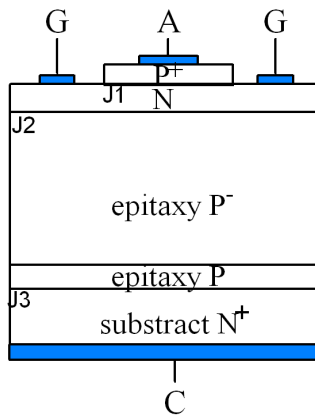


Fig. 1 : Structure of the thyristor

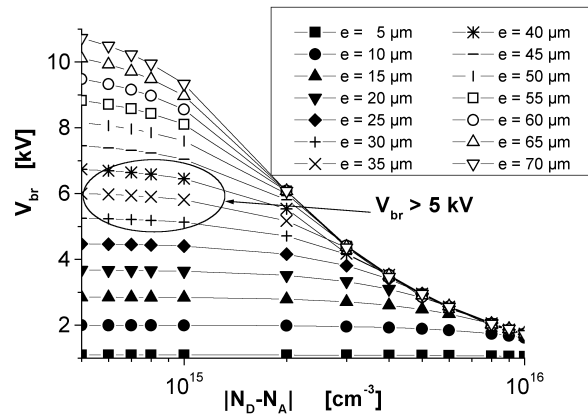


Fig. 2 : Breakdown voltage versus doping for different layer- thickness

For the blocking state, the N gate region must be capable to support 5 kV. With a 2  $\mu\text{m}$  thickness layer doped at  $10^{17} \text{ cm}^{-3}$ , the SCR extension is inferior to 2  $\mu\text{m}$ . For the anode region, the doping must be superior to the one of the gate region, in order to obtain a good injection. So a 1  $\mu\text{m}$  and  $10^{19} \text{ cm}^{-3} \text{ P}^+$  layer has been chosen.

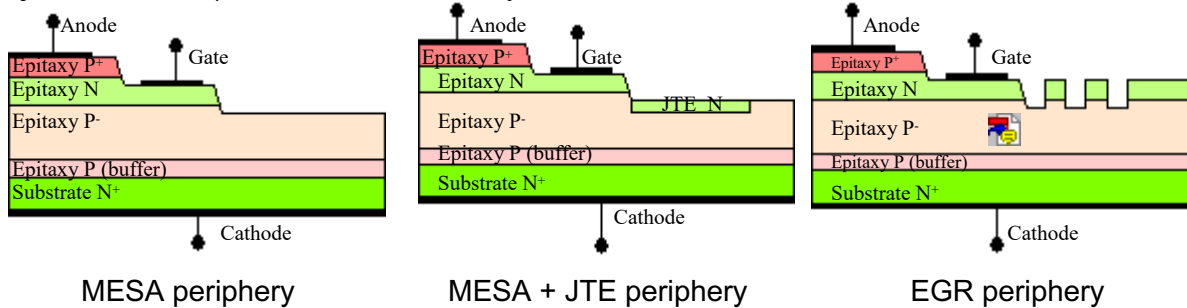
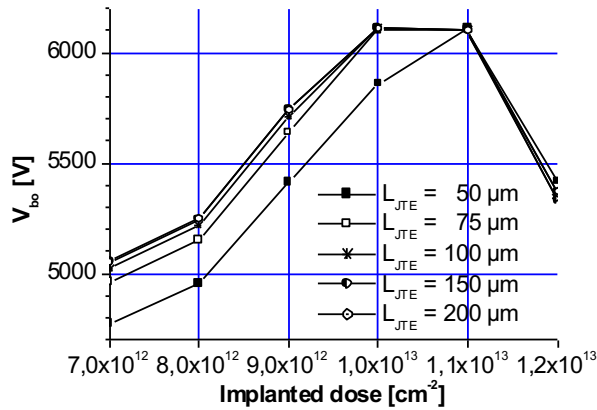


Fig. 3 : 3 Peripheries of the thyristor

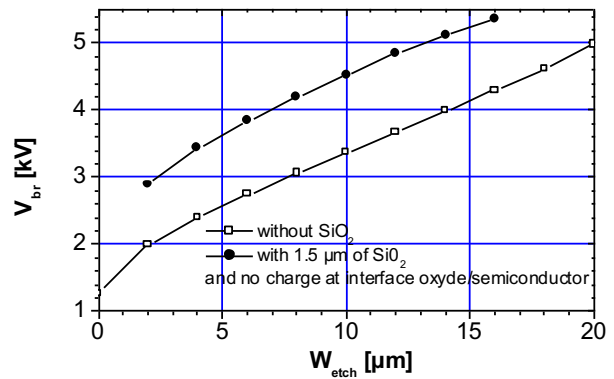
In this study, different peripheries have been developed. The figure n°3 illustrates the MESA, EGR and MESA + JTE structures. Some simulations have been realized to show the influence of different parameters on the breakover voltage. To obtain 5 kV blocking voltage with a MESA structure, it is necessary to etch 18  $\mu\text{m}$  in the P<sup>-</sup> drift layer. With an etch rate of 100 nm/min, it is not easy to realize this structure. For reasons of technology (e.g. lithography or etching rate), the breakover voltage of EGR terminated devices is limited to 4.1 kV [8]. A third periphery (MESA + JTE) was simulated. The breakover voltage is around 80 to 90 % of 6 kV. The results depend on the implanted dose of the JTE (black and white region in the second structure on figure 3), the length  $L_{\text{JTE}}$  of the JTE and the etching depth of the MESA. An example is shown on figure n°4 where the etching depth equals to 1  $\mu\text{m}$ .

With the MESA periphery, other simulations are made to show the influence of the oxide thickness on the breakover voltage. On the figure n°5, the charge density at the interface oxide semiconductor is zero and for a 1.5  $\mu\text{m}$  oxide thickness, the voltage increases by around

1 kV. With a  $5 \times 10^{12} \text{ cm}^{-2}$  charge density, the breakover voltage will vary of  $\pm 50\%$  if the charge is positive or negative, respectively.



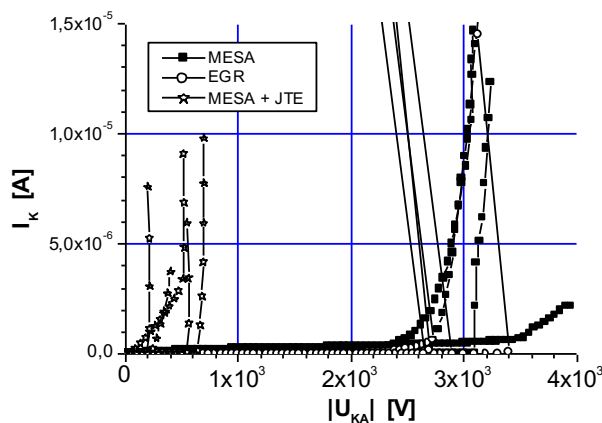
**Fig. 4** : Calculated breakover voltage versus implanted dose in JTE for different JTE lengths



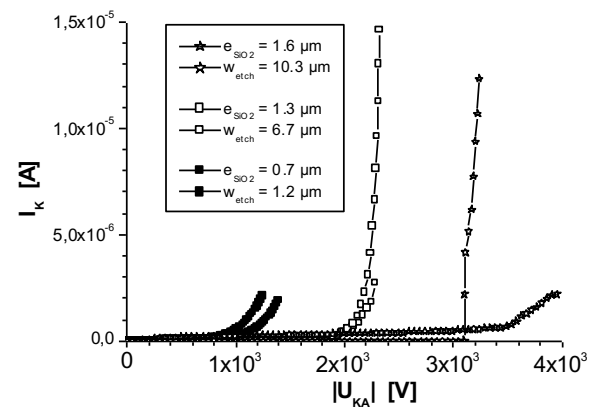
**Fig. 5** : Calculated breakover voltage versus etching depth with or without oxide

### Electrical characteristics

The thyristor is characterized in blocking and forward state. For the blocking state, a 12.5 kV source voltage has been used with a pico-ampermeter. To protect the ampermeter, a circuit has been developed with a 25 MΩ resistance to sustain the high voltage when the thyristor is short-circuited. The figure n°6 shows the best results. Different from what we expected, for the MESA + JTE periphery, the breakover voltage is only 800 V. SIMS (Secondary Ion Mass Spectroscopy) analysis shows a quite high concentration in the JTE, some  $10^{19} \text{ cm}^{-3}$ . According to the simulation shown in figure n°5, the optimal concentration is about  $10^{17} \text{ cm}^{-3}$ . Thus, an error occurred during the technology process. For the EGR periphery, the breakover voltage is 3.4 kV. These results are difficult to increase as there are technology limits due to the lithography and the etching. The MESA protection shows a very good result, 4 kV. In simulation, with 10 μm etching depth and 1.5 μm oxide thickness, the breakover voltage is 4.4 kV.



**Fig. 6** : Measured breakover voltage for the 3 different peripheries, best 5 components each



**Fig. 7** : Measured breakover voltage for the MESA periphery with varying oxide thickness and etching depth

The figure n°7 shows the experimental evolution for the MESA periphery. With the increase of the oxide thickness and the etching depth the breakover voltage increases, too. Considering the simulation results in figure n°5 it could be concluded to have negative oxide charges with a defect density below  $5 \times 10^{12} \text{ cm}^{-2}$ . In order to get more accurate results, it

would be interesting to estimate the charge density by C(V) measurements on MOS capacitors. Otherwise, the charge density could be estimated from the comparison of simulations (like figure n°5) with experimental results of thyristors having the same oxide thickness but different etching depth.

Additionally, electrical characterizations are made in forward. Another set-up has been realized using a Tektronix curve tracer 370A, supplying a sinusoidal (50 Hz) voltage pulse to the cathode. The gate signal supplied by the curve tracer is adapted to the thyristor using a custom-built circuit allowing for a negative gate current with phase, duration and amplitude being adjustable. In figure n°8 the results for Thyristors with an EGR periphery are presented. The best result obtained is 1.3 A ( $340 \text{ A.cm}^{-2}$ ) at 13 V anode-cathode voltage.

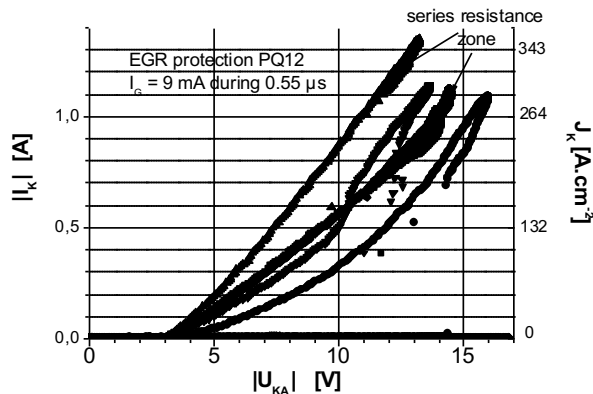


Fig. 8 : Measured on state characteristics for thyristors with EGR periphery

We attribute the high blocking capability of our thyristors to a deep mesa etch and in particular to a thick field oxide. Concerning the on-state behavior certainly we have to solve some problems attributed to the contact resistance.

## Conclusion

4H-SiC GTO thyristors with three different terminations have been realized on samples originated from the same wafer. Compared to state of the art silicon technology these results are encouraging. Moreover, we obtained a blocking voltage of 3.9 kV for devices with a  $35 \mu\text{m}$  drift layer protected by a simple mesa termination. This result is noteworthy compared to recently reported SiC-thyristors [5] where similar blocking voltages are attributed to an improved JTE

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