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SiC power devices onto QUASIC and SiCOI Smart-Cut® substrates : first demonstrations

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Abstract: Wafer bonding technologies have been recognized to provide new substrates structures suitable for the development of Si power devices. Among the multiple examples that could be listed, the possibility to generate PN junctions without thick epitaxial growth and lateral devices onto dielectrically isolated substrates such as SOI (Silicon On Insulator) are significant examples of the interest proposed by wafer bonding. Thin film substrates obtained with the Smart-Cut® technology such as SiCOI (SiC On Insulator) substrates for lateral devices and QUASIC substrates for vertical power devices have already been demonstrated. In this article, we review the recent developments in the field of SiC power devices using these two kinds of SiC Smart-Cut® substrates. Lateral and vertical Schottky diodes have been processed onto SiCOI and QUASIC substrates as a demonstration of feasibility. Simulations, results and prospects are presented in this article.

Introduction

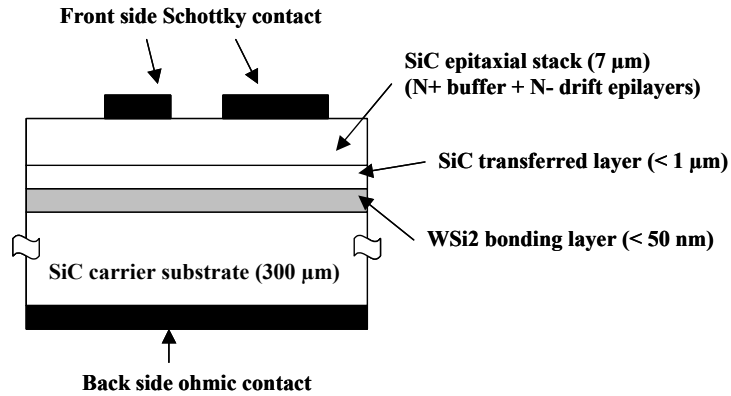
Previous works have been focused on the demonstration and characterization of SiCOI substrates (SiC On Insulator) and QUASIC substrates. In both cases, physical and electrical characterizations have proved that the crystallinity and main electrical features of the SiC transferred layer are not altered by the Smart-Cut® process [1]. Moreover, CVD epitaxial SiC regrowth performed using bulk like growth conditions is possible onto QUASIC substrates [2]. In this article, we will first focus on the fabrication and electrical characteristics of vertical Schottky diodes onto vertically conductive and epitaxially SiC regrown QUASIC substrates. Secondly, electrical simulation, fabrication and electrical results of lateral Schottky devices onto SICOI material will be presented and discussed.

QUASIC Substrates for vertical power devices

This substrate is designed to be compared with conventional 4H SiC low resistivity and low defectivity bulk substrates. Some convincing technical demonstrations have already been demonstrated onto QUASIC substrates. The possibility to grow high quality epilayer with good morphological and electrical properties is one main result. Secondly, the demonstration that the presence of the WSi₂ bonding layer between the seed layer (transferred using the Smart-Cut® process) and the SiC carrier substrate induces no electrical degradation on the current path is also one main point [2].

A Schottky diode structure has been fabricated on one QUASIC substrate. The epitaxial stack has been grown in bulk like conditions in a horizontal cold wall reactor at atmospheric pressure and at a temperature of 1450°C. The epitaxial sequence comprises an N⁺ buffer layer directly grown on the

transferred layer (1 μm thick, doping level $1\text{e}18$ at/cm³), and an N - type drift region with a doping level around $1\text{e}16$ at/cm³. The thickness of the drift layer is about 6 μm . The electrical resistivities of both the thin transferred layer and the SiC carrier substrate are assumed to be 0.03 ohm.cm . Finally, the electrical resistivity of the buried WSi₂ layer is assumed to be 50 $\mu\text{ohm.cm}$. A simple Schottky device has been then manufactured. Vertical Schottky diodes were then fabricated with titanium dots on top and titanium full sheet back side metallization followed by a 400 °C annealing.



The device has no edge termination but it is important to notice that the structure involves the SiC epitaxial layers of a 600V Schottky diode. The complete stack is summarized on figure 1.

Figure 1 : cross section of Schottky diode fabricated onto epilayer stack grown onto QUASIC substrate

Room temperature I(V) forward and reverse measurements

These measurements have been performed onto Schottky diodes of different surfaces (0.05 mm² and 2 mm²). A four probes method has been used. I(V) characteristics are shown on figure 2. Small diodes (0.05 mm²) exhibit classical rectifier behavior (figure 2a) whereas some large diodes (2 mm²) exhibit an excess forward current (figure 2b), in the exponential regime (below 1 V), probably induced by a two barriers behavior. In correlation, we observe a larger reverse current. This effect has been already observed for Ti / 4H SiC diodes onto commercial bulk SiC substrates [3]. Several measurements performed on same diameter diodes along the wafer show that from one diode to another, the measured excess currents are not reproducible. Thus, the most probable reason for such an effect can be attributed to intrinsic material or metal/SiC interfacial defects on the grown structure. This behavior was observed onto commercial substrate [3], but we cannot also exclude that this effect is not induced by the QUASIC substrate.

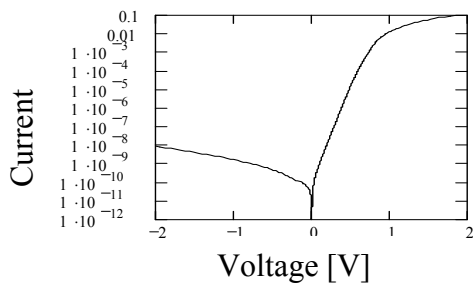
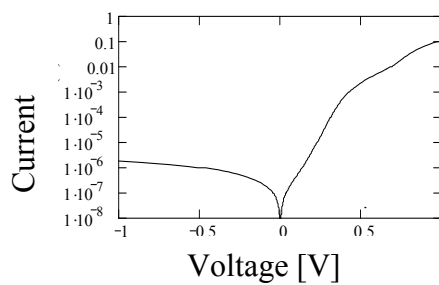


Figure 2a) I(V) on a 0.05 mm² device



2b) I(V) on a 2 mm² device with a double Schottky barriers behavior

Temperature I(V) measurements for ideality factor, SBH and Ron measurements on large diodes (2 mm²)

Further forward current measurements as a function of the temperature in the range of 200-500 K for the extraction of the ideality factor and SBH have been performed. The measurements are shown in figure 3. The ideality factor has been extracted at each temperature by extracting the slope of the ln(I)(V) characteristics. The SBH is extracted from I(V) versus temperature measurements.

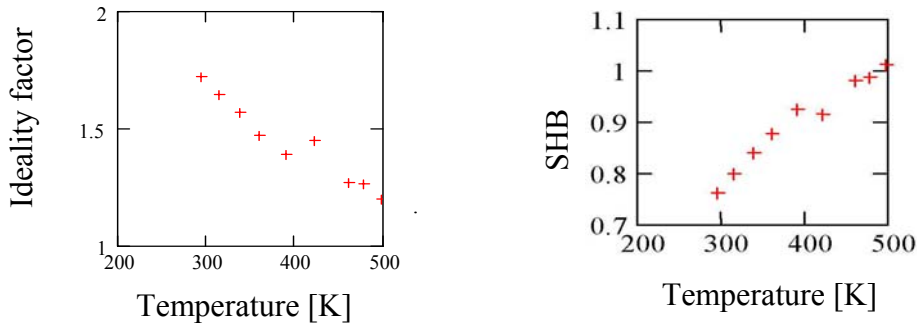


Figure 3a) Ideality factor variation with temperature for the 2mm² diode

3b) SBH extraction for the 2mm² diode

These results show that for large diodes, the ideality factor tends to exhibit an ideal behavior at 500 K, reaching values near 1,2 whereas it is larger than 1.5 at 300 K. Moreover, the extraction of the SBH leads to a value above 1 eV at those high temperatures. These two results show that at 500 K, the diode exhibit nearly ideal behavior. The Ron value variation with temperature has also been measured. The measurement is reported in figure 4a. We also observe a strong variation with temperature with Ron value decreasing from 5 mΩ.cm² at 300 K down to 3 mΩ.cm² at 500 K.

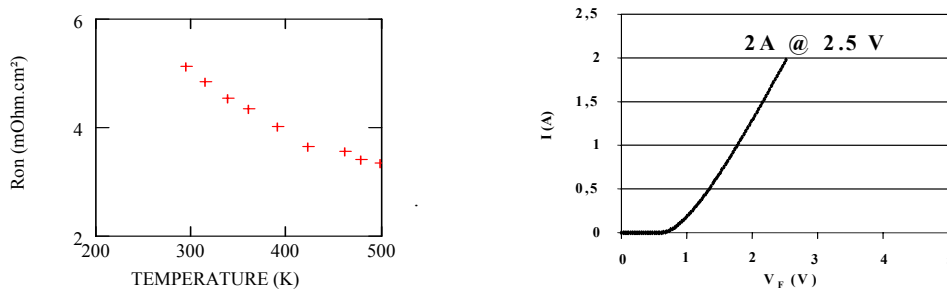


Figure 4a) : Ron variation with temperature

4b) RT forward bias I(V) (S_{diode} : 2 mm²)

Under high current operation (figure 4b), the 2 mm² diodes have shown that 2 amps of forward current can be obtained under 2.5 V bias. This value is quite far from previously published results and also commercially available devices but this result confirms that the QUASIC substrate structure is compatible with power application requiring large vertical current flow. The Schottky diodes manufactured onto this substrate are far from being optimized power devices because of the very simple technology applied and also the choice of metallization that do not provide best electrical characteristics. As an example of improvement, the use of Ni as a back side contact could help improving the electrical behavior of the devices. With using such an improved ohmic contact, we strongly believe that we would obtain state of the art on resistance (in the range of 1 mohm.cm²). Nevertheless, this first result is a good demonstration of the technical viability of the

QUASIC substrates though further improvements and understandings are necessary to optimize the design and fabrication of the substrate itself.

SiCOI Substrates for lateral power devices

SiCOI substrate consists of an active thin SiC layer insulated from the carrier substrate by a buried silicon oxide layer. Conversely to QUASIC substrate, SiCOI ones require lateral device design. As described in [4] for SOI substrates, both top single crystal and buried oxide layers thickness are important for interesting design possibilities in terms of field control (usually known as RESURF design). In the case of SiCOI substrates, thin single crystal SiC layers in the range of 0.2 – 0.5 μm can be achieved on top of thick buried oxide. This kind of structure has been already characterized in terms of electrical properties of the transferred SiC thin film [1]. A typical value of N type doping level of 2×10^{17} at/cm³ with low residual concentrations of compensating defects is demonstrated on top of an oxidized silicon substrate. This kind of structure would be ideal for the demonstration of the RESURF effect on SiC lateral devices.

Aiming a 600V Schottky diode on SiCOI substrate, we have performed electrical simulations, device architecture and process flow definitions, device fabrication and electrical tests. Simulations were carried out with MEDICI software, with most of Ruff SiC parameters [5] and Konstantinov impact ionisation modelling [6]. The structure of the Schottky diode fabricated onto the thin SiCOI substrates is shown in figure 5.

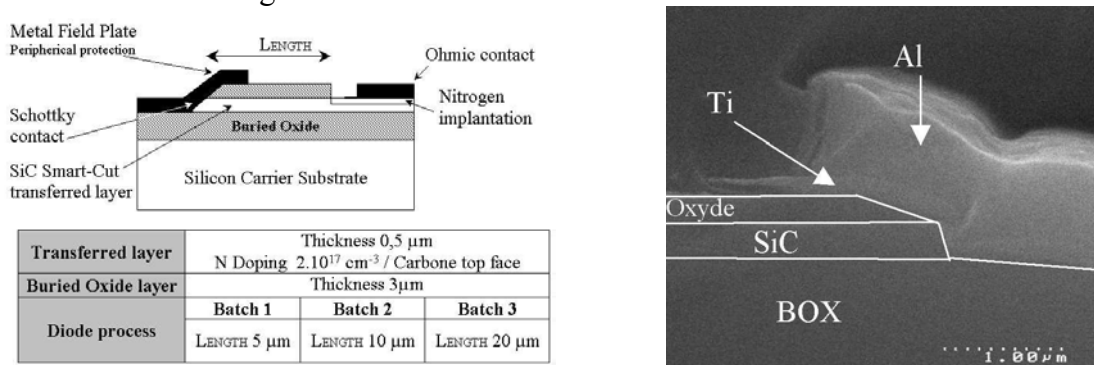


Figure 5: cross sectional of diode structure designed onto thin SiCOI substrate and SEM view of the sloped Schottky contact. Physical and electrical parameters of the substrate are also given.

In this work we use a thin SiCOI substrate, which consists of an 2.10^{17} cm⁻³ N type doped 4H SiC single crystal layer onto an insulated silicon carrier substrate. The transferred crystal is 500 nm thick above a 3 μm silicon dioxide layer. The handle substrate diameter was 4 inches allowing the fabrication process with our 4 inches silicon facilities. The processed SiCOI substrate is shown in figure 6, where the 1,35 inches SiC transferred layer is noticeable onto the large 4 inches carrier substrate (nowadays transferred SiC diameters are 2-3 inches). We have designed devices with three different lengths between anode and cathode contacts : 5 μm, 10 μm and 20 μm. According to simulation results, diodes are designed to sustain 600 V, which is a value calculated for an assumed SBH of 1,2 eV. Forward bias current is estimated to be 300 mA/cm for 2 V forward bias.

The technical process basically contains the following steps. Cathode contact consists of a nickel sputtered layer

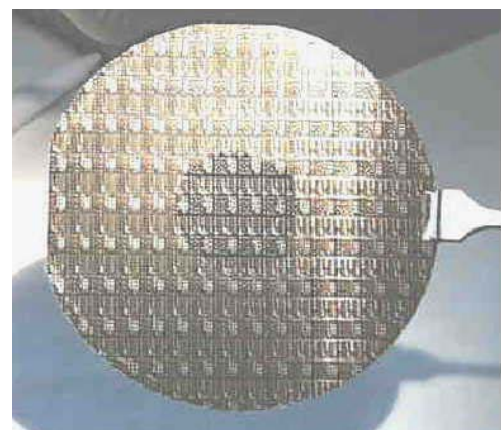


Figure 6:
4 inches SiCOI processed substrate

on a targeted N+ zone 110 nm thick at doping level as high as $7 \cdot 10^{19} \text{ cm}^{-3}$. The low resistivity SiC region for cathode contact was obtained by ion implantation and annealing. Anode contact on the sloped edge of the SiC layer was made by titanium sputtering and subsequent annealing at 400°C during 5 minutes. The fabrication process ended with a $10 \mu\text{m}$ polyimid secondary passivation opened on contacts. This SiCOI substrate has been fully processed onto a 4 inches silicon line including the standard photolithographic tools. Electrical tests have been performed to evaluate both forward and reverse characteristics of these lateral diodes. Figure 7 presents a picture of a device manufactured onto SiCOI substrate.

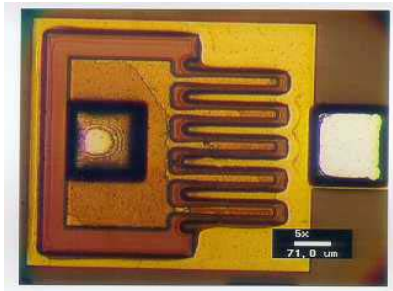


Figure 7:
snapshot of a 2 mm developed Schottky diode onto SiCOI

Electrical measurements

Figure 8 compares for the diode shown in figure 7, the calculated and experimental results on the forward and reverse modes. Die area of the diode is 1.1 mm^2 for active interdigitated area of 0.4 mm^2 . Results on forward mode (left) show that there is two-decade difference between simulation and results meaning the device having high on state resistance. We attribute it to a problem during post-implantation process leading to the partial etching of the N+ zone and leaving a huge ohmic contact resistance. Extracted Schottky barrier heights are closed to 1.2 eV , with an ideality factor of 1.2.

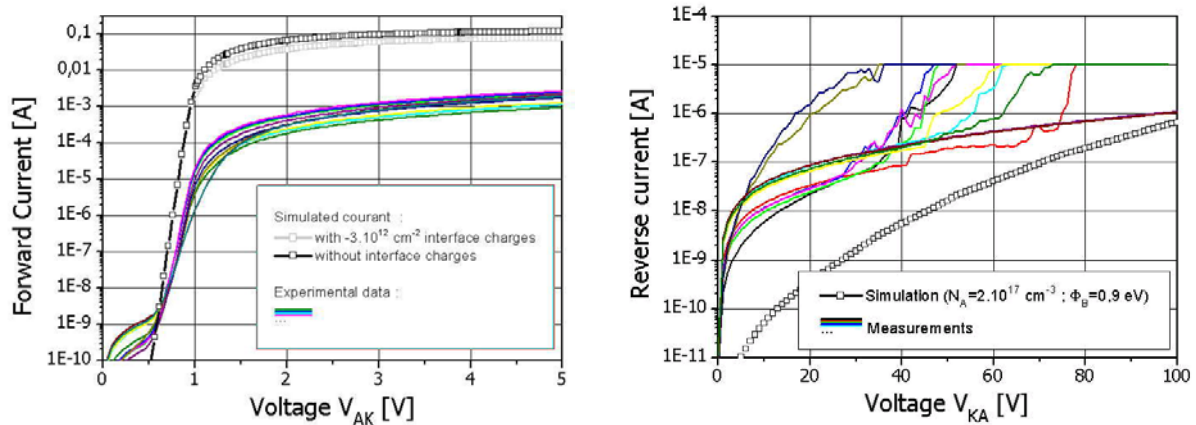


Figure 8: comparison of electrical performances on lateral Schottky diodes between thermo-electrical simulations and experimental results (simulation with interfacial $\text{SiO}_2 / \text{SiC}$ charges is included). Concerned diodes have an inter-electrodes length of $10 \mu\text{m}$ and are developed on 2 mm (active area: $0,4 \text{ mm}^2$). Left is forward and right is reverse measurements.

Reverse characteristics are shown on the right part. Due to the active layer doping Nd-Na of $2 \cdot 10^{17} \text{ cm}^{-3}$, the reverse current is quite high, providing a forward/reverse ratio of 10^2 under 100 V. Nevertheless best components show a blocking voltage of 300 V and the reverse current is consistent with a reverse Ti/ SiC SBH of $0,9 \text{ eV}$. This low SBH instead of $1,2 \text{ eV}$ fully explains the relatively low breakdown voltage of 300 V.

Evidence of RESURF effect on SiCOI

Resurf effect is identified by the influence of the substrate voltage on the electrical field crowding at the Schottky contact. Figure 9 shows the difference between the reverse current characteristics in case of a substrate connexion either to the anode or to the cathode. Assuming that the leakage current is a good representative of the electrical field, this chart demonstrates the RESURF design capability of the SiCOI substrate.

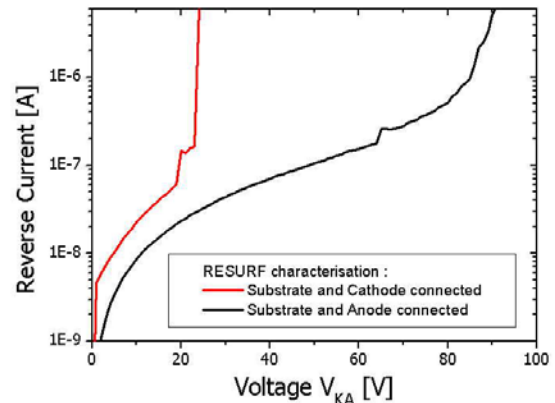


Figure 9: reverse plots of a Schottky diode with substrate connected to anode or cathode.

Conclusions

In this article, two Smart-Cut[®] SiC substrates such as QUASIC and SiCOI are studied for Schottky diode fabrication. Those two substrates use a SiC top single layer ranging from a few hundreds of nanometers to several micrometers, providing silicon carbide power capabilities for devices fabrication with a crystalline quality comparable to SiC bulk substrates. SiCOI substrates potentially support full power system on a single chip and provide the possibility to design new devices not compatible with bulk substrates. QUASIC substrate have demonstrated to sustain a whole Schottky process. Simple fabricated diodes provide high current ratings up to 2 A. Further studies are needed to improve the electrical characteristics of the substrate itself, of the epitaxial layer grown on it.

SiCOI substrates have successfully demonstrated their manufacturability in a 4 inch silicon line allowing technological processes such as ohmic and Schottky contacts, conventional etching, passivation. Those achievements lead to the demonstration of a SiC power Schottky diodes on 4 inches substrate. The presented results show that electrical performances are not yet fully satisfactory though encouraging. Studies are now directed toward thicker SiC structures to improve the electrical conductivity and towards SiC layers with lower doping concentration for increasing the blocking voltage. Those discrete electronics achievements are also useful to pave the way for Systems on Single Chip on SiCOI, which is a promising field of applications for those insulated substrate.

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