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# SINGLE BRANCH OF ENERGY STORAGE SUBMODULES TO INTEGRATE ENERGY STORAGE DEVICES IN HVDC SYSTEMS

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## Abstract

Energy storage systems (ESS) can enhance the reliability of service in power systems with a high share of renewable energy sources. A converter topology that can integrate ESS directly into an HVDC system is presented in this work. The topology consists of a branch of energy storage submodules (ES-SMs) and an inductor. The ES-SMs are based on half-bridges, which are connected to a supercapacitor or a battery by means of a dc/dc converter. The topology is scalable to different voltage levels and since the energy storage elements are distributed among all submodules, it provides a high degree of redundancy. In this work, the converter topology is modelled using an average model and its control designed to regulate the injected dc power and the energy of the ES-SMs. A preliminary sizing of the main elements of the topology is also provided. The simulations show that the ES-SMs can both inject and absorb power from the HVDC system, while maintaining the desired energy in the ES-SMs capacitors.

## 1 Introduction

The rise of the energy consumption and the environmental concerns has increased the growth of renewable energy sources (RES) in recent years [1]. Their variability and remote location contrast with the traditional energy sources, providing drivers to update the power electrical system. In that sense, high voltage direct current (HVDC) is recognised as a key technology to transmit bulk power over long distances, and it is already used to integrate the offshore wind energy, when it is located far from the shore [2]. Energy storage systems (ESS) can be used to cope with the typical power fluctuations of RES, ensuring the continuity of power supply. Grid scale ESS are being connected to the ac grid making use of transformers and low voltage (LV) or medium voltage (MV) power electronic converters to interface with the ESS. Typically, they are based on “plug and play” LV modules inside containers that can be easily delivered and installed [3].

Some authors have also proposed to integrate ESS in the modular multilevel converters (MMC) that are used to exchange power between HVDC and HVAC. Energy storage elements can be distributed in the converter by being connected to capacitors which are present in MMC submodules (SM). An interface device (passive elements or a dc/dc converter) is necessary to connect the ESS with the capacitor in the SM [4], due to the voltage variation of the ESS as a function of the state of charge (SoC) or due to the voltage ripple at the SM capacitor that can lead to an accelerated ageing of the energy storage elements.

Another possibility is to connect the ESS directly to the HVDC without passing through an ac stage as in the previous

solutions. However, the design of the required dc/dc converter to interface both systems is not straightforward as energy storage systems are usually designed for much lower voltages than in HVDC links. In the literature, some dc/dc converters to step down the HVDC have been proposed with [5] and without ac transformers [6],[7]. A grid scale ESS with potentially hundreds of MW, at low voltage is translated in tens of kA considering the ESS connected to a single port. That suggests that converters with distributed ESS may be more attractive to implement such a service. In that sense, some topologies based on series connected MMC SMs have been proposed. In [8] a multiport modular multilevel dc/dc converter that can exchange power between one HV port and several LV ports is introduced. A branch of half-bridge (HB) SMs with a supercapacitor connected to the SM capacitor via an inductive filter is presented in [9]. In this solution, the possible supercapacitor voltage range is limited and then the available energy. Finally, [10], [11] present a converter made of two or more branches of series-connected energy storage submodules (ES-SMs), in which different types of storage can be integrated (supercapacitors, batteries, etc.). The ES-SMs are made of a HB or a full-bridge (FB) that is connected to the storage element via a dc/dc converter. This topology uses an ac circulating current between the two branches to properly balance the ES-SMs.

This paper proposes a single branch of series-connected ES-SMs and an inductor to be connected to an HVDC system. The topology provides less footprint than using two or more branches, at the cost of requiring the same type of storage in each ES-SMs and no possibility to use ac circulating current to balance the modules. This approach is especially suited for applications in which the storage devices of a single branch are

enough to provide the target power and energy. The ES-SMs are made of a HB-SMs connected to a storage element (battery or supercapacitor) via a dc/dc converter. The energy storage elements can then be used over their complete voltage range.

First, topology is presented, highlighting its behaviour during dc faults. Then, its modelling is introduced, considering an average model gathering the behaviour of all ES-SMs in a single one. Finally, the control strategy is presented and validated by means of dynamic simulations in an electromagnetic transient simulation software.

## 2 Converter topology

The converter topology (see Fig. 1) is based on branch of series-connected energy storage submodules and an inductor, which is installed between the two poles of an HVDC system. The ES-SMs are made of a HB connected to a capacitor ( $C_{sm}$ ), which can be inserted or bypassed. Each capacitor is also connected to a storage device by means of a dc/dc converter (composed of another HB and an inductor). The storage device can be a battery or a supercapacitor.

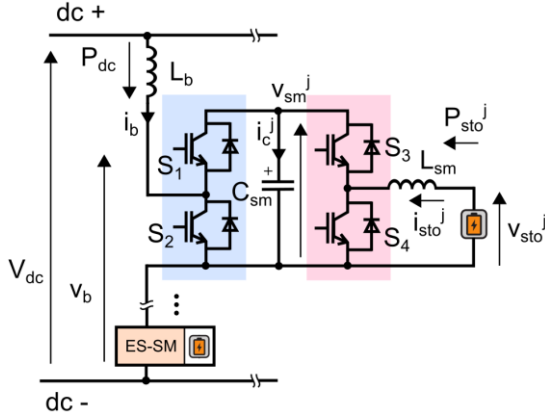


Fig. 1. Scheme of the ES-SM branch detailing the structure of the one of the ES-SMs.

The ES-SM branch can inject or absorb power from the HVDC system. The sign of  $P_{dc}$  determines the sign of  $i_b$ . The use of a single branch does not allow to use an ac circulating current to balance the SMs as it is done in [11].

The switches  $S_1, S_2$  allow to insert or bypass the ES-SM, meaning that for  $P_{dc} > 0$ , the capacitor  $C_{sm}$  is charged with  $i_b$  or bypassed. When  $P_{dc} < 0$ ,  $C_{sm}$  is discharged with  $i_b$  or bypassed.

The switches  $S_3, S_4$  allow to exchange power between the capacitor  $C_{sm}$  and the storage device. When  $P_{dc} > 0$ ,  $P_{sto} < 0$ ,  $C_{sm}$  is discharged ( $S_3$  closed) or disconnected ( $S_4$  closed) from the storage device. When  $P_{dc} < 0$ ,  $P_{sto} > 0$ ,  $C_{sm}$  is charged ( $S_3$  closed) or disconnected ( $S_4$  closed) from the storage device.

Since both  $S_1, S_2$  and  $S_3, S_4$  are operated in a complementary way, two degrees of freedom are provided by the ES-SM branch. The first degree of freedom, given by  $S_3, S_4$  is used to control  $P_{dc}$ . The second degree of freedom,  $S_1, S_2$ , is used to control the energy of the capacitors  $C_{sm}$ , to ensure a constant voltage value to properly operate the converter. The opposite

strategy could also be considered, but it has been decided to follow an analogous approach to the MMC control without energy storage, in which the switches of the SM ( $S_1, S_2$ ) are used to control the energy in the capacitors thanks to voltage balancing algorithms (VBA), also named balancing capacitor algorithms (BCA). The ES-SM presented in this paper requires a BCA to ensure a similar voltage in all capacitors. However, since an average model of the ES-SM is considered (as it is explained in Section 3), the development of the BCA is left out of the scope of this work.

### 2.1 Behaviour in case of a dc fault

This subsection analyses the behaviour of the topology during a dc fault. The analysis is done conceptually without simulations, to have a first insight about the performance of the topology under abnormal conditions. It allows to check if the blocking of the ES-SMs is enough to protect the IGBTs or if additional equipment is needed to ensure their safety. The constraints during dc faults should also be considered for the sizing of components.

A dc fault is considered between the two poles of the HVDC system, next to the ES-SM branch (see Fig. 2). After the fault, the current through the branch starts to increase, following the direction of the red arrows and fed by the capacitors in the inserted ES-SMs.

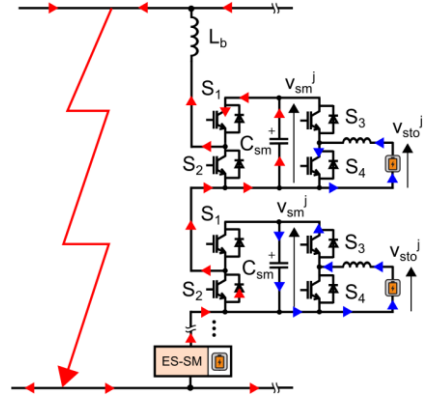


Fig. 2. Scheme of the selected topology showing the current paths of inserted and bypassed ES-SMs during a dc fault.

The highest current is achieved when the converter is already supplying the nominal power to the HVDC system, in the same direction than the red arrows (storage devices discharging).

Once the fault is detected, the ES-SMs must be blocked to protect the IGBTs from the overcurrent. The inductor  $L_b$  serves to limit the di/dt and may be selected to ensure that there is enough time to send a signal and block the ES-SMs, before the current exceeds the rating of the IGBTs. The procedure to obtain the value of  $L_b$  is described in detail in Section 5.1.

Between the starting of the fault and the blocking of the branch, there are a certain number of inserted ES-SMs to provide a voltage similar to  $V_{dc}$ . In the bypassed ES-SMs (lower ES-SM in Fig. 2), the current circulates through the diode in  $S_2$ . On the contrary, in the inserted ES-SMs, the current discharges the capacitor  $C_{sm}$  and circulates through  $S_1$ . The semiconductors must be sized considering the possible overcurrent during these instants.

Both in inserted and bypassed submodules, the storage devices discharge following the direction of the blue arrows. If  $S_3$  is

off and  $S_4$  on, the current flows through  $S_4$  without affecting the capacitor. On the contrary, if  $S_3$  is on and  $S_4$  off, the current flows through diode  $S_3$  and charges the capacitor.

Since the voltage of the capacitor ( $v_{sm}^j$ ) in the inserted ES-SM decreases if  $S_4$  is on or if  $S_3$  is on and the fault current overpasses the current from the energy storage device ( $-i_b > i_{sto}^j$ ), it must be ensured that until the blocking of the ES-SMs, their voltage remains higher than  $v_{sto}^j$ . Otherwise, if  $v_{sm}^j$  becomes lower than  $v_{sto}^j$ , the diode in  $S_3$  will uncontrollably conduct. It can be a criterion to size the capacitance of the ES-SM.

After blocking the ES-SMs (all switches off), the fault current circulates through the diode of  $S_2$  without affecting the capacitor of the ES-SMs. Since all the capacitors are bypassed, there is no voltage source in the path between the fault and the branch, thus, at this stage, the current through the branch will decrease until 0, until the inductor is completely discharged.

Based on the previous analysis, special attention must be put between the starting of the fault and the blocking of the switches, since after the blocking, the current through the branch starts to diminish, as no capacitors are inserted. Then after blocking the switches, the energy storage elements do not contribute to the fault current. This is an interesting feature of the presented topology that some others considered in the literature (some of the converters in [9]) do not have.

### 3 Modelling of the converter

This work assumes that all the ES-SMs are identical and that their voltage is totally balanced. Then, the voltages of the ES-SMs can be modelled as a single voltage for the whole branch. The same applies to the insertion and bypass orders, they can be averaged to a single variable (modulation index) [12]. Based on the previous, the stack of ES-SMs is represented by an equivalent voltage source ( $v_b$ ), which models the voltage generated by the inserted ES-SMs. The model of the ES-SM branch can be seen in Fig. 3.

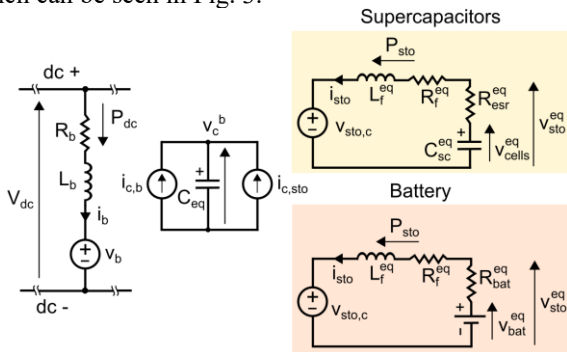


Fig. 3. Average model of the ES-SM branch considering supercapacitors or batteries as storage element.

Separately, in another circuit, the capacitances of the ES-SMs are represented as one equivalent capacitor ( $C_{eq}$ ) with a voltage ( $v_c^b$ ) that corresponds to the sum of all the voltages in the ES-SMs. On one side, the capacitor is connected to a current source ( $i_{c,b}$ ) that models the charge and discharge from the branch current ( $i_b$ ). The current source is coupled with the voltage source ( $v_b$ ) by means of the modulation index ( $m_b$ ), as it is shown by the following expressions:

$$v_b = m_b v_c^b \quad (1)$$

$$i_{c,b} = m_b i_b \quad (2)$$

$$m_b = \frac{n_b}{N_b} \quad (3)$$

$$C_{eq} = \frac{C_{sm}}{N_b} \quad (4)$$

where,  $n_b$  is the number of inserted ES-SMs and  $N_b$  is the total number of ES-SMs in the branch.

On the other side of the equivalent capacitor, another current source ( $i_{c,sto}$ ) is connected, which represents the current coming from the storage device, leading to (5).

$$C_{eq} \frac{d}{dt} v_c^b = i_{c,b} + i_{c,sto} \quad (5)$$

This current source is coupled with a voltage source ( $v_{sto,c}$ ), and together they represent an equivalent dc/dc converter that interfaces the capacitor circuit and the storage circuit (it represents the behaviour of all the dc/dc converters in each ES-SM). The expressions of both coupled sources are:

$$i_{c,sto} = D_b i_{sto} \quad (6)$$

$$v_{sto,c} = D_b v_c^b \quad (7)$$

where,  $D_b$  is the duty cycle of the equivalent dc/dc converter and  $i_{sto}$  is the current coming from the equivalent storage device circuit. The storage devices can be made of batteries or supercapacitors, leading to two different models for the storage circuit (yellow and orange areas in Fig. 3):

$$v_{cells}^{eq} = (R_f^{eq} + R_{esr}^{eq}) i_{sto} + L_f^{eq} \frac{d}{dt} i_{sto} + v_{sto,c} \quad (8)$$

$$v_{bat}^{eq} = (R_f^{eq} + R_{bat}^{eq}) i_{sto} + L_f^{eq} \frac{d}{dt} i_{sto} + v_{sto,c} \quad (9)$$

where,  $R_f^{eq}$  and  $L_f^{eq}$  are the equivalent resistance and inductance of the filter in the equivalent dc/dc converter.  $R_f^{eq}$  is set to have a certain efficiency of the equivalent inductive filter at maximum current.  $L_f^{eq}$  comes from the aggregation of inductors in each ES-SM, whose values are defined to have an acceptable current ripple (as explained in detail in Section 5.6).  $R_{esr}^{eq}$  is the equivalent series resistance of the supercapacitor and  $R_{bat}^{eq}$  is the equivalent series resistance of the battery, both obtained from setting a certain efficiency of the equivalent storage device at maximum current.  $v_{cells}^{eq}$  is the internal voltage of the equivalent supercapacitor,  $v_{bat}^{eq}$  is the internal voltage of the equivalent battery. The equivalent battery is modelled as a dc voltage source, while the equivalent supercapacitor is modelled as a capacitor. This means that the internal voltage of the equivalent battery will remain constant for any SoC, whereas the internal voltage of the equivalent supercapacitor will change as a function of the SoC.

### 4 Control of the converter

As mentioned in Section 2,  $P_{dc}$  is controlled using  $S_3, S_4$ , which in the average model corresponds to the duty cycle of the equivalent dc/dc converter,  $D_b$ . The energy in the equivalent capacitor is regulated with  $S_1, S_2$ , which corresponds to the modulation index,  $m_b$ . Both control schemes are described below.

#### 4.1 Energy regulation of the equivalent capacitor

The control scheme to regulate the energy of the equivalent

capacitor is depicted in Fig. 4.

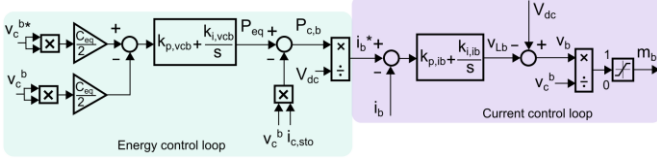


Fig. 4. Control scheme to regulate the energy of the equivalent capacitor with two cascaded controllers: energy and current controller.

The outer energy loop compares the energy of the equivalent capacitor with the measured value. The controller output allows to calculate the necessary power  $P_{c,b}$  that must be provided by the ES-SM branch from the HVDC side. Then, the reference dc current of the ES-SM branch can be computed ( $i_b^*$ ), which is the input for the current loop control. The reference current is compared with the measured current, allowing the controller to calculate the required voltage across the branch inductor. From that, the voltage that must be applied with the controlled voltage source  $v_b$  can be obtained, which is divided by  $v_c^b$  to calculate the desired modulation index.

In order to tune the controller of the energy control loop, it is assumed that the dynamics of the inner control loop are much faster, so that the inner control loop can be neglected. Based on this hypothesis, the system under control is an integrator (capacitive circuit), and an energy closed loop 2<sup>nd</sup> order transfer function is obtained if a proportional integral controller is used (10).

$$\frac{W}{W^*} = \frac{k_{p,vcb}s + k_{i,vcb}}{s^2 + k_{p,vcb}s + k_{i,vcb}} = \frac{2\xi\omega_0s + \omega_0^2}{s^2 + 2\xi\omega_0s + \omega_0^2} \quad (10)$$

The gains of the controller can be also expressed as a function of the desired  $\xi$  and  $\omega_0$  in (11) and (12).

$$k_{p,vcb} = 2\xi\omega_0 \quad (11)$$

$$k_{i,vcb} = \omega_0^2 \quad (12)$$

Regarding the inner current control loop, the plant can be simplified into an inductive plus resistive circuit. In order to obtain a first order closed loop current response, the gains of the controller are set as follow:

$$k_{i,ib} = \frac{R_b}{\tau_{ib}} \quad (13)$$

$$k_{p,ib} = \frac{L_b}{\tau_{ib}} \quad (14)$$

where,  $\tau_{ib}$  is the time constant value for the inner current loop response. In order to ensure that the hypotheses of the control tuning are valid,  $\tau_{ib}$  must be smaller than the inverse of  $\omega_0$  to guarantee that the inner loop is faster.

#### 4.2 Regulation of the dc power

The control scheme to regulate the dc power is shown in Fig. 5. It is composed of two cascaded control loops: an outer power loop and an inner current loop.

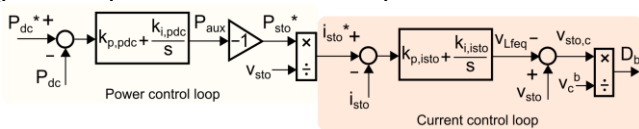


Fig. 5. Control scheme to regulate the dc power, with two cascaded controllers: power and current controller.

The dc power reference is compared with the measured power in the HVDC system, and the error is the input of the power controller. The output is an auxiliary power that is transformed into the power that the storage must provide ( $P_{sto}^*$ ). The difference between  $P_{dc}^*$  and  $P_{sto}^*$  are the losses in the converter, that is why  $P_{dc}^*$  cannot be used to calculate directly the needed current in the storage circuit  $i_{sto}^*$ , since the parasitic resistances and voltage drops in semiconductors in the system will lead to a slightly different measured  $P_{dc}$ . The objective of the previous controller is to compensate the losses by giving a value of  $P_{sto}^*$  that ensures the desired  $P_{dc}^*$ .  $P_{sto}^*$  is then divided by  $v_{sto}$  to obtain the reference current for the storage circuit  $i_{sto}^*$ , which is the input of the inner current loop. The controller in the inner control loop calculates the necessary voltage in the inductive filter and allows to compute the required voltage to be imposed by the dc/dc converter  $v_{sto,c}$ . It is then divided to obtain its duty cycle  $D_b$ .

For the tuning of the controllers, it is assumed that dynamics of the inner control loop are fast enough to be neglected when designing the outer power controller. Then, in order to tune the power controller, the plant can be represented as a unitary gain ( $P_{sto}^* = P_{dc}^*$ ), considering the losses as a perturbation since they are difficult to measure, and they represent a reduced percentage of the total power. The simplified closed loop system is shown in Fig. 6.

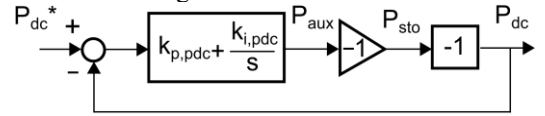


Fig. 6. Simplified closed loop control scheme to regulate the dc power.

Then, the resulting closed loop transfer function has one zero ( $z$ ) and one pole ( $p$ ) (15)-(17).

$$\frac{P_{dc}}{P_{dc}^*} = \frac{k_{p,pdc} + k_{i,pdc} + 1}{k_{p,pdc} + 1} \frac{1}{s + 1} \quad (15)$$

$$z = -\frac{k_{i,pdc}}{k_{p,pdc}} \quad (16)$$

$$p = -\frac{k_{i,pdc}}{k_{p,pdc} + 1} = -\frac{1}{\tau_{pdc}} \quad (17)$$

The objective of the tuning is to obtain a closed loop response as similar as possible to a first order system with a time constant  $\tau_{pdc}$ . To do this, the zero is set to be  $k$  times the pole ( $z = kp, k > 5$ ), which allows to calculate the gains of the controller as a function of  $k$  and  $\tau_{pdc}$  (18)-(19).

$$k_{i,pdc} = \frac{k}{\tau_{pdc}(k-1)} \quad (18)$$

$$k_{p,pdc} = \frac{1}{k-1} \quad (19)$$

The tuning of the inner current controller is analogous to the current controller in Section 4.1, since the plant can also be represented as an inductive and resistive circuit:

$$k_{i,i_{sto}} = \frac{R_f^{eq}}{\tau_{i_{sto}}} \quad (20)$$

$$k_{p,isto} = \frac{L_f^{eq}}{\tau_{isto}} \quad (21)$$

where,  $\tau_{isto}$  is the desired time constant of the inner loop. In order to ensure that the hypotheses of the control tuning are valid,  $\tau_{isto}$  must be smaller (faster control) than  $\tau_{pdc}$ .

## 5 Preliminary sizing

This section presents a preliminary sizing of the main elements of the ES-SM branch assuming the case with supercapacitors as energy storage device.

### 5.1 Inductance $L_b$

The inductance in the ES-SM branch is selected to protect the semiconductors of ES-SMs from the high currents during a dc fault. It is assumed that  $V_{dc}$  (corresponding to the voltage of the inserted ES-SM in steady-state operation) is applied at the inductor terminals, which provokes an increase of the current through the branch. When the current reaches  $i_{threshold}$ , the fault is detected and after a certain time delay ( $t_{delay}$ ), the IGBTs are blocked. The highest current is reached just before blocking, since afterwards the current starts to decrease as explained in Section 2. Assuming that the maximum current rating of the IGBTs is  $I_{max}^{IGBT}$ , the minimum inductance to keep the current below  $I_{max}^{IGBT}$  can be expressed as in (22).

$$L_b = v_L \frac{dt}{di} = \frac{V_{dc} t_{delay}}{I_{max}^{IGBT} - I_{threshold}} \quad (22)$$

### 5.2 Reference voltage of the equivalent capacitor $v_c^{b*}$

The voltage of the equivalent capacitor (or sum of the voltages in all ES-SMs) is related to the inserted voltage of the branch by means of the modulation index as shown in (1). The modulation index is always lower than 1 (according to (3)), and by defining a maximum value  $m_{max}$  (usually around 0.9 to ensure the proper operation during transients), it is possible to calculate the required  $v_c^{b*}$ . Considering that the nominal power ( $P_{dc}^{nom}$ ) is injected to the HVDC system and that there is a voltage drop in the branch inductor (23).

$$v_c^{b*} = \frac{V_{dc} + R_b(P_{dc}^{nom}/V_{dc})}{m_{max}} \quad (23)$$

### 5.3 Required number of ES-SMs $N_b$

The number of required ES-SMs in the branch is calculated considering the previous value of  $v_c^{b*}$  and the nominal voltage of an ES-SM ( $v_{sm}^{nom}$ ) (24).  $N_b$  could be further increased to consider additional ES-SMs for redundancy purposes.

$$N_b = \frac{v_c^{b*}}{v_{sm}^{nom}} \quad (24)$$

### 5.4 Nominal voltage of the storage device $v_{sto}^{eq nom}$

The nominal voltage of the equivalent storage device is calculated by multiplying the number of installed ES-SMs by the nominal voltage of a single storage device ( $v_{sto}^{nom}$ ) (25).

$$v_{sto}^{eq nom} = N_b v_{sto}^{nom} \quad (25)$$

### 5.5 Capacitance of the equivalent supercapacitor $C_{sc}^{eq}$

The capacitance of the equivalent supercapacitor is obtained from the target storage energy in the ES-SM branch ( $W_{sc}$ ). It is assumed that the voltage of the equivalent supercapacitor can vary between  $v_{sto}^{eq nom}$  and a minimum value ( $v_{sto}^{eq min}$ )

$$C_{sc}^{eq} = \frac{2 W_{sc}}{v_{sto}^{eq nom 2} - v_{sto}^{eq min 2}} \quad (26)$$

If considering the capacitance of the supercapacitor in a single ES-SM, the same expression in (26) can be used but replacing the energy and the voltages for the ones of a single supercapacitor. If a more precise sizing of the supercapacitors taking into account the equivalent series resistance is desired, the methodology in [13] can also be employed.

### 5.6 Equivalent filter inductance in the dc/dc converter $L_f^{eq}$

The necessary inductance in the dc/dc converter of a single ES-SM is obtained based on the maximum acceptable current ripple ( $\Delta I_L$ ). It is assumed that the dc/dc converter works at a switching frequency  $f$  (it is not used in the average model). Then, the required inductance is shown in (27).

$$L_{sm} = \frac{(1-D)D v_{sm}^{nom}}{f \Delta I_L} \quad (27)$$

The highest ripple, which leads to the worst-case value of  $L_{sm}$  happens for  $D = D_{wc} = 0.5$ .

Then, the equivalent filter inductance to be used in the average model is obtained as in (28).

$$L_f^{eq} = N_b L_{sm} \quad (28)$$

### 5.7 Equivalent capacitance $C_{eq}$

Three different criteria are considered to obtain the value of  $C_{eq}$ , and the most restrictive value among them is used (29).

$$C_{eq} = \max(C_{eq}^1, C_{eq}^2, C_{eq}^3) \quad (29)$$

To calculate the capacitance of an ES-SM, (4) can be used.

**5.7.1 Criterion 1:** Defining the value of  $C_{eq}^1$  from the acceptable overvoltage in the capacitor after blocking ( $I_b > 0$ ). With the branch current being positive, when the ES-SMs are blocked, the current circulates through  $S_1$  diode, charging the capacitor, while the current in the storage circulates through diode  $S_4$ . The sum of the voltage of all capacitors is higher than  $V_{dc}$ , thus the current will eventually go to 0. In between, an amount of energy coming from the HVDC system, and the inductor  $L_b$  is transferred to the equivalent of the ES-SM, increasing its voltage. By setting a maximum admissible voltage in the equivalent capacitors it is possible to isolate and calculate  $C_{eq}^1$  from:

$$\frac{L_b v_c^{b*} i_{init}^2}{2(v_c^{b*} - V_{dc})} = \frac{1}{2} C_{eq} (v_c^{max 2} - v_c^{init 2}) \quad (30)$$

where,  $v_c^{init}$  and  $v_c^{max}$  are the initial and maximum admissible voltage of the equivalent capacitor, respectively.  $i_{init}$  is the initial branch current at the instant of blocking (the worst case being the nominal current).

**5.7.2 Criterion 2:** Defining the value of  $C_{eq}^2$  from the acceptable overvoltage in the capacitor after blocking ( $I_b < 0$ ). When the branch current is negative and the ES-SM is blocked, the current coming from the storage device is the one charging the capacitor (through diode  $S_3$ ). If analysing a single ES-SM,  $v_{sto}^{nom}$  is lower than  $v_{sm}^{nom}$ , which means that the current will eventually go to 0, but the ES-SM capacitor will be charged during this time interval. By setting a maximum admissible voltage for the capacitor ( $v_{sm}^{max} = v_c^{max}/N_b$ ), a similar expression to (30) can be employed to find  $C_{eq}^2$ :

$$\frac{L_{sm} v_{sm}^{nom} i_{init}^2}{2(v_{sm}^{nom} - v_{sto}^{nom})} = \frac{1}{2} C_{sm} (v_{sm}^{max 2} - v_{sm}^{init 2}) \quad (31)$$



where,  $v_{sm}^{init}$  is the initial voltage of the ES-SM capacitor.

**5.7.3 Criterion 3:** Defining the value of  $C_{eq}^3$  from the acceptable undervoltage in the ES-SM capacitor in between a dc fault and the blocking ( $I_b < 0$ ). As mentioned in Section 2.1, between the time in which the fault is detected and the blocking of the semiconductors, the fault current discharges the inserted ES-SM capacitors (their number being given by  $N_{ins} = m_b N_b$ ). The branch current keeps increasing since the sum of voltages of the capacitors is applied at the inductor terminals. The voltage of the capacitors must not be lower than the voltage of the storage device, to avoid the uncontrollable conduction of diode  $S_3$ . During these instants, the energy of the capacitors is transferred to the inductor (neglecting the losses), then, the following expression can be used to determine  $C_{eq}^3$  and ensure that diode  $S_3$  will not conduct:

$$\frac{1}{2} L_b (I_{max}^{IGBT} - i_{init}^2) = \frac{-N_b C_{eq}}{2N_{ins}} (v_{ins}^f - v_{ins}^{ini})^2 \quad (32)$$

where,  $v_{ins}^f = N_{ins} v_{sto}^{nom}$  is the final voltage value corresponding to the sum of voltages in the capacitors;  $v_{ins}^{ini} = N_{ins} v_{sm}^{nom}$  is the initial voltage corresponding to the sum of inserted capacitor voltages;  $I_{max}^{IGBT}$  corresponds to the final current of the branch (to comply with subsection 5.1 and ensure the safety of the semiconductors).

Finally, the resistances in the average model are defined by imposing a certain efficiency at maximum current ( $R_b, R_f^{eq}, R_{esr}^{eq}$ ).

## 6 Case study

A symmetric monopole HVDC link composed of two MMCs, which are represented considering an average model (see Fig. 7) is implemented in EMTF software. MMC 1 controls the active and reactive power, while MMC 2 controls the reactive power and the voltage of the HVDC system. The ES-SM branch is connected at the terminals of MMC 2. The main parameters of the system are illustrated in Table 1.

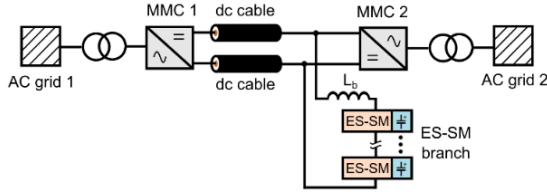


Fig. 7. Scheme of the HVDC link with two MMCs and the ES-SM branch connected at the terminals of MMC 2.

Table 1. Main parameters of the ES-SM for the case study.

Parameter	Value	Units
Nominal dc power $P_{dc}^{nom}$	200	MW
HVDC pole to pole voltage $V_{dc}$	640	kV
Steady-state modulation index $m_{max}$	0.9	-
Branch inductance $L_b$	95.6	mH
Branch resistance $R_b$	10.24	$\Omega$
Reference for the sum of the voltages in the ES-SMs $v_c^{b*}$	714.67	kV
Number of ES-SMs $N_b$	189	-
Branch equivalent capacitance $C_{eq}$	4.06	$\mu$ F

Equivalent filter inductance $L_f^{eq}$	820	mH
Equivalent filter resistance $R_f^{eq}$	0.66	$\Omega$
Equivalent nominal storage voltage $v_{sto}^{eq nom}$	274	kV
Equivalent series resistance of the supercapacitor $R_{esr}^{eq}$	1.69	$\Omega$
Equivalent capacitance of the supercapacitor $C_{sc}^{eq}$	7.9	mF
Minimum equivalent voltage of the supercapacitor $v_{sto}^{eq min}$	82	kV
Energy of the supercapacitor $W_{sc}$	270	MJ

First, the power of the ES-SM branch goes from 0 to the nominal power (200 MW) positive, meaning that the branch is absorbing power from the HVDC link (see Fig. 8(b)). Then, the power is reduced to 0 again, until a new power reference is given, this time negative, which means that the ES-SM branch injects the power to the HVDC link. The measured power follows the power references without overshoot, similarly to a first order response according to the control design strategy. It can be seen in Fig. 8(a) that the dc voltage where the ES-SM branch is connected remains stable during the absorption and injection of power. Fig. 8(c) shows how the control of the ES-SM maintains the voltage of the equivalent capacitor to the reference value during the ES-SM branch operation, with only minor transients when the power changes.

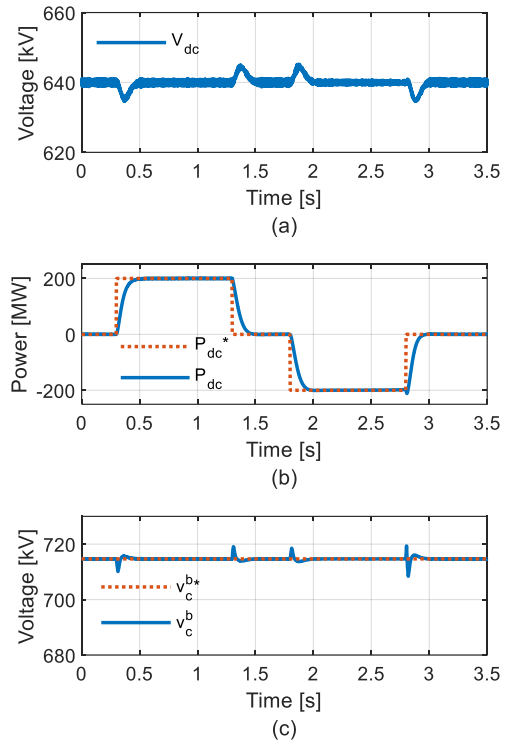


Fig. 8. Simulation results. (a) HVDC voltage. (b) dc power of the ES-SM branch. (c) Voltage of the equivalent capacitor of the ES-SM branch.

Fig. 9 shows the current and the voltage in the supercapacitors (Fig. 9(a) and Fig. 9(b), respectively). Fig. 9(a) shows that the current in the supercapacitors is negative when the nominal

power is absorbed from the HVDC system. Since the power is kept constant between 0.3 s and 1.3 s, the current decreases in absolute value due to the charging of the supercapacitors (see Fig. 9(b)). When the ES-SM starts to inject power into the HVDC system, the current in the supercapacitors increases and keeps doing so to maintain the same power while being discharged (reducing their voltage). The nominal power is absorbed by the ES-SM branch during 1 s and then it is injected 1 s as well. Due to the parasitic resistances in the model, the voltage at the end of the simulation is slightly lower than at the beginning, highlighting that the supercapacitors in the ES-SM branch have lost a small amount of energy in the process.

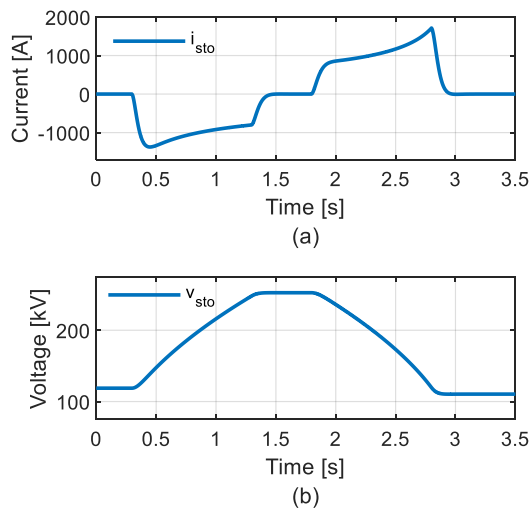


Fig. 9. Simulation results. (a) Current from the supercapacitors. (b) Voltage of the supercapacitors.

In Fig. 10(a) the modulation index, representing the percentage of the inserted ES-SM in the branch, is depicted, showing small variations around 0.9 either when injecting or absorbing power.

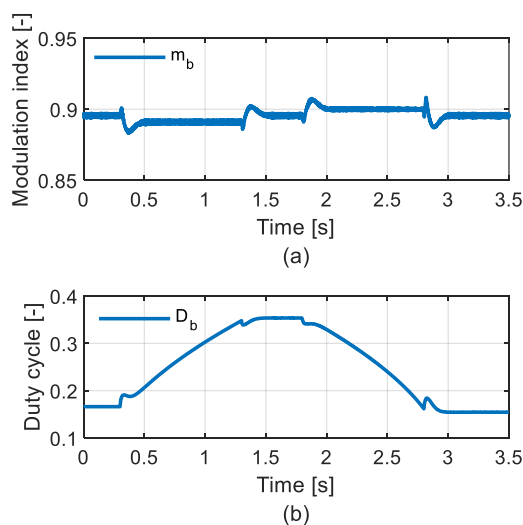


Fig. 10. Simulation results. (a) Modulation index. (b) Duty cycle of the equivalent dc/dc converter.

Fig. 10(b) presents the duty cycle of the equivalent dc/dc converter. The duty cycle changes similarly to the voltage of the supercapacitors to control their current.

## 7 Conclusion

This paper has proposed a converter topology based on a branch of series-connected ES-SM and an inductor to integrate energy storage elements in HVDC applications. It can be scalable to different voltage levels and in case of adding more ES-SMs or oversizing them, it also offers a certain degree of reliability. It has been shown how the topology responds to dc faults in a qualitative way, outlining that the design of the inductor may be employed to protect the semiconductors in the ES-SMs. Then, the converter topology has been modelled and its control strategy and tuning presented. A preliminary sizing of the main parameters of the converter topology is also given. The simulations confirm that the ES-SMs branch can inject or absorb the desired power into the HVDC system, while properly controlling the energy of the capacitors in the ES-SMs. Further work should focus on the strategy to balance the energy in the capacitors of the ES-SMs when considering a detailed model. Also, the power sharing algorithm among the different storage devices in the ES-SMs should be investigated.

## 8 Acknowledgements

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