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Capacitive Modulator Design Optimization using Si and strained-SiGe for Datacom Applications

Ismaël Charlet, Yohan Désières, Delphine Marris-Morini and Frédéric Boeuf

Abstract— Silicon photonics has become an industrial reality for datacom applications. Nevertheless, as Si suffers from a low electro-optic effect, commercial modulators are few-mm long. The efficiency can be enhanced by using strained-SiGe or by using a semiconductor insulator semiconductor (SIS) architecture. In this paper, we develop a model based on a perturbative approach to optimize capacitive modulator using full-Si or including a thin layer of strained SiGe. This model is coupled with an optimization algorithm in order to estimate the highest optimal modulation amplitude for different operating frequencies.

Index Terms— Capacitive modulator, electro-refractive modulator, silicon photonics, strained-SiGe

I. INTRODUCTION

SILICON photonics is a low-cost technology for optical interconnects, by using CMOS facilities. The strong index contrast between Si and SiO₂ enables propagation within compact waveguides. Currently the main commercial application concerns datacom operating at 1310nm wavelength within datacenters. Among the required components used on photonic chips, modulators play a key role. The 2 main standards for datacom are transceivers at 25Gb/s with 4 parallel lines to achieve 100Gb/s, and 4x53GBd using PAM-4 for 400Gb/s [1].

Commercial modulators used for datacom are mainly based on phase-shifter sections within an interferometer structure. Since Si exhibits low Kerr and Pockels effects, modulation is achieved using the free plasma dispersion effect within a Mach-Zehnder Interferometer (MZI). Typically, modulators are based on a PN-junction working on reverse voltage within the optical waveguide. This solution offers bandwidth above 50 GHz and low insertion penalty [2]. However, PN-junction suffers from a relative lack of efficiency, as a consequence the modulator footprint is few millimeters-long. This turns out to be a problem when considering the Electronic Integrated Circuit (EIC). For long phase shifters, the device cannot be driven using a single-

stage electrode. Instead Travelling Wave Electrode (TWE) or Multistage Electrode are required, which represent an extra-energy cost [3] and lead to a more complex EIC design.

It has been estimated that modulators can be driven with single-stage electrodes for lengths below 1mm at 25GBd and 500μm at 53GBd [4]. Si-based PN-modulators are not efficient enough to achieve these footprint targets. Changing electronic structure or materials is required to improve electro-refractive modulator efficiency.

Capacitive modulators are based on a Semiconductor Insulator Semiconductor (SIS) electrical junction. In accumulation regime, the modulator is highly efficient since the free carrier concentration varies linearly with the applied voltage. Several demonstrations have been performed, showing modulation up to 28GHz and $V_{\pi}L_{\pi}$ below 1 V.cm [5][6][7]. Thus capacitive modulators constitute an appealing solution to reduce modulator footprints. However, the capacitive modulator presents several technological challenges. First it requires a more complex integration than PN-modulators, even though CMOS-compatible. Indeed, few steps dedicated to the capacitive modulator fabrication must be added to the conventional photonic flow. Moreover, unless advanced processes based on recrystallization are used [8], in most of the case polycrystalline silicon (polySi) is necessary to form the SIS junction. This has a huge impact on the device performances. Optical losses about 10 dB/cm have been reported within polycrystalline silicon waveguides [9][10]. III-V semiconductor alloys can be used to improve dramatically the efficiency but at the cost of a complex integration process [11].

Alternatively, strained SiGe is CMOS-compatible material which can be used to improve electro-refractive effect. Strained-SiGe takes benefit from a lower effective mass than Si [12], leading to higher efficiency for holes than Si. Several PN-modulators using strained-SiGe have been reported and have shown high efficiency [13] but the impact on insertion losses remains unclear. Indeed, the ratio $\Delta n/\Delta\alpha$ is lower for strained SiGe than for Si at $\lambda=1310$ nm This means that optical losses

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could increase more than the phase shifter efficiency. Therefore, it is not straightforward to know if higher Optical Modulation Amplitude (OMA) can be reached using SiGe alloys, and to determine the optimum operating geometry and Ge concentration for a given operating frequency.

This work focuses therefore on the optimization of Si-based capacitive modulator using an optional strained-SiGe, for datacom applications by maximizing OMA instead of efficiency. The objective is to achieve a footprint small enough such as the phase shifter can be driven by a single-stage electrode. Previous work on modeling SIS modulator were relying on fully analytic model [13][14] or fully numerical approach [15][16]. In [14] optical modes and carrier distribution were determined using fully analytical approach to assess the performance of devices with various materials such as SiGe and InGaAsP, but no device optimization was carried out. In [15][16] a full simulation of Si-based SIS was proposed, including the RF propagation line but no systematic optimization of geometry nor materials was done. In this work we propose to address this point by using a combination of numerical and analytical models allowing to run the exploration of a wide space of parameters. In part I, a numerical model coupled with an optimization algorithm is developed to assess ultimate modulator performances. In part II, optimization is performed for full-Si and Si/SiGe capacitive modulators for 100Gbs/s and 400Gb/s applications. Finally, in part III, we discuss the obtained results.

I. MODELLING CAPACITIVE MODULATOR WITH STRAINED-SiGe

For Datacom applications, dynamic Optical Amplitude Modulation (OMA) is the figure of merit (FoM) that should be considered, which takes into account for both phase shifter efficiency and losses. Fig. 1(a) shows a MZI set in quadrature. Considering ON-OFF Keying (OOK) operation, the intensity differences between the different symbols should be maximized. This FoM is OMA, which corresponds to the optical intensity difference between 0 and 1 bits as shown in Fig. 1(b). In the case of PAM-4 application, 4 different OMA values are involved as indicated in Fig. 1(c). For an electro-refractive modulator within a MZI in quadrature working in push-pull operation, analytic calculations of OMA have been performed in [14]. For OOK-NRZ operation (2 different symbols) with an input power $I_0 = 1\text{mW}$, OMA in mW can be expressed as:

$$\text{OMA} = \exp \left[- \left(\alpha^{\text{prop}} + \frac{\alpha^{\text{max}} + \alpha^{\text{min}}}{2} \right) \cdot L \right] \cdot \sin(|\Delta\Phi \cdot L|) \quad (1)$$

With L the modulator length (mm), $\Delta\Phi$ the phase-shift (rad/mm), α^{prop} the scattering losses of an undoped waveguide (mm^{-1}), α^{Vmin} the linear losses due to material & free carrier absorption at the minimal voltage (mm^{-1}) and α^{Vmax} the linear losses due to material & free carrier absorption at the maximal voltage (mm^{-1}). In the ideal case OMA should be equal to 0dBm, meaning perfect lossless constructive and destructive interferences. PN-modulators exhibiting OMA equal to

-2.25dBm at 50GHz have been reported [17]. From this, the optimum length to maximize OMA can be deduced:

$$L_{\text{opt}} = \frac{1}{\Delta\Phi} \cdot \text{atan} \left(\frac{\Delta\Phi}{\alpha^{\text{prop}} + \frac{\alpha^{\text{max}} + \alpha^{\text{min}}}{2}} \right) \quad (2)$$

For PAM-4 operation, 4 different OMA values are defined. OMA outer is the maximal amplitude difference, whereas OMAs top, central and bottom concern inner amplitude differences between intermediate levels. In the ideal case, OMA outer is 0dB, while OMA top, central and bottom are -4.77dB. In the case where the PAM-4 signal is generated optically using LSB and MSB modulator sections, it is demonstrated that these inner OMA are all equivalent and equal to 1/3 of the outer OMA if the LSB modulator length is around:

$$L = \frac{2}{3} L_{\text{opt outer}} \quad (3)$$

With $L_{\text{opt outer}}$ the optimum length to maximize OMA outer.

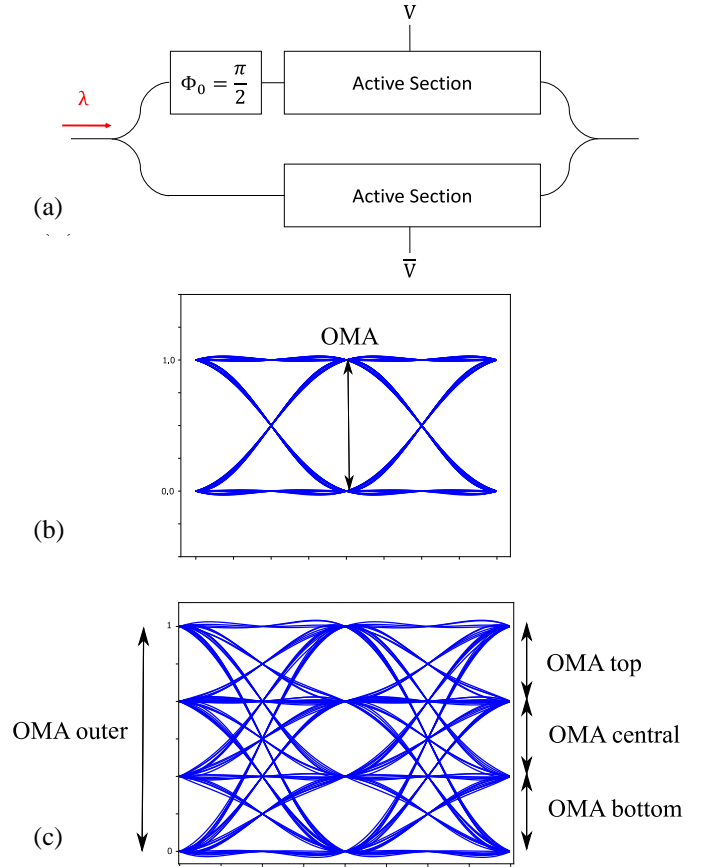


Fig. 1. (a) MZI in quadrature for OOK-NRZ. (b) Eye-diagram for OOK. (c) Eye-diagram for PAM-4 modulation.

A. Capacitive Structure

Studied capacitive modulators are based on stacking a p-doped SOI layer, a dielectric layer (SiO_2) and a n-doped polySi layer. An extra p-doped SiGe-layer can be added between the Si and the capacitor dielectric as shown on Fig. 2.

Waveguide thickness is either 220 or 300nm [18]. Because our Si-Platform relies on 300nm thick SOI waveguides, we

focus the later work on 150nm-thick Si and polySi layers while maximizing the overlap between the guided mode and the accumulation layers. For results presented here, the waveguide width is taken as 400nm as it has been seen as a good compromise to avoid leakage in doped arms and field dissymmetry. Trends are however similar for single-mode waveguide widths in the range 300-500nm. The bandgap of strained SiGe (eV) as a function of the Ge-content is taken from [19]:

$$E_g(x) = 1.12 - 0.96x + 0.43x^2 \quad (4)$$

Strained-SiGe leads to higher optical losses due to bandgap shrinking [20] so thickness should be minimized. A thickness larger than the Debye length (~ 10 nm) is detrimental in term of the $\Delta n/\Delta\alpha$ ratio. Thus, we set the SiGe thickness to 15nm as show in Fig. 2 and take the Ge-content in the SiGe layer as a parameter. The oxide thickness tox has a major impact on both efficiency and electrical bandwidth and is a second parameter. Its maximum value is set to 15nm to achieve higher efficiency than PN-modulator [15].

Finally, when designing capacitive modulators for frequencies > 1 GHz, minimizing the access resistance is mandatory. Therefore, a special emphasis is put on the access resistance optimization, with 3 sections of homogeneous doping for each arm of the modulator (N_{++} , N_+ , N_d for the polySi doping levels, P_{++} , P_+ , N_a for the SOI doping levels, xn_+ , xp_+ , ln_+ , lp_+ for the doping positions). We consider that the strained-SiGe layer is p-doped with a concentration equal to N_d due to fabrication constraints [21]. This constitutes a model with 12 tunable parameters shown in Fig. 2.

In order to optimize capacitive modulators design, a model is developed to be able to compute several thousand devices allowing deep optimization. The model is based on a perturbative approach [22]. The problem can be split into 3 parts: a computation of the mode profile in the undoped waveguide, a carrier profile distribution computation and finally an electro-refractive computation to estimate the resulting impact on the mode's effective index.

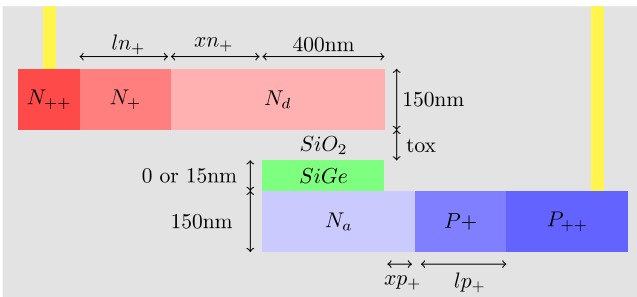


Fig. 2. Studied capacitive modulator using a horizontal capacitor oxide and strained-SiGe

B. Optical Mode calculation

First the optical mode is calculated. Since the oxide thickness lies only between 5 and 15nm, we can approximate that the oxide thickness variation has a little impact on the optical mode. This means only one optical computation is required for Si-

based capacitive modulator, with an oxide thickness set in the middle to 10nm.

For SiGe/Si modulator, the optical mode depends on the Ge-content as well. The refractive index of strained SiGe has been studied experimentally [20]. It has been measured that the refractive index varies slowly with Ge-content, starting at 3.5 for Si and reaching 3.59 for 27% Ge-content at 1310nm. Moreover, the SiGe-thickness is only 15nm, so we can expect a small impact of the Ge-content on the calculated optical mode for Ge-content below 30%. Finally, one field distribution is enough again for SiGe/Si modulator, with a Ge-content set to 20% and an oxide thickness set to 10nm.

These 2 optical mode calculations are performed using Lumerical software as shown on Fig. 3 [23]. Concerning the SiGe device, only 4% of the optical power is within the SiGe layer.

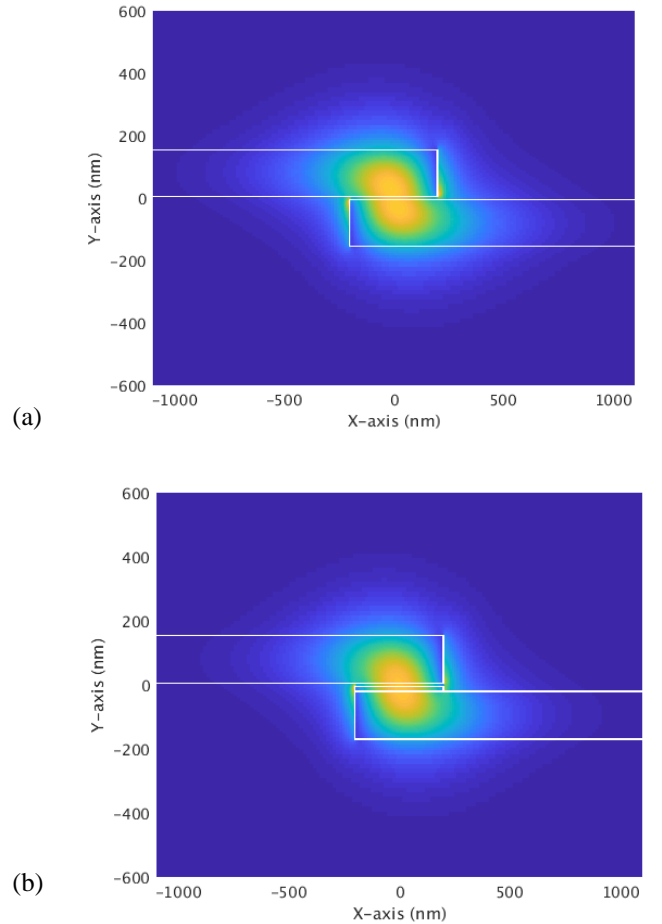


Fig. 3. TE-mode in the capacitive structure. (a) full-Si modulator. (b) SiGe/Si modulator with 15nm-thick $Si_{0.8}Ge_{0.2}$ computed on Lumerical Mode

C. Carrier Distribution Modeling

Additionally, the electrical behavior of the SIS junction must be calculated. The carrier distribution variations are mainly located at the oxide interfaces. In the following, the problem is reduced to a 1D-problem, perpendicular to the junction surface as shown in Fig. 4.

The calculation consists on solving the carrier distribution on the SIS junction. This is performed by computing numerically 1D-Poisson equation on Matlab [24]. In the output results plotted in Fig. 5, the depletion and accumulation regimes are

clearly visible. Moreover, the band offset between Si and SiGe implies a clear and sharp concentration discontinuity at the SiGe/Si interface [25].

Because we are looking for short modulators, the modulator 3dB-bandwidth is given by the low-pass filter formula:

$$fc = \frac{1}{2\pi RC} \quad (5)$$

With R the access resistance and C the junction capacitance. The capacitance of the capacitive modulator (F/mm) is given by the dual plate capacitance:

$$C = \epsilon_{SiO_2} \cdot w_{capa} / t_{ox} \quad (6)$$

With ϵ_{SiO_2} the relative permittivity of SiO₂, w_{capa} the waveguide width (set to 400nm) and t_{ox} the grid oxide thickness.

The access resistance is calculated by integrating the doping profiles of the bottom and top slabs. The integration is performed assuming 2.5 width-slab and stops at the waveguide edges as shown in Fig. 4. Here we assume the same resistivity for Si and polySi, given by Masetti model [26]:

$$R = R_n + R_p \quad (7)$$

$$R_p = \int (q \cdot hslab \cdot N_{Si}(x) \cdot \mu_p)^{-1} \cdot dx \quad (8)$$

$$R_n = \int (q \cdot hslab \cdot N_{polySi}(x) \cdot \mu_n)^{-1} \cdot dx \quad (9)$$

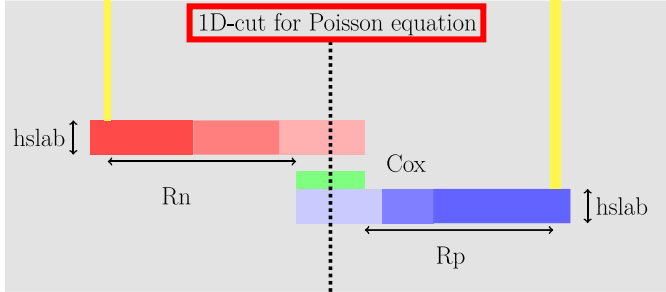


Fig. 4. 1D-cut used for solving 1D-Poisson equation and capacitance and resistance values used for bandwidth computation

With $hslab$ the Si and polySi slab thicknesses set to 150nm, q the elementary electric charge, $N_{Si}(x)$ the doping concentration in the SOI as a function of the position, $N_{polySi}(x)$ the doping concentration in the polySi as a function of the position and $\mu_{n,p}$ respectively the electrons and holes mobility in Si.

D. Electro-refractive Perturbation

Finally, the optical and electrical calculations are combined using the perturbation theory. The electro-refractive coefficients of Si are estimated to be at 1310nm [27]:

$$\Delta n_{Si} = 2,98 \cdot 10^{-22} \Delta n_e^{1.016} + 1,25 \cdot 10^{-18} \Delta n_h^{0.835} \quad (10)$$

$$\alpha_{Si} = 3,48 \cdot 10^{-22} \Delta n_e^{1.229} + 1,02 \cdot 10^{-19} \Delta n_h^{1.089} \quad (11)$$

For strained-SiGe, the theoretical coefficients for Ge-content between 10% and 50% are [28]:

$$\Delta n_{SiGe}(x) = (1,2 + 4 \cdot x) \cdot 1,25 \cdot 10^{-18} \Delta n_h^{0.835} \quad (12)$$

$$\alpha_{SiGe}(x) = (1,4 + 6 \cdot x) \cdot 1,02 \cdot 10^{-19} \Delta n_h^{1.089} \quad (13)$$

This leads to the computation of the phase-shift (°/m) and losses (dB/m) thanks to [29]:

$$\Delta \Phi = \frac{360}{\lambda} \cdot \frac{\int \int n(x,y) \cdot \Delta n(x,y) \cdot |E(x,y)|^2 \cdot dx \cdot dy}{\int \int n_{eff} \cdot |E(x,y)|^2 \cdot dx \cdot dy} \quad (14)$$

$$\Gamma_L = -\frac{20}{\ln(10)} \cdot \frac{2\pi}{\lambda} \cdot \frac{\int \int n(x,y) \cdot k(x,y) \cdot |E(x,y)|^2 \cdot dx \cdot dy}{\int \int n_{eff} \cdot |E(x,y)|^2 \cdot dx \cdot dy} \quad (15)$$

With $\Delta n(x,y)$ the local index variations given by the electro-refractive coefficients, $E(x,y)$ the optical field amplitude from the Lumerical simulation, n_{eff} the effective index and $k(x,y)$ the imaginary part of the refractive index. Optical absorption of intrinsic materials and electro-refractive coefficients are considered for $k(x,y)$. For silicon at 1310nm, intrinsic absorption is assumed to be 0 at 1310nm. Theoretical values have been used for strained-SiGe taken from [30].

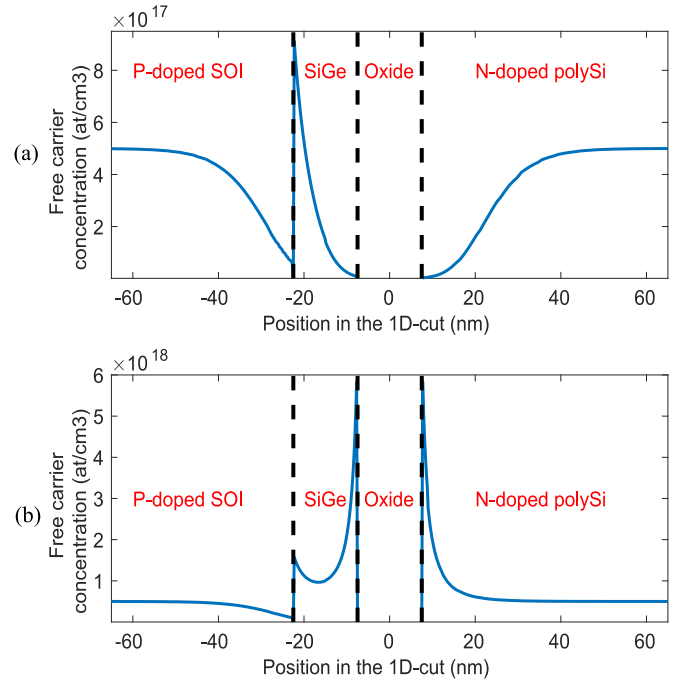


Fig. 5. Free carrier concentration computed by solving 1D Poisson equation for a 15nm-thick grid oxide and $N_a = N_d = 5e17at/cm^3$. (a) in depletion at 0V. (b) in accumulation at 1.8V

E. OMA Optimization

Once the optical simulation is performed, the modulator simulation on Matlab takes approximately 6 s. This is short enough to allow OMA optimization for the 12 optimization parameters. This is performed with a genetic algorithm with elitist selection [31]. Genetic algorithms are suitable to solve this problem since they perform a random search in the parameters space and exhibit a weak dependency on initial values. Fig. 6. shows the algorithm convergence. The algorithm is found to converge after 10000 modulators simulations, which

corresponds to 17h of calculations using 8 cores working at 3GHz.

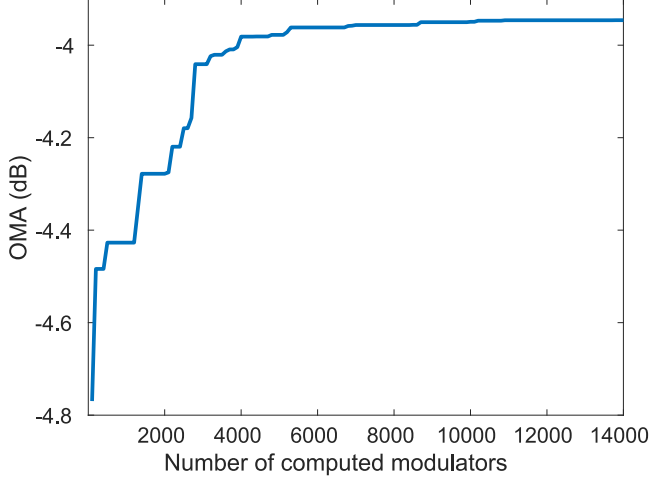


Fig. 6. Optimization of the capacitive modulator. The FoM to maximize is the OMA. The algorithm has converged after 10000 simulations.

II. OPTIMIZED OMA RESULTS

The model coupled with the genetic algorithm is used to optimize OMA. This is done at 25Gb/s OOK for 100G applications and at 53GBd PAM-4 for 400G applications. The minimum voltage is set to 0V, and the maximum voltage to 1.8V.

A. Results for 25Gb/s OOK

As seen previously, 25Gb/s operation can be driven with a single-stage electrode if the modulator footprint is below 1mm. Besides it is shown that modulators with a 3dB-bandwidth of 20GHz are sufficient for 25Gb/s NRZ operation [32]. Thus the optimization is performed to maximize OMA for 1mm-long device, with a cut-off frequency of 20GHz at least. This is done for full-Si modulators and for SiGe/Si modulators. Once the optimized modulator design is found, the model result is compared to full numerical simulation with Lumerical. Optimized OMAs calculated are reported in Fig. 7, the scattering losses α^{prop} (depending on the fabrication platform) is set on the x-axis and decreases the OMA by $\exp(-\alpha^{prop})$.

Concerning the full-Si optimized modulator, the maximum achievable OMA is found to be -1.38dB (for scattering loss = 0). This is obtained with a capacitor oxide thickness equal to 5.5nm, leading to $V_{\pi}L_{\pi}=0.47V.cm$. At 0V, the optical losses are about 0.72dB/mm and increase to 1.43dB/mm at 1.8V. The optimized modulator parameters are given in Table 1.

In addition, using strained-SiGe improves the optimized OMA. The optimized maximum OMA (i.e. for scattering losses equal to 0) is equal to -0.78dB, using 20% Ge in the SiGe alloy and a 9nm-thick capacitor oxide. Despite a thicker grid oxide, this configuration is more efficient thanks to the strained-SiGe with $V_{\pi}L_{\pi} = 0.4V.cm$. Free carrier absorption losses vary from 0.32dB/mm at 0V to 1.09dB/mm at 1.8V. Further, one can notice that the SiGe/Si modulator exhibits higher efficiency than full-Si modulator (71°/mm for full-Si and 78°/mm for SiGe/Si), whereas absorption losses remain lower (1.44dB/mm at 1.8V for full-Si against 1.08dB/mm for SiGe/Si). This is not

completely intuitive considering $\Delta n/\alpha$ is lower for SiGe than for Si. This results will be discussed in more details later.

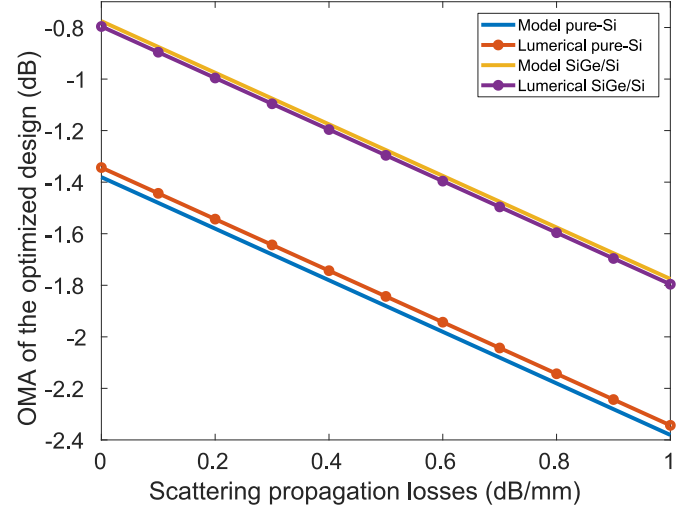


Fig. 7. Optimized OMA for full-Si and SiGe/Si capacitive modulators for 25GBd/s NRZ operation. Optimization is performed for 1mm-long modulator.

TABLE I
OPTIMIZED MODULATOR PARAMETERS FOR 25GBD AND 53GBD OPERATIONS

Name	Si 20GHz	SiGe 20GHz	Si 37GHz	SiGe 37GHz
t_{ox} (nm)	5.5	9	8.4	10
%Ge	--	20%	--	25%
N_d (at/cm ³)	3.8e17	2e17	6.4e17	4.7e17
N_a (at/cm ³)	3.7e17	1.7e17	4.5e17	3.2e17
N_+ (at/cm ³)	3.2e18	1.2e18	5.3e18	4.5e18
P_+ (at/cm ³)	3.6e18	1.2e18	3.6e18	2.8e18
N_{++} (at/cm ³)	7.9e19	5.1e19	9.6e19	8.7e19
P_{++} (at/cm ³)	8.2e19	4.3e19	9.5e19	9.6e19
Length (mm)	1	1	0.5	0.5

B. Results for 53GBaud PAM-4

Here we focus on the possibility to achieve 400G operation, using 53GBd PAM-4 format, with a single-stage electrode for a device length below 500 μ m. A 3dB-bandwidth up to 37GHz is sufficient to achieve 53GBd operation [33]. The optimized results for full-Si and SiGe/Si modulators are plotted in Fig. 8.

For the full-Si modulator, the optimized outer OMA is found to be -4.11dB, meaning inner OMA equal to -8.89dB. Here a 8.4nm-thick capacitor oxide is used leading to $V_{\pi}L_{\pi}=0.59V.cm$. Free carrier absorption varies from 1.27dB/mm to 1.78dB/mm between 0V and 1.8V.

Concerning the SiGe/Si modulators, the best achievable outer OMA shifts to -2.5dB (for scattering losses =0). This corresponds to inner OMA equal to -7.3dB. This result is obtained with a 10nm-thick capacitor oxide and a 25% Ge-content, leading to $V_{\pi}L_{\pi}=0.38V.cm$. Free carrier absorption increases from 1.13dB/mm at 0V to 1.98dB/mm at 1.8V.

III. DISCUSSION

Fig. 7 and Fig. 8 show that the model results are in good agreement with numerical simulations, validating the initial assumption of reducing the electronic simulation into a 1D-problem. Assuming approximatively 10min computation time to simulate a capacitive modulator with Lumerical, a single optimization process would require 70 days using Lumerical with the same hardware configuration (8 cores operating at 3GHz).

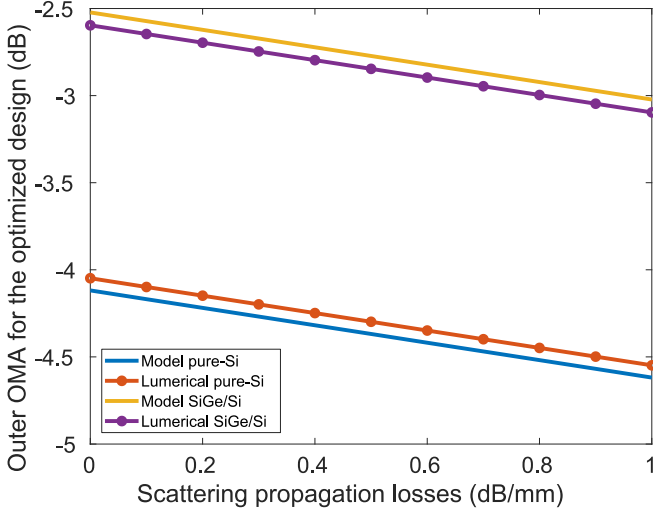


Fig. 8. Outer OMA for optimized full-Si and SiGe/Si capacitive modulators for 53Gbd PAM-4 operation. Optimization is performed for 500 μ m-long modulator.

A. 25Gb/s OOK result discussion

From the 25Gb/s operation results, capacitive modulators seem attractive. Optimum OMA for full-Si modulators is found to be -1.38dB for lossless propagation. This result shifts to -2dB for 7dB/cm propagation losses. Thus, 1mm-long full-Si capacitive modulators with relatively high propagation losses exhibit OMA equivalent to PN-modulators [17]. This indicates that it should be possible to reach high OMAs with capacitive modulators for 25GB/s, even with high scattering losses.

Furthermore, using strained-SiGe improves considerably the OMA. For the optimized SiGe/Si modulator, the OMA increases to -0.78dB. Compared to the optimized full-Si modulator, the optimized strained-SiGe modulator exhibits a higher efficiency. With strained-SiGe, the optimum modulator has a thicker interfacial oxide, leading to a smaller device capacitance. This allows to have a slightly higher resistance and thus lower doping levels in Si ($N_a=1.7e17at/cm^3$ with SiGe against $N_a=3.7e17at/cm^3$ without SiGe). As a result, and even if the ratio $\Delta n/\Delta\alpha$ is lower for SiGe alloys, the SiGe/Si configuration shows higher efficiency while exhibiting lower free carrier absorption losses. In particular, the OMA remains below -2dB for propagation losses up to 10dB/cm. This means that SiGe/Si modulators are even more suitable for 25Gb/s. High OMA is achieved, whereas 1mm-device footprint allows a single-stage electrode driving.

B. 53Gbaud PAM-4 result discussion

The obtained results for 53Gbaud show how challenging it is to design 500 μ m-long modulators operating at 37GHz. Indeed,

the length of the modulator has to be reduced to remain in lumped mode. Compared to the 25Gbd OOK operation, the modulation length is halved while the bandwidth is almost doubled. It means that the capacitance must increase, while at the same time the RC constant must be reduced to increase the bandwidth. Logically, after the genetic optimization process, the bandwidth target is reached by increasing all doping levels compared to the 25Gb/s results (for both full-Si and SiGe/Si modulators). Besides the doping levels get closer to the waveguide center. Both changes lead to higher free carrier absorption. As a consequence, the optimized full-Si modulator exhibits a low outer OMA of -4.11dB even without considering any scattering losses. This value is lower than values already reported for PN-modulators [17]. Thus, using a full-Si capacitive modulator with a single-stage electrode is expected to be less performant than PN junctions for 53Gbd operation.

Using strained-SiGe improves significantly the results again. The ideal outer OMA for lossless propagation reaches -2.5dB, which is close to 2mm-long PN-modulators. For scattering losses below 10dB/cm, the outer OMA remains higher than -3dB. Here the optimal Ge-content in the SiGe layer reaches 25%, while it is only 20% for 25Gbd OOK operation. Nevertheless, the capacitor oxide thickness for 25Gbd OOK and 53Gbd PAM-4 remains close (9nm and 10nm). From this, it is clear that the bandwidth is increased by reducing the access resistance rather than the capacitance. Furthermore, the efficiency is improved slightly (78 $^\circ$ /mm for 25Gbd against 84 $^\circ$ /mm for 50Gbd) compared to the optimized design for 25Gb/s since the Ge-content increases by 5%.

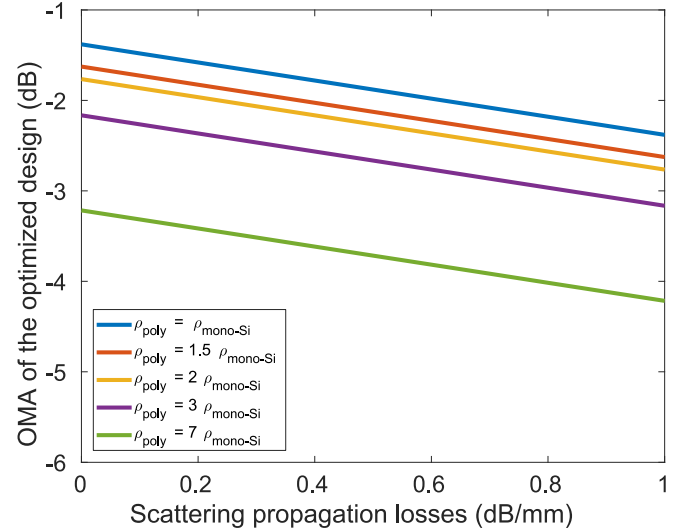


Fig. 9. Influence of the polySi resistivity on the optimal OMA. polySi resistivity is assumed to be proportional to the SOI resistivity.

C. Model limitation

The previous results must be interpreted with caution since several assumptions are made in the model. Here we would like to give an insight on assumptions/approximations made in our model, in order to interpret properly the results and give realistic limits for their validity.

A first limitation concerns the strained-SiGe layer properties. Electro-refractive coefficients and intrinsic optical losses have been estimated theoretically. Experimental data may give different results, depending on epitaxial recipes for instance.

Besides, no relaxation is considered in the SiGe model. If relaxation occurs during the process, electronic and optical properties of SiGe change and affect the overall result. In particular, it has been shown that strained-SiGe relaxes for high thermal budget [34].

In the model we assume the same resistivity for polySi and monocrystalline-Si. Nevertheless, it has been shown that polySi can be more resistive than monocrystalline-Si [35], depending on the polysilicon grain size. The cut-off frequency is affected directly. Moreover, the depletion regime should be less efficient than estimated as shown experimentally [36], decreasing the OMA as well. The polySi resistivity influence on the OMA for 25GBd OOK operation with full-Si modulators is shown on Fig. 9. Here we assume for simplicity that polySi resistivity is proportional to the monocrystalline-Si one. For each curve, optimization is performed to find the best OMA with $f_c > 20\text{GHz}$. For $\rho_{poly} = \rho_{mono-Si}$, the result is the same than Fig. 7. It is clear that resistivity affects the optimum OMA. For resistivity 7 times higher than monocrystalline-Si, OMA drops by 1.8dB compared to $\rho_{poly} = \rho_{mono-Si}$.

On the opposite side, this shows that capacitive modulators are relevant only if a good quality polySi, or monocrystalline-Si, is integrated for the upper slab. Several experimental works are on-going & encouraging using Si recrystallization process [8] or even III-V bonding [11].

From these model assumptions, the obtained results should be then seen as an upper limit and a guideline for technological developments.

CONCLUSION

In this paper, we showed an accurate simplified electro-optical model of capacitive optical modulators. Optimization of modulator parameters is performed to estimate ultimate OMA that can be expected from a modulator short enough to be driven by a single stage electrode. It is demonstrated that full-Si modulators are suitable for 25GBd OOK applications even when using waveguides with scattering losses up to 1dB/mm. Furthermore, strained-SiGe enhances the modulator performances considerably. In particular, using strained-SiGe seems mandatory to reach 53GBd PAM-4 applications with 500 μm -long modulators with an OMA close to PN-modulators one. This work shows that high quality polycrystalline silicon and strained-SiGe are necessary to do so, giving targets for technological & material developments.

REFERENCES

- [1] F. Boeuf *et al.*, "A Silicon Photonics Technology for 400 Gbit / s Applications," *2019 IEEE Int. Electron Devices Meet. (IEDM), San Fr. CA, USA, 2019*, pp. 33.1.1-33.1.4, doi 10.1109/IEDM19573.2019.8993627., pp. 7–10.
- [2] D. Patel, "Silicon Photonic Segmented Modulator-Based Electro-Optic DAC for 100 Gb/s PAM-4 Generation," *IEEE Photonics Technol. Lett.*, vol. 27, no. 23, pp. 2433–2436, Dec. 2015.
- [3] E. I. Ackerman, C. H. Cox, T. H. Ave, and A. Suite, "The Effect of a Mach-Zehnder Modulator's Traveling-Wave Electrode Loss on a Photonic Link's Noise Figur," in *International Topical Meeting on Microwave Photonics*, 2003, pp. 10–13.
- [4] E. Temporiti *et al.*, "Insights Into Silicon Photonics Transmitter Architectures," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3178–3191, Dec. 2016, 2016.
- [5] A. Liu, "A high-speed silicon optical modulator based on a metal-oxide-semiconductor capacitor," *Nature*, vol. 427, no. 6975, pp. 615–618, Feb. 2004.
- [6] M. Webster *et al.*, "An efficient MOS-capacitor based silicon modulator and CMOS drivers for optical transmitters," *IEEE Int. Conf. Gr. IV Photonics GFP*, vol. 1, no. c, pp. 1–2, 2014.
- [7] J. Byers *et al.*, "3D Fin Waveguide on 10nm Gate Oxide Bonded Double-SOI for Low V π L Accumulation Modulator," pp. 13–14, 2018.
- [8] K. Debnath, A. Z. Khokhar, G. T. Reed, and S. Saito, "Fabrication of Arbitrarily Narrow Vertical Dielectric Slots in Silicon Waveguides," vol. 29, no. 15, pp. 1269–1272, 2017.
- [9] M. Douix *et al.*, "Low loss poly-silicon for high performance capacitive silicon modulators," *Opt. Express*, vol. 26, no. 5, p. 5983, 2018.
- [10] S. Zhu, G. Q. Lo, J. D. Ye, and D. L. Kwong, "Influence of RTA and LTA on the Optical Propagation Loss in Polycrystalline Silicon Wire Waveguides," vol. 22, no. 7, pp. 480–482, 2010.
- [11] M. Takenaka *et al.*, "High-efficiency , Low-loss Optical Phase Modulator based on III-V / Si Hybrid MOS Capacitor," pp. 3–5, 2018.
- [12] T. Manku, J. M. McGregor, A. Nathan, D. J. Roulston, J.-P. Noel, and D. C. Houghton, "Drift hole mobility in strained and unstrained doped Si(1-x)Gex alloys," *IEEE Trans. Electron Devices*, vol. 40, no. 11, pp. 1990–1996, Aug. 1993.
- [13] J. Fujikata *et al.*, "High-performance Si optical modulator with strained p-SiGe layer and its application to 25 Gbps optical transceiver," *14th Int. Conf. Gr. IV Photonics, GFP 2017*, pp. 25–26, 2017.
- [14] F. Boeuf, J. H. Han, S. Takagi, and M. Takenaka, "Benchmarking Si, SiGe, and III-V/Si Hybrid SIS Optical Modulators for Datacenter Applications," *J. Light. Technol.*, vol. 35, no. 18, pp. 4047–4055, 2017.
- [15] M. Douix, "Design of integrated capacitive modulators for 56Gbps operation," in *2016 IEEE 13th International Conference on Group IV Photonics (GFP), Shanghai, 2016*, pp. 5–7.
- [16] D. M. Dourado, M. L. Rocha, J. P. P. Carmo, G. B. Farias, and J. E. Ribeiro, "Modeling and trade-off analysis of a capacitive silicon Mach-Zehnder modulator for telecom applications," *2018 Sbfot. Int. Opt. Photonics Conf. Sbfot. IOPC 2018*, 2019.
- [17] S. Monfray *et al.*, "Optimization of deep rib high speed phase modulators on 300mm industrial Si-photonics platform," vol. Proc. SPIE, no. Integrated Photonics Platforms: Fundamental Research, Manufacturing and Applications, 1136403, p. 2, 2020.
- [18] D. Thomson *et al.*, "Roadmap on silicon photonics," *J. Opt. (United Kingdom)*, vol. 18, no. 7, pp. 1–20, 2016.
- [19] D. V. Lang, R. People, J. C. Bean, and A. M. Sergent, "Measurement of the band gap of GexSi1-x/Si strained-layer heterostructures," *Appl. Phys. Lett.*, vol. 47, no. 12, pp. 1333–1335, 1985.
- [20] S. Zollner *et al.*, "Optical constants and ellipsometric thickness determination of strained Si 1 - x Ge x : C layers on Si (100) and related heterostructures," *J. Appl. Phys.*, vol. 88, no. 7, pp. 4102–4108, 2011.
- [21] M. Douix *et al.*, "Capacitive modulator integration in a 300 mm silicon photonics platform for low power and high efficiency," vol. 30379, no. 2016, pp. 2–6, 2017.
- [22] W. H. Weber, S. L. McCarthy, and G. W. Ford, "Perturbation Theory Applied to Gain or Loss in an Optical Waveguide," *Appl. Opt.*, vol. 13, no. 4, p. 715_1, 1974.
- [23] "Lumerical Mode Solutions, <https://www.lumerical.com/tcad-products/mode/>."
- [24] "Matlab, www.mathworks.com/products/matlab/."
- [25] Shaffler, "High-mobility Si and Ge structures," *Semicond. Sci. Technol.*, vol. 12, pp. 1515–1549, 1997.
- [26] G. Masetti, M. Severi, and S. Solmi, "Modeling of Carrier Mobility Against Carrier Concentration in Arsenic-, Phosphorus-, and Boron-Doped Silicon," *IEEE Trans. Electron Devices*, vol. 30, no. 7, pp. 764–769, 1983.
- [27] M. Nedeljkovic, R. Soref, and G. Z. Mashanovich, "Free-carrier electrorefraction and electroabsorption modulation predictions for silicon over the 1-14- μm infrared wavelength range," *IEEE Photonics J.*, vol. 3, no. 6, pp. 1171–1180, 2011.
- [28] M. Takenaka and S. Takagi, "Strain Engineering of Plasma Dispersion Effect for SiGe Optical Modulators," *IEEE J. Quantum Electron.*, vol. 48, no. 1, pp. 8–16, Aug. 2012.

- [29] K. Iizuka, "Elements of Photonics, Volume II For Fiber and Integrated Optics," *Wiley-Interscience*, 2002.
- [30] J. L. Polleux and C. Rumelhard, "Optical Absorption Coefficient Determination and Physical Modelling of Strained SiGe Photodetectors.," *8th IEEE Int. Symp. High Perform. Electron Devices Microw. Optoelectron. Appl. EDMO 2000 [13-14 November, 2000, Univ. Glas.*, p. 280, 2000.
- [31] Davis, *The Practical Handbook of GENETIC ALGORITHMS: Applications*. 1991.
- [32] F. Boeuf *et al.*, "Silicon Photonics R&D and Manufacturing on 300-mm Wafer Platform," *J. Light. Technol.*, vol. 34, no. 2, pp. 286–295, 2016.
- [33] J. Van Campenhout *et al.*, "Silicon Photonics for 56G NRZ Optical Interconnects," *OFC Opt. Fiber Commun. Conf. Expo.*, no. c, pp. 1–3, 2018.
- [34] D. Misra and P. K. Swain, "Strain relaxation in SiGe due to process induced defects and their subsequent annealing behavior," vol. 38, pp. 1611–1619, 1998.
- [35] T. I. Kamins, *Polycrystalline silicon resistors for integrated circuits*, vol. 16, no. 6. 1973.
- [36] M. Douix *et al.*, "SiGe-enhanced Si capacitive modulator integration in a 300 mm silicon photonics platform for low power consumption," *Opt. Express*, vol. 27, no. 13, p. 17701, 2019.

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