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Methodology for Active Junction Profile Extraction in thin film FD-SOI Enabling performance driver identification in 500°C devices for 3D sequential integration

T. Mota Frutuoso, X. Garros, P. Batude, L. Brunet, J. Lacord, B. Sklenard, V. Lapras, C. Fenouillet-Béranger, M. Ribotta, A. Magalhaes-Lucas, J. Kanyandekwe, R. Kies, G. Romano, E. Catapano, M. Casse, J. Lugo-Alvarez, P. Ferrari*, F. Gaillard
CEA, Leti, Minatec Campus, and University Grenoble Alpes, 17 rue des Martyrs, 38054 Grenoble, France

*Univ. Grenoble Alpes, Grenoble INP, RFIC-Lab, 38000 Grenoble, France

tadeu.motafrutuoso@cea.fr

Abstract - We present, for the first time, a new CV based technique to extract the Active Dopant Profile under the spacer in thin film FDSOI devices (CV-AJP). The methodology is successfully applied to FDSOI devices fabricated at 500°C for 3D sequential integration. It shows that the I_{ON}/I_{OFF} trade-off relies mainly on the chemical dopant introduction below the offset spacer, as the activation level obtained with thermal activation is found to be high enough. The LT device demonstrated in this work, already outperforms the literature. The active profile extraction also allows to draw guidelines for further device performance improvement: using a scaled SiCO spacer (5,5nm) allows to circumvent the negligible dopant diffusion at 500°C without dynamic performance penalty due to its low-k dielectric value.

Introduction - 3D sequential integration requires that the top device is processed at Low Temperature (LT) ($\leq 500^\circ\text{C}$) [1]. At this temperature, a key challenge is the activation of Raised S&D (RSD) dopants done by Solid Phase Epitaxy Regrowth (SPER). However, dopants located beneath the offset spacers are thermally activated. Literature on the activation level at 500°C is very poor and extrapolations of activated levels at 500°C lead to widely scattered values [2]. In addition, the activation level is highly dependent on the Si interstitial concentration present in the region. Due to the specific proximity of the interstitial sinks in thin FDSOI accesses [3,4], the activation level can vary significantly. To evaluate the efficiency of LT activation under the spacers, we developed a novel technique called CV-AJP to extract the junction active profile in FDSOI devices using Capacitance Measurements combined with pure electrical TCAD simulations.

Extraction of junction active profile - The measure of (C_{OV}), i.e. the Gate to Channel capacitance (C_{G-CH}) in the depletion regime, is frequently used to compare the position of the junction between devices with equivalent geometries. This is generally done by extracting a single C_{OV} value at $V_G=0V$ (Fig. 1). However this method can be misleading as C_{OV} is not constant over V_G . It strongly depends on the dopant concentration profile as explained in Fig.2. Basically when V_G is reduced, a depleted region is formed beneath the spacers shifting the conductive region in the direction of the S/D. This phenomenon results in a reduction of the inner and outer field capacitance, all the more important as the doping is low (Fig. 1 (right)). Interestingly, this effect can be used to extract the true junction profile on FD-SOI devices, as illustrated in Fig. 3 & 4. To do that, we first compute, the variation of C_{OV} as the function of the Overlap position (Ov), by means of 2D electrostatic simulations using the same values of EOT, T_{Si} , L_G and spacer permittivity as the device. The S/D junction is here considered as abrupt and metallic, leading to a single value of C_{OV} , independent of V_G , at each given Ov (Fig. 3). Then, this unique relation C_{OV} vs Ov is combined to measured values of C_{G-CH} , subtracted from the parasitic capacitance (C_{PAR}), to deduce $Ov(V_G)$ (Fig. 4). C_{PAR} denotes mainly the V_G -independent 3D Gate-to Contact parasitic capacitance, and is directly deduced from the difference between measured & simulated CV in the inversion regime. Finally, we derive the dopant concentration as the function of the overlap, from the derivative of $Ov(V_G)$ in the depletion regime ($V_G < V_T$) using Eq. (I). Fig 5 highlights the suitability of the technique to extract the dopant profile (N_D) in FD-SOI devices: the simplified expression (I) perfectly reproduces the Gaussian profiles entered as inputs in TCAD simulations. Moreover, Fig. 6 reports the sensitivity of the technique to the C_{PAR} evaluation, the only parameter of the method. A 10% error in C_{PAR} leads to a 0.75nm variation in the overlap position, but hardly affects the density of N_D dopants. This demonstrates the robustness of the CV- AJP method for the quantitative

assessment of the true concentration of electrical active dopants. The potential of the method is further highlighted in Fig. 8. The profile of active dopants extracted with the CV- AJP technique well agree with the as-implanted chemical profiles (Fig.7) given by KMC simulation.

LT Device fabrication – Fig. 9 shows the LT ($\leq 500^\circ\text{C}$) N-FDSOI device process flow fabricated with $\langle 100 \rangle$ oriented channel ($T_{Si}=6,5\text{nm}$). The gate stack consists of a HFO₂/TiN (EOT=0.91nm) with UV nanoseconds laser anneal (UV-NLA) for poly-Si activation. Low-k SiCO spacers ($\epsilon_r=4.5$), Si Raised Source Drain (RSD) epitaxy followed by SPER activation @ 500°C are carried out. Various implantations conditions (energy and dose) using phosphorous (S1-S5) have been studied (Fig.10). High Pressure Deuterium (HPD₂) and a tensile CESL are also included. Final device ($L_G=27\text{nm}$) cross-section HRTEM is displayed in Fig.10.

Optimization of LT junction profile – Fig. 11 & 12 show the CV capacitances measured for four (S1-S4) variants and the corresponding active donor profiles extracted with our CV-AJP technique. The key features are that (1) increasing the energy or the dose allow the dopants to extend closer to the gate while reducing the abruptness of the junction (2) the majority of dopants implanted on the crystalline region are thermally activated ($N_D > 2.10^{19} \text{ cm}^{-3}$) by the 500°C anneal (Fig. 13). The technique is then used to analyze the device performance and to draw guidelines to improve it. Fig. 14 & 15 first shows that extending the junction over the spacer (reduced underlap region) also increases DIBL and $V_T(L)$ magnitude because of the increase of SCE. For S1, an abnormal behavior is yet observed, and due to the fact that this device with the lowest N_D density becomes highly sensitive to the repealing effect produced by a small amount negative charges in the spacer [5]. Then, access resistance R_{acc} is extracted using the modified Y2 method [6] and plotted as the function of the junction position for the 4 splits (Fig 16 & 17). The benefit to reduce the device underlapping by optimizing the P implant is twofold on R_{acc} . It allows to (1) strongly decrease the R_0 component independently of V_G & (2) also to reduce the sensitivity of this resistance to gate bias, resulting from a reduced control of the gate potential over the spacer region (Fig. 18). Finally, Fig. 19 & 20 show new FOMs of I_{OFF} and I_{ON} , plotted as the function of overlap position. The key feature is that both follows a single trend with Ov . I_{OFF} exponentially increases as SCE becomes important, while I_{ON} rises almost linearly mainly due to the combined effect of R_{ACC} & V_T reduction. From this picture, we could predict that reducing the underlap of 1.5nm could lead to $I_{OFF}=10^{-8} \text{ A}/\mu\text{m}$ & $I_{ON}=900\mu\text{A}/\mu\text{m}$ for this LT technology. This can be achieved either by increasing energy/dose of P implant or by reducing the thickness of the spacer of 1.5nm. However, the first solution attempted here (S5) has not been successful leading to partially recrystallized access. Indeed an almost vertical amorphous/crystalline interface below the spacer cannot properly acts as a seed for the SPER at 500°C [7]. Nevertheless, the optimization made here with the S4 variant leads $I_{ON}=940\mu\text{A}/\mu\text{m}$ @ $I_{OFF}=100\text{nA}/\mu\text{m}$ that already outperforms our former and literature results for LT technology [8] (Fig. 20).

Conclusions - The CV- AJP method proposed in this paper offers the unique opportunity to quantify directly the density of electrically active dopants in thin film FDSOI device junctions with nanometer resolution, which is not possible so far even with complex and costly physico-chemical characterizations like SSRM. Thanks to the technique, it is shown that a high activation level can be achieved without pre-amorphization of the thin critical region in LT devices, and that junction can be finely optimize to achieve record I_{ON}/I_{OFF} performance compared to the state of the art for Low Temperature technologies [8,9] ($< 500^\circ\text{C}$).

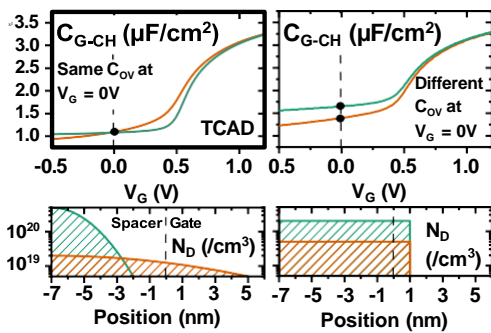


Fig. 1: Simulation of the FDSOI C_{G-CH} for different S/D N_D profiles. C_{ov} at $V_G=0$ can be misleading to represent the S/D overlap position, as it is highly dependent on the dopant density in the junction.

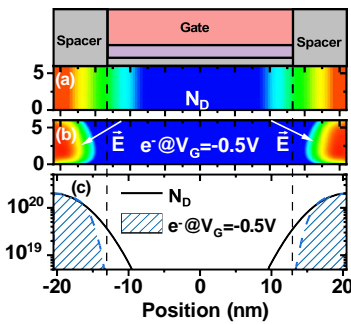


Fig. 2: 2D TCAD simulation of the N-FDSOI device for $V_G < 0$. (a) S/D N_D profile & electron density mapping (b) e^- density vs ch. position. C_{G-CH} is reduced due to the formation of a depleted region in the S/D junction area (c) 1-D profile of (a) and (b).

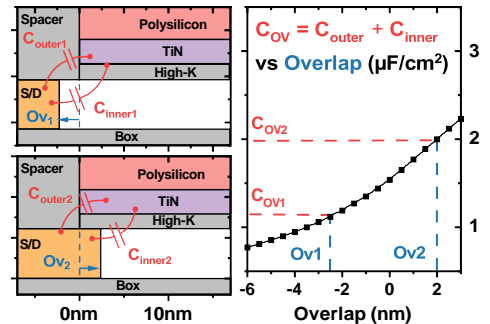


Fig. 3: (left) Fringe capacitance for two overlaps considering a metallic and abrupt junction (right) $C_{ov}(Ov)$ is computed from CV TCAD simulation with the same EOT, T_{Si} , L_G and Spacer permittivity as the device to obtain the variation of the depleted region wrt V_G .

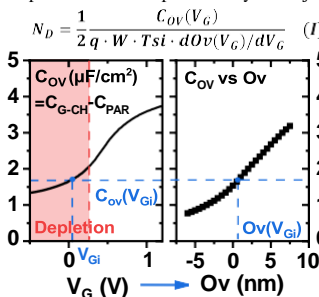


Fig. 4: Illustration of overlap as function of V_G obtained from interpolation of C_{G-CH} with $C_{ov}(Ov)$ from fig. 3. N_D is obtained from the derivative of $Ov(V_G)$.

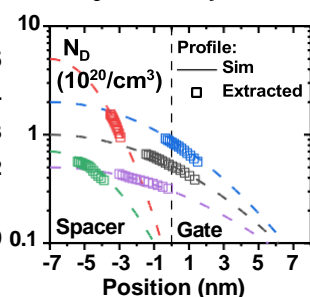


Fig. 5: Extraction of N_D profile from simulated C_{G-CH} for different S/D profiles. Simulated and extracted results are in good agreement.

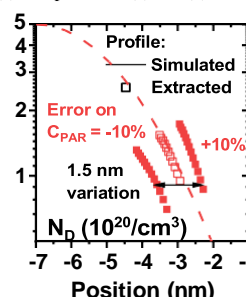


Fig. 6: Robustness evaluation of profile extraction. A 10% error in C_{PAR} leads to a 0.75nm variation in the overlap position, but hardly affects the density of N_D dopants.

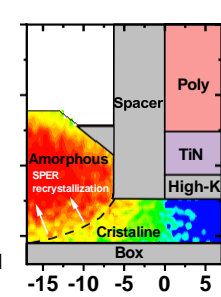


Fig. 7: KMC simulation of an S/D as implanted profile.

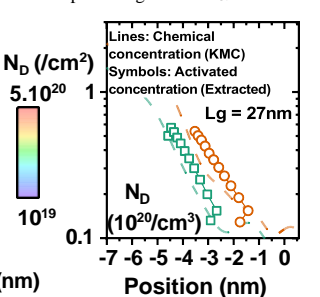


Fig. 8: 1D N_D predicted by LKMC simulation vs electrically active doping concentration obtained from capacitance measurements.

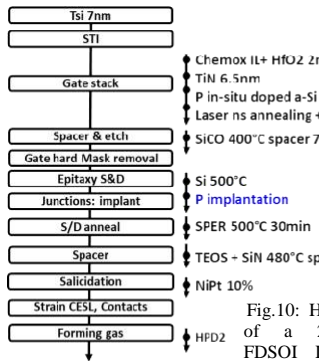


Fig. 9: Key steps involved on the LTB process flow.

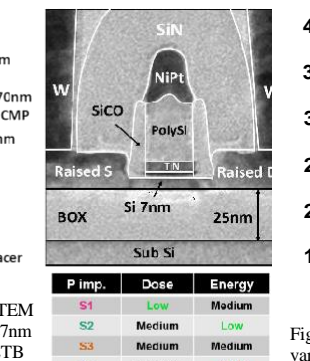


Fig. 10: HTEM of a 27nm FDSOI LTB MOSFET.

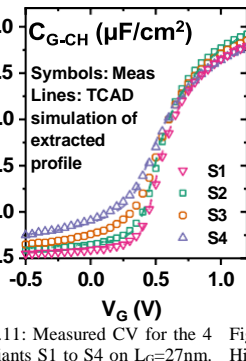


Fig. 11: Measured CV for the 4 variants S1 to S4 on $L_g=27$ nm. The depletion domain is used to extract N_D profiles.

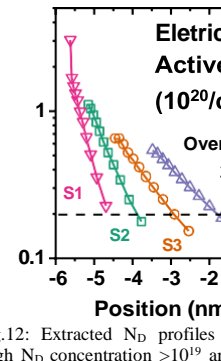


Fig. 12: Extracted N_D profiles for S1-S4. High N_D concentration $> 10^{19}$ are achieved, proving that dopants under the spacers can be electrically activated within a 500°C process.

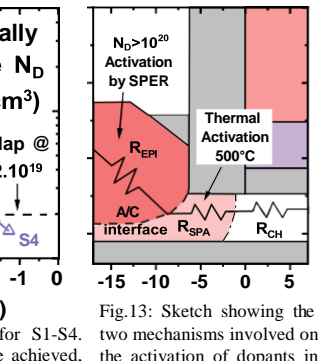


Fig. 13: Sketch showing the two mechanisms involved on the activation of dopants in the amorphized and crystalline regions of S&D.

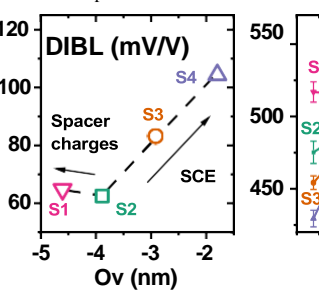


Fig. 14: DIBL vs Overlap. SCE increases with overlap. Unusual variation of S1 can be explained by the presence of charge under the spacers [5].

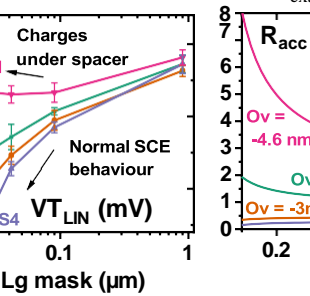


Fig. 15: V_T vs L_g . Abnormal variation due to spacer charges vanishes when underlap is reduced.

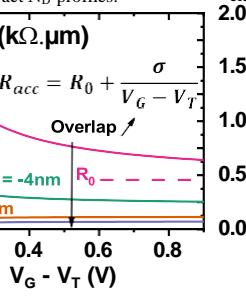


Fig. 16: Access resistance from Y2 method [6] vs $V_G - V_T$. Underlapped devices exhibit the highest variation of access resistance with V_G .

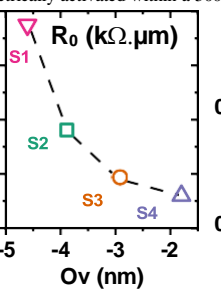


Fig. 17: R_0 component ind. of V_g vs overlap R_0 strongly reduces when underlap is reduced.

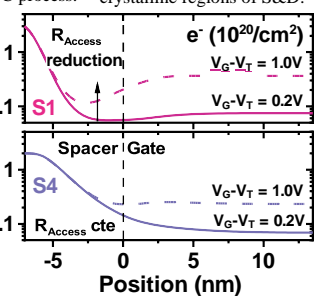


Fig. 18: Electron density from TCAD for S1 & S4. The higher variation of access resistance on S1 is explained by a higher control of the region under the spacers by the gate voltage.

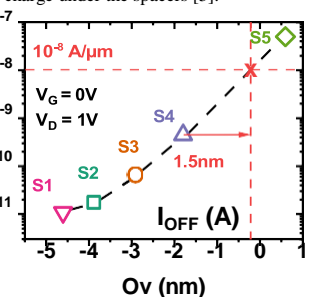


Fig. 19: Off state current vs Overlap. A shift of the overlap of 1.5 nm from S4 is estimated to obtain I_{OFF} equals to 10^{-8} A/μm.

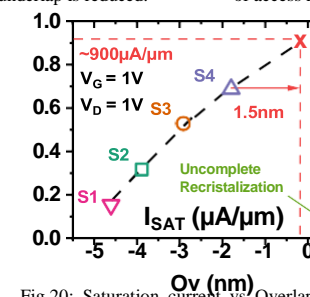


Fig. 20: Saturation current vs Overlap. I_{SAT} increases with overlap until in S5 where implant condition is too strong for complete recrystallization [7].

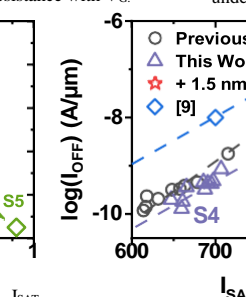


Fig. 21: Summary of the state-of-the-art I_{SAT}/I_{OFF} for LTB MOS technologies. Thanks to Ov optimization (S4), record I_{ON} @ $I_{OFF}=100$ nA/μm is achieved.

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