Surge Current Interruption Capability of Discrete IGBT Devices in DC Hybrid Circuit Breakers

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***Abstract*— The power electronic interrupter (PEI) determines the current interruption rating of the dc hybrid circuit breaker (HCB). This paper deals with discrete insulated gate bipolar transistor (IGBT) based PEI modules. The influence of the voltage clamping circuit (VCC) on the surge current interruption capability (SCC) of the discrete IGBT is unveiled for the first time. Two commonly used VCC configurations are considered: a purely MOV based voltage clamp and an MOV-RC combination clamp designated as type I and type II PEI modules respectively. Comprehensive measurements are used to analyze the device turn-off behavior under each PEI module type to determine their limitations as well as their failure modes. The type I PEI is limited by the turn-off thermal stresses arising from the hard switching dynamics. The type II PEI, on the contrary, has the potential to achieve lower turn-off energy among other benefits but exhibits a unique failure mode during the tail current stage. Therefore, static and mixed-mode Technology Computer-Aided Design (TCAD) device simulations are introduced to provide further insights into the internal processes that alter the type II turn-off and in turn explain the failure mechanism. Finally, the influence of the various circuit parameters on the turn-off process are evaluated and methods to enhance the SCC of the IGBT based PEI are presented.**

***Index Terms*—Discrete IGBT, failure modes, power electronic interrupter, surge current interruption capability, tail current, voltage clamping circuit.**

I. Introduction

FAST acting, high performance fault protection and its management are paramount to the widespread adoption of dc distribution systems. Several dc circuit breakers (DCCBs) have been proposed to detect and isolate short-circuit faults [1]-[7]. Among these, the hybrid circuit breaker (HCB) is an attractive solution for medium-voltage dc (MVDC) distribution systems offering high efficiency along with reasonable response times (~ 500 µs) to limit the peak current [8]-[11]. The typical structure of an HCB system is shown in Fig. 1(a) [11]. The power electronic interrupter (PEI) forms a critical part of the HCB consisting of the power semiconductor branch and the voltage clamping circuit (VCC) for fault current interruption and extinction respectively. The semiconductor devices used in the PEI are subject to non-repetitive surge currents during the operation of the HCB (durations of up to 1 ms required for mechanical contact separation) as shown in Fig. 1(b). It is desirable to achieve maximum utilization (i.e., peak interruption current/voltage versus rating) of the semiconductor device(s) to enable low-cost and compact PEI designs.

Insulated Gate Bipolar Transistors (IGBTs) are widely used

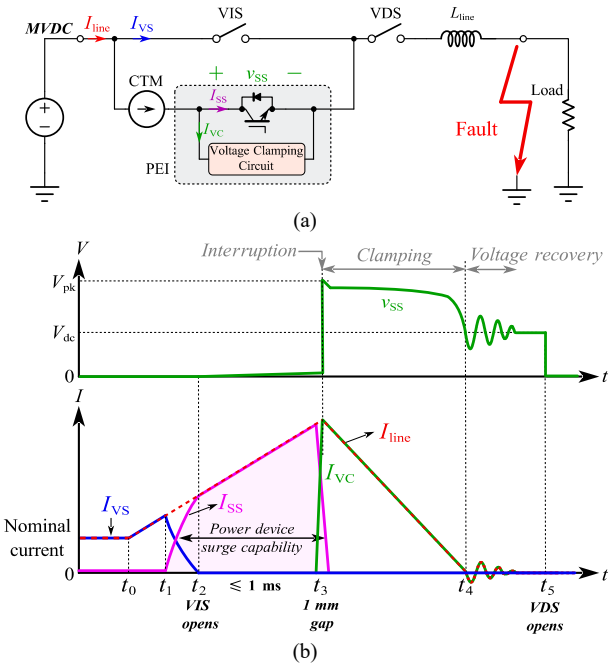

Fig. 1. (a) HCB unit with an IGBT based PEI using a current transfer module (CTM) to enable current commutation from the vacuum interrupt switch (VIS) to the PEI branch; (b) Typical fault interruption waveforms of the HCB.

in PEIs due to their high pulse current (I_{CM}) ratings [12]-[14]. Several commercial off-the-shelf (COTS) discrete IGBTs possess high pulse current densities (PCD), defined as I_{CM} over device volume (v_{dev}), making them good candidates for high power density, modular PEIs [15]-[16] applied to low- and medium-voltage dc systems (see Fig. 2). Successful operation of the PEI translates into two major requirements for the IGBT which together constitute its surge ruggedness: (i) conduction of fault current without desaturation and (ii) interruption of fault currents exceeding the reverse-bias safe operating area (RBSOA) without device failure. In contrast to a short-circuit event, the surge current turn-off process takes place while the device contains stored (free) charges. Historically, IGBT manufacturers have restricted the surge current turn-off capability to about twice the rated current at voltages below its rating (RBSOA limit), whereas, in the short-circuit mode (desaturation) the device can safely turn off 5–7 times the rated current [17]. The short-circuit capability of IGBTs has been studied extensively [18]-[20], but its surge ruggedness relevant to the PEI application is yet to be fully explored. The first requirement could potentially be addressed by increasing the gate voltage to

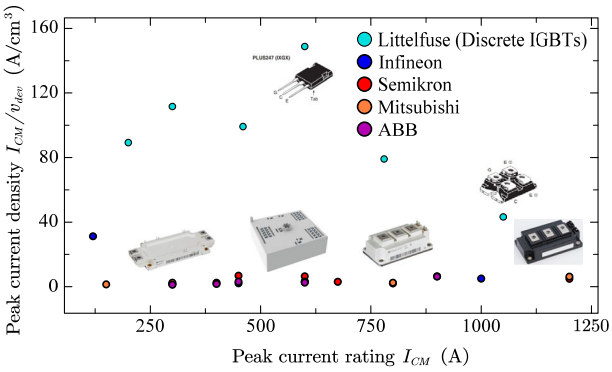

Fig. 2. Pulse current densities of commercially available IGBTs showing discrete IGBTs offer high surge current ratings in compact packages.

thereby increase the saturation current level [14], [21]-[22]. The second requirement, however, depends on the turn-off stresses which are influenced by device-circuit interactions. Specifically, the current interruption process involves both the IGBT and the parallel VCC which sets the turn-off voltage and *dv/dt* of the PEI. Therefore, to understand the surge current interruption capability or SCC (i.e., the peak turn-off current that can be safely interrupted) of the IGBT, the following questions require further investigation:

1) How does the VCC affect the turn-off process?
2) What are the internal dynamics of the IGBT during surge current interruption and the corresponding failure mechanisms?
3) What are the main design variables (i.e., VCC parameters), if any, that can enhance the SCC of a given IGBT?

Literature can be found on the design and optimization of VCCs for circuit breaker overvoltage suppression [23] - [25] but they do not cover the issue of the SCC. Therefore, this paper aims to address the above topics for the first time through comprehensive circuit analysis and evaluation of the device turn-off process. A 3 kV rated very-high-voltage series discrete IGBT from Littelfuse [26] was evaluated in this work for its high PCD featuring an I_{CM} rating of 7× its continuous current rating in a compact package that has been found to adiabatically conduct these pulse currents for durations ≤ 1 ms [28]-[31]. It is worth noting that the I_{CM} specification only provides a reference for the surge current conduction capability based on the device junction temperature limit, which, while essential to this application, is not an indication of the SCC.

PEI modules with two commonly used VCC configurations were considered in the study as shown in Fig. 3; the type I module – with a purely metal-oxide varistor (MOV) based clamp and the type II module – with an MOV-Resistor-Capacitor (RC) combination snubber. First, the turn-off process under both VCC configurations were analyzed. Next, a surge current experimental circuit was built to mimic the PEI operation. Extensive experimental results (including destructive test cases) were obtained for both module configurations under a wide range of turn-off voltages/currents. Technology Computer-Aided Design (TCAD) mixed-mode simulations were performed to further analyze the turn-off behavior of the device and corresponding failure mechanism relevant to the topic under consideration.

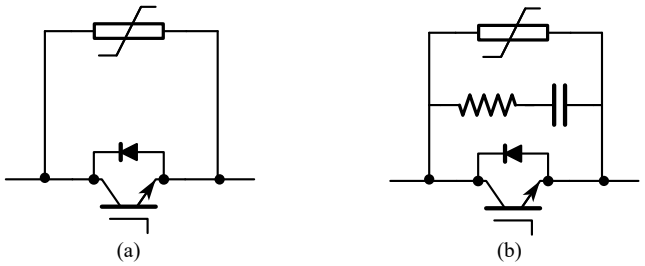

Fig. 3. PEI configurations: (a) MOV based VCC; (b) MOV-RC combination snubber.

The outline of this paper is as follows: in Section II, the working principle and governing equations of the two PEI module types under consideration are presented to describe the turn-off process. The surge current experimental platform is introduced, and the test results of the two PEI module types are presented in Section III. Section IV presents device TCAD simulations to further analyze the observations. The main VCC parameters affecting the interruption performance are explored in Section V and methods to enhance the SCC of the device are presented. Finally, Section VI concludes this article with a summary of the work.

II. PEI Module Types and Operating Principles

The operating stages showing the current commutation paths of the two module types during fault interruption are provided in Fig. 4 (type I) and Fig. 5 (type II). The circuit is a simplified DC transmission line with a power source V_{dc} and a load. The total system inductance (including DC cable inductance) is modelled as L_{line}. It is assumed that the ohmic resistance of the line is negligible. Unavoidable stray inductances in the snubber and MOV paths are included. For both module types, Stage I ($0 \le t < t_1$) depicts the start of the fault where the system current is conducted by the VIS. Once the fault is detected, in Stage II ($t_1 \le t < t_2$), the fault current is diverted to the IGBT(s) in the PEI branch to start the interruption process.

$$i_{ss}(t_2) = I_{pk} \tag{1}$$

The system fault current at the end of Stage II is given by (1), where I_{pk} is the peak fault current in the system and can be assumed to be a constant value until the PEI voltage v_{SS} increases to V_{dc}. The currents can be linearized during the different stages of the analysis due to the short duration of the turn-off transient (on the order of a few hundred nanoseconds). The different VCCs result in distinct interruption dynamics which will be described below.

A. Type I PEI Module: Purely MOV Based VCC

The type I module uses a simple VCC based on the nonlinear MOV. The MOV selection is such that its rated dc voltage should be ≥ V_{dc} to satisfy the steady-state thermal limit of the part [32]. The turn-off transient waveforms are shown in Fig. 6.

- Stage III ($t_2 \le t < t_3$): Once the IGBT is turned off, in Stage III, the current exits the channel, and the PEI voltage v_{SS} begins to increase as the output capacitance is charged.
- Stage IV ($t_3 \le t < t_4$): As the v_{SS} reaches the MOV reference voltage V_{ref} (typically 1.1× to 1.3× V_{dc}), the MOV enters the low impedance region and the current transfers from the

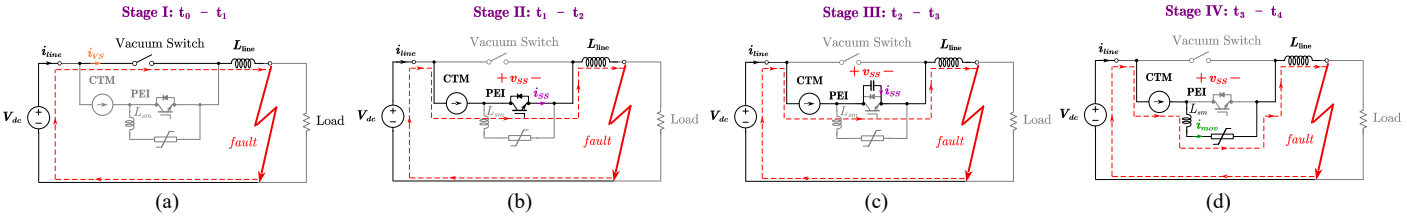

Fig. 4. Type I module turn-off sequence showing the current commutation stages.

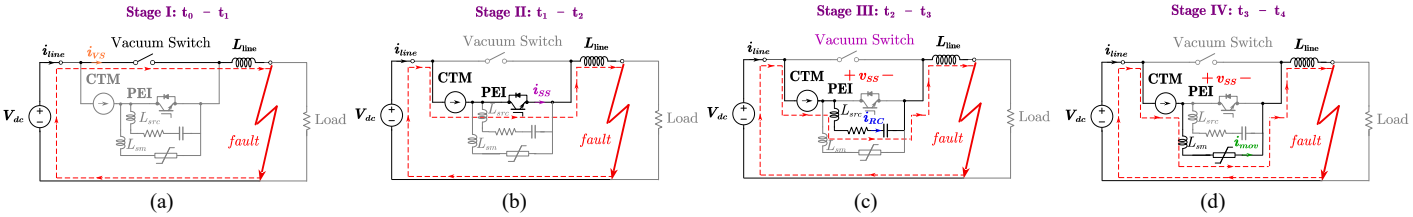

Fig. 5. Type II module turn-off sequence showing the current commutation stages.

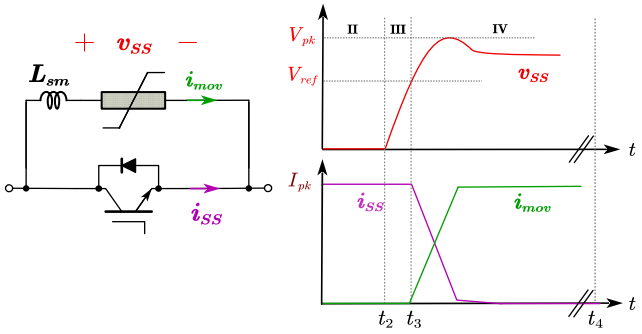

Fig. 6. Type I module turn-off transient waveforms.

$$\begin{cases} v_{ss}(t) = L_{sm}\dfrac{di_{mov}(t)}{dt} + v_{mov}(t) \\ v_{mov(t)} = ki_{mov}^{(t)\frac{1}{\alpha}} + f\left(\dfrac{di_{mov}(t)}{dt}\right) \end{cases} \quad (2)$$

$$\max(v_{ss}) = V_{pk};\ \{V_{pk}|[2\times V_{dc}, 3\times V_{dc}]\} \quad (3)$$

IGBT to the MOV branch driving the voltage to the MOV clamping value (with a peak value of V_{pk}). The IGBT then exhibits a typical tail current due to its bipolar nature [33]. The MOV remains in the clamping region until the fault is cleared. The device turn-off trajectory is typical of a hard turn-off event where the IGBT current remains at the peak value until V_{ref} is reached as shown in Fig. 7.

The v_{SS}, is also affected by the MOV path stray inductance L_{sm} as given by (2). The MOV voltage itself depends on the specific part's static nonlinearity coefficient α, the ohmic resistance constant k when MOV current density is 1 mA/cm^2, and the MOV current (i_{mov}) rate of rise (determined by the turn-off di/dt of the IGBT) [32], [34]. The peak MOV voltage, V_{pk}, can be greater than 2× V_{dc} [35] in this configuration as given in (3). Accordingly, the device voltage rating $V_{CE,rated}$ is selected with some safety margin (~5% – 10%). It is possible to slow down the IGBT turn-off current slew rate to an extent to suppress the overvoltage albeit at the expense of increased energy dissipation in the device. It should also be noted that a higher system fault current, not only results in higher voltage overshoot but also higher turn-off energy and therefore a higher

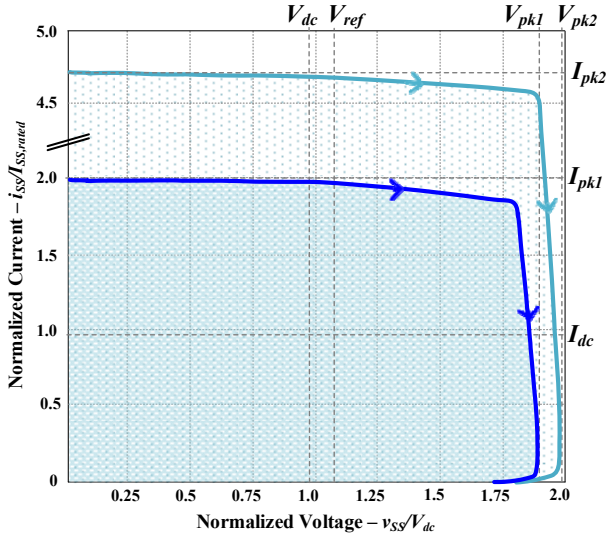

Fig. 7. Type I module expected IGBT turn-off trajectory.

thermal stress on the device. It is possible to estimate the junction temperature rise of the IGBT during the surge event as the convolution integral of its transient thermal impedance (z_{th}) and the power dissipation (p) as shown in (4). The z_{th} can be calculated from the n^{th} order foster network (R and τ) for a given power device.

$$\begin{cases} z_{th}(t) = \sum_{i=1}^{n} R_i\left\{1 - e^{\frac{-t}{\tau_i}}\right\} \\ \Delta T_j(\tau) = \int_0^{\tau} p(t).\dfrac{d}{dt} z_{th}(\tau - t)dt \end{cases} \quad (4)$$

However, the chip's critical temperature (i.e., the temperature boundary exceeding which can lead to device failure) value, which can be significantly higher than the rated junction temperature, is not readily known. Therefore, the device SCC is best determined through experiments as will be shown in Section III.

B. Type II PEI Module: MOV-RC Combination Snubber

It is widely acknowledged in the literature that RC snubbers are used in PEIs in addition to the MOV for the following reasons: 1) reduction of IGBT turn-off power/energy and 2)

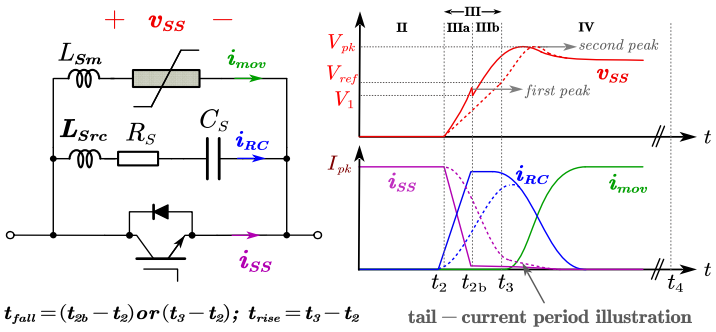

Fig. 8. Type II module turn-off transient waveforms. Dashed line depicts a case with a slower IGBT turn-off *di/dt*.

mitigation of MOV voltage overshoot by lowering the MOV current rate of rise [15], [36]. Accordingly, RC snubber design for PEIs have considered voltage suppression and *dv/dt* control to protect the device from overvoltage failure and to help meet the *dv/dt* limit (dv/dt_{lim}), if any, for the vacuum interrupter (VIS) in HCBs. For the snubber capacitor C_s, the standard practice is as shown in (5), ignoring the stray inductance L_{src}, while for the snubber resistor R_s, (6) is recommended to suppress the overcurrent spike at turn on, if required, and to dampen the resonance during the voltage recovery stage after the fault current is extinguished (although the system can be stable with an underdamped design and critical damping/overdamping are not necessary) [23], [37].

$$C_s \geq max\left(\frac{t_{rise} I_{pk}}{2(V_{pk}-V_{ref})}, \frac{I_{pk}}{dv/dt_{lim}}\right) \quad (5)$$

$$R_s \geq max\left(\frac{V_{dc}}{I_{CM}}, 2\sqrt{\frac{L_{line}}{C_s}}\right) \quad (6)$$

where t_{rise} is the desired rise time for MOV current to sufficiently suppress V_{pk}, I_{CM} is the maximum surge current rating for the IGBT. The traditional design procedure for the RC snubber in (5) and (6) do not consider, however, the SCC and the device internal dynamics during the interruption event. The turn-off process of the type II module with the MOV-RC combination snubber is described below. The turn-off transient waveforms are depicted in Fig. 8.

- Stage III ($t_2 \leq t < t_3$): When the IGBT gate voltage is removed, at the end of Stage II ($t_1 \leq t < t_2$), the device enters Stage III where its channel turns off and the fault current is transferred to the RC branch. The v_{SS} during Stage III, rises as the snubber capacitor is charged, its *dv/dt* dependent on the IGBT turn-off current slew rate (and therefore the rate of rise of RC branch current i_{RC}) as shown in (7) where L_{src} is the stray inductance in the RC branch.

$$\frac{dv_{SS}(t)}{dt} = L_{src}\frac{d^2 i_{RC}(t)}{dt} + R_s\frac{di_{RC}(t)}{dt} + \frac{i_{RC}(t)}{C_S} \quad (7)$$

Based on this slew rate, the i_{RC} and i_{SS} can either follow the solid line (fast turn-off) or the dashed line (slow turn-off) as seen in Fig. 8. For the fast turn-off case, Stage III can be split into two sub-stages, IIIa and IIIb, with different *dv/dt* rates based on the di_{RC}/dt. As can be seen from (7), the snubber resistor R_s can significantly affect the voltage rate of rise during IIIa whereas the snubber capacitor C_s dominates during IIIb (when di_{RC}/dt is zero). The voltage at the end of IIIa, V_1, is approximated in (8), and that at the end of IIIb is the MOV reference voltage V_{ref}.

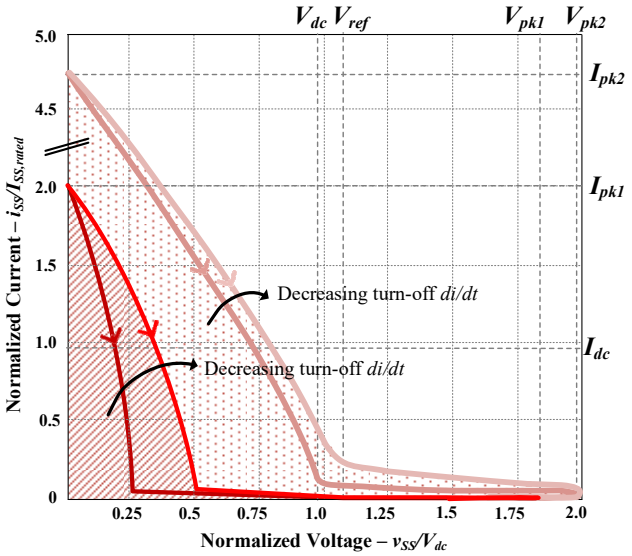

Fig. 9. Type II module expected IGBT turn-off trajectory.

$$V_1 \approx \frac{I_{pk}}{2C_s}.(t_{2b} - t_2) + I_{pk}.R_s \quad (8)$$

After the current in the channel is extinguished, the stored charges in the IGBT are removed as hole current (internal recombination) in what is called the "tail-current" period. The stray inductance L_{src} along with the i_{RC} slew rate causes a voltage overshoot at the end of the di_{RC}/dt transient labeled in Fig. 8 as "first peak". Practical values of L_{src} do not significantly affect the final peak PEI voltage V_{pk}.

- Stage IV ($t_3 \leq t < t_4$): Once the v_{SS} voltage reaches V_{ref}, the fault current transfers from the RC to the MOV branch, where the MOV current rise time depends on the RC snubber parameters. The inductive energy is dissipated, and the fault current is reduced to zero through the MOV clamping action as in the type I circuit. The v_{SS} in Stage IV follows (2) with MOV path stray inductance L_{sm} resulting in a voltage overshoot ("second peak") directly affecting the PEI peak voltage V_{pk}. The IGBT's tail current, in general, depends on the amount of stored charges and the minority carrier lifetime of the device [33], [38]. The former depends on the peak current in the channel prior to turn-off while both are affected by the chip design itself. It is known that the increase of voltage across the device (Stage IV) requires removing these injected charges. The expected turn-off trajectories of the type II PEI are provided in Fig. 9. Lower turn-off currents result in smaller tail current magnitudes due to lesser stored charges at turn-off. In summary, the addition of the snubber has the potential to reduce the total E_{off}.

However, the magnitude and duration of the tail current could significantly increase the E_{off}, therefore negating one of the main benefits of the RC snubber.

The SCC of the IGBT under the two PEI configurations analyzed herein are experimentally evaluated in the following section.

III. Surge Current Testbed and SCC Evaluation

A. Surge Current Experimental Setup

The discrete IGBT in [26] was selected as the device under test (DUT) for the PEI surge current experiments (see Table I for specifications). The device has a rated voltage $V_{CE,rated}$ of 3000 V with a 1 ms I_{CM} rating of 600 A (higher than that found in COTS counterparts). The device RBSOA curve indicates ~1.25× $I_{C,rated}$ as the peak turn-off current.

TABLE I. Specification of the Discrete IGBT under Study.

IGBT P/N [26]	Rated $V_{CE,rated}$ (V), $I_{C,rated}$ (A)	I_{CM} (A) 1 ms rating	RBSOA Peak Current (A)/ Voltage (V)
IXBF55N300	3000 V, 86 A	600 A	110 A/1500 V

An experimental platform (see Fig. 10) was constructed to conduct a surge current through the IGBT (higher than the RBSOA) and subsequently turn off the current to evaluate the SCC of the PEI modules under test. The dc bus capacitance was selected to have a near constant bus voltage for the duration of the surge. The inductance and the turn-on pulse width were varied to adjust the peak current value as desired. In each case, the DUT gate-driver was tuned to the maximum allowable gate voltage to modulate its transconductance and extend its saturation current levels. The gate resistor (R_g) value was fixed at 10 Ω for these tests to suppress turn-off ringing. The clamping voltage values were increased by varying the circuit parameters (MOV selection). Due to the limited avalanche capability of the IGBT, the MOV peak clamping voltage was kept below its rating $V_{CE,rated}$

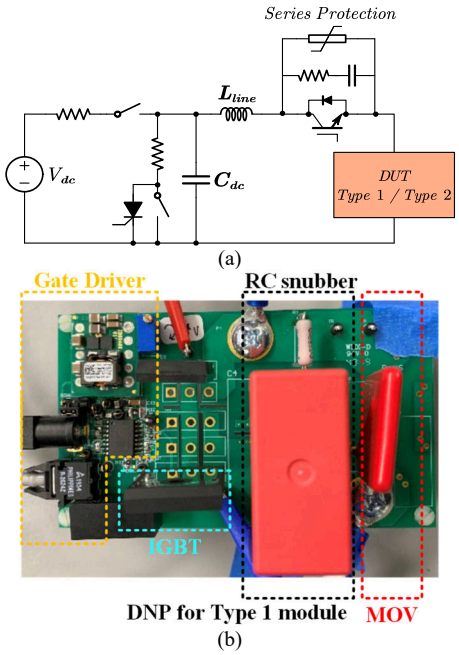

Fig. 10. (a) IGBT surge current test circuit; (b) DUT testbed PCB.

for all test cases. In addition, to improve the power density of the PEI, it was desired to have a minimum device voltage utilization factor (VUF = $V_{pk}/V_{CE,rated}$) of at least 70 %. Accordingly, the v_{SS} limits were defined as shown in (9).

$$0.7.V_{CE,rated} \leq v_{ss} \leq 0.95.V_{CE,rated} \quad (9)$$

Surge current tests were conducted on the DUT, under both configurations, wherein the peak current and the clamping voltage were increased from a value at or close to the maximum indicated in the RBSOA curve (Table I) until either the device failed or the voltage upper limit in (9) was reached. The goal was to determine the SCC of the device at the highest possible VUF for improved PEI power density, along with the possible failure modes and associated dependencies. As the discussion in this paper is specifically about the IGBT SCC, only the IGBT current and voltage waveforms are provided to illustrate the performance.

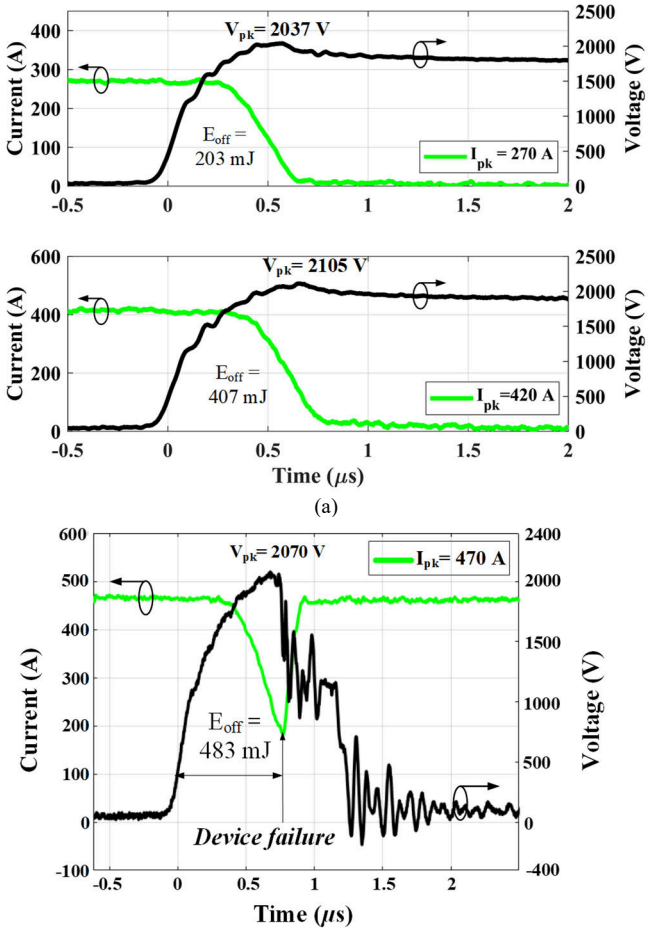

Fig. 11. (a) Device 1 performance under type I module configuration showing succesful turn-off of the device at up to 420 A and ~2100 V.; (b) Device 1 failure at 470 A, 2070 V, turn-off energy of 483 mJ.

B. PEI Performance under Type I Configuration

In this configuration, the IGBT operates in a hard switching condition where it is exposed to simultaneous high current and voltage well outside the device RBSOA, a condition that is known to cause avalanche multiplication [40]. Fig. 11 shows the

experimental results for the DUT (zoomed in on the turn-off transient). From Fig. 11(a), it can be seen that the DUT could safely turn-off (consistently) currents up to 420 A (4.8× rated I_C value) at a peak voltage of ~2108 V (0.7× $V_{CE,rated}$). The IGBT exhibits a typical tail current of magnitude < 20 A for a duration < 2 µs. Further, it was seen that the device failed during the turn-off transient when the peak turn-off current was increased to about 470 A (~ 5.4× rated I_C value). The turn-off switching energy (E_{off}) increased from ~407 mJ (at 420 A) to ~483 mJ (at 470 A), which apparently exceeded the device critical thermal limit leading to its failure. Excessive turn-off stress also impacts reliability by accelerating wear out. In general, operation outside the SOA can lead to device degradation, and, eventual— or direct— failure. The SCC performance of the device under type I is summarized in Table II.

TABLE II. TYPE I PEI SCC PERFORMANCE SUMMARY

SCC (A)		V_{pk} (V)	VUF (%)	E_{off} (mJ)
420 A (4.88 × $I_{c,rated}$)		2108 V	70.2 %	407 mJ

C. PEI Performance under Type II Configuration

In this configuration, the turn-off device stress is affected by a delay in the turn-off along with an increase in the energy dissipated due to the tail-current (Fig. 9). The RC component values are conservatively selected as given in Table III with an assumed dv/dt_{lim} of 5 kV/µs (based on industrial VIS products), t_{fall} of 0.5 µs for I_{pk} values up to 1000 A as per (5). The t_{rise} was not considered in the RC parameter selection because the resulting MOV voltage is directly monitored and limited as per (9).

TABLE III. RC PARAMETERS USED BASED ON (5), (6).

R_s (Ω)	C_s (µF)
1.2 Ω	0.44 µF

The surge current experiments of the DUT in the type II module configuration are provided in Fig. 12. It can be seen that the device could successfully interrupt 400 A (~4.6 × $I_{C,rated}$) at 2152 V (Fig. 12(a) bottom). The device current waveform reveals an atypical "bump" in the tail current which increases in magnitude with the peak turn-off current. The turn-off dynamics observed deviates from the expected trajectory presented in Fig. 9, especially during the tail current stage. The maximum turn-off energy recorded for the 400 A case was ~ 480 mJ. It should be noted that the tail current stage is the major contributor to the E_{off} lasting for > 5 µs with a peak current bump magnitude of ~100 A. Subsequently, it was found that the device failed at a peak turn-off current of 415 A (4.8 × $I_{C,rated}$) and a clamping voltage of ~ 2104 V (see Fig. 12(b)) with a calculated E_{off} of 339 mJ up to the point of failure. It was suspected that the higher "tail bump" magnitude (125 A peak), with a tail duration (up to failure) of ~ 3.5 µs, in the presence of high device voltage, may have led to the device failure. The failed device was opened for further analysis, and, the findings (see Fig. 12(c)) showed a small melted region within the active area of the chip, which evidence of localized heating. However, the internal device dynamics leading to the failure was not apparent and requires further investigation. The SCC results for the type II PEI are summarized in Table IV. It should be noted that, sacrificing the VUF can enable a higher SCC, as expected.

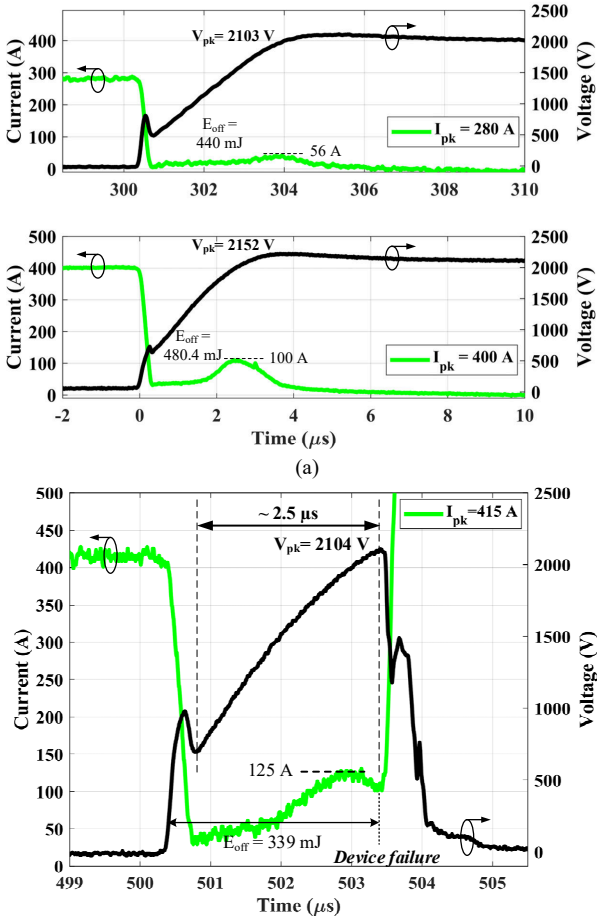

Fig. 12. (a) DUT performance under type II configuration; (b) DUT failure at 415 A/2100 V with bump magnitude of 125 A (E_{off}=339 mJ); (c) DUT after decapsulation showing local hotspot failure.

TABLE IV. TYPE II PEI SCC PERFORMANCE SUMMARY

SCC (A)	V_{pk} (V)	VUF (%)	E_{off} (mJ)
400 A (4.6 × $I_{c,rated}$)	2152 V	71.7 %	480 mJ

TABLE V. PEI MODULE TURN-OFF PROCESS SUMMARY

Parameter	Type I	Type II
Turn-off process	Hard switched	Soft-switched
E_{off} primary contributors	V_{pk} & I_{pk} values	Tail current value

Device turn-off process for the two module types are summarized in Table V. For the type I module, the SCC depends directly on the chip thermal stress (turn-off current and voltage) and the corresponding thermal capability. Further improvements are not attainable due to inherent chip limitations. For the type II PEI, however, the turn-off process is more complex as seen above and the main failure occurs during the tail current period. The internal physics behind the type II failure will be further explored in the following section through device-circuit mixed-mode simulations.

IV. TCAD PHYSICAL SIMULATION

Former test results indicate a similar critical level of E_{off} for both type I and type II PEI, yet their E_{off} originates from very different stages. While the overlap between voltage and current during the hard turn-off process contributes to most of E_{off} in type I PEI, losses from the unique tail current bump provides the majority contribution in the type II. It is expected that IGBT, as a conventional bipolar device, suffers from high (hard) turn-off loss, whereas the current bump behavior is not easily understood. This section deals with the internal physical dynamics and failure mechanism of the IGBT current bump during a soft turn-off process. Physics-based, device-circuit mixed-mode, electrothermal TCAD simulations were performed in Silvaco Atlas.

TABLE VI. IGBT MODEL PARAMETERS

Parameter	Value	Unit
Cell pitch	17.5	μm
Drift layer doping	3e13	cm^{-3}
Drift layer thickness	240	μm
Substrate doping	1e19	cm^{-3}
P-well doping	2e17	cm^{-3}
P-well thickness	1	μm
Gate oxide thickness	850	nm
Channel width	1	μm

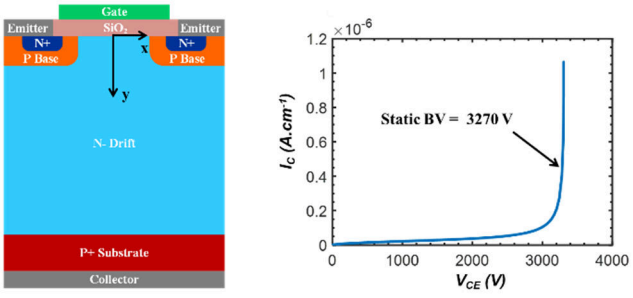

Fig. 13. (a) Schematic of a planar NPT IGBT cell structure, and (b) breakdown voltage characteristics of the IGBT simulation model.

A. Simulation Model

To probe the carrier dynamics within an IGBT, the classic non-punch through (NPT) structure was built in simulation, with a cross-sectional cell structure shown in Fig. 13(a). Key model parameters of the simulated IGBT cell are listed in Table VI. While not identical to the DUT (due to confidentiality of commercial device parameters), the model can be used to reproduce and analyze the internal dynamics of interest. Physical models were included to account for mobility, recombination, avalanche breakdown, and lattice heating [44]. Static simulation was performed, as shown in Fig. 13(b), revealing a static avalanche breakdown voltage (BV) of 3270 V.

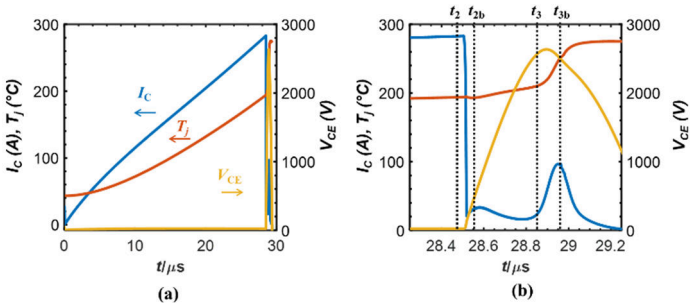

Fig. 14. (a) Simulated waveforms of an IGBT surge current interruption with an RC snubber, and (b) zoomed-in view of the soft turn-off process.

B. Dynamic Physical Behavior

To validate the IGBT model under switching conditions, a simulation circuit was built similar to the type II PEI, with an RC snubber (but no parallel MOV). As plotted in Fig. 14, surge current waveforms (device voltage V_{CE}, device current I_C, and device junction temperature T_j) in a soft turn-off process which results in a tail current bump could be well reproduced by TCAD simulations. Note that T_j rises dramatically with the bump current, which could lead to a thermal overstress and finally a runaway failure mode. In addition, it is seen that the current bump occurs when V_{CE} is around 2600 V, a level that is much lower than the device static BV of the IGBT cell built.

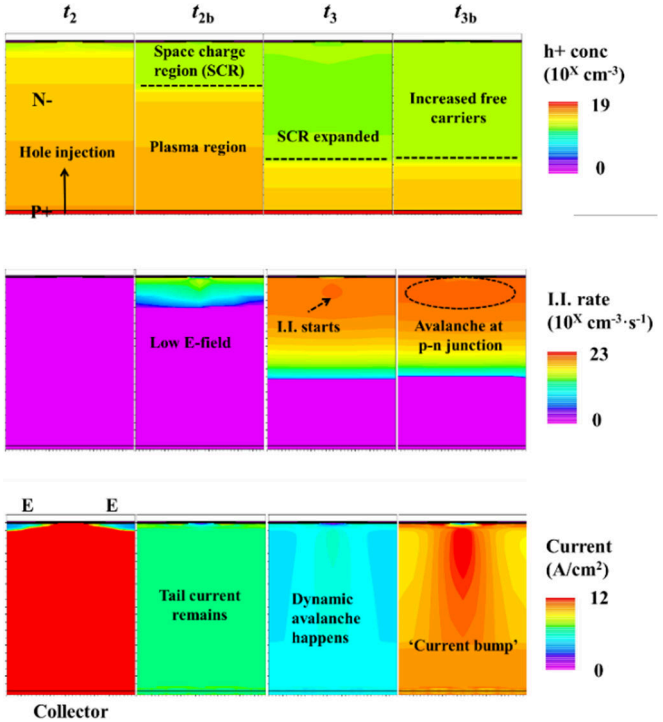

Fig. 15. Simulated contours of hole concentration, I.I. generation rate, and current density during type II surge current interruption.

To further gain a deeper insight of the internal physical process behind the current bump phenomenon, Fig. 15 shows the evolution of the simulated contours during the type II surge current interruption, including the hole concentration, impact ionization (I.I.) generation rate, and current density.

When IGBT conducts high current (t_2), a large number of holes are injected into the drift region, resulting in a strong conductance modulation. At this time, two types of free carriers, electrons and holes, exist inside the drift region. When the device is turned off, electrons in the channel disappear rapidly (t_{2b}). The carriers begin to diffuse and recombine, formulating a space charge region (SCR) that blocks the voltage. At the same time, a large number of excess carriers are still present inside the drift region in the electron-hole plasma which is close to the p-n junction near the P+ substrate. As the voltage across the device keeps rising during turn-off, SCR continues to expand downwards (t_3) and the holes in the plasma region are removed. Until this point, the process remains the same for type I and type II configurations. Due to the employment of the RC snubber in type II, the device voltage rises slowly (compared to type I turn-off) and the electric field strength in the SCR is not enough to complete the hole removal in a short time. Therefore, the hole concentration in the SCR remains high. The positively charged holes (p) add to the effective doping (N_{eff}) in SCR, and the electric field in the N- drift region (according to the Poisson's equation) is given by:

$$\frac{dE}{dx} = \frac{q}{\varepsilon} N_{eff} \tag{10}$$

$$N_{eff} = N_D + p \tag{11}$$

where q is the elementary charge, ε is the dielectric constant, and N_D is ionized donor concentration. It can be seen that the electric field in the SCR becomes steeper. At a relatively high voltage (but lower than the static BV), electric field strength in the SCR reaches its critical value, when the impact ionization begins, leading to an avalanche breakdown (t_{3b}). Current multiplications occur under avalanche conditions, presenting an abnormal tail bump current phenomenon, as it was identified earlier in test and simulation waveforms.

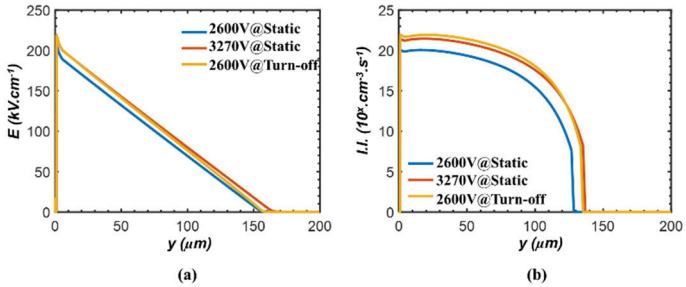

Fig. 16. Simulated (a) electric field distribution and (b) I.I rate of IGBT at different static and dynamic conditions.

As the device is at a high voltage bias, the transient loss is extremely large, and the temperature rise is obvious. The current bump phenomenon fundamentally comes from the "dynamic avalanche" mechanism [42], [43] which is well known in bipolar devices, where the device avalanche breakdown voltage shifts from its static value during the turn-off dynamics. As shown in Fig. 16, when the device voltage is 2600 V after turn-off, the peak electric field is higher than that at 2600 V static bias condition and similar to the one at 3270 V in static BV. In addition, at 2600 V dynamic condition, the impact ionization rate has reached or even exceeded the static avalanche level (Fig. 16(b)).

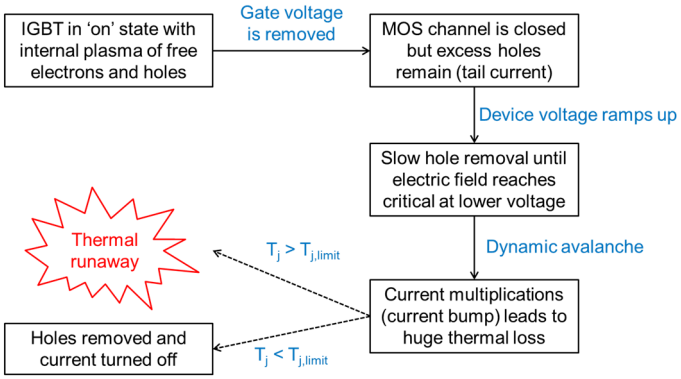

Fig. 17. Flowchart describing the tail-current bump mechanism.

Based on the above discussion, the internal dynamic process of the current bump phenomenon and failure process is summarized in Fig. 17. After the channel is closed, the excess holes remain (forming the tail current) and need to be removed. Due to the RC snubber that suppresses *dv/dt*, voltage (and therefore E-field) is low at the initial stage of hole removal. The slow hole removal results in a steeper E-field distribution and finally triggers the dynamic avalanche at a lower bias. During avalanche, current multiplies, and the current bump manifests. It should be noted that during the current bump, device voltage is at a high level, and a huge thermal loss exists. Device failure can occur due to thermal runaway when junction temperature (T_j) exceeds its intrinsic critical limit. The described failure mechanism matches with the hotspot observed under device decapsulation (in Fig. 12(c)).

The current bump phenomenon is related to the amount of remaining holes when device voltage reaches the dynamic avalanche level. At higher turn-off current, the holes injected in the device during the on state is more, so the current bump increases. At higher *dv/dt* (low C_s values), hole current increases as the voltage rises quickly (relatively), so the current bump becomes obvious. The current bump can be suppressed by lowering the peak clamping voltage, as it prevents the device voltage from reaching dynamic avalanche level. Knowing the type II PEI module failure is associated with the device tail current dynamics, the following section investigates how key circuit parameters affect the tail bump and the turn-off SCC.

V. Methods for SCC Enhancement in Type II PEI

The DUT was evaluated in the type II configuration using different non-destructive tests to characterize the IGBT tail current and reveal the associated dependencies. Several approaches are then presented for mitigation of the detrimental

tail current bump phenomenon to enhance the SCC.

A. Peak Turn-off Current

In the PEI application, the turn-off current value is pushed to several times the continuous rating of the device (exceeding RBSOA). Therefore, the effect of peak current on the tail bump was investigated. The R_s and C_s values were kept constant at 1.2 Ω and 0.44 µF (same as Table III). An MOV with rated clamping voltage value of 2000 V (at 100 A) was selected. With all other parameters being the same, the peak turn-off current value was increased in steps (peak value kept ≤ SCC in Table IV) to observe the tail bump characteristics. The results are provided in Fig. 18.

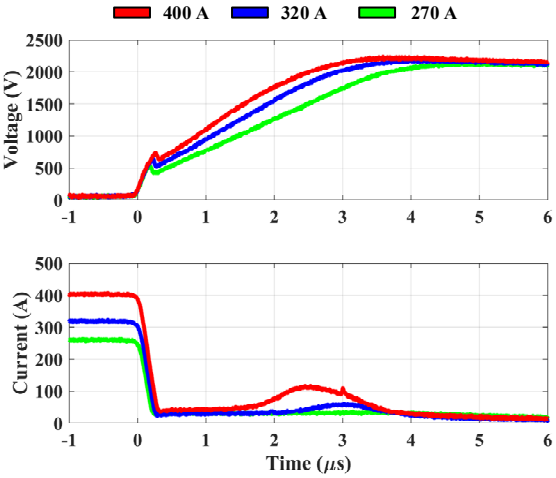

Fig. 18. Influence of peak turn-off current on the tail bump.

As the turn-off current value was increased it was found that the bump magnitude increased as well. A maximum of 100 A tail bump was observed at a turn-off current of 400 A, whereas a turn-off current of 250 A showed no bump at all. This can be attributed to the increased free carriers stored in the device at the point of turn-off with increased turn-off current magnitudes. Therefore, it is concluded that the bump magnitudes are exacerbated at higher turn-off currents, which, if not addressed, can result in device failure.

B. PEI Voltage dv/dt - Snubber Resistor and Capacitor

As explained in the previous section, the reason for the manifestation of the tail bump is because the device voltage is still increasing (slow voltage rise due to RC snubber) while the current has dropped to the tail-current or hole recombination level. Therefore, it is advisable to evaluate the impact of *dv/dt* on the bump characteristics. As per (7), the snubber parameters, R_s and C_s can change the *dv/dt* during the di_{RC}/dt and the tail current stages respectively. A series of tests were conducted where the R_s and C_s values were varied separately with other circuit parameters being the same.

As in the previous case, the MOV rated clamping voltage is 2000 V (at 100 A). In the first test, R_s was varied, and the C_s value was kept at 0.44 µF while the peak turn-off current was fixed at 370 A. In the second case, C_s was varied, and the R_s value was kept at 1.2 Ω while the peak turn-off current was fixed at 340 A. The results for the first case are presented in Fig. 19; a larger R_s, as expected resulted in additional voltage stress across the PEI in addition to a higher *dv/dt* during the i_{RC} rising stage (as seen in the inset). This increased voltage leads to higher electric field inside the device resulting in a higher overall tail current magnitude. Due to the higher device stress resulting from the higher voltage and tail current magnitude, larger R_s values are not recommended. The selected value should still satisfy (6) if deemed necessary. RCD snubbers are another option, if cost allows, to avoid the negative impact of R_s on the tail current during the turn-off transient.

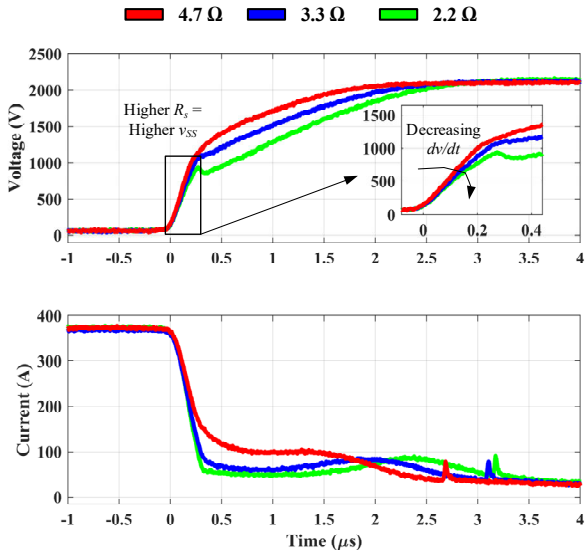

Fig. 19. Influence of snubber resistor (Stage IIIa *dv/dt*) on the tail bump.

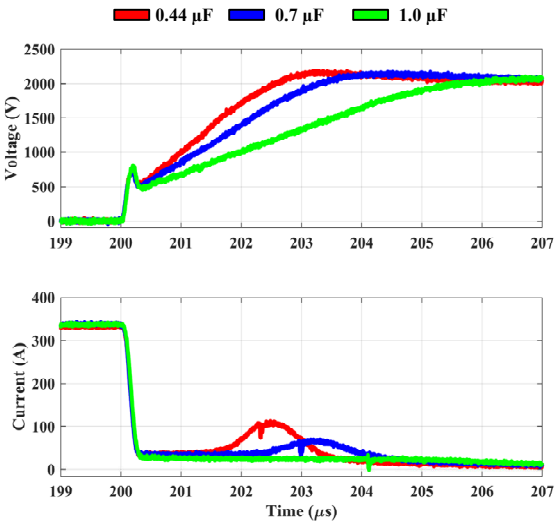

Fig. 20. Influence of snubber capacitor (Stage IIIb *dv/dt*) on the tail bump.

The results for the second test case are presented in Fig. 20. Larger C_s values help slow down the device *dv/dt* during the tail current stage in addition to lowering the instantaneous voltage during this time (due to a mitigated MOV steep front effect). It is observed that this is helpful in mitigating or even possibly eliminating (depending on C_s value) the tail bump current. Therefore, larger C_s values are recommended (final value based

on experimental evaluation) so that the bump magnitude can be suppressed to acceptable levels, to enhance the device SCC without the threat of bump-induced failure.

C. MOV Clamping Voltage Level

The MOV sets the final clamping voltage of the device during the turn-off. A lower clamping voltage is favorable in terms of the device stress under any configuration (type I/II). In the following test, the effect of MOV voltage on the tail bump was evaluated. The C_s and R_s values were fixed at 0.44 µF and 1.2 Ω. The peak current value was fixed at 340 A while the clamping voltage level was changed by using different MOV parts. The results are provided in Fig. 21.

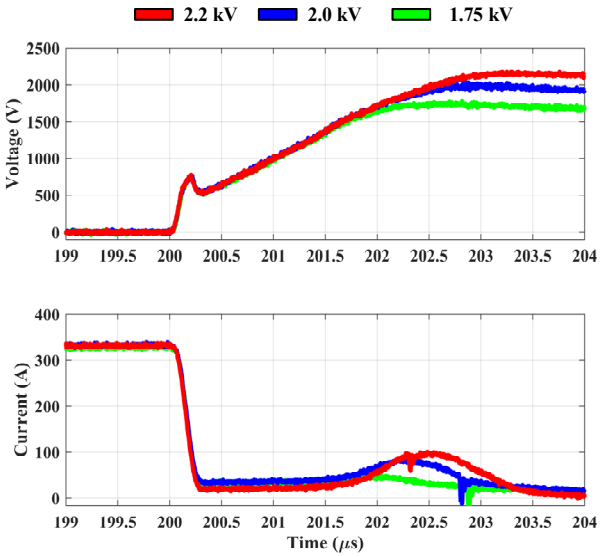

Fig. 21. Influence of MOV clamping voltage level on the tail bump.

It can be seen that the device *dv/dt* values are identical for all cases as there is no change to the RC parameters; the only difference is the final clamping voltage value as set by the chosen MOV. Lower MOV voltage ratings result in lower tail bump magnitudes. In other words, the manifestation of the tail bump results in reduced device VUF. Lowering the clamping voltage can yield higher device SCCs.

TABLE VII. CIRCUIT PARAMETER INFLUENCE ON TAIL CURRENT BUMP

Parameter	I_{pk}	R_s	C_s	V_{pk}
Tail Current Bump	Positive Correlation	Positive Correlation	Negative Correlation	Positive Correlation

The summary of the investigation in this section is presented in Table VI. Two methods are identified, that can be used to suppress the tail current bump and thereby improve the SCC of the device under type II configuration:

i. Larger C_s values (reduced voltage and *dv/dt*)
ii. Reduced clamping voltage setting (V_{pk})

It is not recommended to sacrifice the device VUF in pursuit of a higher SCC as it ultimately affects the PEI power density (requiring more devices in series). Therefore, higher values of C_s is the more desirable method to increase the device SCC (lower volume penalty) while retaining its VUF. The required value must be selected to suit the application needs as there is a necessary trade-off between capacitor value/size/cost and the required peak turn-off current. To validate this conclusion, the DUT was subjected to a surge test with $C_{s,new}$ = 1 µF while the remaining parameters were kept the same as in the destructive test in Fig. 12(b); i.e., R_s = 1.2 Ω, peak MOV voltage = ~2.1 kV. The results are shown in Fig. 22, where it is seen that the device could successfully interrupt a peak current of 530 A (~33 % higher I_{pk} than that in Table IV) with a reduced tail bump magnitude of 60 A, thanks to the higher capacitance value.

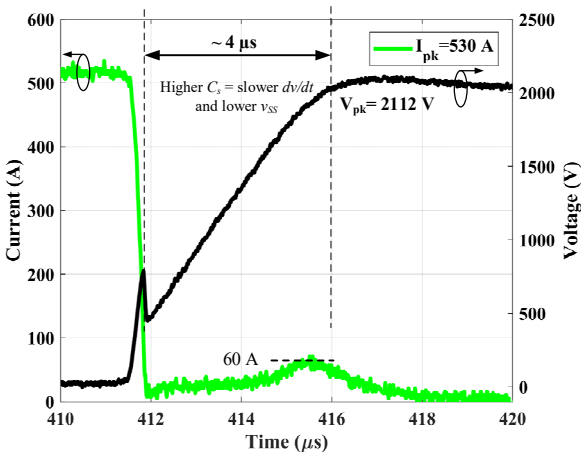

Fig. 22. Device 1 under type II circuit with $C_{s,new}$ = 1 µF (R_s = 1.2 Ω) successfully turning off 530 A peak current with V_{pk} of ~2.1 kV and reduced maximum current bump magnitude of ~ 60 A.

Therefore, it can also be concluded that the standard RC snubber design equations are not sufficient for superior SCC performance. Higher values of C_s (chosen through experiments) are recommended to sufficiently suppress the current bump phenomenon and enhance the SCC for type II discrete IGBT based PEI circuits.

VI. CONCLUSION

This work deals with the surge current interruption capability and performance of discrete IGBTs as applied to PEI modules. Specifically, the device SCC and main failure mode under two commonly used VCC configurations, type I – purely MOV based clamp; type II – MOV-RC combination clamp, were evaluated. In addition, physics-based device simulations were presented to further explain the device internal dynamics and associated failure mechanism. Finally, methods to improve the SCC of the device under type II configuration were presented. The main findings are summarized below:

i. The general assumption that RC snubber results in lower device stress is not necessarily true as the tail current magnitude and duration can become significant under type II especially at high turn-off currents such as those seen in circuit breaker applications.
ii. The failure mechanism in the type I module configuration is related to high turn-off energy arising from hard

switching. The peak SCC in this case is limited by the chip's thermal limit.

iii. The type II module suffers from the tail current bump phenomenon and the corresponding dynamic avalanche induced failure which was revealed through TCAD simulations.

iv. The SCC of a given discrete IGBT in the type II configuration can be enhanced by using a large enough snubber capacitance (C_s) value (slower turn-off *dv/dt*) in the design to suppress the tail current bump magnitude.

These findings for a single device can be scaled to parallel device combinations if current, voltage and applied *dv/dt* are kept the same.

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