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AC stress analysis of trench-based multi-gate transistors in a 40 nm e-NVM technology

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Abstract

This work addresses the reliability of different architectures of novel high-density multi-gate transistors manufactured in a 40 nm embedded Non-Volatile Memory process technology. The multi-gate architectures are based on lateral transistors integrated in deep trenches built alongside the main planar transistor. These architectures increase the conduction channel width with a weak impact on the footprint. A reliability study based on AC stress tests is carried out to monitor the multi-gate oxide degradation and in particular the interaction between planar and vertical oxides is highlighted. Finally, a benchmark of stress immunity, among the three studied multi-gate architectures, is presented.

1. Introduction

The semiconductor industry is facing a continuous scaling of the physical feature sizes. However, the downscaling of devices encounters physical limits in terms of trade-off between fabrication and costs for the integrated circuits in an embedded Non-Volatile Memory (e-NVM) environment [1]. Embedded memories, digital and analog circuits need to be integrated together sharing some production steps. Sometimes the scaling operation of a single device is not compatible with the complete process flow. The research in new transistor architectures is welcome to improve the single device performance requirements in a low-cost and high-volume production. This is a real challenge for e-NVM technology which targets the market of consumer electronics including Internet of Things (IoT) applications.

In this context, alternatives to classical planar MOSFETs have emerged in the last few years such as multiple-gate transistors [2], triple gate transistors [3], octagonal transistors [4], vertical MOS transistors [5], gate all around transistors [6], and the most relevant double gate SOI MOSFETs [7-9] and FinFETs [10-13] architectures. Alternatively, and mostly for passive devices, deep silicon trenches are used in different ways to increase integration density (insulators, sensors, or capacitors [14]).

The aim of this work is to study the reliability aspects of three architectures of Multi-Gate Transistors

(MGT) manufactured in a 40 nm e-NVM technology. These multi-gate structures have been fabricated to improve the driving capability with a low impact on the area of planar transistors used in column decoders to address the memory cells. A description of the functioning and performances of these devices are presented in [15] [16]. The MGT architecture design is based on a typical planar MOS transistor to which two lateral conduction channels are added by integrating deep trench transistors alongside the planar one between source and drain regions. After fabrication, electrical measurements and reliability tests are conducted on gate oxides for different types of multi-gate configurations to assess their performances compared to the equivalent standard transistor.

Section 2 presents the manufacturing process and operation mode of three different MGT devices, while the section 3 summarizes experimental AC stress test results. Section 4 concludes the paper.

2. Trench-based MGT

2.1. MGT manufacturing process

The fabrication process of new MGT architectures implies the integration of two vertical trenches on both active sides of the planar gate transistor connecting source and drain regions. For clarity, simulation process views, based on the virtual fabrication tool Coventor@SEMulator3D, are proposed in Fig. 1.

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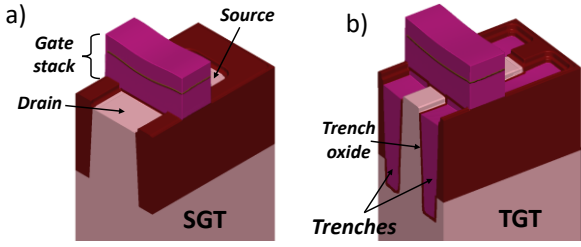


Fig. 1. Coventor images of (a) planar transistor SGT with standard lateral shallow trench isolations and (b) Triple Gate Transistor TGT where the vertical transistors are integrated in trenches.

The standard planar device called Single Gate Transistor (SGT) (Fig. 1 (a)) is integrated in the NVM process and its fabrication takes advantage from the eSTMTM [17] Flash floating gate memory stack. This limits the number of additional production steps, and no more masks are required. Thus, the gate stack consists of a tunnel oxide (~10 nm) and two polysilicon layers called poly1 and poly2 separated by an oxide/nitride/oxide (ONO) interpoly dielectric, present in the memory process flow. To obtain the standard MOS configuration both poly1 and poly2 are shorted, and the contact is made through the gate stack. Finally, source and drain are created with n+ implantations. In order to develop the MGT device starting from the SGT architecture, the trench transistors are thus integrated in the lateral shallow trench isolation regions (Fig. 1 (b)). This enables the possibility to create two additional conduction channels between source and drain terminals. Note that the trench oxide thickness is around 10 nm, like the tunnel oxide. This results in the architecture called Triple Gate Transistor (TGT). It is important to notice that the vertical embedded trench already exists in the fabrication process flow of eSTMTM Flash memory cell [17].

Moreover, another architecture associating one planar and only one lateral gates is available. This architecture is defined as Dual Gate Transistor (DGT).

2.2. Operating mode

In Fig. 2 (a) we represented the electrical schematic of TGT architecture. The two lateral transistors have a common gate contact, and the three channels enable the conduction between source and drain regions. The first conduction path is controlled by the planar gate (PG) and its current flow is represented by the blue arrow in Fig. 2 (b) and (c). The current flow due to the lateral transistors is controlled by the vertical trench gates (TG) and it is represented by the green arrow in the Fig. 2 (b) and (c) [9].

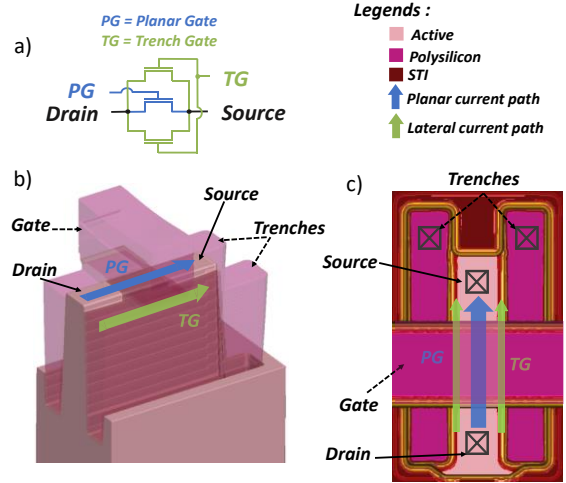


Fig. 2. (a) Electrical schematic of a TGT structure, conduction paths represented on a (b) 3D view and (c) top view.

2.3. Physical details of MGT architectures

In Fig. 3 we present the physical parameters of the studied devices [10]. The SGT, which is the standard planar transistor, is considered as the reference in this work. It will be compared to the DGT, which has only one vertical trench, and to two TGT architectures.

	SGT	DGT	TGT1	TGT2
Layout				
Legends :	<ul style="list-style-type: none"> ■ Active ■ Gate ■ Trench Contact 			
Electrical Schematic				
W_p (nm)	200	180	160	110
Area (μm^2)	0.304	0.328	0.412	0.374

Fig. 3. Layout, electrical schematic, planar width (W_p) and area of each multi-gate architecture.

The presence of a vertical trench enables a planar width (W_p) decrease of 20 nm. One can notice that the DGT active area includes the PG and TG channel widths. The third architecture is the TGT1 which is composed of the SGT planar transistor with two in-trench lateral transistors. The TGT1 channel includes the widths of the two TG and the W_p of the PG which is defined by the space between the trenches (160 nm). Finally, the last architecture is the TGT2 designed using an aggressive shrink of the TGT1 architecture with a smaller width (110 nm). For each device, the equivalent electrical schematic is provided to highlight the number of transistors as well as the designed area. The integration of only one trench has a slight impact on the global area.

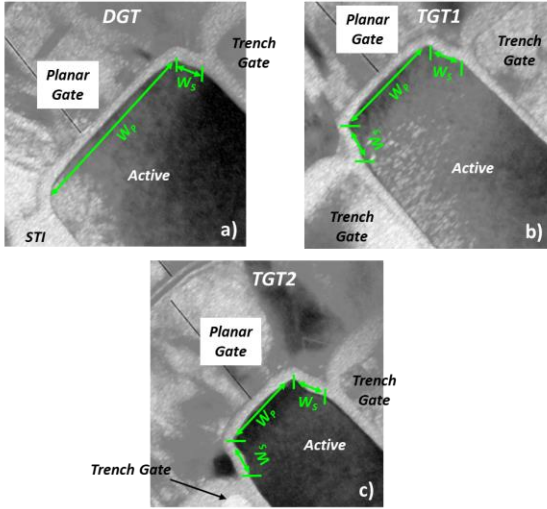


Fig. 4 TEM pictures of: (a) dual gate transistor (DGT), (b) Triple Gate Transistor 1 (TGT1), (c) Triple Gate Transistor 2 (TGT2).

Regarding the TGT1 structure, the integration of a double trench results in a higher area increase. One can notice that for multi-gate devices one supplementary contact is needed for trench gate. A design optimization can provide a solution with TG contacts above the active area.

In Fig. 4 the Transmission Electron Microscopy (TEM) pictures are presented for each multi-gate transistor. As previously discussed, the physical planar width can be modified with respect to the layout dimensions when the trench gates are integrated. Moreover, we observe the planar gate rounds the active area and a supplementary width (W_s) dimension has to be considered during the PG conduction experiments. The top of trench gates is lower than the active surface, this suggests the possibility of degradation interaction between PG and TG. This motivates the work on the AC stress alternatively applied on planar or vertical gates presented in next section.

3. Experimental results: AC stress analysis

The aim of this section is to study the behaviour of the different multi-gate devices under AC gate stress. The quasistatic drain current versus gate voltage, characteristics are reported in a previous work [16], where we benchmarked our MGT architectures in terms of single device performances. As these have similar architecture of FinFET transistor, we report here some electrical parameters to compare these two devices with similar dimensions we refer to [18] and [19]. From [16] we calculate the normalized: ON current (I_{ON}), OFF current (I_{OFF}) and subthreshold slope (S_s), using a vertical channel width of 50nm. This last depends on source/drain implantations. The results are reported in

Table I, they show the interest we have in these devices.

	I_{ON} (mA/ μ m)	I_{OFF} (pA/ μ m)	S_s (mV/dec)
DGT	1.22	0.13	95
TGT1	1.78	2.31	79
TGT2	2.10	19	83
FinFET [18]	1.14	70k	68
FinFET [19]	0.549	10k	79

Table I. Comparison of MGT devices and FinFETs.

3.1. Experimental setup

The proposed MGT architectures are stressed to assess the reliability of gate oxides including both planar and lateral transistors. Regarding the experimental setup, an Agilent B1500 semiconductor parameter analyser is used for electrical characterizations and pulsed stress. The SMU (Source Measure Unit) and SPGU (Semiconductor Pulse Generator Unit) modules are alternatively switched by the Keithley 7001 switch matrix. To perform the positive pulsed AC stress, a trapezoidal signal with a period of 200 μ s, a duty cycle of 50 % and a rising/falling time of 100 ns is used. The drain, source and bulk terminals are connected to the ground during the gate stress. As discussed in [15], PG and TG cannot support the same stress voltage because the vertical oxide thickness slightly decreases down to the sidewalls, which makes it more sensitive compared to the planar oxide. Moreover, the tip of the planar gate between the active and trench gate regions locally enhances the electric field (Fig. 4). Therefore, the stress of the planar gate is performed at the voltage V_{PG} of 10 V and at the trench gate V_{TG} of 8 V. The stress is periodically interrupted to measure the drain current (I_D) versus gate voltage characteristics at drain voltage (V_D) of 0.7 V, where the gate voltage is either V_{PG} or V_{TG} . Two main parameters are extracted: the threshold voltage (V_t) at $I_D = 100$ nA and the transistor ON current for a gate bias of 3 V.

Finally, we decided to perform the AC stress of the planar gate while the TG is grounded (or on the contrary stress on TG while V_{PG} is 0V) for an aggregate time of 300 s, monitoring the parameters of both transistors during the oxide degradation.

3.2. Impact of PG stress on MGT architectures

The aim here is to study the impact of the PG stress on the different architectures and more specifically on the trench gates of the MGT architectures.

In Fig. 5, the evolution of V_t and I_{ON} of MGT and SGT devices during the PG stress is extracted for both planar (Fig. 5 (a), (b)) and lateral (Fig. 5 (c), (d)) transistors. Note that the relaxation time of the AC stress is not considered. Regarding the PG electrical parameters, the V_t shift increases for all architectures

(Fig. 4 (a)), demonstrating an electron charge trapping in the oxide bulk. The highest V_t shift is observed for the SGT, followed by the DGT and the TGT1. Finally, a weak V_t variation is observed for the TGT2. The difference between the ΔV_t evolution of all architectures can be explained by the larger area (higher W_P) of planar oxide impacted by the stress. Therefore, the SGT with the largest gate oxide area ($W_P = 200$ nm) shows the highest V_t shift while the TGT2 shows the lowest shift ($W_P = 110$ nm). All architectures in Fig. 5 (b), show a decrease of the I_{ON} current, and the SGT is still the most impacted. This is coherent with the previous results on threshold voltages increasing. The shift of V_t and I_{ON} of the lateral transistor versus PG stress is reported in Fig. 5 (c), (d). The V_t (Fig. 5 (c)) remains constant for the TGT1 architecture, but slightly decreases for the DGT and TGT2. Hence, for the different MGT architectures, the lateral transistors seem to be marginally damaged by the PG stress. To better investigate the TG oxide degradation versus PG stress time, we report the I_D - V_{TG} characteristics in Fig. 6 (a), (b), (c) before and after stress. The post-stress characterizations are performed with $V_{PG} = 0$ V (red curve) and $V_{PG} = -3$ V (green dashed curve). Even if the electrical parameters V_t and I_{ON} remain almost constant during the stress, the I_D - V_{TG} characteristics show a variation of the subthreshold slope (S_s) and I_{ON} , highlighted in Fig. 6 (d).

For each architecture, one can notice that the fresh characteristic (black curve) can be recovered after stress if the planar gate is biased at $V_{PG} = -3$ V. This behaviour is explained by the accumulation region created at the channel/PG oxide interface by the negative V_{PG} bias (Fig. 7). The planar gate oxide degradation is thus masked at the trench/planar gate oxide corner. Therefore, the vertical effective TG channel width is decreased, which is confirmed by the fact that the I_{ON} current before stress is higher than its post-stress value at $V_{PG} = -3$ V. This is validated for the three MGT devices.

3.3. Impact of TG stress on MGT architectures

To complete the study on AC stress, we measured the impact of the TG stress on the different architectures. The evolution of V_t and I_{ON} of the TG transistor is reported in Fig. 8 (a) and (b) while the PG transistor parameters are reported in Fig. 8 (c), (d). For the lateral transistors, a strong ΔV_t increase is observed for some TGT2 samples corresponding to a higher I_{ON} shift plotted in Fig. 8 (b). In Fig. 8 (c) and (d) the evolution of V_t and I_{ON} for the PG transistor of the MGT devices is reported. In general, these parameters remain constant during the stress. In the case of high damaged TGT2, a weak variation is reported also for PG.

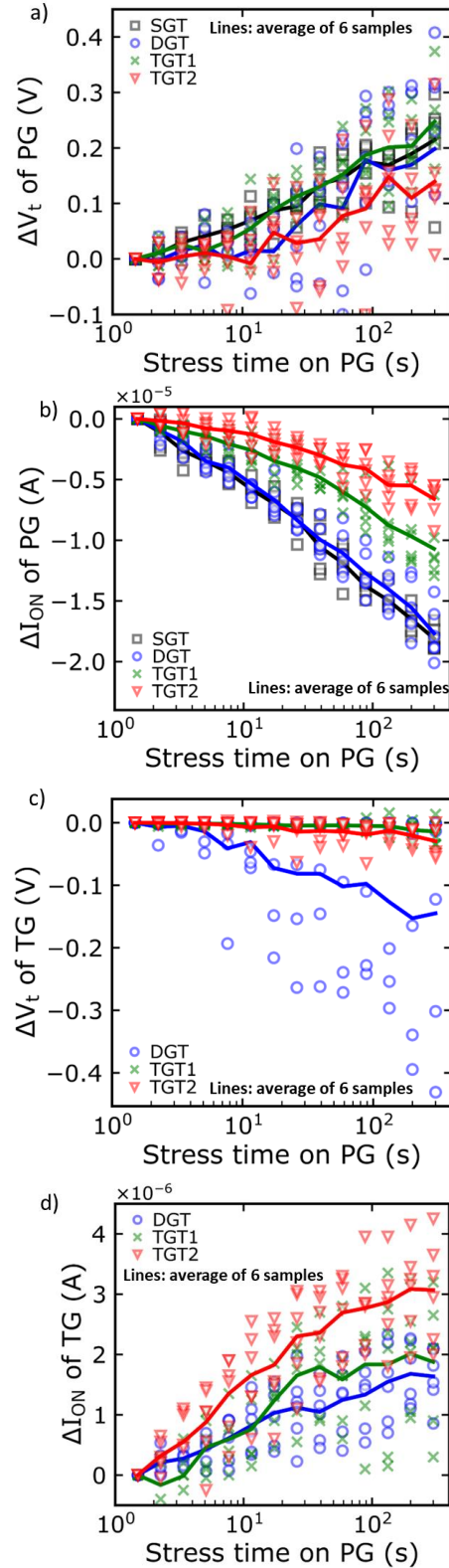


Fig. 5. ΔV_t and ΔI_{ON} versus AC PG stress time for the planar transistors (a), (b) and lateral transistors (c), (d).

It is worth to notice that for the planar conduction, the variation of V_t is sixty times lower with respect to the lateral, while the I_{ON} variation is twenty times lower. This demonstrates that the AC stress applied to the TG does not impact the conduction of the planar transistor. This is due to the height of the trench gate being lower than the active region, as the planar gate oxide is preserved when the lateral transistor is stressed.

This study shows the degradation at high gate biasing that needs to be correlated to other experiments to self-heating induced hot carrier injection. This kind of degradation is recently addressed as a main problem of FinFET devices that present similar architecture to MGT. In [20] and [21] the FinFETs has, a very low oxide degradation, in the case of gate stress, while the main weakness is represented by the threshold voltage shift under hot carrier stress conditions. Thus, this aspect will be focused on future works.

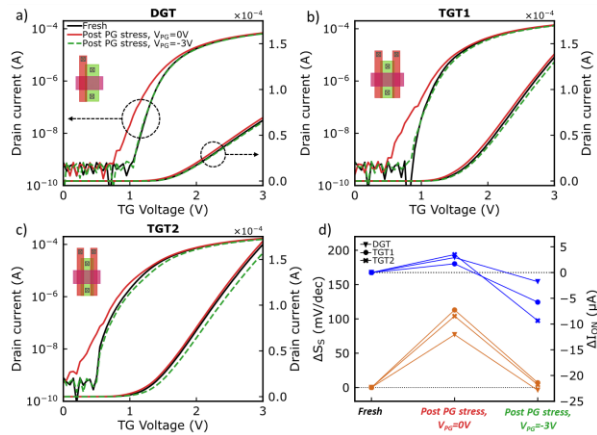


Fig. 6. I_D - V_{TG} characteristics of the TG transistor before stress with $V_{PG}=0V$ (black curve), post-stress with $V_{PG}=0V$ (red curve) and $V_{PG}=-3V$ (green dashed curve) for the (a) DGT, (b) TGT1 and (c) TGT2 architectures. (d) Variation of subthreshold slope (S_s) and I_{ON} after stress for each device.

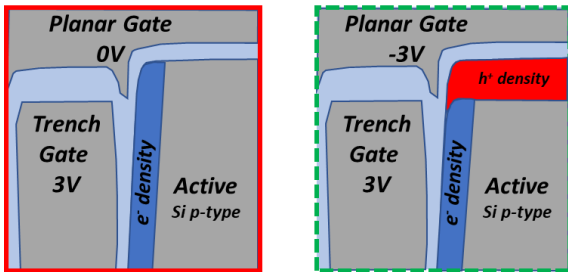


Fig. 7. Schematics of electron and hole densities in the active region when the lateral transistor is on ($V_{TG}=3V$) with $V_{PG}=0V$ and $V_{PG}=-3V$.

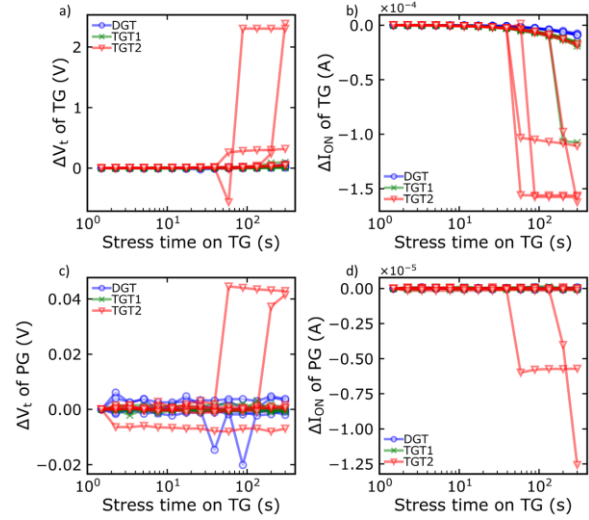


Fig. 8. V_t and I_{ON} variation versus AC stress time for PG stress for (a), (b) PG transistor and (c), (d) TG transistor.

4. Conclusion

In this paper we present a reliability study carried out on different multi-gate transistor architectures. The experimental investigations have been performed on the MGT devices and on a standard planar transistor for quantitative comparison. Moreover, a benchmark with some FinFET devices has been reported to show the interest in these new low-cost architectures. The gates of these devices have been submitted to positive AC stress. Regarding the PG stress, the planar gate of the TGT2 has the best immunity compared to the others integrating one or two lateral trenches. This is explained by the fact that the TGT2 has the smallest planar oxide area followed by the TGT1 and finally by the DGT. For the TG stress, the DGT architecture has the best immunity due to the single trench integration. The overall behaviour can be explained by considering the gate oxide area of each architecture. We focus on drain current versus gate voltage characteristics to explain the interaction between the planar and lateral conduction when the stress is applied on one gate. The actual MGT architectures show a degradation of lateral transistors when the PG is stressed. On the contrary the planar conduction is immune from the lateral stress, taking advantage from the lower height of vertical trenches with respect to the planar active region. Finally, the DGT architecture is the best candidate regarding the electrical performances [16] and the reliability results. A benchmark of experimental results is summarized in Table II.

	DGT	TGT1	TGT2	
Area (μm^2)	+ 8 %	+ 36 %	+ 23 %	
$I_{\text{ON}} / \text{Area}$ ($\mu\text{A}/\mu\text{m}^2$)	+ 81 %	+ 139 %	+ 167 %	
PG stress	PG Degradation	Moderate	Moderate	Low
	TG Immunity	Moderate	Moderate	Moderate
TG stress	TG Degradation	Low	Moderate	High
	PG Immunity	High	High	Low

Table II. Comparison of MGT devices against AC stress.

References

- [1] M. T. Bohr and I. A. Young, "CMOS Scaling Trends and Beyond," IEEE Micro, p. 10, 2017.
- [2] J.-P. Colinge, "1 The SOI MOSFET: from Single Gate to Multigate," FinFETs Multi-Gate Transistors, pp. 1–48, 2008.
- [3] C. Auth, "22-nm fully-depleted tri-gate CMOS transistors," Proceedings of the IEEE 2012 Custom Integrated Circuits Conference, 2012.
- [4] Y. Joly et al., "Octagonal MOSFET: Reliable device for low power analog applications," ESSDERC, 2011.
- [5] J. Locati et al., "AC stress reliability study on a novel vertical MOS transistor for non-volatile memory technology", Microelectronics Reliability, vol. 114, 2020.
- [6] S. Bangsaruntip et al., "High performance and highly uniform gate-all-around silicon nanowire MOSFETs with wire size dependent scaling," IEEE IEDM, 2009.
- [7] S. Hayashi, Y. T., "Calculated threshold-voltage characteristics of an X MOS Transistor having an additional bottom gate," Solid-State Electronics, vol. 27, no. 8/9, pp. 827–828, 1983.
- [8] J. Widiez et al., "Experimental Gate Misalignment Analysis on Double Gate SOI MOSFETs," IEEE international SOI Conference, pp. 185–186, 2004.
- [9] X. Lin, C. Feng, S. Zhang, W.-H. Ho, and M. Chan, "Characterization of double gate MOSFETs fabricated by a simple method on a recrystallized silicon film," Solid-State Electronics, vol. 48, p. 5, 2004.
- [10] D. Bhattacharya, N. K. Jha, "FinFETs: From Devices to Architectures", Advances in Electronics, vol. 2014, Article ID 365689, 21 pages, 2014.
- [11] W. Zhang, J. G. Fossum, L. Mathew, and Y. Du, "Physical insights regarding design and performance of independent-gate FinFETs," IEEE Transaction on Electron Devices, vol. 52, no. 10, p. 9, 2005.
- [12] D. Hisamoto et al., "FinFET-a self-aligned double-gate MOSFET scalable to 20 nm," IEEE Transaction on Electron Devices, vol. 47, no. 12, p. 6, 2000.
- [13] K. Okano et al., "Process integration technology and device characteristics of CMOS FinFET on bulk silicon substrate with sub-10 nm fin width and 20 nm gate length," IEEE IEDM, p. 4, 2005.
- [14] S. Banzhaf et al., "Post-trench processing of silicon deep trench capacitors for power electronic applications," ISPSD, pp. 399-402, 2016.
- [15] R. Gay et al., "A Novel Trench-Based Triple Gate Transistor With Enhanced Driving Capability," in IEEE EDL, vol. 42, no. 6, pp. 832-834, 2021.
- [16] R. Gay et al., "Benchmarking and optimization of trench-based multi-gate transistors in a 40 nm non-volatile memory technology," DTIS, pp. 1-4, 2021.
- [17] F. Melul et al., "Hot Electron Source Side Injection Comprehension in 40nm eSTM™," 2021 IEEE International Memory Workshop.
- [18] B. S. Doyle et al., "High performance fully-depleted tri-gate CMOS transistors," in IEEE Electron Device Letters, vol. 24, no. 4, pp. 263-265, April 2003.
- [19] C. Lin et al., "Effects of Fin Width on Device Performance and Reliability of Double-Gate n-Type FinFETs," in IEEE Transactions on Electron Devices, vol. 60, no. 11, pp. 3639-3644, Nov. 2013.
- [20] A. Gupta, C. Gupta, R. A. Vega, T. B. Hook and A. Dixit, "Reliability Modeling and Analysis of Hot-Carrier Degradation in Multiple-Fin SOI n-Channel FinFETs With Self-Heating," in IEEE Transactions on Electron Devices, vol. 66, no. 5, pp. 2075-2080, May 2019.
- [21] C. Gupta, A. Gupta, R. A. Vega, T. B. Hook and A. Dixit, "Impact of Hot-Carrier Degradation on Drain-Induced Barrier Lowering in Multifin SOI n-Channel FinFETs With Self-Heating," in IEEE Transactions on Electron Devices, vol. 67, no. 5, pp. 2208-2212, May 2020.