



SuperCAST: a full free addressable memory array

Vincenzo Della Marca, Julien Guilleau-Tavernier, Pierre Laine, Franck Melul, Marc Bocquet, Thibault Kempf, Loic Welter, Jean-Michel Moragues, Arnaud Regnier, Jean-Michel Portal

► To cite this version:

Vincenzo Della Marca, Julien Guilleau-Tavernier, Pierre Laine, Franck Melul, Marc Bocquet, et al.. SuperCAST: a full free addressable memory array. IEEE 34th International Conference on Microelectronic Test Structures (ICMTS 2022), Mar 2022, Cleveland, OH, United States. pp.1-4, 10.1109/ICMTS50340.2022.9898189 . hal-04063478

HAL Id: hal-04063478

<https://hal.science/hal-04063478>

Submitted on 17 Apr 2023

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

SuperCAST: a full free adressable memory array

Vincenzo Della Marca¹, Julien Guilleau-Tavernier¹, Pierre Laine¹, Franck Melul^{1,2}, Marc Bocquet¹, Thibault Kempf², Loic Welter², Jean-Michel Moragues², Arnaud Regnier² and Jean-Michel Portal¹

¹Aix-Marseille Université, IM2NP, CNRS, UMR 7334, 5 rue Enrico Fermi, 13397 Marseille, France

²STMicroelectronics, 190 Av. Coq, 13106 Rousset, France

vincenzo.della-marca@im2np.fr

Abstract— In this paper we present a full free addressable 4kb EEPROM memory array. This test structure based on CAST vehicle has been upgraded with flexible addressing logic to select any numbers of cells on single or multiple word lines. To this aim, column/row shift registers, to enable an easy cell biasing, have been implemented in an embedded non-volatile memory environment. High voltage circuits, driven by low voltage shift registers, are used to bias selected cells for electrical characterizations and reliability tests purposes. This kind of structure has been developed to improve the efficiency of electrical characterization laboratory, resulting in an enhanced acquisition with respect to standard CAST test techniques, opening the path to fine statistical analysis.

Keywords—CAST, non-volatile memories, array

I. INTRODUCTION

The Cell Array Stress Test (CAST) is a very useful vehicle to study reliability of charge storage memory cells since the 1990s [1]. It provides for example the possibility to detect overerased bit tails or weaknesses in terms of data retention [2, 3]. Furthermore, the problems due to the access resistance of a cell in a memory array can be modeled to optimize the number of contacts to bring the voltage biasing in a specific area without loss [4]. The equivalent transistor of charge storage memory, that corresponds to the memory cell where the floating and control gates are shorted, is also used in CAST structures to study the oxide reliability. A schematic of CAST structure is presented in Fig. 1a. The data collection enables to carry out drain current (I_D) versus control gate voltage (V_{CG}) characteristics before and after stress (Fig. 1b). These highlight two populations of memory devices: intrinsic cells (standard behavior) and extrinsic cells (tail bits or weak components). The main problem for this kind of extraction is the capability to verify the physical position of these bits in the memory block. This information is fundamental for the process control of large memory array to detect edge or specific signatures due to the different behaviors. Complex calculation techniques, combined with specific physical analysis [5], are used to estimate the number of extrinsic cells [4]. Finally, only electrical characterization on test products, can show the vulnerability localization [5]. To avoid these issues, the SuperCAST structure has been developed. The sequential addressing of each bit in the array is provided using low voltage (LV) shift registers for columns (Bit Lines), rows (Word Lines) and control gates. The high voltage (HV) circuits lead the memory biasing up to carry out electrical characterizations of EEPROM demonstrator memory array. We point the fact that the SuperCAST can be integrated in any embedded non-volatile memory technology: charge storage, charge trapping or resistive. This approach reaches standard reliability tests, improving the experimental

characterization protocols to attempt in-memory computing applications.

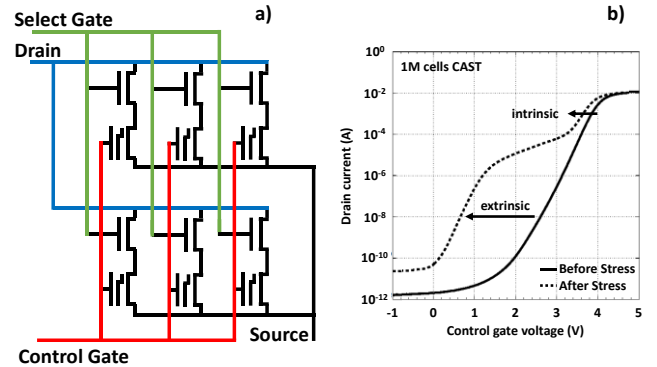


Fig. 1. a) Schematic of a 3x2 (Bit Lines x Word Lines) example of CAST. b) Drain current versus control gate voltage characteristics of a 1M cells CAST before and after stress.

II. SUPERCAST STRUCTURE

The studied CAST consists of 4k EEPROM cells connected in parallel. The bit selection is made biasing: the word line (WL) connected to select transistor gate, the control gate (CG) and the bit line (BL) connected to the drain. The source and bulk are common to all the cells. This architecture is developed around a standard CAST memory array. The novelty is represented by the circuits to address and bias the cells. We had considered the importance of structure sizing as well as the simplicity of logic circuits in order to minimize the number of structure pads, suitable to standard equipment in electrical characterization laboratory. Moreover, as the high voltages are necessary to write the EEPROM cells, we designed analog circuits to support those levels. The SuperCAST architecture is shown in Fig. 2. The size of the memory array is 4096 bits, 32 WL and 128 BL. The principle of functioning of this test structure can be summarized in three steps: i) an input digital signal to select rows, control gates and columns (selected or not); ii) some control signals to inhibit the memory matrix during the address time; iii) each WL, BL, CG must be able to supply selected or unselected cells. Another important point is the separation between the HV and LV domains. Typically, the circuits used to test a high number of memory cells are testchip solutions, close to product environment with complex peripherals and a large number of access pads. These test-chips need costly Automatic Test Equipment (ATE) to be emulated as well as complex test flow, with a reduced or no direct access to memory cells for characterization purpose. Our solution to address different portions of the memory array is to use sequential logic circuits. In this way the granularity one bit operation or on the contrary is possible to operate on the whole memory block.

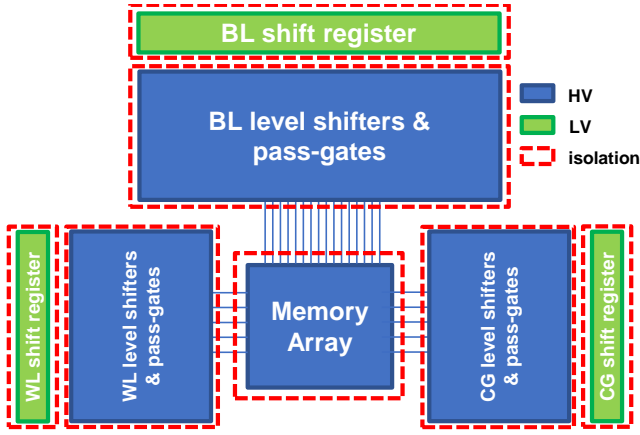


Fig. 2. SuperCAST block schematic. The high voltage (HV) and low voltage (LV) circuits are highlighted, as well as the well isolations.

A. Management of serial memory address

The sequential logic circuits are designed to use a maximum number of twenty-five pads. A synchronous shift register (SR) based on D flip-flops (FF) for each line has been designed using a low voltage V_{DD} bias (Fig. 3). The flip-flops are clocked with a maximum frequency of 250kHz, but this parameter can be adjusted as a function of the used technology to reduce the test duration. The address sequence enters in the first flip-flop (add_in) and it comes out after a number of clock (clk) cycles equal to the number of lines/columns (add_out). The address is ready for the columns after 128 clock cycles while it is done after 32 clk for the rows and control gates. These lasts can be addressed simultaneously. Once the addressing phase is finished, an asynchronous enable low voltage (en_LV) signal activates the AND logic gates to transfer the information. Moreover, a reset signal is present if needed. In Fig. 4, the bit output of the word line shift register is measured after 32 clk cycles demonstrating the bit entered in the first FF is well transferred to the output of the 32nd FF. The WL/BL/CG add_out pads have been added to verify the cells addressing, this is the only point to be sure the logic circuits are functioning. For future applications after the structure assessment, these pads can be suppressed to decrease the test structure size. Finally, the control signals (ctrl_in) for the level shifters are generated to bias the selected cells and inhibits unselected cells.

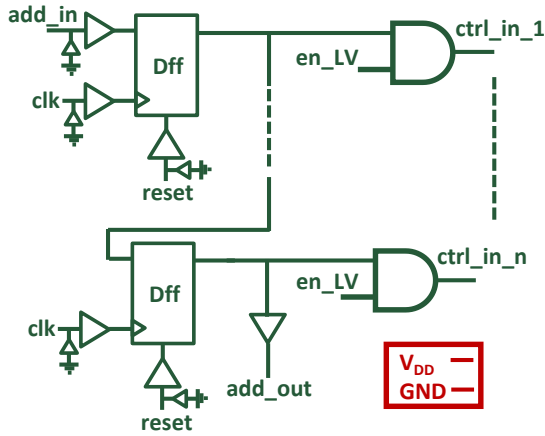


Fig. 3. Schematic of shift register structure.

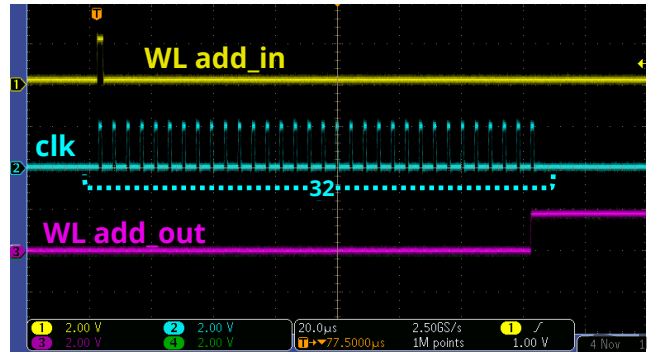


Fig. 4. Measurement of Word Line shift register output.

B. Level shifter and pass-gate: power supply transposition

The logic output from the shift registers deliver a low voltage signal ctrl_in, this represents the input for the level shifters that have to be able to provide high voltages for the EEPROM array. Thus, once the addressing phase finishes, the control signals to supply the selected memory cell are generated. The V_{DD} is pulled up to V_{CC} using a level shifter (LS) for each line (Fig. 5a). Two signals CTRL and \overline{CTRL} are used to activate the pass-gate (PG) to characterize the memory cells (Fig. 5b). The two signals: selected and unselected in Fig. 5b come from arbitrary pulse generators and they represent the analog patterns to write/erase the memory cells. At this stage it is important the maximum voltage of the bias patterning is less than the difference between V_{CC} power supply and the threshold voltage of HV transistors used for the pass gates. Moreover, the pass gates connected to the bit lines (columns) have to be designed to tolerate a driving current corresponding to the sum of maximum drain current that can flow toward 32 cells (maximum number of word lines) if all the cells in the column are selected. This aspect impacts the size of pass gate that represents the area dominant element in the structure. A tradeoff is thus necessary between the circuit area and the current driven by the pass gates. The en_HV signal enables the selected cell biasing and pulldown to the ground all the cell terminals before each write/erase/read operation.

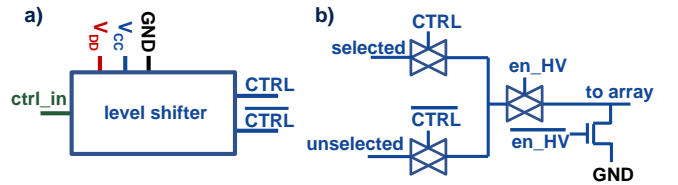


Fig. 5. Block diagram of a) level shifter and b) pass-gate.

III. EXPERIMENTAL DETAILS

The SuperCAST demonstrator has been integrated in 200mm wafers embedded non-volatile memory technology. In Fig. 6a, the top view of final layout is presented, while the picture of 25 pads final test structure is reported in Fig. 6b. One can notice that the memory block is smaller than the control circuits. Those have been designed around the array with the column driver on top, and on both left and right sides the word line and control gate lines are symmetrically disposed. This twenty-five pad structure is used for this demonstrator, but the number of pads can be reduced to decrease the occupied area.

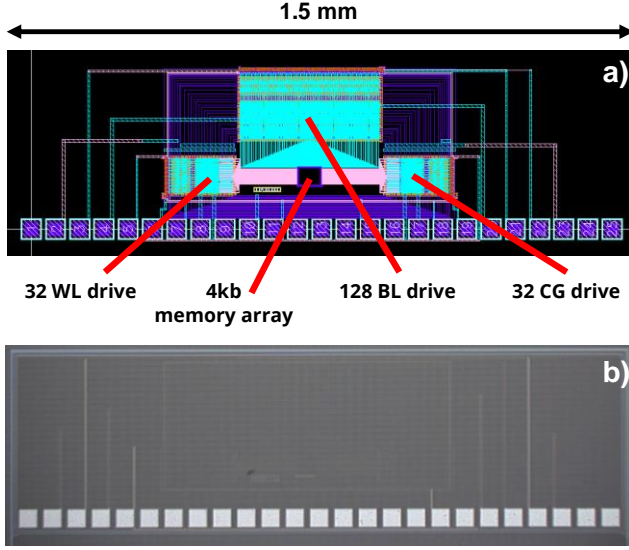


Fig. 6. SuperCAST a) layout and b) picture.

The complexity of experimental setup is linked to the high number of pads that must be biased as well as the number of test configurations to be deployed. In Fig. 7, a schematic of the experimental setup is depicted. Four programmable power supply sources are used to deliver V_{CC} , V_{DD} , reset and en_HV signals, to ensure high stability. In the sequence of different operations, the V_{DD} that supplies the digital circuits is turned on before the V_{CC} biasing to avoid the stress of low voltage transistors. Furthermore, two Agilent 33500B arbitrary pulse generators are employed for the memory addressing. The input addresses for columns/rows selection and clock signals for the shift registers are sequentially produced. Three Tektronix AWG2005 arbitrary pulse generators are also included. The first one generates the en_LV signal to activate the output of flip-flop shift registers. It is independent on two others because the en_LV signal is used during the addressing phase. The two remaining are used to address the memory cells to execute Fowler-Nordheim write/erase and read operations. The eight pulse sources are triggered to selected and unselected CG/WL/BL as well as the source and bulk terminals. The general biasing conditions are reported in Table 1. To reach higher voltages, a four-channel homemade operational amplifier stage is cascaded with pulse generators. While the selected memories are operating, it is important to inhibit the unselected cells grounding WL_{Unsel} , BL_{Unsel} and CG_{Unsel} . The drain voltage (I_D) versus control gate voltage (V_{CG}) electrical characteristics to read the threshold voltage (V_T) of EEPROM devices are carried out with a HP4156C parameter analyzer, it can activate one pulse generator to bias the remaining terminals. Finally, the HP4156C is connected to the device under test alternatively with the Tektronics pulsers thanks to the Keysight 708A switch matrix. We want to emphasize that all this set-up is fully compatible with standard electrical characterization lab, providing a complete control to all addressing mode and direct access to each memory cells, without the use of complex and costly ATE equipment.

TABLE I. ELECTRICAL EEPROM CELL ACTIVATION

	WL	BL	CG	Source	Bulk
Write	HV	HV	GND	LV	GND
Erase	LV	GND	HV	GND	GND
Read	LV	LV	$V_T=?$	GND	GND

IV. ELECTRICAL RESULTS

We reported here, as examples, some electrical results obtained on SuperCAST vehicle. In Fig. 8, the I_D - V_G characteristic of one selected written cell in the array is compared with the characteristic of the whole block. This experiment emulates the case of an extrinsic cell, typical, of tail bits signature on extraction of standard CAST structures. The characteristic of memory array is impacted by one written bit, presenting the typical hump due to the lower V_T of the written cell. In Fig. 9, we repeated the experiment for an entire selected row (128 cells). The total drain current driven in conductive state (I_{ON}) by the cells corresponds to the I_{ON} of a single device multiplied by 128. To conclude in Fig. 10, one can observe both written and erased states, thus the programming windows, for multiple cell selection: 1, 128 and 4096 cells. One can notice that on larger memory block the I_{ON} depends on the driven current of single cell and on access resistances to contact each single bit. This shows the possibility to implement experimental protocols to analyze memory cells unproper electrical response depending on cell localization. This feature of our SuperCast structure is a real assess for electrical characterization lab, in order to speed up memory cell technologies development and qualification without long test development on costly ATE.

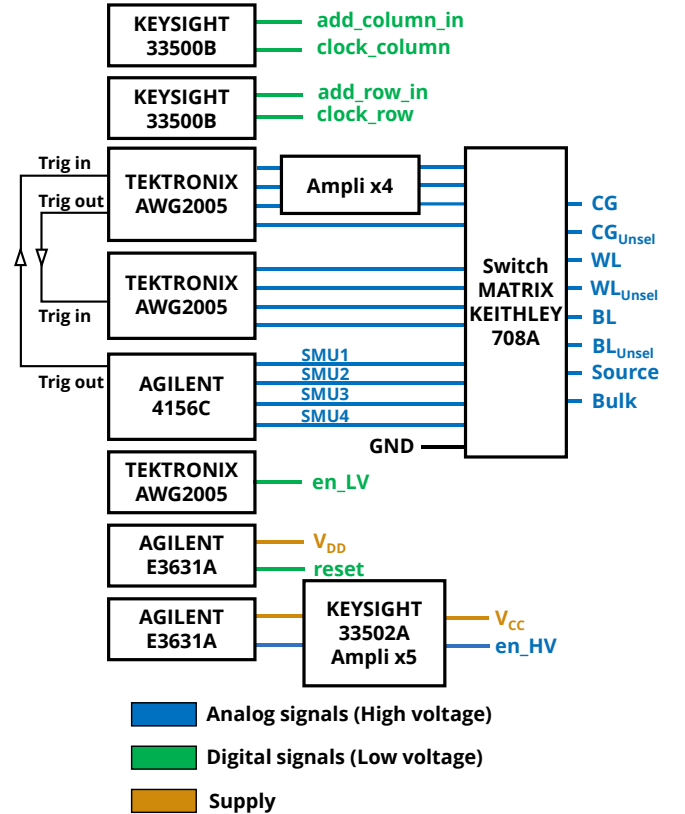


Fig. 7. Schematic of experimental setup.

V. CONCLUSIONS

In this work we designed and developed a new flexible addressable memory array called SuperCAST. We demonstrate the functioning of logic circuits to address the memory cells. The shift registers serially select the EEPROM devices par bit or blocs. Level shifters and pass-gates are used to pull up the voltage supply in the range suitable for EEPROM technology. These blocks can be adapted depending on the biasing values of the memory technology. We highlight the possibility to fit any embedded non-volatile memory technology with this kind of approach. This opens the opportunity to perform electrical characterizations and reliability tests on a large device population in a electrical characterization lab environment.

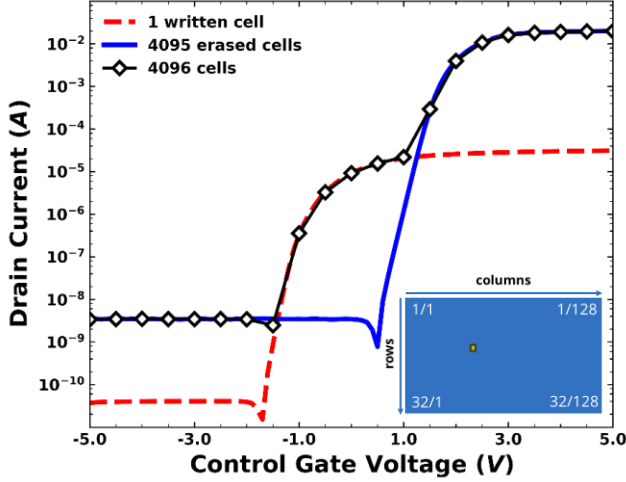


Fig. 8. Drain current versus gate voltage characteristic of one written cell compared to the rest of erased memory array and the whole block.

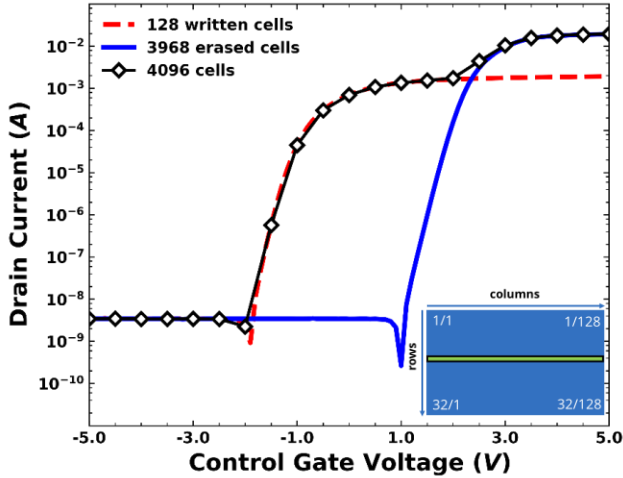


Fig. 9. Drain current versus gate voltage characteristic of 1 written row (128 cells) compared to the rest of erased memory array and the whole block.

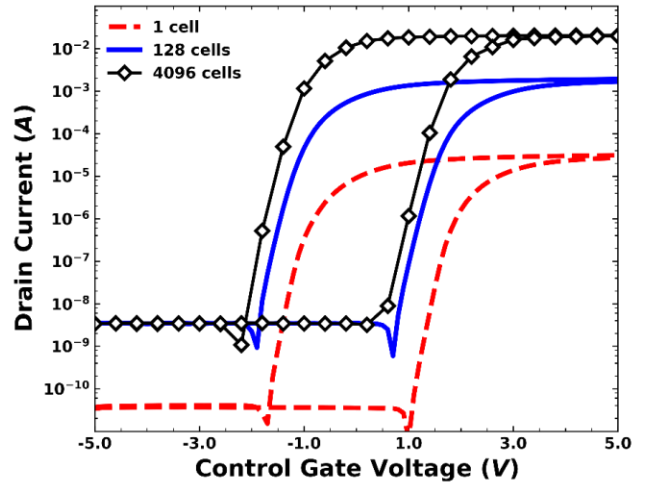


Fig. 10. Drain current versus gate voltage characteristic of multiple selection in written and erased state.

ACKNOWLEDGMENT

The authors gratefully acknowledge all manufacturing teams and TR&D of STMicroelectronics TR&D as well as all the memory team of IM2NP laboratory for the fruitful discussions and strong collaboration on this new SuperCAST structure.

REFERENCES

- [1] P. Cappelletti, R. Bez, D. Cantarelli, D. Nahmad, L. Ravazzi, "Cast: an electrical stress test to monitor single bit failures in flash-EEPROM structures," *Microelectronics. Reliability.*, vol. 37, no. 3, pp. 473-481, 1997.
- [2] R. Djenadi, G. Micolau, J. Postel-Pellerin, P. Chiquet, R. Laffont, J.-L. Ogier, A. Regnier, F. Lalande, J. Melkonian, "Data retention under gate stress on a NVM array," *Solid-State Electronics*, vol. 78, pp. 80-86, 2012.
- [3] F. Pio and E. Gomiero, "Select transistor modulated cell array structure test for EEPROM reliability," *Proc. of IEEE ICMTS 2000*, pp. 217-222.
- [4] P. Canet, J. Postel-Pellerin, J.L. Ogier, "Access resistor modelling for EEPROM's retention test vehicle," *Microelectronics Reliability*, vol. 53, no. 9-11, pp. 1218-1223, 2013.
- [5] C. Le Roux, L. Lopez, A. Firiti, J.L. Ogier, F. Lalande, R. Laffont, G. Micolau, "An experimental method allowing quantifying and localizing failed cells of an EEPROM CAST after a retention test", *Solid-State Electronics*, vol. 52, no. 10, pp. 1550-1554, 2008.
- [6] R. Djenadi, G. Micolau, J. Postel-Pellerin, R. Laffont, J. L. Ogier, F. Lalande, J. Melkonian, "An evaluation of the extrinsic cells number in a memory array using cross-correlation products and deconvolution: an instance of a microelectronics experimental inverse problem", *Inverse Problems in Science and Engineering*, vol. 19, no. 8, pp. 1043-1062, 2011.
- [7] T. Kempf, V. Della Marca, L. Baron, F. Maugain, F. La Rosa, S. Niel, A. Regnier, J.-M. Portal, P. Masson, "Threshold voltage bitmap analysis methodology: Application to a 512kB 40nm Flash memory test chip," In: *2018 IEEE International Reliability Physics Symposium*, pp. 6E.41-6E.48, 2018.