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Cirio

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# Efficiency improvement of an UWB rectifier by using optimized pulse modulation signal: simulation and experiments

Mahdi Hamidouche Univ Gustave Eiffel CNRS, ESYCOM F-77454 Marne-la-Vallée, France amine-mahdi.hamidouche@univeiffel.fr Hakim Takhedmit Univ Gustave Eiffel CNRS, ESYCOM F-77454 Marne-la-Vallée, France hakim.takhedmit@u-pem.fr Patrick Poulichet Univ Gustave Eiffel, ESIEE-Paris CNRS, ESYCOM F-77454 Marne-la-Vallée, France patrick.poulichet@esiee.fr

Laurent Cirio Univ Gustave Eiffel CNRS, ESYCOM F-77454 Marne-la-Vallée, France laurent.cirio@u-pem.fr

Abstract— This paper presents the contribution of RF pulse modulation signals on the efficiency improvement of an ultrawide band (UWB) rectifier based on the voltage doubler topology. Simulations and measurements show that the RF-to-DC conversion efficiency is improved compared to CW (Continuous Wave) signal, especially on high loads. It has also shown, for the same average RF power value, that the optimum duty cycle to achieve maximum efficiency decreases as the load increases. Furthermore, the influence of the modulation frequency is lower. Indeed, when the modulation frequency varies, the maximum efficiency varies only slightly. For an output load of 99 kΩ and an RF power of -20 dBm, a voltage gain of 8.5 dB, compared to a CW signal, is obtained by ADS simulation. This value is of 10 dB in measurement. The results also show that the optimum output load moves from 3  $k\Omega$  for a CW signal to more than 20  $k\Omega$  for a pulse modulated signal. This allows making more convenient impedance matching when powering wireless sensors. Indeed, the power requirements of wireless sensors for IoT for example are constantly decreasing while their input impedance tends to increase.

Keywords—Rectifier, UWB, Pulse modulation signal, Power conversion efficiency, Power optimized waveform, Wireless power transfer.

#### I. INTRODUCTION

Far-field wireless energy transfer is considered as a major area of research due to recent applications such as Internet of things (IoT), Smart cities, Wireless Sensor Networks (WSN) and implantable medical devices. Facing the necessity to satisfy the energy needs of smart circuits and sensors, the improvement of DC voltage and/or RF-to-DC conversion efficiency of rectifying circuits and more generally rectennas is presented as a key challenge in particular for low power levels. In order to rise it, and instead of focusing on the rectenna cell, one can take benefit from the transmission strategy by changing the excitation signal [1-2]. In [3-4], the authors present the impact of different waveforms on a series diode converter circuit using signals such as chaotic signal, white noise as well as OFDM and show that waveforms with high Peak to Average Power Ratio (PAPR) increase the RFto-DC conversion efficiency. In [5-8], multisine and RF pulsed signals are applied for the same purpose and show that when the number of sub-carriers increases for multisine signal, or when the duty cycle for RF pulsed signal varies, the RF-to-DC conversion efficiency can be significantly improved. In [9-10], multisine, Gaussian, and square waveforms are used to improve the tag sensitivity and increase the read-range and reliability of passive RFID tags.

Many of the works reported in the literature on POW (Power Optimized Waveform) for wireless energy transfer are investigative studies based on experiments. The objectives of the work carried out and presented in this paper is to develop a fast and sufficiently accurate simulation tool to characterize the contribution of specific excitation signals to the RF-to-DC conversion efficiency. More specifically, the aim is to evaluate the potential of the pulse modulation signal numerically before validation with measurements. In [11], the author shows via a theoretical and experimental development how to perform the output DC voltage and the efficiency of a CW signal on a 10 GHz and 30 GHz single-shunt rectennas. The same concept is taken up in [12] with multisine waveform on a 5.8 GHz single-shunt rectennas to evaluate the maximum output power and power conversion efficiency (PCE).

Even if the literature on waveform design provides useful information on the impact of POW on Wireless Power Transfer performance, one limitation concerns the absence of a formal tool to synthetize nonlinear circuits with total flexibility [13] on the excitation signal.

In this study, we have developed a simulation tool based on the Envelope Analysis simulator of Advanced Design System (ADS) software from Keysight Technologies, and a methodology for extracting the results and post-processing. This allows performing more simulations and making parametric studies in parallel thus optimizing the computation time. The simulated results are then compared to experiments for validation. The measurements were carried out by an automated measurement setup, built around a vector signal generator, and able to handle several waveforms, including the pulse modulated signal.

An ultra-wideband rectifier operating from 1.65 to 2.54 GHz [14] has been used in order to cover the spectrum of the pulse modulated waveform, especially for very low duty cycle values. The simulated and measured DC voltages and voltage gains are also characterized to evaluate the

improvement obtained by using a pulsed RF signal compared to a CW.

#### II. DESCRIPTION OF THE UWB RECTIFIER AND PULSE MODULATION RF SIGNAL

#### A. UWB Rectifier.

The UWB rectifier was designed and optimized to operate in a frequency range from 1.65 to 2.54 GHz, which cover the GSM, UMTS, Wi-Fi and LTE2100/4G frequency bands. It is based on a voltage doubler topology, Skyworks SMS7630-079LF Schottky diode is chosen for its low threshold voltage which makes it suitable for low input RF power levels.



Fig.1. Generic circuit layout of the UWB rectifier with the picture of the fabricated prototype. Parameters are:  $W_1 = 2.2$  mm,  $W_2 = 9.4$  mm,  $W_3 = 5.5$  mm,  $W_4 = 12.8$  mm,  $W_5 = 2.2$  mm,  $W_6 = 11$  mm,  $W_7 = 1.8$  mm,  $W_8 = 8.2$  mm,  $W_9 = 3.4$  mm,  $L_1 = 2.6$  mm,  $L_2 = 6.6$  mm,  $L_3 = 21.1$  mm,  $L_4 = 11.4$  mm,  $L_5 = 8.2$  mm,  $L_6 = 2.4$  mm,  $L_7 = 20.6$  mm,  $L_8 = 8.2$  mm,  $C_1 = C_2 = 100$  pF,  $R_L = 3$  k $\Omega$ .

Figure 1 shows the rectifier layout and the fabricated prototype. It is designed and optimized with ADS software, by using Harmonic Balance circuit simulation. The prototype in microstrip technology is printed on a 1.6 mm thick FR-4 substrate with  $\varepsilon_r = 4.3$  and  $\tan \delta = 0.02$ . The circuit is optimized to operate around -15 dBm RF input power and shows an optimum load resistance of about 3 k $\Omega$ .

The measured and simulated DC output voltages as a function of frequency and for different input power levels (-20, -10 and 0 dBm) are depicted in Figure 2. This is a characterization using a CW as input signal and the output load is optimized at 3 k $\Omega$ . At 0 dBm power, the maximum simulated power conversion efficiency (PCE) is about 40%. The bandwidth of the rectifier at half-power (or halfefficiency) is found to be 890 MHz, from 1.65 to 2.54 GHz. The fractional bandwidth is about 42%. The measured curves have the same shape as those obtained by simulation. Nevertheless, some differences can be noticed between them. This is mainly due to the performed simulation approach. Indeed, as the number of simulations to be performed is high, especially those of the pulse modulation signal, Harmonic Balance circuit simulation has been adopted to decrease the computational time. This simulation approach, unlike an electromagnetic/circuit co-simulation (Momentum/Harmonic Balance for example), does not take into account the interactions and couplings between the different parts of the rectifier, such as the transmission lines. The manufacturing tolerances, the Schottky diodes losses and the parasitic effects of the SMD components are also additional sources of error that increase the discrepancy between the simulation and measurement.



Fig.2. Measured and simulated output DC voltage as a function of frequency for different RF power levels ( $R_L$ =3 k $\Omega$ ).

#### B. Pulsed RF signal.

The pulse modulation RF signal consists of a carrier signal with a frequency  $f_c$  modulated by a square signal of frequency  $f_m$  with a duty cycle  $\beta$ . In one period of the modulated signal, the time during which the pulse is turned on is called T<sub>on</sub>. The duty cycle is then calculated by the following formula:

$$\beta(\%) = 100 \frac{T_{on}}{T_m} \tag{1}$$

Where  $T_m$  is the period of the modulated signal.

Figure 3 shows a pulsed RF signal with a duty cycle of 5%, a carrier frequency of 2.45 GHz and a modulation frequency of 1 MHz. It is assumed that the average power remains constant. As the duty cycle decreases, the peak power increases because the total energy over a period is focused on a shorter time period.

The peak power is defined by the following formula:

$$P_{peak} = 200 \frac{\langle P \rangle}{\beta(\%)} \tag{2}$$

Where *<*P> is the average signal power.



Fig.3. Pulse modulation RF signal with  $f_{\rm m} = 1$  MHz,  $f_{\rm c} = 2.45$  GHz and  $\beta = 5\%$  (time and frequency domains).

#### **III. SIMULATION AND MEASUREMENT**

#### A. ADS simulation.

The numerical simulation is performed under the ADS software and using envelope analysis method. The envelope of the signal is first generated using a Matlab code that has been developed, for different duty cycle values ranging from 2 to 20 % with a step of 2 and then ranging from 30 to 100 % with a step of 10. Several modulation frequencies were also used: 100 kHz, 1 MHz and finally 10 MHz. The resistance load ranges from 0.5 to 99 k $\Omega$ . The data files are then imported into ADS and an envelope analysis simulation is performed to characterize the DC output of the circuit as a function of the duty cycle and as a function of the modulation frequency, for different RF power levels and load values. To optimize the computation time and the convergence to the steady state, the envelope parameters such as the sampling frequency and the number of periods are optimized. The sampling frequency needs to be sufficiently high to obtain sufficient non-zero samples at the lowest duty cycle value being considered (2% in this work). The number of periods of the modulated signal needs also to be high enough to reach the steady state for the largest load value being considered (99 k $\Omega$  in this work).

#### B. Measurement setup description.

The measurement setup (Figures 4 and 5) used for the experimental characterization is automated and controlled using a MATLAB program. The signal generator (Keysight N5182A) receives the command from the control station and compares the output power with that measured by the power meter (Keysight E4419A) to calibrate, and then set the correct value of power at the input of the rectifying circuit. After fixing the value of the load via a programmable resistor (Transmille 2090), the multimeter (Agilent 34401A) measures the DC voltage and sends the data to the control station after each measurement. The control program generates a CW signal as a carrier signal modulated by a square pulsed wave signal. For each load value, the duty cycle is swept from 2 to 100 % by a step of 2 in order to evaluate the optimum duty cycle as a function of the output load.



Fig.4. Schematic of the measurement setup.



#### Fig.5. Measurement setup.

#### C. Simulation and experimental results.

Figure 6 represents the simulated and measured optimum duty cycle as a function of the load for different input power levels: -20, -15 and -10 dBm. The simulated and measured results are close and show that the optimum duty cycle decreases when the load resistance increases.



Fig.6. Simulated and measured optimum duty cycle versus output load resistance for different power levels.

Indeed, the DC output voltage increases when the duty cycle decreases since the input voltage, when the pulse is turned-on, increases. It should be mentioned that the average power remains constant, which means that the energy consumption is the same for all duty cycle values and also for the CW signal. This is particularly the case if the pulse width is sufficient to charge the capacitor to its maximum voltage. Otherwise, the capacitor will not be able to charge to its maximum voltage and the optimum duty cycle value will be shifted to higher values. Also, when the output load decreases, the capacitor will discharge more rapidly and the voltage ripple will consequently increase. This is why the optimum duty cycle decreases as the output load increases.

Furthermore, for low input power levels and in the CW regime, the voltage across the diode is often small or comparable to the threshold voltage of Schottky diodes. This increases losses and therefore strongly limits efficiency. The pulse signal brings higher input voltages, much higher than the threshold voltage of Schottky diodes. This allows higher conduction of the diodes and therefore a more efficiency.

One should then, depending on the load value, optimize the duty cycle of the pulsed RF signal in order to reach the optimum efficiency shown in Figures 7 and 8 as the results indicate the presence of an optimum load value/duty cycle for which the efficiency is maximized.

The power conversion efficiency (PCE) of the rectifier is defined as follow:

$$\eta_{RF-DC} = \frac{P_{DC}}{P_{RF}} = \frac{V_{DC}^2}{P_{RF}R_L}$$
(3)

Where  $P_{RF}$  is here the RF input power,  $P_{DC}$  the power defined at the output of the rectifier and  $V_{DC}$ , the DC voltage at the output of the rectifier across the load resistance  $R_L$ .



Fig.7. Simulated optimum efficiency under CW and RF pulse signal.



Fig.8. Measured optimum efficiency under CW and RF pulse signal.

The measurement results are in good agreement with the simulation in terms of the shape of the curves and the optimal loads, despite some value differences. The error between the measured and simulated curves, as explained above, is essentially due to the simulation approach that was chosen in order to optimize the computational time. In addition, there are manufacturing tolerances, losses in the Schottky diodes and parasitic elements in the SMD components that contribute to the error between measured and simulated curves.

At an input power equal to -15 dBm, a measured efficiency of almost 15 % for an optimum load value of 20 k $\Omega$  and a duty cycle of 4 % is reached. Also, the optimum duty cycle tends to increase while increasing the input power level for low load values.

Figure 9 shows the simulated DC output voltage and voltage gain as a function of output load and for different power levels (-20 and -15 dBm). The voltage gain is defined in this work as the ratio between the DC voltages obtained for a pulse signal and a CW signal, respectively.

$$G_P = 20 \log \frac{V_{DC_Pulse}}{V_{DC_CW}} = 10 \log \frac{\eta_{Pulse}}{\eta_{CW}}$$
(4)

Where  $V_{DC\_Pulse}$  and  $\eta_{Pulse}$  are respectively the DC output voltage and efficiency for the pulse RF signal,  $V_{DC\_CW}$  and  $\eta_{CW}$ , the DC output voltage and efficiency for the CW signal.

The DC voltage increases when the output load increases. More than 8 dB voltage gain is obtained at -20 dBm input power and 99 k $\Omega$  output load. At -15 dBm, this value is about 10 dB.



Fig.9. Simulated output DC voltage (A) and voltage gain (B) as a function of load resistance at -20 and -15 dBm.

Figure 10 depicts the measured DC output voltage and voltage gain as a function of output load and for different power levels (-20 and -15 dBm). The measured curves are in good agreement with simulation. The maximum measured voltage gain is about 10 dB for both power levels obtained at 99 k $\Omega$ .



Fig.10. Measured output DC voltage (A) and voltage gain (B) as a function of load resistance at -20 and -15 dBm.

#### **IV. CONCLUSION**

This paper addresses the issue of improving the performance of far-field energy transfer devices by optimizing the transmitted waveform. The main focus is made on the RF pulse modulation waveform, where an efficient simulation tool based on ADS coupled with Matlab to generate the input pulsed signal and perform parametric studies is presented. An ultra-wideband rectifier operating from 1.65 to 2.54 GHz is used so as to match low duty cycle values. The results were compared to those of a CW signal for low and high load values with an optimum output load moving from 3 k $\Omega$  for a CW signal to more than 20 k $\Omega$  for a pulse modulated signal. For an input power of -15dBm, the efficiency reaches almost 15% for a pulsed RF signal with an optimum duty cycle of 4%, against 8% of efficiency for a CW. For an input power of -20 dBm, the simulated and measured gain is improved up to respectively 8.5 dB and 10 dB for 99 k $\Omega$  load value and with an optimum duty cycle of 2 %. For both input power results, the carrier frequency was set at 2.45 GHz and the modulation frequency at 1 MHz.

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