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Preconditioning of p-GaN power HEMT for reproducible V_{th} measurements

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Abstract

In reliability studies, the instability of the threshold voltage (V_{th}) is problematic when V_{th} is used as an indicator as it totally blurs an eventual drift due to real device aging. This instability is observed during electric characterization measurements and is related to the “biasing history” of the transistor which can introduce carrier trapping/detrapping in different layers of the structure. New methods are therefore required to overcome this trapping related instability issues in order to accurately monitor device aging. To solve the repeatability issue of threshold voltage measurement, we investigated its instability on GaN transistors. A preconditioning step applied right before the actual V_{th} measurement was studied. The proposed preconditioning method is based on the application of a dedicated $V_{GS}(t)$ biasing on the gate terminal which leads to a stable and repeatable value of V_{th} . The mechanisms enabling the observed stability of V_{th} are identified through the analysis of the drain leakage measurement after the preconditioned V_{th} measurement. It demonstrates the role of hole injection into the structure. The preconditioned- V_{th} measurement method is proposed as a complementary measurement to correctly follow the ageing of pGaN HEMT in future reliability studies.

Keywords:

Schottky p-GaN transistors, preconditioning protocol, reliability, threshold voltage shift, trapping

1. Introduction

Monitoring of electrical characteristics is often used to follow transistor degradation in reliability studies. However, in AlGaIn/GaN High Electron Mobility Transistors (HEMTs), measurements are often not reproducible and could vary depending on the previous-operation history which blurs the shift related to the degradation of the transistor. In particular, the V_{th} instability has been observed [1].

Nevertheless, reproducible characterization measurements are mandatory to study irreversible degradation and drift of electrical parameters of transistors.

We studied a preconditioning step before the V_{th} measurement to stabilize it and make it perfectly reproducible. Some preconditioning methods have been proposed for SiC devices [2-4]. Preconditioning for GaN devices is very new and seems to be only reported in the recent work of A. Deb [4]. Compared to the work proposed here, it adopts a more experimental view with limited physical explanations and presents preconditioning steps with different gate-voltage-pulse amplitudes and time durations than the one described in this paper.

To identify mechanisms that occurred during the proposed preconditioning step, additional measurements were done post preconditioned V_{th} measurements.

Section 2 illustrates the instability of the threshold voltage and presents the experimental setup. The gate preconditioning protocol is explained in details in section 3. Section 4 is about the observations on the drain leakage after the preconditioning

and the physical mechanisms that ensure the stability of the preconditioned V_{th} value.

2. Experimental details

The main device under test (DUT) is a commercial, 100V, 90A, 7m Ω packaged p-GaN gate AlGaIn/GaN HEMT. The same protocol was also applied on a 650V, 30A, 50m Ω device from the same manufacturer.

In our setup, the threshold voltage (V_{th}) is measured by ramping up gate and drain voltages simultaneously (The measurement thus behaves as if the drain and gate terminals were shorted together.). V_{th} value has been chosen as the gate voltage value when the drain current I_D equals 400mA. This value is high enough to be on the linear part of the curves of Fig.2 (a) and to measure the drift precisely. As the duration of the V_{th} measurement is very short (well below the second), the measured value is not significantly influenced by the self-heating effect.

Like in [1] and [5] we observed that the threshold voltage is unstable depending on the history of the device. For instance, V_{th} will be shifted positively, up to 40% after drain leakage measurement $I_{dss} = f(V_{DS})$ at $V_{GS} = 0V$ because of the high voltage and the high electric field Fig.2 (b).

This positive shift (increase of V_{th}) is ascribed to two distinct mechanisms according to [6]. One of them is an electron trapping mechanism at the AlGaIn/GaN interface caused by the 100V applied on the drain at the OFF-state during the I_{dss} measurement. The trapped electrons do not have the time to be released before the threshold voltage measurement that

follows the I_{dss} measurement (10 to 20 min are needed to retrieve the initial value of V_{th}). The other one appears when the leakage current of the Schottky diode D_{Sch} (represented on Fig.1) is high enough to polarize and switch on the pin diode D_{pin} . A hole current, limited by D_{Sch} , can go through the gate stack and the barrier to the buffer. The displacement of the positive charges (holes) that were partially in the P-GaN makes the charges within the P-GaN layer dominated by electrons. The hole current leaves a net negative charge within the P-GaN layer under the gate.

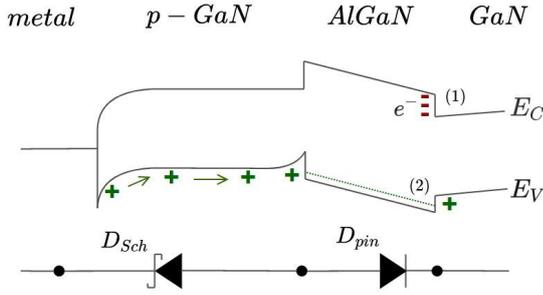


Fig. 1. Simplified band diagram of the gate stack of the DUT, the mechanism (1) is electron trapping at the interface AlGaIn/GaN, (2) is the hole depletion over the barrier to reach the buffer.

The two mechanisms increase the electrical potential necessary to activate the two-dimensional electron gas (2DEG) in the channel i.e. increase V_{th} . Even if the shift observed is fully recoverable, it makes the monitoring of the transistor degradation based on the monitoring of its electrical-characteristics drift very challenging.

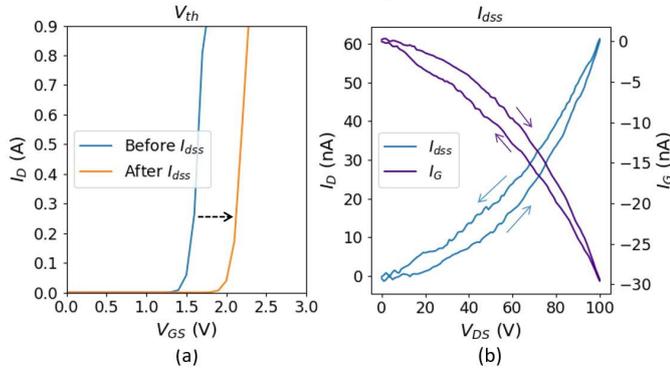


Fig. 2. (a) Observation of the instability of the threshold-voltage measurement after an I_{dss} measurement with V_{dss} up to 100V (b) Measurement of the current leakage at $V_{GS}=0V$ of the transistor during the I_{dss} that causes the shift of V_{th} of (a) (forward and backward sweeps pointed by the arrows). All measurements were done at room temperature 20°C. The sweep rate is 33V/s.

3. Preconditioning of the gate of the DUT

The preconditioning is applied right before the threshold voltage measurement using the *direct control* mode of the used power device analyzer and curve tracer (Keysight B1505A). Therefore, the time between the preconditioning step and the threshold voltage measurement is controlled precisely.

The preconditioning consists on applying a positive voltage to the gate during a few seconds. This time affects the stability

of the measurement and could be minimized with further future studies but should be taken long enough to saturate the phenomena and to obtain a repeatable result on V_{th} value. Indeed, this duration must be sufficient compared to the time constant of the involved physical mechanism and in order to reach the saturation of the trapped charge density detailed later. We have not yet found other studies about this saturation.

Immediately after this preconditioning step the V_{th} measurement is carried out by increasing V_{GS} and V_{DS} simultaneously (Fig.3).

In order to test the V_{th} measurement reproducibility and its independence from the biasing history of the device, a preconditioned- V_{th} measurement following an I_{dss} measurement was done in the same way the non-preconditioned- V_{th} was measured in Fig.2. It is striking that the preconditioned- V_{th} measurement is essentially reproducible and not affected by the history (Fig.4). This was observed on all of the sixteen devices tested on this part number. To evaluate the robustness of the proposed preconditioning, this process was repeated successfully with other biasing conditions, besides I_{dss} measurement (biasing on the gate and the drain without exceeding the manufacturer's limits given in the datasheet).

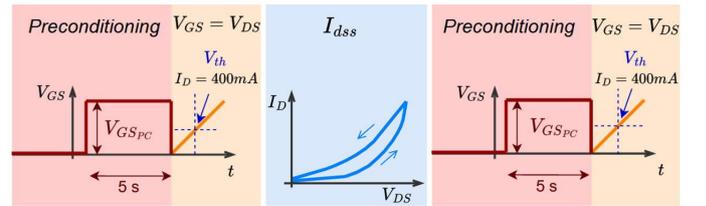


Fig. 3. Protocol used in measurements on the test system: first in red the gate preconditioning step to obtain reproducible values of V_{th} , then in orange the actual V_{th} measurement, in blue another measurement (e.g. I_{dss} on the figure) that could influence the measurement of the threshold voltage.

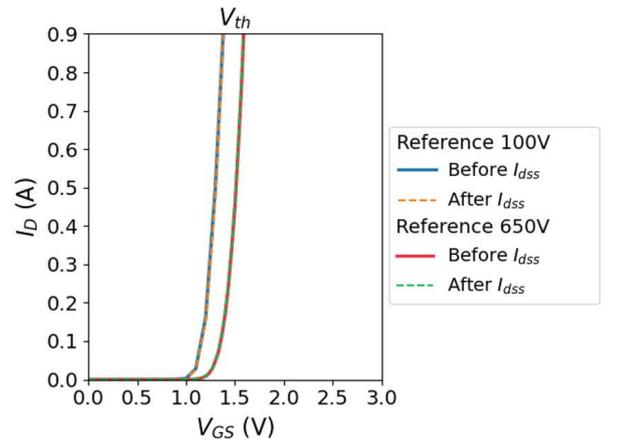


Fig. 4. Preconditioned- V_{th} measurement (at $V_{GS,PC}=7V$) before and after an I_{dss} measurement for a 100V and a 650V pGaN HEMT.

The preconditioned- V_{th} measurement is recoverable and repeatable (Fig.4 (a)). The two values obtained for the threshold voltage differ by less than 0.1% ($\approx 1mV$). V_{th} is then only affected by the preconditioning step, it allows to do the measurement of a steady value of V_{th} . This value varies

depending on the preconditioning voltage $V_{GS,PC}$. It increases for $V_{GS,PC}$ between 1 and 4V and decreases for $V_{GS,PC}$ between 4 and 7V (Fig.6). The reasons this evolution are explained in the last paragraph of section 3. Such influence of the gate forward bias on V_{th} shift has also been observed in [7-9] on transistors with similar structures.

It has to be underlined that only the highest values of $V_{GS,PC}$ ($>5V$) lead to a stable, repeatable and bias-history independent preconditioned- V_{th} as shown in Fig.5. Therefore, it could be advised to select the highest V_{GS} value allowed. For the tested device the value $V_{GS,PC} = 7V$ allows obtaining a reproducible measurement of the threshold voltage. This value should not degrade the device nor affects its performances since it fits in the limits recommended by the manufacturer (V_{GS} in the range $[-10V; +7V]$ in DC mode) and no shift of the preconditioned value of the threshold voltage $V_{th,PC}$ has been observed.

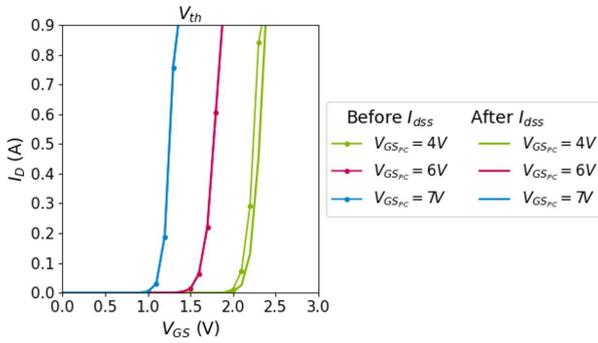


Fig. 5. Measurements of the threshold voltage before (solid lines with dots) and after (solid lines) an I_{dss} measurement. The curve for the preconditioning of 6 and 7V are the only ones that give precisely the same value of V_{th} as the curves after and before I_{dss} for these two preconditioning values. For smaller preconditioning values, such as $V_{GS,PC} = 4V$, it can be seen that I_{dss} measurement influences the value of V_{th} .

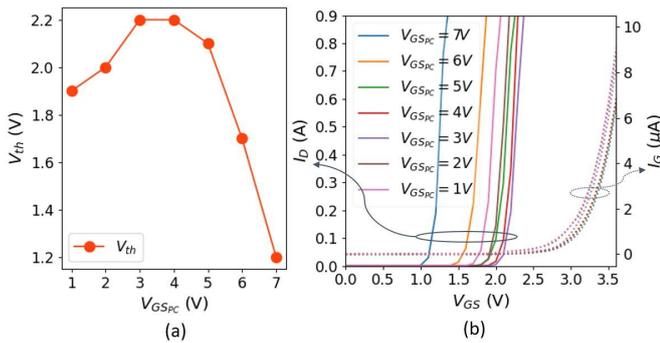


Fig. 6. Effect of the voltage applied during the preconditioning step on the measurement of the threshold voltage (all measurements are made after a leakage current I_{dss} measurement).

On Fig.6 the positive shift for ($V_{th} < V_{GS,PC} < 4V$) can be explained by the injection of electrons from the 2DEG to the AlGaIn layer that occurs when there are enough electrons in the channel (mechanism (1) on Fig.1) [9]. The negative shift (V_{th} decreases) is observed for $V_{GS,PC} \geq 4V$ i.e. when the gate stack starts conducting at $V_{GS} = 3V$ (voltage threshold of D_{pin}) see Fig.6 (b). From this voltage, holes start to flow through the

AlGaIn, this mechanism provokes hole trapping in the AlGaIn and in the GaN buffer (Fig. 1(2))[7-8][10].

4. Drain leakage current after preconditioning.

4.1. Observations

The leakage current curve in between the two measurements of V_{th} on Fig.4 (a) is visible on Fig.7. In comparison with “normal” I_{dss} measurement (Fig.2 (b)), two changes can be observed due to the preconditioning: the average current I_D is three orders of magnitude larger than before (comparison of drain current reached at 100V for $V_{GS,PC} = 7V$ compared to $V_{GS,PC} \leq 3V$), and a spike of 7 μA occurs in the first 20 sec that adds up to the existing drain leakage current. The excess current disappears after the I_{dss} measurement is done, i.e. another following I_{dss} measurement gives a “normal” curve (Fig.2 (b)).

The drain currents for different values of $V_{GS,PC}$ are represented on the Fig.9 (a). Here the sweeping time is shorter than in the previous measurement (33V/s against 3V/s before) as shown on the Fig.9 (b). Therefore, the “spike” of current is not entirely evacuated during the forward sweep (upper line of each color on the graph). The increase in the average current is visible starting at $V_{GS,PC} = 5V$, like the current spike, which corresponds to the hole injection threshold during the preconditioning step.

The bell shape of the spike is influenced by the structure of the HEMT part number especially its field plates layout. The field plates of the structure influence the evolution of the leakage current-path resistance R during the I_{dss} measurement. At OFF state the spreading of the 2DEG in the region between gate and drain (D_{2DEG^x}) depends on the voltage V_{DS} . As V_{DS} increases the 2DEG will be depleted progressively between the gate and the drain which extends the blocking surface $S_{blocking}$, therefore the path resistance R increases with V_{DS} .

The increase of $S_{blocking}$ also reduces the capacitance value C_{DS} . The C_{DS} evolution regarding V_{DS} is often given by the manufacturer and visible on Fig.10. The depletion of the 2DEG at OFF state can then be deduced. Indeed, when the 2DEG surface varies, the size of the electrode of the equivalent capacitance varies which affects the capacitance.

At OFF-state, the blocking region is under the p-GaN only for $V_{DS} = 0V$. On Fig.11 it is the uncolored region of the 2DEG with the associated path resistance of R_{0V} .

As V_{DS} increases between 0V and 18V the 2DEG is depleted progressively under the field plate: D_{2DEG^x} increases in the pink region on Fig.11. The path resistance seen by I_{dss} increases up to $R_{0V} + R_{0V < V_{dss} < 18V}$ at $V_{DS} = 18V$. At this point, the maximum of the spike current is reached due to the strong increase of the leakage path resistance related to the polarized field plate that acts like a negatively polarized gate.

As V_{DS} continues to increase, the relative “negative polarization” of the field plate reaches a threshold value that depends on the thickness of the AlGaIn barrier and the thickness of the isolating layer around the gate stack (“e” in Fig.11), which continues to depletes the 2DEG.

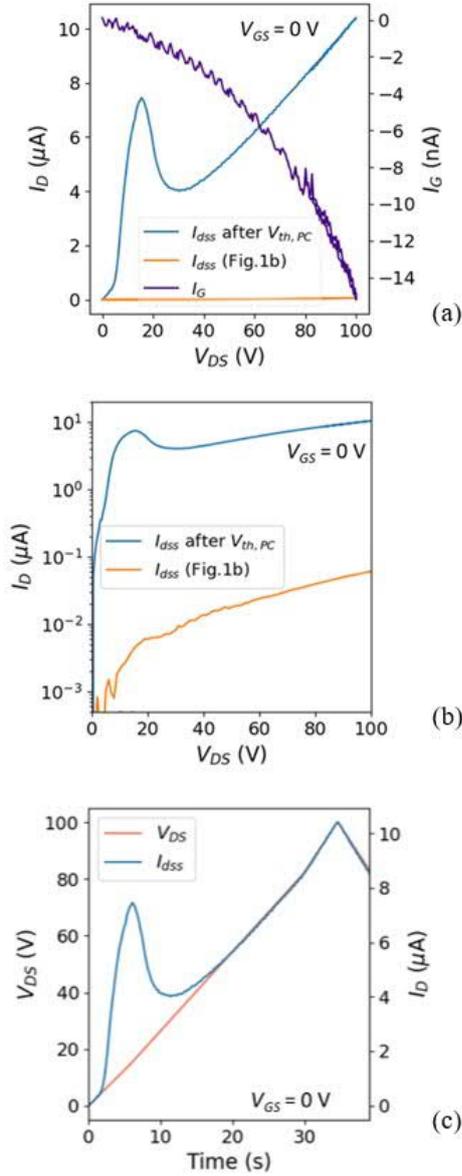


Fig. 7. (a) Drain leakage-current measurement (with slower and constant increase of $V_{DS} \approx 3V/s$) after a preconditioned- V_{th} measurement ($V_{GS,PC} = 7V$), (log scale on (b)), to be compared with Fig.2 (b) in orange. The overall level of drain current has increased abnormally (three orders of magnitude) and a current spike appears at the beginning of the measurement and lasts approximately 20 sec.

The following decreasing exponential form on Fig.7 between 18 and 40V shows that there are still charges to evacuate. Above 18V the 2DEG continues to be depleted in the yellow region (slower than with a field plate) which increases the path resistance with the increase of $R_{V_{dss} > 18V}$. The yellow part of the 2DEG on the Fig.11 is fully depleted when C_{oss} is constant (above 100V).

The following simplified formula as well as Fig.11 describe this resistance evolution (ΔR) as a function of $S_{blocking}$ knowing

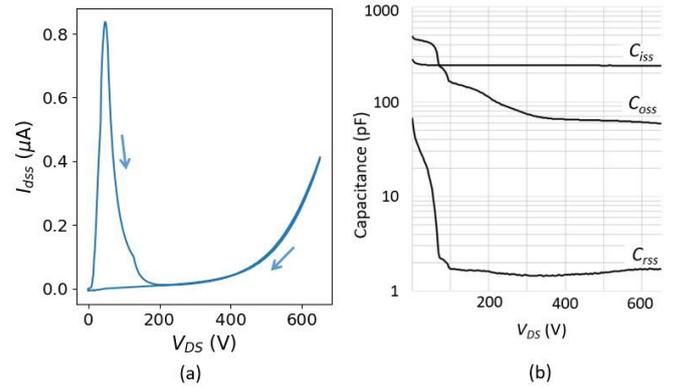


Fig. 8. (a) Drain leakage-current measurement after a preconditioned- V_{th} measurement ($V_{GS,PC} = 7V$) for the 650V part number. A current spike appears similarly as with the 100V part number the maximum is reached at $V_{DS} \approx 100V$. Another change near 150V (less pronounced) appears due to the different field plates layout of this part number. (b) Intrinsic capacitance at $V_{GS} = 0V$ of the transistor under V_{DS} given by the transistor datasheet. The field plates layout is more elaborated for this part number which influences the capacitance variation with V_{DS} .

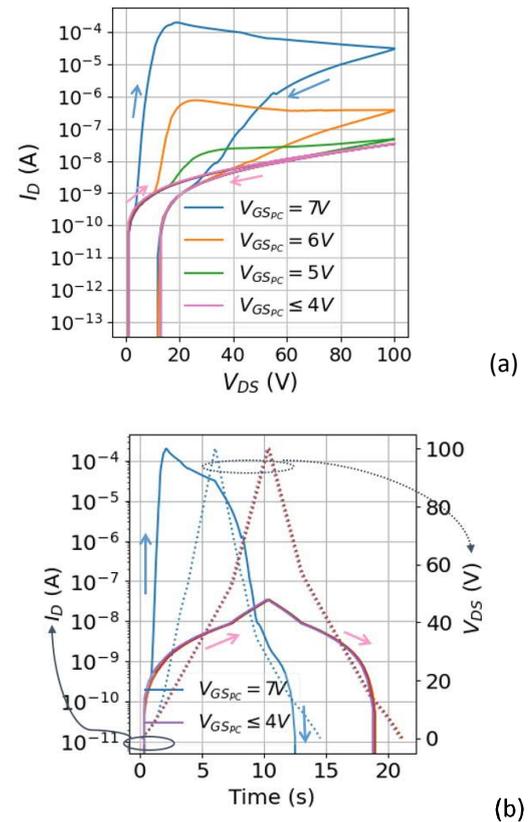


Fig. 9. Drain leakage current for several values of preconditioning gate voltage applied before, (a) as function of the drain voltage applied, (b) evolution over time of the drain voltage and current. As the sweeping is faster than in Fig.7 (33V/s against 3V/s), the additional current leakage spike does not have enough time to be evacuated only on the forward sweep phase. The additional current of the spike is evacuated more rapidly during the measurement with faster sweeping ($\approx 12s$ against 20s in Fig.7), since the charge to be evacuated is the same for the same $V_{GS,PC}$, the maximum current reached is higher at faster sweeping rates.

the evolution of the simplified equivalent capacitance C_{DS} of the transistor given in Fig.10 and illustrated in Fig.11:

$$\Delta C_{DS} = \frac{\epsilon \times (S - S_{blocking})}{e} \propto -\Delta R \quad (1)$$

Where e is its thickness (AlGaIn barrier and isolating layer illustrated on Fig.11), ϵ the equivalent permittivity of the equivalent capacitor, S the surface where the 2DEG can be formed and $S_{blocking}$ is the blocking surface of the drain current at a given V_{DS} . $S - S_{blocking}$ can be modeled as follow:

$$S - S_{blocking} = D_{tr_z} D_{tr_x} - D_{tr_z} D_{2DEG_x} \quad (2)$$

Where D_{tr_z} is the length of the transistor on z-axis and D_{tr_x} is the space between the drain and the source electrode at AlGaIn/GaN interface. $D_{tr_z} D_{tr_x}$ is therefore the surface where the 2DEG can be formed. D_{2DEG_x} is the spreading of the depletion of the 2DEG on x-axis that depends on V_{DS} .

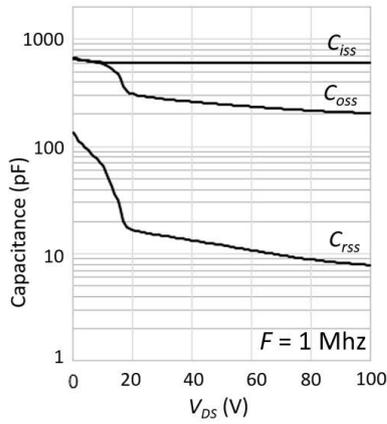


Fig. 10. Intrinsic capacitances at $V_{GS} = 0V$ of the transistor under V_{DS} given by the transistor datasheet.

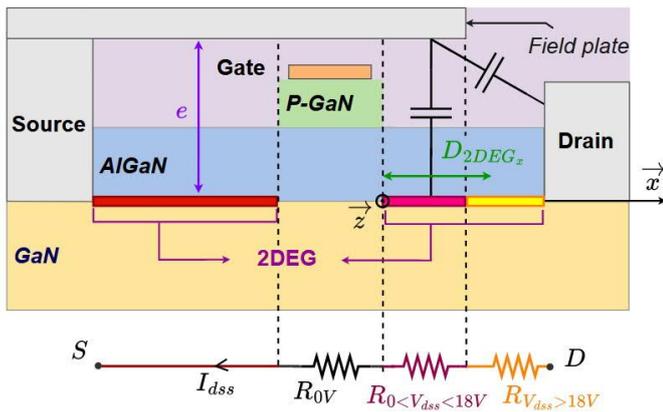


Fig. 11. Simplified view of the transistor and its 2D electron gas location for a given $V_{DS} = V_{dss}$. The equivalent model of the resistance path is illustrated below. The pink (R_{0V}) and the yellow ($R_{0<V_{dss}<18V}$) resistance are varying, R_{0V} is constant at OFF-state.

For other part numbers of pGaN HEMT the spreading of the 2DEG will be affected in the same way by V_{DS} . As 600V pGaN HEMT have a different field plate structure with additional field plates, the 2DEG will be depleted with more sections. Each plate border adds a curvature on the curve $C_{DS} = f(V_{DS})$ and adds

a virtual gate threshold that depletes the 2DEG beneath at a given V_{DS} at OFF-state.

4.2. Physical explanation

The impact of V_{GSPC} on I_{dss} shows that hole injection in a sufficient amount allows to reach saturation and is responsible for both the success of the preconditioning and the consequences on the leakage current post preconditioned- V_{th} measurement.

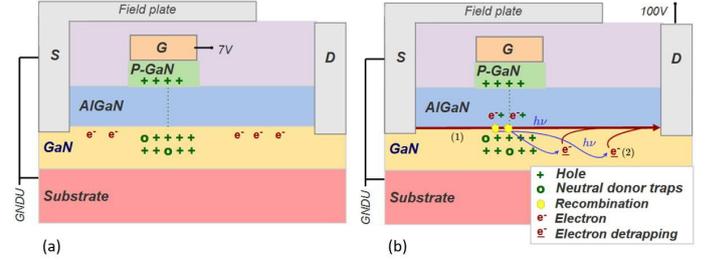


Fig. 12. (a) Illustration of the injected holes due to the application of a high V_{GSPC} , (b) effect on the leakage current, the thick reddish arrow illustrates a high leakage flow of electron, the yellow clouds show recombination processes that emit electrons of energy $h\nu$ that release trapped electron from the buffer and that participate in the increase of the leakage current.

During the preconditioning step at $V_{GSPC} = 7V$, the holes reach the buffer under the gate region, see Fig.12 (a). This hole injection lowers V_{th} and affects the drain-source blocking capability at OFF-state of the transistor under voltage which results in a larger drain leakage current during the following I_{dss} measurement ($V_{GS} = 0V$ and $V_{DS} = 100V$)[11-12]. Therefore, this phenomenon, that reduces the threshold voltage V_{th} , is also responsible for the increase of the average leakage current (the order of magnitude of I_{dss} is μA compared to nA without this phenomenon).

The additional current that appears at the beginning of the measurement (Fig.7) might be explained by the recombination of electron-hole pairs, this recombination would emit a photon that will ionize electrons deeply trapped in the buffer as illustrated in Fig.12 (b). These electrons are in the GaN buffer independently from the preconditioning and are a consequence of the quality of the buffer layer [13]. Those will be released in the channel creating the observed current spike. This phenomenon is related to persistent photo-conductivity [10]. The same increase in the leakage current amplitude with similar duration until equilibrium (approximately 30 sec) was also observed in [14-15] for a transistor from the same manufacturer. The measurement of this spike is an indicator of the quality of the buffer layer of a transistor and could be studied in other future work.

5. Conclusion

By adding a preconditioning step right before the threshold voltage measurement, it is possible to obtain reproducible V_{th} measurements.

During this preconditioning step we demonstrate that the gate needs to be forward biased above V_{th} close to the highest V_{GS} value admissible and long enough to saturate the negative

shift of the threshold voltage related to hole injection into the buffer (Fig. 8).

The phenomena observed on the leakage current measurement (I_{dss}) after the preconditioned threshold voltage measurement confirms that hole injection is the mechanism responsible for the preconditioned state that gives a stable value of V_{th} . The increase in the static leakage I_{dss} current after the preconditioned V_{th} measurement in the OFF-state and the additional flow of electrons in the leakage current is a direct consequence of the presence of holes coming from the preconditioning sequence. The preconditioning method is currently tested to follow the ageing of devices and shows encouraging results.

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