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Design and characterization of a novel 3.3 kV 4H-SiC JFET

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Abstract. This paper presents the methodology for the design of a novel 4H-SiC JFET structure able to sustain 3.3 kV. Comparisons between simulation and characterization res will be made. Taken into account the process limitation, we will also discuss the critical steps and their impact on the electrical characteristics. A design methodology based on Baliga's criterion is proposed to obtain the optimal structure. A 50 nm thick thermal oxide grown above vertical channel and the use of a buried p^+ layer as second gate electrode are brand new in front of what is found in literature.

Introduction

In the context of more electrical transports, mechanical devices tend to be replaced by their smaller electrical counterparts. However the device itself must support harsh environment and electrical constraints (high voltage, high temperature) thus making existing silicon devices inappropriate. Silicon Carbide (SiC) is today's favorite candidate for the fabrication of devices able to sustain high voltage with a high integration level. Thanks to its 3.3 eV wide band gap energy and its $2.5 \text{ MV}\cdot\text{cm}^{-1}$ high critical field, 4H-SiC allows to design a 3.3 kV Junction Field Effect Transistor (JFET).

A study of a single vertical channel structure leads us to conclude that this structure is not the best for the high voltage we have to sustain. Structures with a buried implanted p^+ area add a lateral channel to the vertical channel are more suitable to reach high voltage. The vertical channel still exists between an aperture in the p^+ area.

Such a structure depends of many parameters, that need to be optimized. Since the influence of the variation of each parameter could not be isolated, we tried to find mathematical methods to emphase optimal values leading to set an optimization criterion, inspired from Baliga's works [1].

Limitations of single channel JFET

Fig. 1 shows the cross-section of a single channel vertical JFET designed by Semisouth in 2006. The main benefit of this structure is its low on-state resistance (about $2.86 \text{ m}\Omega\cdot\text{cm}^2$) [2]. So it enables high current levels with a low rise of temperature. Moreover it is easy to make a normally-off device with such a structure by narrowing the channel width. Nonetheless our

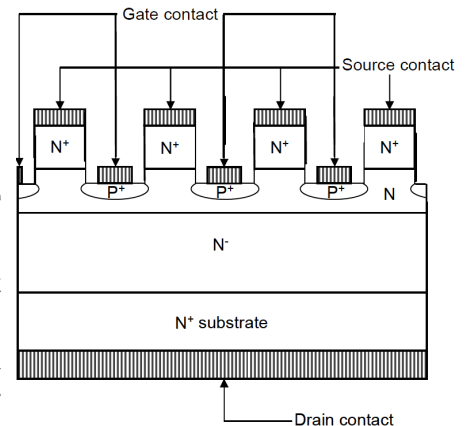


Fig. 1: Cross-section of a single channel vertical JFET [2]

simulation results show an important drawback. The high voltage on device backside goes up to the source through the vertical channel. The gate is still protected by the reverse junction. Thus, while this structure is really efficient for 1200 V, it cannot be led to 3.3 kV without important leakage current in blocking mode.

Design of lateral and vertical device

State of the art. As it can be seen in Fig. 2 and 3, a buried p^+ layer is frequently used. This layer is related to the source electrode [3-4]. Thus, it is always at a constant (and often null) potential, and it can be used as a free-wheeling diode. The interest of such a configuration is that the vertical channel is no more a limitation and just protect the source electrode against the spread of high drain voltage. But its drawback is that the blocking capabilities depends only on the surface gate electrode. Consequently an efficient channel blocking depends on a thin lateral channel (that leads to high channel resistivity) or on a high (in absolute value) blocking voltage.

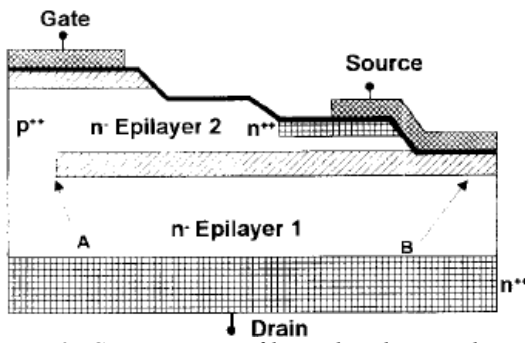


Fig. 2: Cross-section of lateral and vertical JFET designed by SiCED [3]

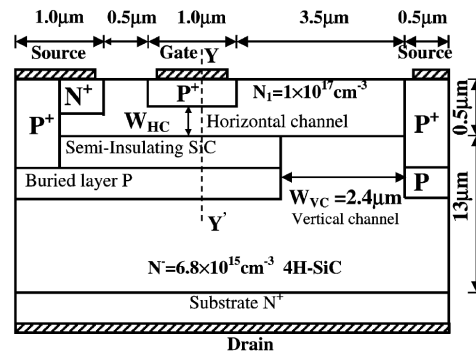


Fig. 3: Cross-section of lateral and vertical JFET designed by Zhao [4]

Our challenge was designing a lateral channel with a low on-state resistivity, low pinch-off voltage and high breakdown voltage.

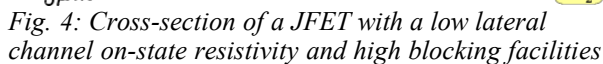
Technological elements and innovative advances. In order to perform a 3.3 kV, we first optimized the first epilayer with a 10^{15} cm^{-3} doping level and $40 \mu\text{m}$ thick. For this optimization, we have taken into account the edge termination and the passivation efficiency. The vertical channel needs a 10^{16} cm^{-3} doping level (N_V), which will be realized by a second epilayer. Known as W_2 in Fig. 4, it will be $3 \mu\text{m}$ wide. Then we implant double charge of aluminum (Al) at 320 keV to perform a $0.5 \mu\text{m}$ thick p^+ layer, that will make the buried layer after a $W_1 = 3 \mu\text{m}$ @ $N_L = 10^{16} \text{ cm}^{-3}$ third epilayer. Prior to the etching of this layer to access the buried layer, we implant a single charge of nitrogen (N) at 180 keV energy that will make the $0.2 \mu\text{m}$ thick n^+ source layer.

The high electrostatic potential can flow from the backside drain electrode through the drift region to the third epilayer *via* the vertical channel, even if it is designed to avoid high potential in lateral channel. So we decided to protect the surface gate with a 50 nm thick thermal oxide above vertical channel [5]. It is brand new in front of what is found in literature.

As it has been explained above, the buried p^+ layer is traditionally related to source electrode to set a constant potential. If this layer is related to the gate electrode, it can be helpful to block the lateral channel, hence reduce the pinch-off voltage. That is why we decided to use it as a buried gate electrode.

The structure and its parameters.

Fig. 4 shows the parameters we have to optimize. W_1 and W_2 are the widths of lateral and vertical channel respectively, while N_L and N_V their respective doping levels. LN is the margin between the



Those last three parameters form the length of the lateral channel. They can vary from 3 to 5 μm , respectively the shorter we can fabricate and the longer to reduce lateral channel resistivity.

SentaurusTM software which is based on the finite elements method. Electrical characteristics that have to be increased is the breakdown voltage V_{BR} and to be decreased, the pinch-off voltage V_{GS-off} and the on-state resistance R_{on} . So we have used a criterion inspired from Baliga's one [1] :

$$\max \left| \frac{V_{BR}^2}{V_{GS-off} \cdot R_{on}} \right|$$

Figure 10 is a plot showing the criterion value $V_{BG}/R_{on} \cdot V_{eff} \cdot 10^6$ versus device length (μm). The plot includes data points for three different values of LN ($3 \mu m$, $4 \mu m$, and $5 \mu m$) and two different values of LO ($3 \mu m$ and $5 \mu m$). The criterion value decreases as device length increases. The legend indicates: $LN=3 \mu m$ (red plus), $LN=4 \mu m$ (red square), and $LN=5 \mu m$ (red triangle). The text inside the plot area specifies: $3 < LO < 5 \mu m$ and $3 < L_{sch} < 5 \mu m$.

Tab. 1 : Optimal parameters values and related electrical characteristics

| W_1 μm | W_2 | N_L cm^{-3} | N_V | LO | LN μm | L_{Sch} | V_{BR} kV | R_{on} $\text{m}\Omega\cdot\text{cm}$ | V_{GS-off} V |
|------------------------|-------|---------------------------|-----------|------|-----------------------|-----------|----------------|--|-------------------|
| 3 | 3 | 10^{16} | 10^{16} | 5 | 3 | 4 | 4.3 | 171 | -19.5 |
| 3 | 3 | 10^{16} | 10^{16} | 5 | 4 | 3 | 4.3 | 171 | -20 |

Device's length is compound by 5 μm for gate contact and 5 μm for source contact. In Fig. 5, it can be seen that for a 20 μm long device, it left only 10 μm for LN+LO+Lsch. So if LN = 3 μm , then LO+Lsch = 7 μm =3+4 or 4+3. That is why two crosses can be found at the 20 μm point.

While the result given by this criterion is not homogeneous, we will focus only on the absolute value. E.g. in fig. 5, we can clearly see that 3 μm is the best value for LN . 3 μm is the low technological limit. Over 5 μm , the lateral channel will be too long to have a low on-state resistance. Therefore, we must choose values between 3 and 5 μm , and 3 μm is the best.

The mask layer set was designed according to optimal parameters. To fabricate this transistor, 14 photolithography levels have been performed. Fig. 6 shows an elementary field where two 4 mm^2 JFETs and four 0.16 mm^2 JFETs are implemented. Test structures like vertical diodes in order to evaluate the vertical breakdown voltage were also implemented. Electrical measurement are shown on figure 7. The devices have been manufactured at IBS.

Blocking voltage of gate-drain junction is about 3 kV. This measure has been performed in vacuum at ISL [6].



Fig. 8 shows the electrical characteristics $J_{DS}(V_{DS})$ with different V_{GS} at 25°C. The increase of control voltage V_{GS} clearly affects the channel modulation. To block the JFET, -20 V as V_{GS} are sufficient. Fig. 9 shows a clear trend of JFET effect : a channel modulation affected by the increase of control voltage V_{GS} from 0 V to -20 V. Measurements have been performed under probes without thick metal layer. So the on-state resistance is lower than expected value.

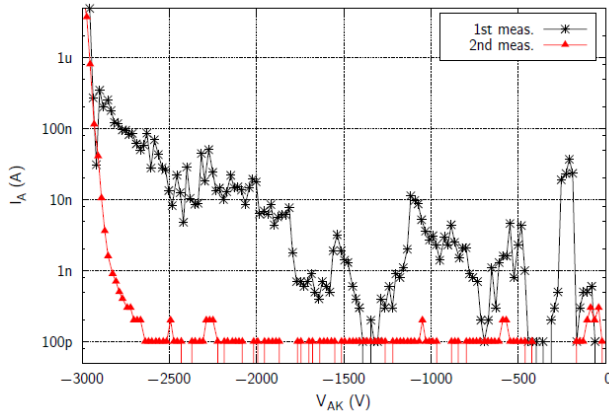


Fig. 7 : Electrical characterization of 3.3 kV bipolar test diode equivalent to gate-drain junction

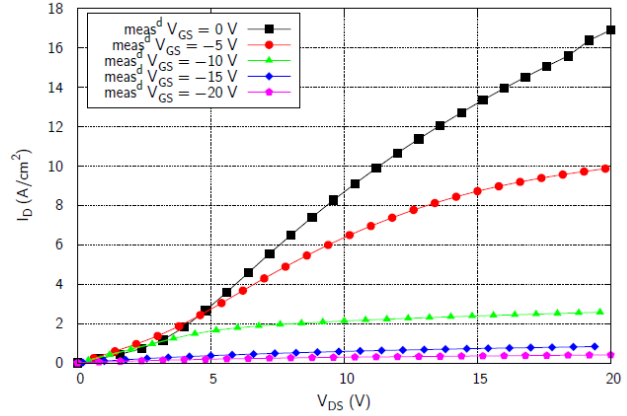


Fig. 8 : Measured $J_{DS}(V_{DS})$ for different V_{GS} at 25°C for a 4mm² fabricated JFET

Summary

Actually existing vertical JFET are generally unable to sustain high voltage due to an inadequate gate topology. To address this issue, we presented a novel JFET structure that is able to sustain voltage up to 3.3 kV. The optimal design of such a structure is obtained thanks to the introduction of a modified Baliga criterion. Characterization results confirms simulation results, reaching over than 3 kV, and thus validate the design methodology.

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