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Quasi-Flying Gate Concept Used for Short-Circuit Detection on SiC Power MOSFETs Based on a Dual-Port Gate Driver

Mathis Picot-Digoix, Frédéric Richardeau, Jean-Marc Blaquière, Sébastien Vinnac, Stéphane Azzopardi and Thanh-Long Le

Abstract—The proposed dual-port gate driver architecture relies on a quasi-flying gate concept to protect SiC power MOSFETs against short-circuit events. Hard Switching Faults (HSF) extract charges from the gate by causing a leakage current towards the source, while Faults Under Load (FUL) lead to charge injection into the gate through the reverse transfer capacitance (C_{GD}). Such phenomena lead to perturbations of the gate-source voltage (V_{GS}) which are amplified by the gate resistor, acting as an enhancer of short-circuit signatures. Thus, a small gate resistance is used to ensure high switching dynamics, while a larger one is switched on during PWM on-state operation to identify possible faults. A dual-port gate driver is then proposed to ensure fast switching with HSF and FUL monitoring. The fault detection scheme relies on comparing two thresholds to V_{GS} relative changes to the nominal gate voltage. Experimental results using TO-247 package 1.2kV/36A SiC MOSFETs exhibit promising inverter leg short-circuit detection and protection against faults in less than 300ns.

I. INTRODUCTION

SiC MOSFETs afford high efficiency and density of medium to high power range converters [1]. Beyond usual first plan characteristics, the power chip's ability to withstand extreme operating conditions is critical in a certification approach, to comply with a broad application spectrum [2]. In short-circuit operation, a critical and irreversible failure mode would happen in only a few microseconds [3]. Short-circuit protection methods [4] rely exhaustively on either the ruggedness of the power transistor itself - which is still at an early development stage [5], on a current limiting in-package hybridization [6], [7] - increasing conduction losses, or on detection methods such as desaturation, gate charge integration or absence of Miller plateau [8], [9], all showing a compromise between reactivity, complexity, and ruggedness. As of today, no solution clearly complies with all three criteria. The proposed approach consists in reconsidering the gate capacitance not only as a control element (turn-on/turn-off management), but also as an on-state high-sensitivity monitoring sensor providing low gate voltage fluctuations that do not impede normal operation thanks to intrinsic properties of SiC MOSFETs.

In HSF mode [10] (Fig. 1 in red color line), an internal Schottky emission thermionic gate leakage current arises at high temperatures and discharges C_{GS} , in turn decreasing the quasi-flying V_{GS} , naturally limiting the channel current.

In FUL mode [11] (Fig. 1 in yellow color line) the DUT is initially in an on-state. Its drain-source voltage V_{DS} is therefore

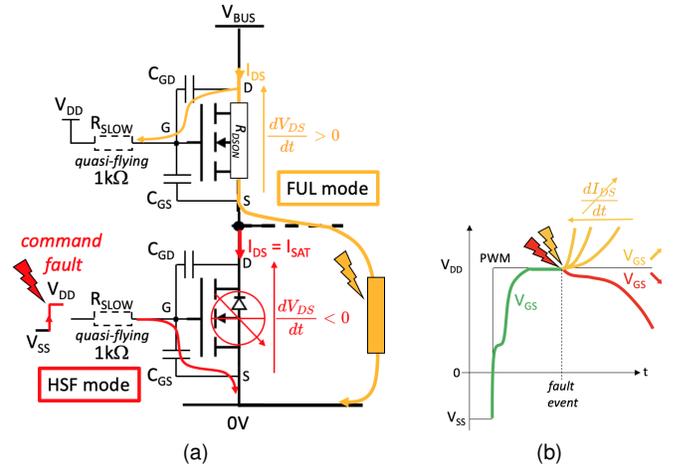


Fig. 1. HSF Schottky gate leakage current in red color and FUL gate charge injection in yellow color illustration (a), influence on gate-source voltage (b)

low, which makes C_{GD} exhibit a high value. On the other hand, the MOSFET still being in its ohmic region, the faulty drain current I_{DS} rise creates an ohmic dV_{DS}/dt through its drain-source on-resistance R_{DSON} . The strong capacitive coupling between C_{GD} and this V_{DS} rise injects charges from drain to gate, back to the driver through the gate resistance. This increases V_{GS} , thus extending the MOSFET ohmic region and high C_{GD} value. In this case, a gate clamp is needed not to damage the SiO_2 gate oxide layer.

Both these mechanisms prove to enhance fault detection sensitivity and ruggedness during on-state operation using a very large external gate resistance to virtually isolate the gate between turn-on and turn-off events. However, switching dynamics would then be greatly impeded. The use of different gate resistors is mandatory for switching and for on-state operation using a dedicated switched-resistors gate driver architecture (Fig. 2a), as generically introduced in [12].

II. CONCEPT HARDWARE IMPLEMENTATION

It appears in Fig. 1b that comparing the quasi-flying on-state V_{GS} to upper (V_{HT}) and lower (V_{LT}) thresholds would allow the detection of all short-circuit events. Commercial 3-lead TO-247 package Gen. 2 80m Ω 1200V/36A SiC MOSFETs underwent short-circuit tests in an inverter leg configuration on a 600V capacitor-bank-based power bench (Fig. 4a). Short-circuit detection is then made possible thanks to a proposed

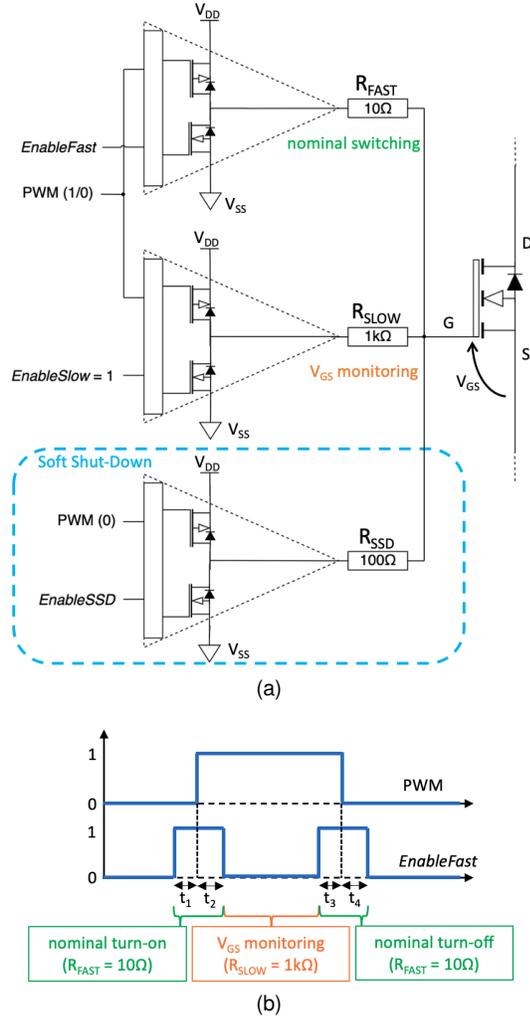


Fig. 2. Multi-port switched gate driver architecture (a) and *Fast* low resistance buffer control signals (b) ($V_{DD} = 20V$, $V_{SS} = -5V$, $t_1 = 50ns$, $t_2 = 830ns$, $t_3 = 50ns$, $t_4 = 830ns$)

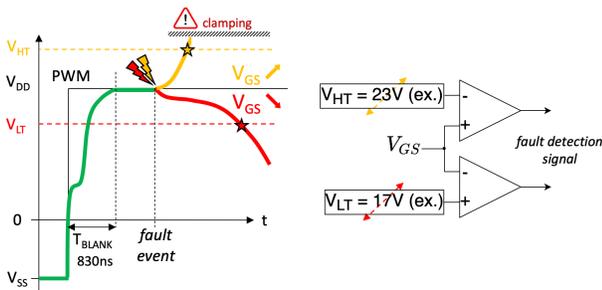


Fig. 3. V_{GS} double threshold comparison short-circuit detection principle

double threshold on V_{GS} (Fig. 3) and a double-comparator-based daughterboard (Fig. 4b) plugged into a multi-port gate-driver-based motherboard (Fig. 4d) to ensure fast switching (“Fast” buffer), increased fault detection sensitivity (“Slow” quasi-flying buffer), and Soft Shut-Down protection (SSD buffer). *Fast* mode should be long enough to allow for complete charge and discharge of the gate capacitances, and to protect the complementary MOSFET during turn-on events against C_{GD} coupling. Both *Fast* and *Slow* buffers receive

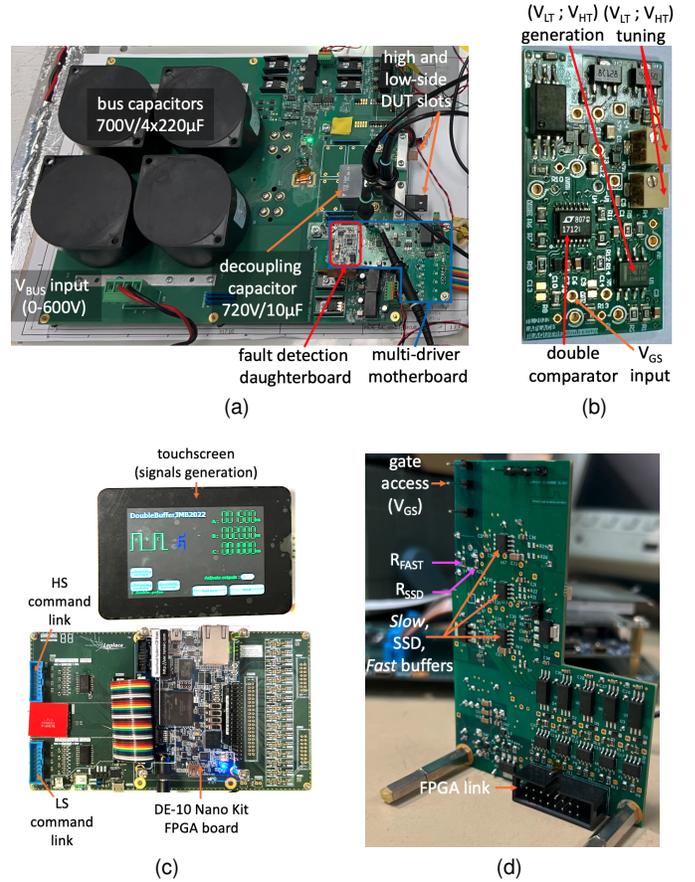


Fig. 4. Setup: short-circuit test bench (a), double threshold detection daughterboard (b), FPGA-based control board (c) and multi-buffer motherboard (d)

the same PWM signal. For practical reasons, the *Slow* buffer is always active, while the *Fast* one is only enabled during switching events and otherwise in high impedance during static states as shown in Fig. 2b. A FPGA-based control board (Fig. 4c) generates PWM and $EnableFast$ signals, introduces a blanking time and receives the V_{GS} comparison result to the two thresholds and imposes the $EnableSSD$ signal accordingly.

III. EXPERIMENTAL RESULTS AND ANALYSIS

A. Hard Switching Faults

HSF faults happen following an undesirable turn-on (Fig. 1a) thus generating an extreme temperature rise, which gives way to a Schottky emission current leakage (I_{SE}) through the gate oxide [13]. I_{SE} causes V_{GS} to drop proportionally to R_{SLOW} a few microseconds after the appearance of the fault (Fig. 5a area 2). This natural V_{GS} drop participates in shrinking the MOSFET channel, limiting the saturation current, and thus the chip temperature rise. In the case of a HSF, this phenomenon provided by the proposed gate architecture ensures that should the above-mentioned protection method fail, the MOSFET would still enter into a safe failure mode characterized by a gate-to-source short, thus naturally turning off the switch [14]. Once V_{GS} falls below the low detection threshold V_{LT} , the FPGA sends the SSD order and enables the SSD buffer while setting all PWM signals to 0.

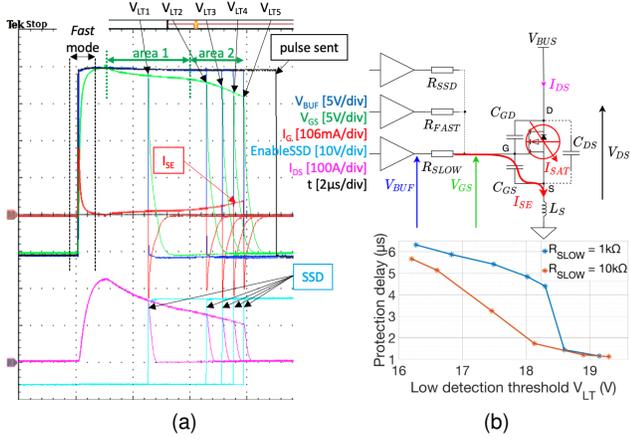


Fig. 5. HSF gate behavior (a), equivalent schematic and protection delay results (b) ($V_{BUS} = 600V$, $R_{FAST} = 47\Omega$, $R_{SLOW} = 1k\Omega$, $R_{SSD} = 82\Omega$)

Moreover, Fig. 5a shows an advantageous decrease in V_{GS} as soon as the fault happens (area 1) thanks to a high R_{SLOW} value ($1k\Omega$) likely to result from the chip source wires and lead stray inductance (L_S) coupling due to the high inrush fault current, and probably also from a pre-thermal phenomenon. The SSD total protection delay is measured between the instant the fault appears and the effective turn-off. The closer the low detection threshold to the nominal on-state gate voltage, the faster the protection. However, the low detection threshold V_{LT} can only be increased so much before risking false detections, hence a trade-off between protection speed and robustness. This compromise can be solved by increasing R_{SLOW} and making V_{GS} area 1 drop even lower, as illustrated in Fig. 3 red curve. A HSF protection delay of $1.2\mu s$ is achieved including a total inherent propagation delay of $230ns$ partly due to optocouplers between the FPGA and the SSD buffer. This protection delay is well inferior to the MOSFET short-circuit withstand time (T_{SCW}) of $8\mu s$ and limits the dissipation of energy to $140mJ$ (20% of the critical energy of $0.7J$ [15]) in the power transistor. In comparison, although the desaturation method can theoretically achieve fast short-circuit protection, in industrial applications, blanking windows are implemented as a safety margin to avoid false detections. It also still requires expensive and non-integrable high-voltage sensing diodes. The expression (1) of the maximum V_{GS} transient drop in HSF mode shows both contributions in areas 2 and 1 of Fig. 5a:

$$|\delta V_{GS}|_{HSF} = \underbrace{R_{SLOW} I_{SE}}_{area\ 2} + \underbrace{L_S \frac{dI_{DS}}{dt}}_{area\ 1} \quad (1)$$

With I_{SE} the Schottky emission current defined in (2).

$$I_{SE} = A_0 \frac{4\pi q k^2 m_{ox}}{h^3} T^2 \cdot \exp\left(\frac{-\Phi_B + \sqrt{\frac{q^3 E}{4\pi\epsilon_r\epsilon_0}}}{kT}\right) \quad (2)$$

Where T is the temperature and A_0 is the chip active surface. Other physical parameters are defined in [13].

B. External Faults Under Load

External FUL are characterized by a current rise through an on-state switch following the appearance of an inductive path

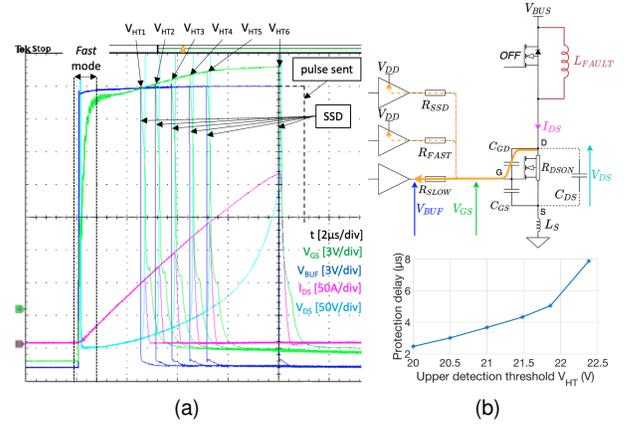


Fig. 6. External FUL gate behavior (a), schematic and protection results (b) ($V_{BUS} = 600V$, $R_{FAST} = 47\Omega$, $R_{SLOW} = 10k\Omega$, $R_{SSD} = 82\Omega$, $L_{FAULT} = 11.6\mu H$)

(Fig. 1a). This additional current creates a V_{DS} ohmic rise and participates in increasing V_{GS} by injecting charges back to the driver through C_{GD} , thus further extending the MOSFET ohmic region – the region of interest, as the thermal stress is the lowest. Although the fault current rise is slow, R_{SLOW} acts as a gain amplifier and makes it possible for this gate driver architecture to also detect this type of fault as shown in Fig. 6a. Effective protection happens in $2.5\mu s$ (Fig. 6b), including $190ns$ of propagation delay, in the MOSFET ohmic region. The associated dissipated energy is only $2.2mJ$ (0.3% of $0.7J$). This guarantees a correct safety margin as the chip will be able to withstand several repeated short-circuits.

$$|\delta V_{GS}|_{ext.FUL} = R_{SLOW} C_{GD} (V_{DS}) \frac{dV_{DS}}{dt} \quad (3)$$

Equation (3) shows external-FUL-induced V_{GS} overvoltage. It should be noted that, in this case, L_S has a negligible effect due to the slow current rise.

C. Internal Faults Under Load

Internal FUL are characterized by the failure of a complementary switch in an inverter leg or an erratic command, leading to an extreme sudden drain current rise in an initially on-state switch. The current rise is now only limited by the faulty switch V_{GS} slew rate. This ensures a strong and dynamic coupling with the gate through L_S in addition to C_{GD} capacitive coupling, as in external FUL, as shown in (4).

$$|\delta V_{GS}|_{int.FUL} = (R_{SLOW} C_{GD_{MAX}} R_{DS_{ON}} + L_S) \frac{dI_{DS}}{dt} \quad (4)$$

Given the large value of R_{SLOW} , the gate-source stray inductance is not considered as V_{GS} transients show no ringing. Fig. 7 shows effective protection against internal FUL in $250ns$ only. The extreme channel current rise and the large value of R_{SLOW} are sufficient to generate an overvoltage on V_{GS} that triggers the detection circuit even before the MOSFET reaches its saturation area. During the on-state, the *Fast* and *SSD* buffers are in a high-impedance state and the gate voltage excursion is naturally clamped by their high-side PMOS body diodes as illustrated in Fig. 2a, thus protecting the gate. In

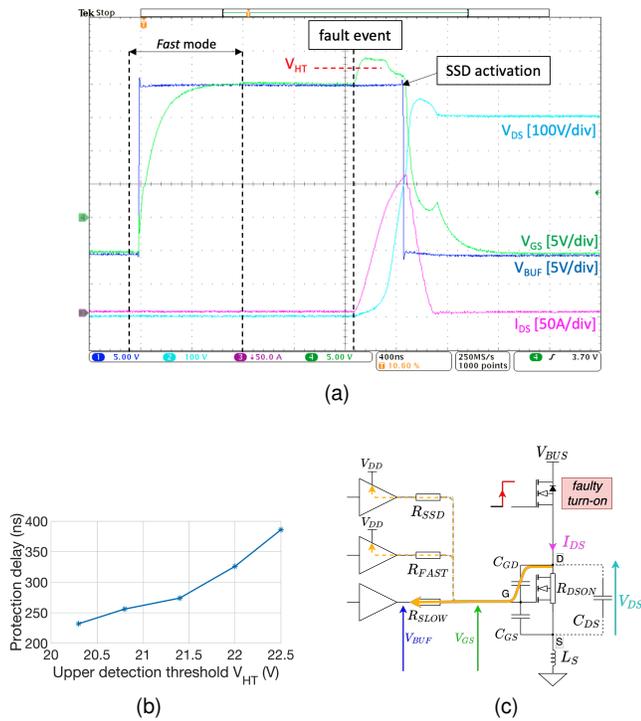


Fig. 7. Internal FUL gate behavior (a), protection results (b) and schematic (c) ($V_{BUS} = 600V$, $R_{FAST} = 47\Omega$, $R_{SLOW} = 10k\Omega$, $R_{SSD} = 82\Omega$, $V_{HT} = 22.4V$)

internal FUL, the gate charge injection is sudden and intense which requires great reactivity and sensitivity of the detection system, while in external ones, it is considerably slower and more moderate. The inductive effect provided by L_S is predominant and adds to the contribution of C_{GD} solicited by the drain-to-source voltage rise.

D. Implementation and concept properties in an inverter leg

For a practical implementation in an inverter leg, the faulty turn-on (HSF) and the subsequent extreme current rise happening in one switch will impact its already-on counterpart that, in turn, endures a HSF-induced internal FUL. This property allows the detection of HSF faults thanks to a FUL detection on the complementary switch gate driver. It is thus possible to detect HSF faults with the same dynamics as internal FUL.

IV. CONCLUSION

This paper demonstrates a comprehensive short-circuit protection method provided through an original SiC MOSFET dual-port gate driver architecture. A small gate resistance channel is used during switching events, and a large gate resistance channel handles fault event monitoring. The detection relies on putting the gate into a quasi-flying state to enhance its sensitivity to possible gate charge variations, which are short-circuit signatures, and turn it into a fault sensor. The measure of the MOSFET gate-source voltage effectively allows the protection of an inverter leg against HSF-type faults in 1.2 μ s, and against internal FUL in 250ns. In the case of HSF faults, the coupling of high-side and low-side protections puts them into competition allowing the fastest to protect the inverter leg. This redundancy significantly decreases HSF protection time

and adds a layer of robustness. The proposed fault detection scheme relies on gate-source low voltage fluctuations and is thus highly integrable with analog IC technology.

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