A TCAD-based Analysis of Substrate Bias Effect on Asymmetric Lateral SiGe HBT for THz Applications

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***Abstract*— In this work, a new asymmetric lateral SiGe HBT is proposed. This asymmetric structure allows one to modulate the carrier densities in the collector region by the application of substrate bias that causes significant improvements in the device performances. The open base breakdown voltage can be tuned from 2.2 V to 3.6 V and the transit frequency (f_T) is improved up to ∼90% by varying the substrate bias. The bias-dependent variation in transit time is elaborately discussed using regional analysis. This work, for the first time, demonstrates an oscillation frequency (f_{MAX}) of 2.7 THz achievable by tuning the substrate bias in an asymmetric SOI lateral SiGe HBT.**

***Index Terms*— Lateral SiGe HBT, SOI devices, MOS effect, THz performance, Substrate bias**

I. Introduction

THE exponential growth in the wireless communication (4G, 5G, and upcoming 6G) market demanded scaled down faster transistors in order to fuel the development of improved radio frequency integrated circuit (RFIC) technology. Now the need is mainly to offer the lowest cost and, depending on the required integration, to accommodate as many RFIC subsystems on a silicon substrate as possible. This will help the technology and economy to improve in appropriate pace and fulfill the researchers dream of truly system-on-chip (SoC) realization. BiCMOS process allows more flexibility in integrating complex circuits in a single chip.

For SoC applications, silicon on insulator (SOI) substrate is best suited due to its (i) superior quality of device isolation, (ii) reduction in leakage current, (iii) reduced crosstalk and noise due to substrate, and (iv) increased packing density. In general, compared to the bulk silicon, SOI offers 20-30% performance improvement at the same operating voltage. Although the complementary metal oxide semiconductor (CMOS) transistors enjoy the above discussed added advantages of SOI, integrating vertical silicon germanium heterojunction bipolar transistor (SiGe HBT) with CMOS on SOI is a cumbersome task [1] as the vertical bipolar device needs at least a few hundred of nanometers thick silicon region above the oxide layer [2]. In fact, though vertical SiGe HBT has already been demonstrated by IBM and STMicroelectronics on SOI layer, its architecture cannot be implemented on advanced SOI nodes such as the 28 nm technology having a thin Si film of less than 10 nm [3] [4] [5]. In this situation, lateral bipolar devices come out to be an interesting and economical choice. Here the current flows horizontally as in the MOS transistors. Additionally, the key figures of merits (FoMs) like f_T and f_{MAX} of the high frequency vertical SiGe HBTs are limited by the *RC* time constants originating from the external parasitics [6]. Adapting a lateral bipolar structure, the parasitic junction capacitances and collector cum base resistances can be reduced allowing further improvements in f_{MAX} and noise figure [7]. Here, the collector and base resistances are lowered because of the close proximity of the top contacts to the active regions.

Both symmetric and asymmetric SOI lateral bipolar transistors with key FoMs are already reported in the literature. The silicon-based asymmetric devices proposed by Dekker et al. [8] and Shahidi et al. [9] resulted in 15 GHz and 20 GHz transit frequencies, respectively. Similarly, with a little modification in architecture, Sun et al. [1] proposed a device with f_T/f_{MAX} up to 16/46 GHz. Nii et al.'s [10] cobalt silicided extended base device yields up to 67 GHz f_{MAX}, whereas base modified horizontal current bipolar transistor (HCBT) by Suligoj et al. [11] [12] [13] presented an f_{MAX} up to 490 GHz. Cai et al. [14] [15] [16] proposed a symmetric device that suppresses the high current density degradation and base push out effects, and predicted a THz f_{MAX}. Raman et al. [17] and Derrickson et al. [18] predicted f_{MAX} up to 1.2 to 2 THz, respectively, with constant and graded germanium profiles. In [19], the collector and emitter are highly doped making them insensitive to the substrate bias, whereas the least-doped base region remains highly sensitive.

On the contrary, in this work we propose a new asymmetric lateral SiGe HBT having a lightly doped collector that can be electrostatically adjusted by tuning the substrate bias (V_{sub}). The low collector doping of 10^{17} cm^{-3} becomes very sensitive to the substrate bias and allows one to switch from a high-speed device to a high voltage device. This proposed device projects an f_{MAX} of 2.7 THz at V_{sub}=2 V with a BV_{CEO}=2.2 V and can switch to an f_{MAX} of 0.8 THz with

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a BV_{CEO}=3.6 V for a V_{sub}=-2 V. The high f_{MAX} observed is mainly caused by the low internal base resistance. This results from the significant downscaling of what is usually called the lateral dimension in conventional vertical HBT, equivalent to a technological node lower than 10 nm. Moreover, as explained above, the parasitics associated with the device are dramatically reduced.

In the next section, the device architecture is discussed within a simulation setup. Section III describes the influence of substrate bias on DC and RF performance. In section IV the device fabrication steps are briefed. Finally, we conclude in section V.

II. Simulation Setup And Device Architecture

In this work, the lateral SiGe HBT structure as shown in Fig. 1 is investigated. Device simulations have been carried out using commercially available Sentaurus TCAD in a calibrated environment [20]. The results published in [21] substantiate our confidence in the choice of the adopted model parameters and overall calibration of the high frequency device simulation. The hydrodynamic model (HD) is used for solving the current density equations and the Slootboom bandgap narrowing model is used to account for the effect of carrier concentration at heavy doping. Caughey-Thomas mobility model is included; also the excess carrier recombination (Auger and Shockley-Read-Hall) models and breakdown effects at the high electric field (using Lackner's model) are included following the works of [17] [18] [21] [22] [23]. As shown in Fig. 1, both the emitter

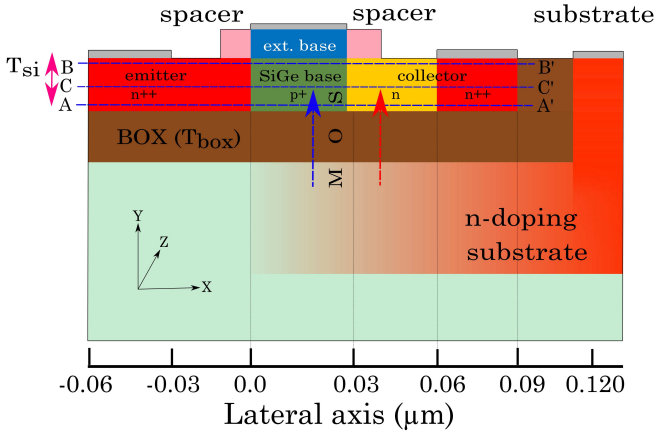

Fig. 1: Cross-sectional view of the proposed asymmetric lateral SiGe HBT. The dashed lines indicate different cut-lines used to plot spatial data in Figs. 2, 3, and 5(a).

and collector widths in the investigated SiGe HBT structure are fixed at 60 nm, while the physical base width and silicon layer thickness (T_{si}) are, respectively, kept at 28 nm and 7 nm in order to ensure compatibility with the STMicroelectronics 28 nm FD-SOI technology. The collector is divided into two (a low doped (n) and a high doped (n^{++})) regions with appropriate doping levels given in Table:I. The BOX oxide thickness (T_{box}) is 25 nm and the device is extended across a width of 5 μm (Z-direction). In case of a lateral SiGe HBT, it is essential that the intrinsic and extrinsic base regions are fully self-aligned. Moreover, the extrinsic base must not be

TABLE I: Dimensions and doping concentration of the LHBT device in Fig. 1.

Region	Dimension (nm)	Doping (cm^{-3})
emitter (n^{++})	60	5×10^{20}
collector (n^{++})	30	5×10^{20}
collector (n)	30	1×10^{17}
base (p^{+})	28	3×10^{18}
extrinsic base	28	2×10^{20}
substrate	NA	1×10^{20} to 1×10^{15}
Ge	28	20%
T_{si}	7	–
T_{box}	25	–

wider than the intrinsic base; else the unwanted widening of the base can cause a reduction in both transit frequency (f_T) and ac current gain at low frequency [7]. Therefore, in the simulation, the width of the extrinsic base is kept at 28 nm. Spacers are added on both sides of the base to avoid unwanted contact shorting. In the lateral npn SiGe HBT discussed here, the n-regions are doped with arsenic and the p-region is doped with boron; and both have their respective advantages over the other possible dopants from a fabrication point of view. Additionally, the n-type substrate is doped with a non-uniform Gaussian profile as shown in Fig. 1. The detailed dopant values and the regional dimensions are given in Table: I.

III. Impact Of Substrate Bias On Device Performance

In this section first, we compare the physics of the symmetric and asymmetric HBTs. Afterwards, the asymmetric device is analyzed elaborately with an emphasis on its improved FoMs achievable by means of substrate bias tuning. Note that unlike the asymmetric device, the symmetric HBT has only one (60 nm wide) collector region that is heavily doped (n^{++}). Unless specifically mentioned, in the later sections of this paper, the collector region in the asymmetric device will always indicate the low doped collector.

A. Comparison Of Symmetric And Asymmetric Devices

In order to clarify the differences between the symmetric and asymmetric lateral HBTs, we need to understand the modulation of carrier density of different transistor regions under the varying substrate-bias. This can be understood from the plots of Fig. 2 that shows the TCAD simulated conduction and valence bands along the cut-lines A-A' (Fig. 2(a)) and B-B' (Fig. 2(b)) as mentioned in Fig. 1. It is clear that the carrier densities in the heavily doped emitter and collector remain insensitive to the substrate bias (V_{sub}). We observe from Fig. 2(a) that at close proximity of BOX and Si interface (cut-line A-A), carrier density of the symmetric device is modulated only at the base region whereas in case of the asymmetric device, the electron density at the n-collector (having N_D=1 $\times$ 10^{17} cm^{-3}) is impacted significantly compared to the hole density in the base (with N_A=3 $\times$ 10^{18} cm^{-3}) region. For the asymmetric device, it is observed that V_{sub} modulates the

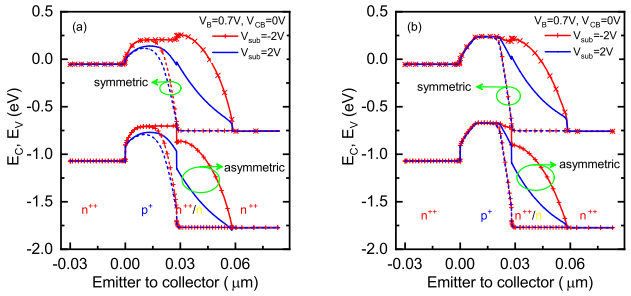

Fig. 2: Conduction band and valence band (a) at the bottom (A-A' in Fig.1) of the thin film SOI, (b) at the of the top (B-B' in Fig.1) thin film SOI.

middle of the base region by around 67 meV whereas the middle of the n-collector by around 500 meV. On the other hand, Fig. 2(b) shows that the band diagram at the top of the thin film (cutline B-B), is hardly modulated within the base region for both the devices. Essentially the V_{sub}-dependent field-effect is significantly reduced at a larger distance within the Si film away from the BOX. Comparing Figs. 2(a) and (b) it appears that the n-collector of the asymmetric device is similarly modulated within all the thickness of the thin film due to its lighter doping. This modulation of the conduction band results into a modulation of the collector carrier density by more than three orders of magnitude as shown in Fig. 3. The potential within the Si film (base or collector) due to the applied V_{sub} can be expressed as

$$\phi_{B/C} = V_{Sub} - \Delta Q_{B/C}/C_{BOX} \tag{1}$$

where $Q_{B/C}$ is the charge variation in the base or the collector region and C_{BOX} is the buried-oxide capacitance. Since the modulation of charge within the collector is much more than that in the base, the collector region potential is strongly affected. In the following, we focus our attention to the

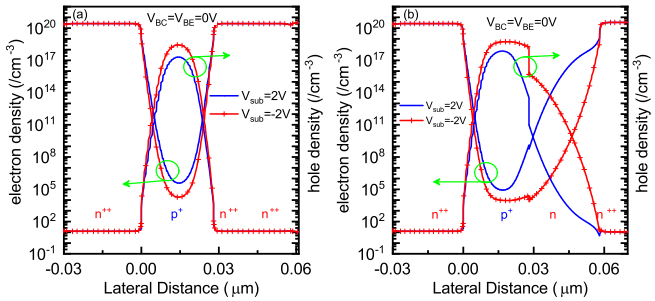

Fig. 3: Spatial electron/hole density modulation in the base and collector regions with substrate bias variation (a) in symmetric (b) asymmetric devices at the middle of silicon (refer C-C' -Fig.1).

asymmetric device to understand the impact of V_{sub} onto its various performance FoMs.

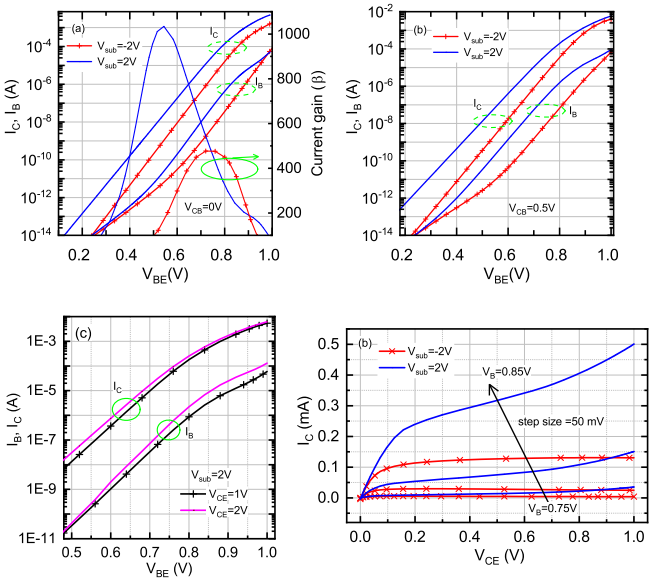

Fig. 4: (a) Gummel characteristics for asymmetric device at V_{sub}=-2 V and 2 V, V_{CB}=0 V, (b) at V_{sub}=-2 V, 2 V, and V_{CB}=0.5 V (c) at V_{sub}= 2 V, and higher reverse bias V_{CE}=1 V and 2 V, (d) Forced-V_B output characteristics at V_{sub}=-2 V and 2 V for lateral SiGe HBT with W_{si}=5 μm.

B. Impact Of Substrate Bias On DC Operation

Fig. 4(a)(b)(c) presents the Gummel characteristics of asymmetric SiGe HBT at different substrate biases. At V_{sub}=2 V, band lowering of the asymmetric device at the base-emitter junction (Fig. 2(a)) allows more electrons and holes to cross from the emitter and base, respectively. This causes increased collector and base currents as shown in Fig. 4(a)(b). Additionally, the positive V_{sub} results in a higher electron density in the n-collector causing an increment in the space charge region inside the base. This leads to a shrinking in the quasi-neutral base (QNB) width subsequently increasing the collector current. Although the substrate field-effect tends to deplete the holes near the BOX/Si interface of the base region, electron accumulation effect in the collector is significantly higher as the donor doping in the collector is less by more than one order compared to the acceptor doping in the base region. Output characteristics in Fig. 4(d) indicates that the collector current is increased by around 100% when V_{sub} is varied from -2 V to 2 V; however, due to the reduction of the QNB width, Early voltage reduces and output conductance value increases. Additionally, we investigate the effect of V_{sub} onto the open base breakdown voltage (BV_{CEO}). Electric field ($E(x)$) in the n-collector as a function of V_{sub} can be expressed as

$$\frac{dE\left(x\right)}{dx} = \frac{q}{\varepsilon_{Si}}\left(N_C + \Delta n\left(V_{sub}\right) - \frac{j_n}{qv_n}\right) \tag{2}$$

where ε_{Si} is the silicon permittivity, N_C is the collector doping, v_n is the electron velocity, j_n is the electron current density and $\Delta n(Vsub)$ is the increased carrier density due to the positive substrate bias. In case of a negative V_{sub}, $\Delta n(Vsub)$ gets a negative value reducing the slope dE/dx in (2). This leads to a reduced electric field peak at the BC

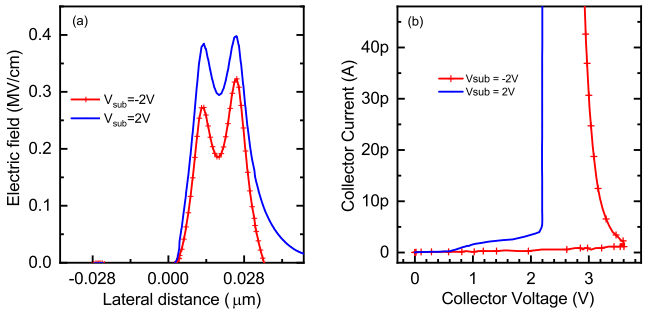

Fig. 5: (a) Electric field distribution through C-C cut-line (see Fig. 1) and (b) open base output characteristics showing BV_{CEO} values at V_{sub}=-2 V and 2 V.

junction (see Fig. 5(a)). Hence, the impact ionization effect becomes weaker resulting in a higher BV_{CEO} value. Fig. 5(b) shows collector current at open base condition, for two different V_{sub}. It is observed that BV_{CEO} varies from 3.6 V to 2.2 V as V_{sub} changes from -2 V to 2 V. This way, one can achieve a relatively high power device just by tuning the substrate bias of a given lateral SiGe HBT.

C. Impact Of Substrate Bias On RF Performance

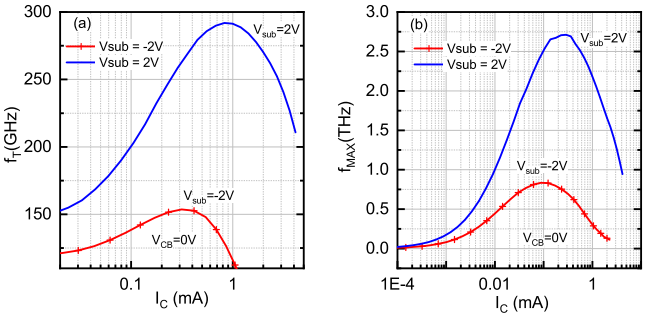

Fig. 6: Collector current dependent (a) transit frequency and (b) maximum oscillation frequency at V_{CB}=0 V and different V_{sub}.

The transit frequency (f_T) and the maximum oscillation frequency (f_{MAX}) are the main FoMs of a transistor from the perspective of its high-speed performances. Fig. 6 shows the impact of V_{sub} onto the collector current dependent f_T and f_{MAX} curves. It is observed that both f_T and f_{MAX} are significantly increased when V_{sub} changes from -2 V to 2 V. Also the peak of f_T and f_{MAX} occurs at higher I_C levels showing a change in the collector current corresponding to the onset of the Kirk effect that is directly related to $dE(x)/dx$ in (2). Essentially, as $\Delta n(Vsub)$ increases with positive V_{sub} values, obtaining the null point of $dE(x)/dx$ requires a higher electron current density, j_n; hence, the Kirk effect is pushed to a higher collector current (I_C) leading to the peaks of f_T and f_{MAX} occurring at higher I_C. The relation between the f_T and emitter-to-collector transit time (τ_{ec}), can be expressed

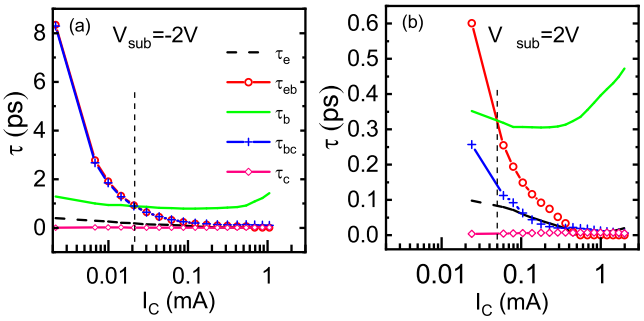

Fig. 7: Regional transit time components versus collector current at V_{CB}=0 V with (a) V_{sub}=-2 V and (b) V_{sub}=2 V. The vertical dashed lines indicate the point of change from low to intermediate injection.

as

$$\frac{1}{2\pi f_T} = \tau_{ec} = \tau_e + \tau_{eb} + \tau_b + \tau_{bc} + \tau_c \tag{3}$$

where τ_e, τ_b, and τ_c, are the transit times in neutral emitter, base, and collector regions, respectively. The components τ_{eb} and τ_{bc} correspond to the transit times related to the base-emitter (BE) and base-collector (BC) junctions. In order to investigate the impact of V_{sub} on various transit time components, we carried out a regional analysis at V_{CB}=0 V and different V_{sub}. We extracted the BE and BC boundaries (X_{jE} and X_{jC}) from the intersection points of spatially varying $q\frac{dp}{dj_c}$, $q\frac{dn}{dj_c}$ curves (at the C-C' cut-lines), where p and n denote the hole and electron density, respectively while j_c corresponds to the current density. Note that the differential data are extracted following an infinitesimal change in the base-emitter voltage as reported in [24].

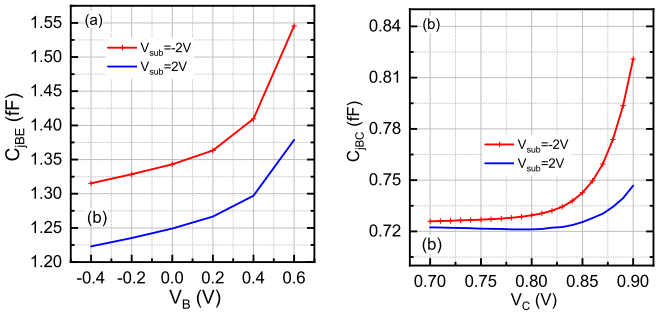

Fig. 8: TCAD simulated (a) base emitter and (b) base collector capacitances at $V_{sub=}$=-2 V and 2 V.

Fig. 7 shows that in the low injection regime, the total transit time is dominated by the junction related transit time components (τ_{eb} and τ_{bc}). Both τ_{eb} and τ_{bc} are found to decrease rapidly with increasing collector current which can be easily comprehended if (3) is rewritten as

$$\frac{1}{2\pi f_T} = \tau_{ec} = \tau_e + \frac{kT}{qI_C}C_{jBE} + \tau_b + \left(\frac{kT}{qI_C}C_{jBC} + \frac{x_d}{2v_{sat}}\right) + \tau_c \tag{4}$$

where x_d, v_{sat} indicate the base-collector depletion width and the electron saturation velocity respectively, while C_{jBE} and

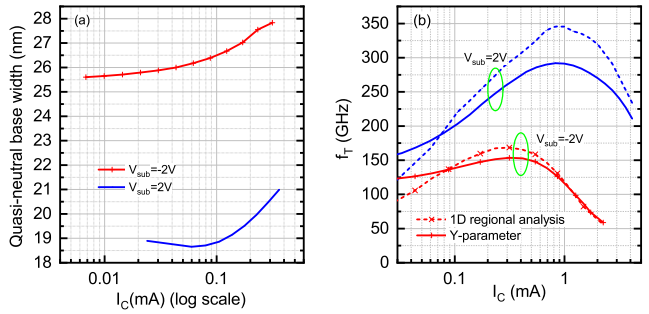

Fig. 9: TCAD simulated (a) effective quasi-neutral base width at different V_{sub}; (b) comparison of transit frequency extracted using 1D regional approach (dashed line) and that obtained from small-signal Y-parameters (as done in Fig. 6).

C_{jBC} are junction capacitances. Note that the overall transit time values are significantly reduced as V_{sub} is changed from -2 V to 2 V.

Application of a positive V_{sub} reduces the hole charge within the base (near the BOX/Si interface) while the carrier concentration within the highly doped emitter remains unchanged leading to an enlargement of the BE SCR within the base. This causes a reduction in C_{jBE} in (4)) (see Fig. 8(a)) consequently reducing the τ_{eb} in (3) (see Fig. 7(b)). On the BC side, positive V_{sub} causes relatively higher accumulation of electron density in the n-collector and at the same time a decrease of hole in the base. The resulting equilibrium of carriers produces a decrease of C_{jBC} and τ_{bc} (see Figs. 7(b) and 8(b)).

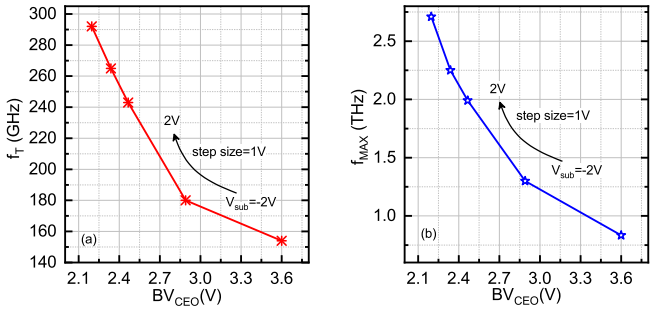

Fig. 10: BV_{CEO} dependent f_T and f_{MAX} at different substrate bias; the extraction of f_T and f_{MAX} are carried out at V_{CB}=0 V.

As shown in Fig. 7, τ_b and τ_{bc} dominate at the medium injection regime. Finally, at the high injection level τ_b dominates and it counts almost 80% of the total transit time. At positive V_{sub}, the average neutral base width is reduced due to the encroachment of BE and BC SCRs within the base. Additionally, information of X_{jE} and X_{jC} obtained from the regional approach yield the QNB width. Our estimate shows that the QNB is reduced from ∼26 nm to ∼19 nm as V_{sub} changes from -2 V to 2 V (see Fig. 9(a)). This leads to a significant increase in f_T as shown in Fig. 6(a). Fig. 9(b) compares the transit frequency extracted from 1D regional approach and that from the y-parameters of the device. Although, we observe a certain mismatch in the approximated 1D f_T values from the exact ones in Fig. 6(a), the bias-dependent trends are in agreement. This also confirms that the modulation of f_T is dominated by the intrinsic 1D device and that the contributions from the parasitic capacitances are minimal.

Fig. 6(b) demonstrates that an increase in V_{sub} from -2 V to 2 V causes an almost 225% (∼1.9 THz) increase in f_{MAX}. It is well known that f_{MAX} depends on f_T, base resistance (r_b) and collector-base capacitance (C_{jBC}) [4] following

$$f_{MAX} \simeq \sqrt{\frac{f_T}{8\pi r_b C_{jBC}}}. \tag{5}$$

Fig. 8(b) shows that there is around 6% reduction in C_{jBC} as V_{sub} changes from -2 V to 2 V at peak f_T bias point. Regarding the base resistance, we understand that it has a bias-independent extrinsic component (r_{bx}) that is estimated to be around 0.33 Ω (due to heavy doping) [19] and a bias-dependent intrinsic component which requires special attention for the device under investigation. For the conventional device, typical emitter width and base thickness are about ∼90 nm and ∼20 nm, respectively. In case of our device, these dimensions are 7 nm and 28 nm, respectively. Hence, the dominant hole flow direction is horizontal (and not vertical in this lateral device) and accordingly, the r_{bi} formulation is modified as

$$r_{bi} \approx \frac{\rho_B L_{Beff}}{3W_{si}T_{si}}, T_{si} < L_B \tag{6}$$

where ρ_B is the base resistivity [20], L_{Beff} is the QNB length in the lateral direction that varies from ∼19 nm to ∼26 nm as V_{sub} changes from 2 V to -2 V (Fig. 9(a)), W_{Si} is width of the device in the Z-direction, and T_{si} is the silicon thickness of the base region. The intrinsic base resistances calculated using (6) are 4.16 Ω and 2.8 Ω for V_{sub}=-2 V and 2 V, respectively. This estimates a reduction of 40%. The term 1/3 in (6) accounts for the 3D distribution effect. It is clear that due to a change in V_{sub} from -2 V to 2 V, an increase of f_T and reduction of C_{jBC} and r_b significantly improve the f_{MAX} value following (6).

TABLE II: Variations in FoMs due to V_{sub} at $V_{CB} = 0$ V.

V_{sub}	I_C in μA (at peak f_T)	β	f_T (GHz)	f_{MAX} (THz)	BV_{CEO} (V)
-2 V	87.81	440	154	0.834	3.6
2 V	361.4	1035	292	2.71	2.2

Finally, Figs. 10(a) and (b) present, respectively, the breakdown voltage-dependent variation of f_T and f_{MAX} obtainable by tuning the V_{sub}. Table: II shows that with an optimal choice of device dimension and bias, the proposed device can deliver the desired FoMs. Following Fig. 10, and Table: II, a device engineer can suitably decide on the intended combination of breakdown voltage, f_T and f_{MAX} targeting suitable applications. Comparing the RF performance with some state-of-the-art devices of competitive technology [15] [25] [26]; the proposed device has the potential to deliver higher RF

performance and breakdown voltage with appropriate device engineering to suit intended applications.

IV. Integration With STMicroelectronics' FDSOI Technology

As shown in Fig.11 the proposed process in line with STMicroelectronics's technology starts from shallow trench isolation (STI) formation followed by chemical mechanical polishing (CMP). After forming the STI, the entire wafer can be implanted with arsenic to form the n-type lightly doped collector (n-LDC). The energy and angle should be such that arsenic can fully penetrate the SOI films and no p-type region remains at the SOI/BOX interface. Dose levels in the order of 10^{11} cm^{-2}-10^{12} cm^{-2} are used to produce an LDC concentration of roughly 10^{17} cm^{-3}, in order to ensure sufficient trade-off of both breakdown and collector resistance. The substrate doping implantation can be done in two ways, (i) self-aligned with emitter-collector doping, which will save one mask, or (ii) if a specific substrate doping is planned, it can be done using a separate mask extending up to the right edge of the STI. However, in the earlier method, the depth of the substrate region doping will not be much because the dose and energy will be chosen precisely based on the requirement for emitter and collector.

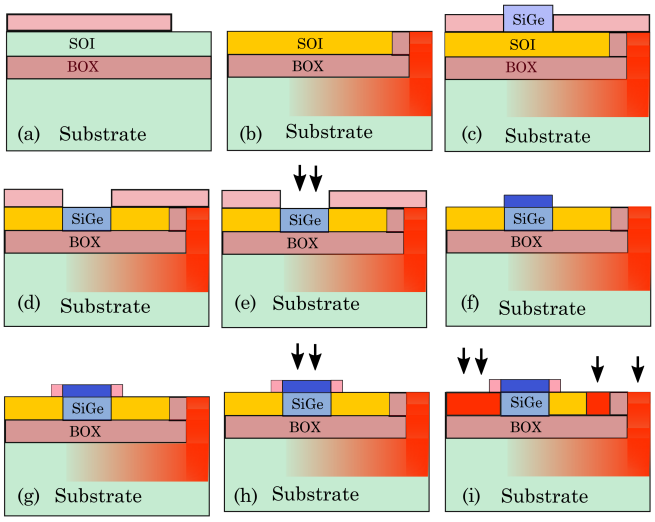

Fig. 11: The simplified process flow is as follows (a) STI formation (b) entire SOI doping and substrate doping shown in one figure (note: to keep the flow simple, multiple steps like BOX oxide etching for substrate contact, etc., that exists between step (a), and (b) are skipped) (c) base pattern and SiGe deposition after oxidation (d) germanium condensation (e) base implant and rapid thermal annealing (RTA) (f) poly-base growth (g) spacer formation (h) base-poly doping (i) emitter, collector doping, and final device. To be noted: germanium mole fraction kept to be 20% which falls within the well-suited range of high-quality SiGe base formation.

While fabricating a lateral device within a BiCMOS framework, the main deviation from the CMOS process line occurs in the realization of the SiGe base. Fortunately for the lateral

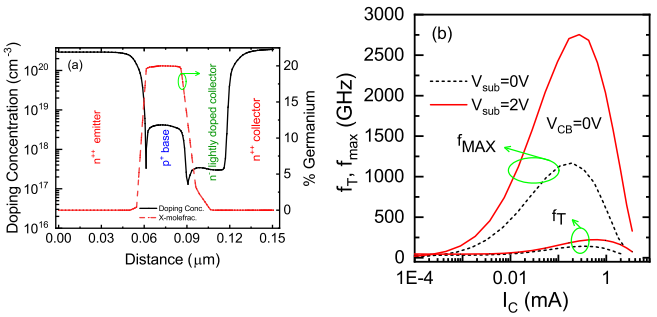

Fig. 12: (a) Doping profile of the LHBT device after following the discussed process flow, and corresponding (b) f_T, f_{MAX} at different substrate bias, V_{CB}=0 V.

SiGe HBT, it does not require any additional mask saving the overall process cost. In fact [27] has demonstrated condensation as the method of choice to achieve high-quality SiGe with a germanium mole fraction up to 30%. The base realization can start with patterning the base region and depositing SiGe on top of the base by a low pressure chemical vapor deposition (LPCVD) method. This SiGe layer, when oxidized, will give an excellent crystalline SiGe [17]. Then poly-silicon deposition has been done with the same base mask to have a 20 nm extrinsic base region. The spacer can be formed around the anisotropically grown poly-silicon with 5 nm nitride and 3 nm oxide. Then a mask can be used to cover the base and n-LDC region and heavy does implantation of arsenic is carried out to realize the emitter and collector regions. Base poly-silicon is separately doped reusing base mask to extract the base contact. The doping profile of the device and corresponding f_T, and f_{MAX} obtained after following the above-discussed process flow is shown in Fig.12.

V. Discussion And Conclusion

The proposed lateral SiGe HBT architecture suitably designed in advanced FDSOI nodes presents a number of advantages compared to the conventional vertical SiGe HBTs. The first advantage concerns the trade-off between C_{jBE} and r_{bi}. In a conventional vertical HBT, the base is highly doped to obtain a low r_{bi} and subsequently a high f_{MAX}. However, an increased base doping reduces the BE SCR leading to a higher C_{jBE}. Our new lateral HBT architecture is free from this trade-off. Since the proposed device has dramatically reduced dimensions in the direction perpendicular to the electron flow, r_{bi} component automatically becomes negligible allowing one to work with a relatively lower base doping that effectively reduces C_{jBE}. This results in a significantly high f_{MAX} reaching to THz level.

The second advantage involves the nearly absent parasitic elements due to the significant reduction in the access of internal emitter, base, and collector regions. The peripheral junction capacitances and the buried layer for the collector access are suppressed. The third advantage is the simplified process for realizing an SiGe HBT since the proposed device can be suitably implemented in an advanced FDSOI technology [28].

Finally, the major advantage lies in the configurability of the device, thanks to the asymmetrical structure and a provision of back-bias from the substrate. Indeed, the results reported in this paper demonstrate that the substrate terminal can be judiciously used to adjust the device performance to the requirement of the circuit designer. For example, a positive voltage on the substrate terminal turns the device into a high-speed mode while a negative substrate bias modifies it into a high voltage transistor.

The major drawback of the device concerns its lower current level compared to that in a conventional HBT; however, a multi-finger architecture can partially address this problem. Also, this drawback turns into an advantage in the case of applications involving low power consumption and high-frequency performances. For example, in applications such as $WiGig$ at 60 GHz, it is mentioned in [29] that the 28 nm FDSOI MOSFET requires to be biased at a drain current density of about $\sim$200 μA/μm. Hence, the proposed device has approximately same current density with an equivalent wafer footprint. In addition, the lateral HBT offers the advantage of working at higher voltage (observed from breakdown characteristics in Fig.5(b)) compared to its MOSFET counterpart and the device delivers significantly higher f_{MAX}. Therefore, this new architecture can generate plenty of opportunities for innovative circuit design on SOI technology.

REFERENCES

[1] I.S. Sun, W. T. Ng, K. Kanekiyo, T. Kobayashi, H. Mochizuki, M. Toita, H. Imai, A. Ishikawa, S. Tamura, and K. Takasuka, "Lateral high-speed bipolar transistors on SOI for RF SoC applications," *IEEE transactions on Electron Devices*, vol. 52, no. 7, pp. 13761383, 2005.

[2] G. Avenier, P. Chevalier, B. Vandelle, D. Lenoble, F. Saguin, S. Fregonese, T. Zimmer, and A. Chantre, "Investigation of fully-and partially depleted self-aligned SiGeC HBTs on thin film SOI," in *Proceedings of 35th European Solid-State Device Research Conference, 2005. ESSDERC 2005. IEEE, 2005*, pp. 133136.

[3] Q. C. Ouyang, J. Cai, T. Ning, P. Oldiges, and J. B. Johnson, "A simulation study on thin SOI bipolar transistors with fully or partially depleted collector," in *Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting. IEEE, 2002*, pp. 2831.

[4] S. Fregonese, G. Avenier, C. Maneux, A. Chantre, and T. Zimmer, "Thin film SOI HBT: A study of the effect of substrate bias on the electrical characteristics," *Solid-state electronics*, vol. 50, no. 11-12, pp. 16731676, 2006.

[5] G. Avenier, T. Schwartzmann, P. Chevalier, B. Vandelle, L. Rubaldo, D. Dutartre, L. Boissonnet, F. Saguin, R. Pantel, S. Fregonese, C. Maneux, T. Zimmer, and A. Chantre, "A self-aligned vertical HBT for thin SOI SiGeC BiCMOS," in *Proceedings of the Bipolar/BiCMOS Circuits and Technology Meeting, 2005*. IEEE, 2005, pp. 128131.

[6] M. Schroter, J. Krause, N. Rinaldi, G. Wedel, B. Heinemann, P. Chevalier, and A. Chantre, "Physical and electrical performance limits of high-speed SiGeC HBTspart II: Lateral scaling," *IEEE Transactions on Electron Devices*, vol. 58, no. 11, pp. 36973706, 2011.

[7] J. Hamel, Y. Tang, and K. Osman, "Technological requirements for a lateral SiGe HBT technology including theoretical performance predictions relative to vertical SiGe HBTs," *IEEE Transactions on Electron Devices*, vol. 49, no. 3, pp. 449456, 2002.

[8] R. Dekker, W. van der Einden, and H. Maas, "An ultra low power lateral bipolar polysilicon emitter technology on soi," in *Proceedings of IEEE International Electron Devices Meeting*. IEEE, 1993, pp. 7578.

[9] G. Shahidi, D. Tang, B. Davari, Y. Taur, P. McFarland, K. Jenkins, D. Danner, M. Rodriguez, A. Megdanis, E. Petrillo et al., "A novel high performance lateral bipolar on SOI," in *International Electron Devices Meeting 1991 [Technical Digest]*. IEEE, 1991, pp. 663666.

[10] H. Nii, T. Yamada, K. Inoh, T. Shino, S. Kawanaka, M. Yoshimi, and Y. Katsumata, "A novel lateral bipolar transistor with 67 GHz f_{MAX} on thin-film SOI for RF analog applications," *IEEE Transactions on electron devices*, vol. 47, no. 7, pp. 15361541, 2000.

[11] T. Suligoj, M. Koričić, P. Biljanovic, and K. L. Wang, "Fabrication of horizontal current bipolar transistor (HCBT)," *IEEE Transactions on Electron Devices*, vol. 50, no. 7, pp. 16451651, 2003.

[12] T. Suligoj, M. Koričić, H. Mochizuki, S.-i. Morita, K. Shinomura, and H. Imai, "Horizontal current bipolar transistor with a single polysilicon region for improved high-frequency performance of BiCMOS ICs," *IEEE Electron Device Letters*, vol. 31, no. 6, pp. 534536, 2010.

[13] T. Suligoj, J. Zilak, Z. Osrecki, and M. Koričić, "On the potential of lateral BJTs and SiGe HBTs in advanced CMOS technologies," *ECS Transactions*, vol. 98, no. 5, p. 111, 2020.

[14] J. Cai, T. H. Ning, C. D'Emic, K. K. Chan, W. E. Haensch, J.-B. Yau, and D.-G. Park, "Complementary thin-base symmetric lateral bipolar transistors on SOI," in *2011 International Electron Devices Meeting*. IEEE, 2011, pp. 163.

[15] T. H. Ning and J. Cai, "On the performance and scaling of symmetric lateral bipolar transistors on SOI," *IEEE Journal of the Electron Devices Society*, vol. 1, no. 1, pp. 2127, 2013.

[16] T. H. Ning and J. Cai,, "A perspective on symmetric lateral bipolar transistors on SOI as a complementary bipolar logic technology," *IEEE Journal of the Electron Devices Society*, vol. 3, no. 1, pp. 2436, 2014.

[17] S. Raman, P. Sharma, T. G. Neogi, M. R. LeRoy, R. Clarke, and J. F. McDonald, "On the performance of lateral SiGe hetero junction bipolar transistors with partially depleted base," *IEEE Transactions on Electron Devices*, vol. 62, no. 8, pp. 23772383, 2015.

[18] A. Derrickson, A. H. Peterson, K. English, A. Haslam, S. Nath, and J. F. McDonald, "Assessment of THz performance for a lateral SiGe HBT on SOI with a laterally graded base," *IEEE Transactions on Electron Devices*, vol. 65, no. 11, pp. 47474754, 2018.

[19] J.-B. Yau, J. Cai, and T. H. Ning, "Substrate-voltage modulation of currents in symmetric SOI lateral bipolar transistors," *IEEE Transactions on Electron Devices*, vol. 63, no. 5, pp. 18351839, 2016.

[20] U. Manual and J. Version, "Synopsys TCAD sentaurus", *Synopsys, San Jose*, CA, USA, 2017.

[21] S. R. Panda, S. Fregonese, M. Deng, A. Chakravorty, and T. Zimmer, "TCAD and EM co-simulation method to verify SiGe HBT measurements up to 500 GHz," *Solid-State Electronics*, vol. 174, p. 107915, 2020.

[22] T. Van Vu, D. Celi, T. Zimmer, S. Fregonese, and P. Chevalier,"Advanced Si/SiGe HBT architecture for 28-nm FD-SOI BiCMOS," in *Bipolar/BiCMOS Circuits and Technology Meeting (BCTM)*, 2016 IEEE, 2016.

[23] J. Korn, H. Rücker, and B. Heinemann, "Experimental verification of TCAD simulation for high-performance SiGe HBTs," in *2017 IEEE 17th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF)*. IEEE, 2017, pp. 9496.

[24] J. Van Den Biesen, "A simple regional analysis of transit times in bipolar transistors," *Solid-State Electronics*, vol. 29, no. 5, pp. 529534, 1986.

[25] B. Heinemann, H. Rücker, R. Barth, F. Barwolf, J. Drews, G. Fischer, A. Fox, O. Fursenko, T. Grabolla, F. Herzel et al., "SiGe HBT with f_x/f_{max} of 505 GHz/720 GHz," in *2016 IEEE International Electron Devices Meeting (IEDM)*. IEEE, 2016, pp. 31.

[26] P. Chevalier, G. Avenier, G. Ribes, A. Montagn'e, E. Canderle, D. C'eli, N. Derrier, C. Deglise, C. Durand, T. Qu'emerais et al., "A 55 nm triple gate oxide 9 metal layers SiGe BiCMOS technology featuring 320 GHz f_t/370 GHz f_{max} HBT and high-Q millimeter-wave passives," in *2014 IEEE International Electron Devices Meeting*. IEEE, 2014, pp. 39.

[27] M. Park and W. S. Choi, "New graded Ge condensation method for formation of Ge-on-insulator layer," *Journal-Korean Physical Society*, vol. 51, no. 3, p. 1100, 2007.

[28] P. Chevalier, G. Avenier, E. Canderle, A. Montagn'e, G. Ribes, and V. Vu, "Nanoscale SiGe BiCMOS technologies: From 55 nm reality to 14 nm opportunities and challenges," in *2015 IEEE Bipolar/BiCMOS Circuits and Technology Meeting-BCTM*. IEEE, 2015, pp. 8087.

[29] N. Planes, S. Kohler, A. Cathelin, C. Charbuillet, P. Scheer, and F. Arnaud, "28 FDSOI technology for low-voltage, analog and RF applications," in *2016 13th IEEE International Conference on Solid-State and Integrated Circuit Technology (ICSICT)*. IEEE, 2016, pp. 1013.