



**HAL**  
open science

## SiGe-based Nanowire HBT for THz Applications

Soumya Ranjan Panda, Sebastien Fregonese, Anjan Chakravorty, Thomas Zimmer

► **To cite this version:**

Soumya Ranjan Panda, Sebastien Fregonese, Anjan Chakravorty, Thomas Zimmer. SiGe-based Nanowire HBT for THz Applications. IEEE Electron Devices Technology and Manufacturing (IEEE EDTM) Conference 2023, Mar 2023, SEOUL, South Korea. hal-04037313

**HAL Id: hal-04037313**

**<https://hal.science/hal-04037313>**

Submitted on 20 Mar 2023

**HAL** is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.

Copyright

# SiGe-based Nanowire HBT for THz Applications

Soumya Ranjan Panda<sup>1,2</sup>, Sebastien Fregonese<sup>1</sup>, Anjan Chakravorty<sup>2</sup> and Thomas Zimmer<sup>1</sup>

<sup>1</sup>IMS Laboratory, University of Bordeaux, Talence, 33400, France, email: [soumya-ranjan.panda@u-bordeaux.fr](mailto:soumya-ranjan.panda@u-bordeaux.fr)

<sup>2</sup>Indian Institute of Technology, Madras, Chennai, India

**Abstract**— This paper proposes a novel 3D nanowire (NW) based SiGe HBT for the first time. The overall purpose is to estimate the RF performance of an NW device based on the state-of-the-art B55 technology from STMicroelectronics. The challenges associated with the device fabrication and corresponding solutions are briefed. The proposed NW-HBT array predicts an  $f_{MAX}$  ( $> 900$  GHz) that is more than twice of that obtainable from the corresponding bulk SiGe HBT. (**Keywords:** SiGe HBT, Nanowire,  $f_{MAX}$ )

## I. INTRODUCTION

Even after 75 years of the first bipolar transistor, untiring research particularly focusing on the devices high-frequency performance is still ongoing. High-speed III-V technologies exhibit fairly low integration levels and yield; hence, unlike SiGe BiCMOS technologies, they cannot leverage today's process scaling to explore its full capacity in order to enable more complex mm-Wave systems and to feed the required wafer volume for the exponentially growing market. On the other hand, SiGe BiCMOS technologies offer superior performance like high gain, low noise figure, and low power consumption at high frequencies compared to CMOS-only technologies. Therefore, today SiGe BiCMOS is the technology of choice for demanding (sub) mm-wave applications [1].

Among all the advancements in MOS domain, gate-all-around (GAA) architecture is one of the most promising technologies. The purpose of GAA NW is to offer improved gate control over the channel. Unlike in MOS NW transistor, objective of the NW-HBT is to reduce the external parasitic RC time constants by removing the extrinsic component of a conventional bipolar device and consequently to achieve an improved RF performance. Due to the removal of the lateral extrinsic regions (or paracitics) of the B55 device from STMicroelectronics [2] [3] [4], the proposed NW architecture yields improved  $f_{MAX}$ .

## II. OPERATION PRINCIPLE AND DEVICE STRUCTURE

The SiGe NW HBT structure (Fig. 1(a)) with doping profile (Fig. 1(b)) is designed and analyzed using commercially available 3D Sentaurus TCAD tool. The results published in [4] substantiate our confidence in the choice of the adopted models along with the parameters and overall calibration of the device simulation environment.

The main challenge of this innovative device lies in the lateral base contact. Three different architectures are investigated as highlighted in Fig. 2(a): (i) device with a uniform radius of

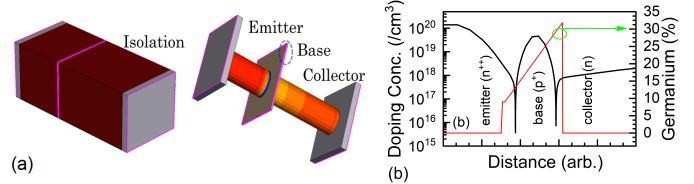


Fig. 1: (a) 3-D view of vertical SiGe NW device with isolation (left), without isolation (right); (b) corresponding doping profile and germanium mole fraction (in %) that are identical with B55 device from STMicroelectronics [4].

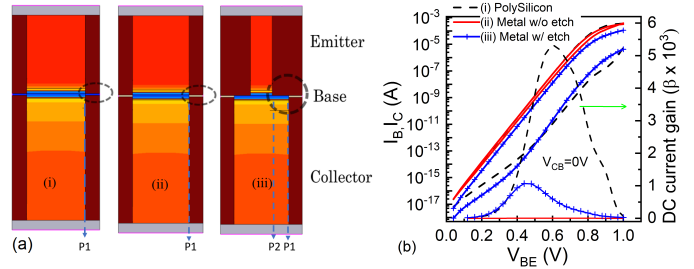


Fig. 2: (a) (i) device with a polysilicon base contact, (ii) same as (i) but with metal base contact, (iii) same as (ii) but with etched emitter; (b) Gummel characteristics for the three chosen devices at  $V_{CB}=0$  V.

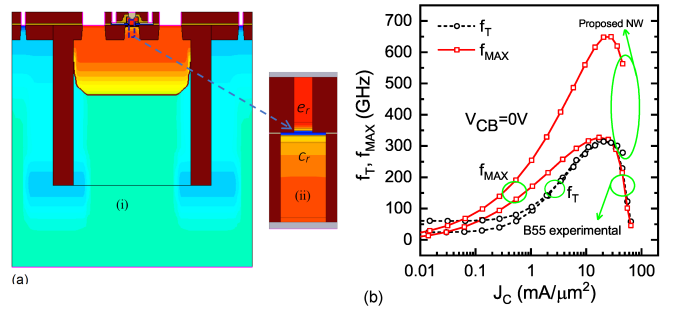


Fig. 3: (a) (left) B55 device from ST Microelectronics [3] [4], (right) proposed NW device; (b) comparison of  $f_T$  and  $f_{MAX}$  of B55 device ( $A_E = 0.09 \times 4.8 \mu m^2$ ) and proposed NW device ( $A_E = \pi (0.025 \mu m)^2$ ).

40 nm from emitter to collector and polysilicon base contact; (ii) same as (i) but with metal base contact; (iii) same as (ii) but with a reduced emitter radius ( $e_r$ ) of 25 nm although the collector radius ( $c_r$ ) remains at 40 nm. The Gummel characteristics of these three different devices are presented in Fig. 2(b). For the device of Fig. 2(a)(i), the base current ( $I_B$ ) is

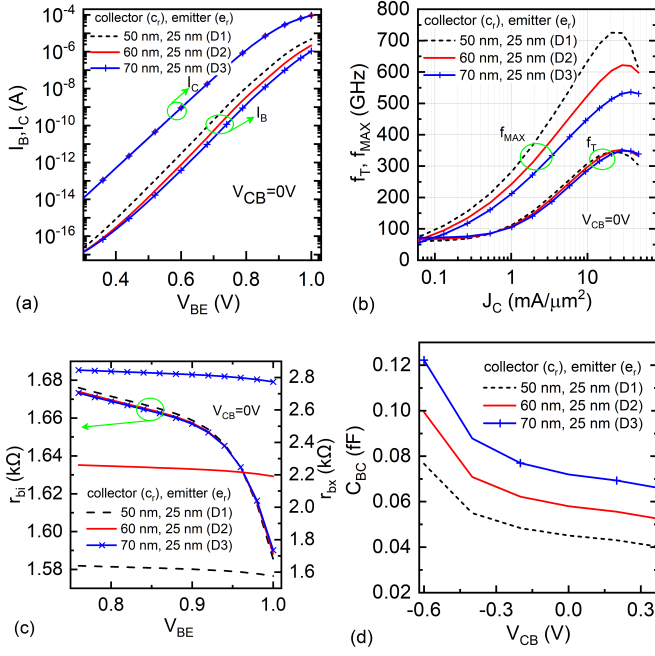


Fig. 4: TCAD simulation results for the NW devices, D1 (with  $e_r=25$  nm  $c_r=50$  nm), D2 (with  $e_r=25$  nm  $c_r=60$  nm) and D3 (with  $e_r=25$  nm  $c_r=70$  nm): (a) comparison of Gummel characteristics; (b)  $f_T$  and  $f_{MAX}$  characteristics at  $V_{CB}=0$  V; (c) variation in intrinsic ( $r_{bi}$ ), extrinsic base resistances ( $r_{bx}$ ) and (d) BC capacitances.

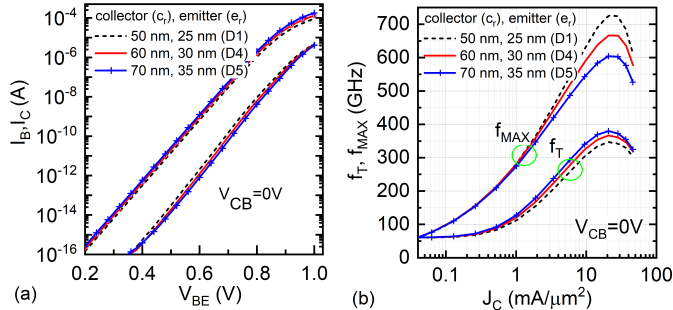


Fig. 5: Comparison of TCAD results for the NW devices, D1 (with  $e_r=25$  nm  $c_r=50$  nm), D4 (with  $e_r=30$  nm  $c_r=60$  nm) and D5 (with  $e_r=35$  nm  $c_r=70$  nm): (a) Gummel characteristics; (b)  $f_T$  and  $f_{MAX}$  vs.  $J_C$  at  $V_{CB}=0$  V.

relatively low, emulating a high DC current gain ( $\beta$ ) of  $\sim 5500$ . However, since realizing a lateral polysilicon contact through isotropic polysilicon layer deposition is nearly impossible, the device in Fig. 2(a)(i) cannot be fabricated with existing state-of-the-art technology. Therefore, we replace this polysilicon contact by metal in subsequent variants. As observed in Fig. 2(b), the simulation of the structure of Fig. 2(a)(ii) shows a significant increase in  $I_B$  (lowering the  $\beta$  to a level slightly  $> 1$ ) due to the very high level of recombination of electrons at the base-metal peripheral interface while being transferred from the emitter to the collector. In order to solve this issue, one

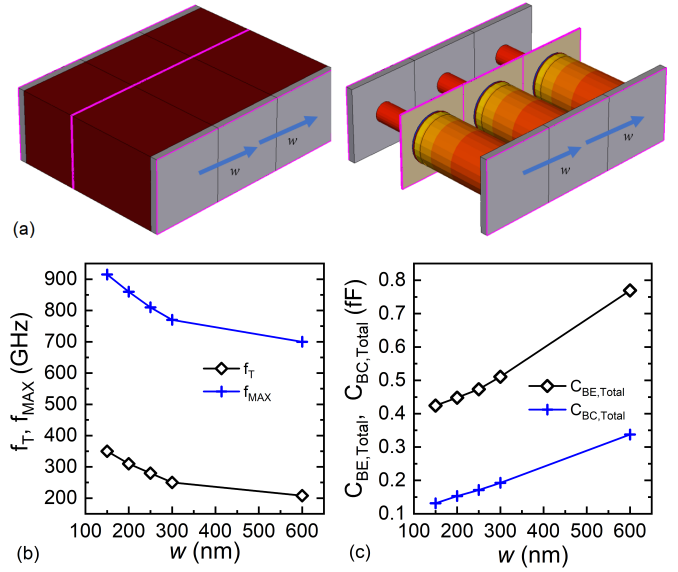


Fig. 6: (a) A vertical NW array of three D1-type devices with  $SiO_2$  isolation (left) without isolation (right); the devices are separated by a distance ( $w$ ). TCAD simulated results for an array of three devices with  $SiO_2$  isolation: (b)  $f_T$ ,  $f_{MAX}$  variation with  $w$ ; maximum  $f_{MAX}$  value of 910 GHz for  $w=150$  nm; (c) variation in the total array capacitances,  $C_{BE,Total}$  and  $C_{BC,Total}$  with  $w$  at  $V_{CB}=0.5$  V.

has to keep the recombination centers away from the carrier flow path. The proposed structure, as shown in Fig. 2(a)(iii), consists of a reduced emitter area introducing a small extrinsic base region that separates the metallic base contact from the internal transistor region. Hence, this arrangement partially suppresses the electron recombination, improving the overall  $\beta$ . Although the reduced emitter area ( $A_E$ ) causes a relatively lower collector current ( $I_C$ ), here the primary requirement is to arrest the electron recombination at the metal-base.

### III. DESIGN OF THE PROPOSED DEVICE

Since the doping profile (Fig. 1(b)) of the proposed device (Fig. 2(a)(iii)) is adopted from the SiGe HBT fabricated in B55 technology from STMicroelectronics (Fig. 3(a)) [3] [4], we compare the RF performance of the proposed NW device with that of the B55 SiGe HBT in Fig. 3(b). We observe a significant improvement in  $f_{MAX}$  in the NW device while  $f_T$  is not altered much. The main purpose of demonstrating both the devices here in Fig. 3(a) is that one can envisage to realize a large area transistor in its *FEOL* using the B55 technology and then to apply a double-etch process for fabricating the proposed NW-HBT. Due to the reduction of lateral parasitics, i.e., reducing the distance from internal base to the external base,  $f_{MAX}$  is significantly improved according to the conventional relation:  $f_{MAX} = \sqrt{\frac{f_T}{8\pi r_b C_{BC}}}$  [2]. As the vertical doping and vertical dimension of the intrinsic transistor are kept unaltered, the base Gummel number does not change [5] resulting in an almost same collector current density ( $J_C = I_C/A_E$ ) at peak  $f_T$  or  $f_{MAX}$  for the B55 and NW HBTs as depicted in Fig. 3(b).

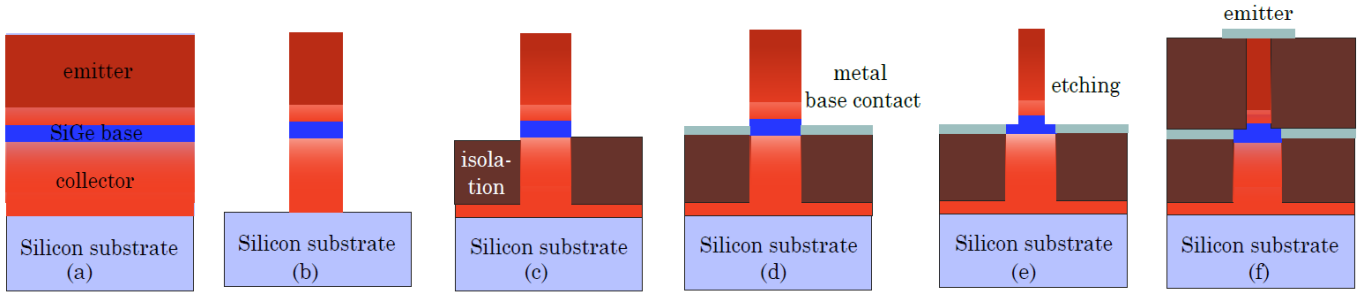


Fig. 7: Fabrication steps: (a) silicon substrate with doping and SiGe base, (b) etching for the nanowire formation, (c) isolation oxide growth, (d) base contact extension, (e) etching for narrow emitter (f) oxide growth for isolation and emitter contact.

#### IV. DEVICE PERFORMANCE AND OPTIMIZATION

Next we vary the device-dimensions of the structure given in Fig. 3(a)(ii) to ensure the best possible RF performance. In a first step, we choose three devices whose  $e_r$  is kept constant at 25 nm while considering  $c_r=50$  nm (D1), 60 nm (D2) and 70 nm (D3). Fig. 4(a) presents the TCAD simulated Gummel plot of these three devices. It is evident that a constant  $e_r$  ensures an invariant  $I_C$ ; however, the  $I_B$  appears to be the least in D3 due to the maximum distance between the electron flow-path and the base metal contact. For the same set of devices,  $f_T$  and  $f_{MAX}$  are plotted in Fig. 4(b) at  $V_{CB}=0$  V. Although a negligible variation in  $f_T$  is observed (up to its peak value) for devices with different  $c_r$ ,  $f_{MAX}$  varies significantly. Since  $e_r$  is fixed, it causes negligible variation in  $I_C$ , transconductance ( $g_m=I_C/V_T$ ), and base-emitter capacitance ( $C_{BE}$ ) leading to comparable  $f_T$  values for the three devices. Although internal base resistance ( $r_{bi}$ ) does not vary for these three devices (Fig. 4(c)), external base resistance ( $r_{bx}$ ) changes from 1.6 k $\Omega$  (for D1) to 2.8 k $\Omega$  (for D3) (see Fig. 4(c)) as the length of the external base increases with  $c_r$ . At the same time,  $C_{BC}$  also increases with  $c_r$  (Fig. 4(d)) due to the overall increase in the base-collector junction area; hence the device D3 shows the maximum  $C_{BC}$ . As both the overall base resistance,  $r_b$  ( $=r_{bi} + r_{bx}$ ) and  $C_{BC}$  are low for D1, it shows the highest  $f_{MAX}$  value among the three variants.

In a second step, we choose another set of three devices where both  $c_r$  and  $e_r$  are varied maintaining a constant ratio,  $c_r/e_r=2$ . Here, along with the device D1 ( $c_r=50$  nm,  $e_r=25$  nm), we chose two more variants, D4 (with  $c_r=60$  nm,  $e_r=30$  nm) and D5 (with  $c_r=70$  nm,  $e_r=35$  nm). Figs. 5(a) and (b) present the Gummel and RF performance FoMs, respectively. Although the DC currents are comparable, it is evident that  $\beta$  increases with larger NW diameters. Also a slightly increasing trend in  $f_T$  is observed with increasing  $e_r$  mainly due to relatively higher contribution of the perimeter capacitance.

In spite of higher  $f_T$ , the largest diameter device (D5) shows the lowest  $f_{MAX}$  value as shown in Fig. 5(b). The only cause of this reduction in  $f_{MAX}$  is the increase in  $C_{BC}$  with NW diameter, since one can analytically prove that D1, D4 and D5 NW-HBTs have identical  $r_b$ . From the results of Fig. 4(b) and

5(b), one observes that the highest  $f_{MAX}$  is achievable from D1.

In order to deliver appropriate power, one NW-HBT is not sufficient and many of them have to be arranged in 1-D or 2-D arrays. A 1-D array of three D1-type NW-HBTs (Fig. 6(a)) is investigated from the perspective of device-to-device separation ( $w$ ) as shown in Figs. 6(b) and (c). It is observed that an increased parasitic capacitance resulting from the device-array with larger  $w$  (see Fig. 6(c)) effectively reduces the  $f_T$  and  $f_{MAX}$  values as demonstrated in Fig. 6(b). The highest  $f_{MAX}$  is found to be more than 900 GHz for  $w=150$  nm. Finally, Figs. 7(a) to (f) briefly present a proposed fabrication procedure partially following the steps reported in [6]. The individual fabrication steps are mentioned within the caption.

#### V. CONCLUSION

A vertical NW SiGe HBT architecture is proposed for the first time. The issue with fabricating the device is identified, and corresponding solutions are discussed. Influences of the cylindrical device dimensions on the frequency behavior are analyzed. We found that the optimized NW-HBT doubles the high frequency performance in terms of  $f_{MAX}$  compared to its bulk SiGe HBT counterpart. In case of an array of NW-HBTs, devices placed with a smaller separation provide better RF performance. However, the proximity to which the devices can be placed during fabrication must be carefully determined.

#### ACKNOWLEDGMENT

We would like to thank Dr. B. Heinemann from IHP Frankfurt (Oder), Germany, and Dr. G. Larrieu from CNRS-LAAS Toulouse, France, for fruitful discussions and valuable technological information.

#### REFERENCES

- [1] T. Zimmer *et al.*, "SiGe HBTs and BiCMOS technology for present and future millimeter-wave systems." IEEE Journal of Microwaves, 2021.
- [2] M. Schroter *et al.*, "Physical and electrical performance limits of high-speed SiGeC HBTs Part II: Lateral scaling", IEEE TED, 2011.
- [3] P. Chevalier *et al.*, "A 55 nm triple gate oxide 9 metal layers SiGe BiCMOS technology featuring 320 GHz  $f_T$ /370 GHz  $f_{MAX}$  HBT and high-Q millimeter-wave passives", IEDM 2014.
- [4] S. R Panda *et al.*, "TCAD and EM co-simulation method to verify SiGe HBT measurements up to 500 GHz", SSE, 2020.
- [5] M. J. Rodwell *et al.*, "Submicron scaling of HBTs", IEEE TED, 2001.
- [6] Y. Guerfi *et al.*, "Vertical silicon nanowire field effect transistors with nanoscale gate-all-around", Nanoscale research letters, 2016.