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IR-UWB Pulse Synthesizer Based on a Sample & Hold Envelope Shaping Circuit

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Abstract— This paper presents an ultra-wideband impulse radio pulse synthesizer circuit based on a gated voltage-controlled oscillator and an envelope shaping circuit, which deploys a sample & hold envelope synthesis. The envelope shaping circuit is mainly composed by parallel shift registers loaded in a parallel manner. The use of a sample & hold envelope enables the reduction of circuit complexity, size area and leakage power. The pulse synthesizer is designed in FD-SOI 28 nm CMOS technology with a supply voltage of 1 V. It can be programmed to address all the IEEE 802.15.4 standardized channels and respects the FCC indoor spectrum requirements. Moreover, it can be turned-on and turned-off which allows to generate nanosecond pulses, where the generated pulse amplitude, central frequency, width, and repetition frequency can be tuned.

Keywords— FCC regulations, IEEE standards, Impulse Radio, Low power, Pulse Generator, Spectral masks, UWB.

I. INTRODUCTION

Since the Federal Communications Commission (FCC) has authorized Ultra-Wideband (UWB) communications in the 3.1-10.6 GHz frequency band, several technologies have been developed in order to exploit it, mostly the Impulse Radio (IR) communications [1-2]. It is essential to develop low-power and high data rate transmission circuits in order to attend the demand of the high-quality data transfer within short-medium range coverage, given that wireless transmission chains usually consume the majority part of the system power budget [3]. The ultra-wideband impulse radio (IR-UWB) is a technique which consists in low duty cycle short duration pulses transmission and has demonstrated low-power consumption and high data rates capabilities thanks to its large spreading factor and lower power spectral density. It is also well-suited for applications as Wireless Personal Area Network (WPAN), and Wireless Body Area Network (WBAN) [4]. Since the transmitter only needs to be operational when the pulse is emitted, the IR-UWB signal presents a gated-cycled nature, resulting in high energy efficiency [5].

Several IR-UWB pulses generation techniques were reported in literature. A first one is based on an edge combiner, which uses simple logic gates to combine two or more delayed logic signals [6-7]. It is simple to integrate in CMOS technology and also presents a low-power consumption. A second one consists in the multiplication of a carrier generated by an oscillator with a baseband pulse, where this architecture has presented a better power consumption and pulse magnitude than the first technique, although the oscillator has leakage issues [8-9]. Ring oscillators can be used as the local oscillator to be modulated for the pulse generation. The IR-UWB circuits are susceptible to process-voltage-temperature (PVT) variations which reduce their performances, regarding the emitted pulse power spectrum density (PSD) shape and amplitude.

Furthermore, the output pulse waveform shaping control is important to ensure that the output pulse PSD fits in the FCC and IEEE standards.

Gaussian pulse shape allows to optimize the bandwidth and sidelobe rejections leakage to respect the FCC spectral masks. However, this pulse shape claims a more complex circuit design and presents higher power consumption. On the other hand, the triangular-shaped pulse has a more straightforward design, lower power, and area requirements. However, to reduce more the complexity of the pulse shaping method, sample & hold envelopes can be applied [8].

In this paper, an IR-UWB pulse synthesizer, that covers the 3.1-10.6 GHz FCC band and fulfils the IEEE 802.15.4 standard requirements is proposed. The IEEE 802.15.4 standard defines 15 channels divided in 3 groups (sub-GHz, low, and high band), where each channel has a central frequency and a 3 dB attenuation bandwidth. For a particular group, an UWB device must cover at least one specific channel, where the mandatory ones are 0, 3, and 9. The proposed circuit is a synthesizer based on a local oscillator with a pulse shaper circuit, where this last one is the focus of this work. The envelope control circuit consists of several shift registers charged in parallel manner, targeting to shape the generated pulse whose envelope approximates the targeted envelope using a on sample & hold method. Indeed, the envelope control circuit modulates the amplitude of the pulses generated by the oscillator. The envelope shape and the pulse duration are critical to have a pulse spectrum that fits in spectrum masks defined by the IEEE 802.15.4 standard, given that those delimits the UWB pulse frequency bandwidth and its power spectrum density (PSD). Finally, since the pulse synthesized is based on a gated oscillator, it can be powered down between two consecutives emitted pulses, hence consuming only during a pulse transmission.

This paper is organized as follows. Section II discusses several IR-UWB pulses envelopes, mainly the sampled & hold, that is applied on the pulse synthesizer. Section III focuses on the envelope control circuit architecture designed with a FD-SOI 28 nm design kit. Finally, simulation results in section IV demonstrate that pulses generated by the synthesizer address IEEE 802.15.4 standardized channels and respect the FCC regulations.

II. IR-UWB PULSE ENVELOPPES

In the IR-UWB pulse generator design, the shape of the transmitted pulse envelope is critical to achieve a pulse frequency response which complies with the standard spectrum masks. The pulse envelope has a major effect over pulse spectrum side lobes levels. For an oscillator generating sinewave signal, the pulse waveform $p(t)$ can be expressed as follows:

$$p(t) = x(t) \cos(2\pi f_M t - \varphi) \quad (1)$$

where $x(t)$ represents the pulse envelope, f_M the frequency for which the pulse spectrum density is maximum, and φ the sinewave phase. The mono-lateral Fourier transform of the emitted pulse can be written as:

$$P^+(f) = \frac{1}{\sqrt{2}} X(f - f_M) \exp(-j\varphi) \quad (2)$$

where $X(f)$ is the envelope Fourier transform. Three types of envelopes shapes are addressed in this work: rectangular, triangular, and sample & hold triangular. The most trivial to generate, the rectangular envelope based on a rectangular function $\Pi_T(t)$, thereby expressed as follows:

$$x_R(t) = A \cdot \Pi_T\left(\frac{t}{\tau_p}\right) \quad (3)$$

where A and τ_p are the generated pulse amplitude and width, respectively. This envelope performs a rectangular windowing over the signal generated by the local oscillator. The rectangular envelope Fourier transform is:

$$X_R(f) = A \cdot \tau_p \text{sinc}(\pi f \tau_p) \quad (4)$$

The duration τ_p of $p(t)$ can be expressed as a function of the oscillation frequency f_m as follows:

$$\tau_p = \frac{N}{2f_M} \quad (5)$$

where N is the integer number of sinusoidal half-periods of the generated pulse. However, the minimal pulse width, in relation of the bandwidth BW_{-XdB} , can be written:

$$\tau_{p-\min} = \frac{\alpha}{2BW_{-XdB}} \quad (6)$$

where α is a coefficient that has a value of 1.8, 3 and 10.8 when the targeted attenuation XdB is 3 dB, 10 dB and 18 dB, respectively. Fig. 1 presents a pulse waveform and spectrum, addressing the channel 3 ($BW_{-3dB} = 499$ MHz) from IEEE 802.15.4 standard, having a rectangular envelope. From Fig.1, it can be noticed that the signal spectrum fits into the IEEE 802.15.4 mask, nevertheless the signal bandwidth for an attenuation of 10 dB is not wide enough to be considered as an UWB signal, where the minimum required is 500 MHz or 20% of the carrier frequency according to FCC regulations [2].

The triangular envelope is defined by the following expression:

$$x_T(t) = \begin{cases} A \left(1 - \frac{2|t|}{\tau_p}\right) & \text{if } 0 < |t| \leq \frac{\tau_p}{2} \\ 0 & \text{if otherwise} \end{cases} \quad (7)$$

The triangular envelope Fourier transform can be computed as:

$$X_T(f) = A \cdot \tau_p \text{sinc}^2(\pi f \tau_p) \quad (8)$$

For the triangular envelope, the pulse minimum width τ_p can be calculated in (6), however with α with a value of 2.56, 4.49, or 5.68 when the attenuation is 3 dB, 10 dB or 18 dB respectively. Fig. 2 displays a pulse waveform and spectrum, addressing the channel 3 ($BW_{-3dB} = 499$ MHz)

from IEEE 802.15.4 standard, having a triangular envelope. From Fig 2, it can be noticed that the spectrum from Fig. 2 fits into the IEEE 802.15.4 masks and presents side-lobes with lower power spectrum density than the rectangular envelope. A digital realization composed of sampled envelopes arises as an exciting and simpler option because the digital cells are not well-suited to produce analog pulse shapes, even though an analog realization of pulse shaper presents better tuning performance. The sample & hold envelope is a combination of rectangular time shifted functions, such that:

$$x_S(t) = \sum_{k=0}^{K-1} x_C\left(k\tau_e - \frac{K-1}{2}\tau_e\right) \cdot \Pi_T\left(t - k\tau_e + \frac{K-1}{2}\tau_e\right) \quad (9)$$

where τ_e is the duration of an elementary pulse, K the number of elementary pulses, $x_C(t)$ a waveform defined in a closed interval from $-t_0$ to t_0 , that represents a non-discrete envelope [8]. In this work, the non-discrete envelope is the triangular one. Shifting into frequency domain, the hold & sample envelope Fourier transform can be expressed as:

$$X_S(f) = \exp\left(-j\pi f \tau_e \left(\frac{K-1}{2}\right)\right) \text{sinc}(\pi f \tau_e) \sum_{k=0}^{K-1} X_C\left(f - \frac{k}{\tau_e}\right) \quad (10)$$

Fig. 3 presents an emitted pulse waveform and spectrum, addressing the channel 3 from IEEE 802.15.4 standard, having a sampled & hold envelope. From Fig. 3, it can be noticed that the spectrum from Fig. 3 fits into the IEEE 802.15.4 mask, although it presented stronger side-lobes than the triangular envelope. Therefore, the sample & hold envelope is feasible to be implemented in the IR-UWB pulse synthesizer, reducing its complexity design.

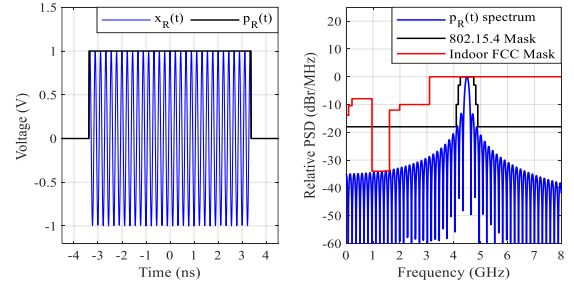


Fig. 1. IR-UWB pulse with rectangular envelope compliant with the channel 3 of IEEE 802.15.4 standard ($BW_{-3dB} = 499$ MHz and $\tau_p = 6.75$ ns).

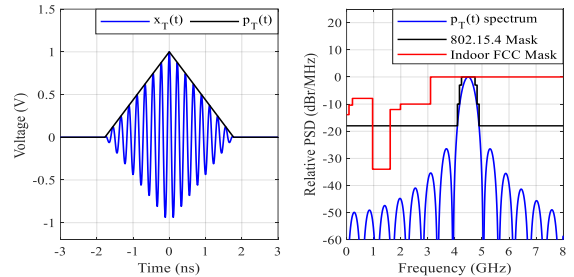


Fig. 2. IR-UWB pulse with triangular envelope compliant with the channel 3 of IEEE 802.15.4 standard ($BW_{-3dB} = 1355$ MHz and $\tau_p = 3.55$ ns).

III. ASSOCIATED PULSE SYNTHESIZER CIRCUIT DESIGN

A. Pulse synthesizer architecture

The IR-UWB pulse synthesizer design is performed to comply with the FCC regulations and the IEEE 802.15.4 standard. Moreover, it targets programmable capabilities for the pulse discrete amplitude, width, and central frequency, thus being capable to address several standardized channels.

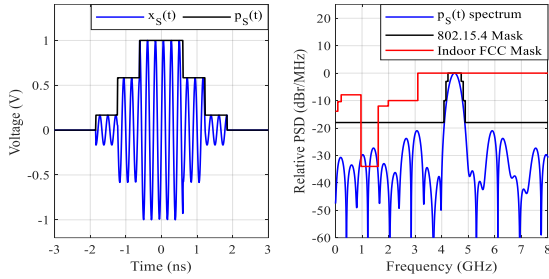


Fig. 3. Example of IR-UWB pulse with sampled & hold envelope compliant with the channel 3 of IEEE 802.15.4 standard ($K = 6$, $BW_{-3dB} = 499$ MHz and $\tau_p = 4$ ns).

This circuit has an architecture based on carrier generation and envelope shaping (Fig. 4). There are three main blocks: (a) carrier generation (Voltage Controlled Oscillator and buffer stage); (b) envelope shaping; and (c) the digital to analog converter (DAC). The first and last blocks have been done in Current Mode Logic (CML), that is a differential digital logic family, commonly used in high-date rate integrated systems. As a matter of simplicity, the VCO, the buffer stage and the DAC are not detailed in this work. The main focus of this paper is the envelope control circuit.

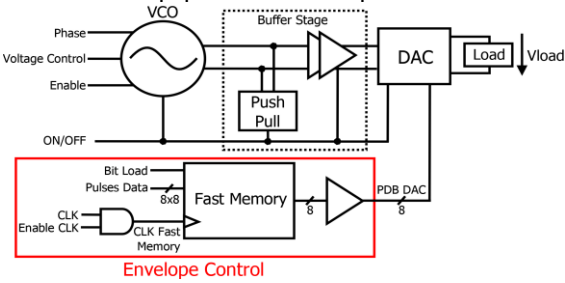


Fig. 4. IR-UWB synthesizer proposed design architecture.

The oscillator controls the pulse central frequency by generating the carrier signal, whereas the shaping circuit controls the pulse amplitude and width. The buffer stage duty is to maintain a good integrity of the VCO output signal throughout the entire frequency band of interest. The DAC performs a PAM modulation on the carrier signal using an 8-bit data bus from the envelope shaping circuit. The modulated signal is the IR-UWB signal, that has a sample & hold envelope and a discrete amplitude. Besides, the proposed architecture allows to turn-on and turned-off the carrier generation circuits and the DAC to reduce the power consumption.

B. Envelope control circuit design

Done in full custom CMOS logic, a digital circuit has been designed whose output is an 8-bit data bus, that addresses the DAC, controlling the IR-UWB pulse amplitude level. This control is done through an 8-byte memory composed by parallel shift registers with parallel loading. Fig. 4 shows the main elements of the envelope shaping circuit: an AND logic gate, a fast memory, and a buffer stage, composed by 8 buffers in parallel.

Among the input signals, the pulse data is an 8-byte data bus, where each byte corresponds to one elementary pulse amplitude level. Thus, this signal stocks data for envelope shaping of a pulse composed by 8 sampled pulses. The Fig. 5 shows the chronograms of the envelope control circuit. “D0” to “D7” correspond to sampled pulses amplitude level codified in 8 bits. When no pulse is transmitted, the 8-bit

data bus has null value. The AND logic gate control if the external clock signal arrives at the fast memory. If the “ENABLE CLK” has low logic level, the fast memory clock signal has a low logic level, otherwise, it has the same logic level of the external clock signal. The “ENABLE CLK” has a high logic level for 8 clock cycles. The “LOAD BIT PULSES” is the signal that defines when the fast memory loads the 8-byte data bus. The both signals which are the two first signals displayed in Fig. 5 should not have high logic level at same time. A clock period corresponds to one elementary pulse duration.

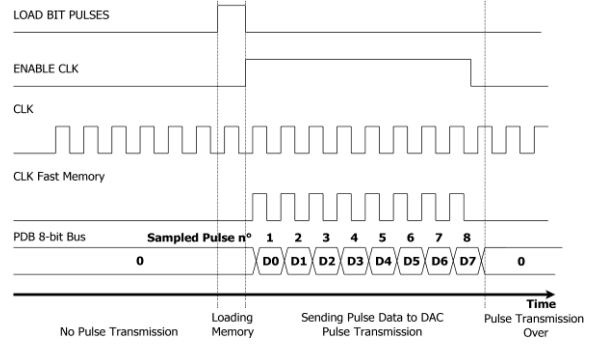


Fig. 5. Chronograms of the envelope control circuit.

The fast memory design is based on 8 parallel shift registers. The shift registers are loaded in a parallel manner. The bit 0 of each byte is generated using one shift register, the bit 1 using another shift register, successively until the bit 7 that requires the eighth shift register. Fig. 6 shows the 8-bit shift register design. The register is composed by D flip-flops, a buffer, NAND gates and inverters. The first sampled pulse data load the last D flip-flop, whereas the last sampled pulse data the first D flip-flop. For example, considering that “Bit load” has a high logic level, if “dataP7” signal has a high logic level, the first D flip-flop will be set, hence its output has high logic level. After the shift register load, the pulse amplitude data will propagate through the D flip-flops. After 8 clock cycles, all D flip-flops will have an output signal with low logic level.

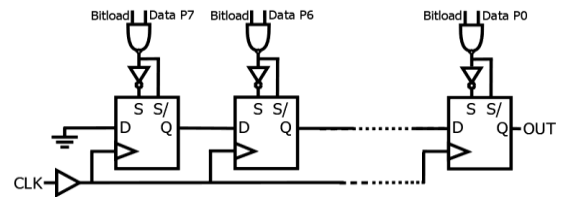


Fig. 6. Schematic of the proposed shift register with parallel loading

IV. SIMULATION RESULTS

This section presents transient simulation results of the programmable IR-UWB pulse synthesizer. The proposed circuit has been implemented using the FD-SOI 28 nm CMOS design kit from STMicroelectronics, with a supply voltage of 1 V. During the schematic design, parasitic capacitances have been estimated at each node, relying upon a more realistic simulation. The values of the parasitic capacitances were extracted from a parasitic extraction of another previous design. The main goal here is to observe the IR-UWB pulse waveform and spectrum, mainly if this complies with the IEEE 802.15.4 standard and FCC

regulations masks. Here, all the generated pulses have an envelope sampled from a triangular continuous envelope, with $K = 6$. The Figs. 7, 8 and 9 shows IR-UWB pulses and its related power spectrum density (PSD), addressing the IEEE 802.15.4 standardized channels 1, 14 and 15, respectively. Table I indicates the IR-UWB pulses parameters for every addressed channel.

In Figs. 7, 8, and 9, it can be noticed that the three presented generated pulses respect the IEEE 802.15.4 standard masks. Even though some IR-UWB pulses did not respect the FCC indoor masks, in particular for 0.5-2 GHz bandwidth, this is not a major concern because the UWB antenna filters the signal within this frequency bandwidth. In terms of power consumption, the simulated pulses from The power consumption of the envelope shaping circuit when it generates pulses shown on Figs. 7, 8, and 9 is 16.83 pJ/pulse, 14.17 pJ/pulse and 9.30 pJ/pulse respectively and the overall pulse synthesizer power consumption is 182.35 pJ/pulse, 298.09 pJ/pulse and 120.43 pJ/pulse, respectively. Table II presents a state of art comparison of the recent pulse synthesizer designs that have been reported in the literature. The IR-UWB pulse synthesizer presented in this work presents the widest F_c range.

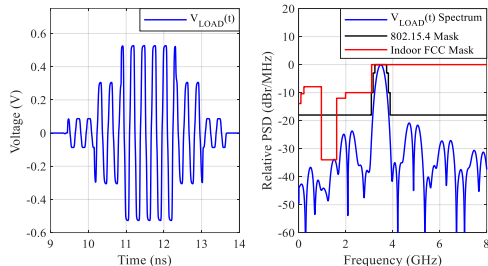


Fig. 7. IR-UWB pulse for the channel 1 of the IEEE 802.15.4 standard.

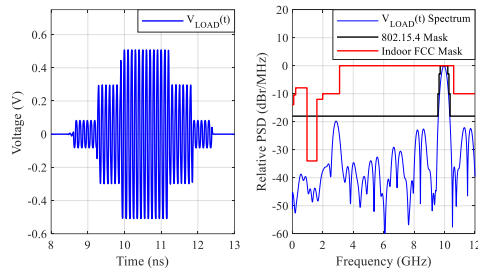


Fig. 8. IR-UWB pulse for the channel 14 of the IEEE 802.15.4 standard.

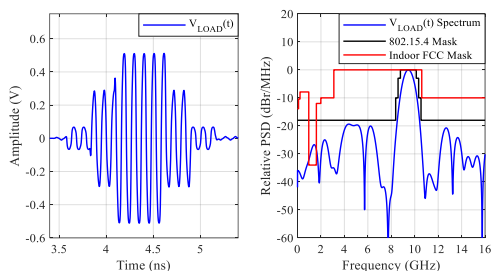


Fig. 9. IR-UWB pulse for the channel 15 of the IEEE 802.15.4 standard.

V. CONCLUSION

In this paper, an IR-UWB pulse synthesizer based on a local oscillator and an envelope shaping has been presented. It is mainly composed by a gated voltage-controlled oscillator, an 8-bit DAC, and an envelope control circuit formed by parallel shift registers. The envelope applied in the pulse synthesizer is the sample & hold, which requires a less complex envelope shaping circuit architecture. The

pulse synthesizer has been designed in FD-SOI 28 nm CMOS technology from STMicroelectronics. The simulation results show that this circuit is capable to address the IEEE standardized channels and respect the FCC indoor regulations.

TABLE I. GENERATED IR-UWB PULSE PARAMETERS

Channel	1	14	15
VCO voltage control (mV)	500.58	192.88	216.26
Central Frequency (MHz)	3494	9984	9484.8
BW _{-3dB} (MHz)	499	499	1355
Sampled pulse duration (ps)	716	651	256
Pulse total duration (ps)	4296	3906	1536

TABLE II. STATE OF THE ART COMPARISON

	This Work ^a	[5]	[7]	[8]	[9]
Techno.	FD-SOI 28 nm	65 nm	130 nm	65 nm	90 nm
Power Supply (V)	1	1.2	1.2	1.2	0.9
F_c (GHz)	3-12	6.5-8	3-5	3-5	3.1-5
BW _{-3dB} (GHz)	0.5-1.3	0.5	0.5-1.3	0.5-1.3	0.5-1.4
Amplitude (V)	0.53	0.45	0.45	0.4	0.09-0.12
E_{ac} (nJ/pulse)	0.16	0.048	0.146	1.9	NA
Static power (μ W)	27	0.48	100	NA	170
Architecture	LO based	Edge Combiner	Edge Combiner	LO based	LO based

^aSimulation results with parasitic capacitances

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