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► **To cite this version:**

Jean-Pierre Chante, Dominique Tournier, Dominique Planson, Christophe Raynaud, Mihai Lazar, et al.. SiC-based current limiter devices. International Conference on Silicon Carbide and Related Materials (ICSCRM'2003), Oct 2003, Lyon, France. pp.951-956, 10.4028/www.scientific.net/MSF.457-460.951 . hal-04032970

HAL Id: hal-04032970

<https://hal.science/hal-04032970>

Submitted on 16 Mar 2023

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SiC-based current limiter devices

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Keywords : Silicon carbide, current limiter, JFET, protective devices, high voltage

Introduction

Since the early 90's, Cree Research supplies SiC wafers. Only a few number of components had been realized, mainly low or very low power devices, although material properties seemed to be very interesting for power or high frequency electronics. A great number of research studies have then been conducted to demonstrate the real potentialities of this material in different applications such as high voltage, high current densities and high frequency devices. The feasibility of such devices has therefore been demonstrated but without a significant technological breakthrough justify their development from an economic point of view, except for the Schottky diode in a voltage range up to 1500 V. The SiC Schottky diode is a good example of component able to replace fast bipolar diodes made from Si PN junctions. For example, they should increase both the efficiency and reliability of power converters if they are especially designed by taking into account the use of these SiC high voltage Schottky diodes. The interest in SiC for high and very high voltages (up to 20 kV) is motivated by real needs. However the reduced financial markets are not economical promoter for the development of this material. In the opposite, in the mean power range, some specific components which benefit from SiC characteristics such as protective devices can open important markets, in addition to Schottky diodes. Indeed these components must sustain very high powers, ie. sustain high current intensities under high voltages. The aim of this paper is to show a serial protective component made of SiC, to demonstrate the technological step from a power density and/or current density point of view.

Serial and parallel protection

Generally, all electronic systems need to be protected against over-voltages due to electrostatic discharges (ESD) or lightning for example. A component set in parallel (PP) to the equipment that must be protected, have to, in a very short time, limit the voltage between its electrodes, and evacuate the high energy of the discharge. In power electronics, over-current can appear due to a short circuit of the load for example. A component set in series (SP) with the equipment to protect must, in a very short time also, limit or stop the current flow in order to avoid more important damages and to allow the working of the rest of the installation. The serial component must therefore be able to sustain very high power during a long enough time to allow an easier intervening (using a mechanical break-over). Figure 1 shows how the two kinds of protective components (PP and SP) are connected.

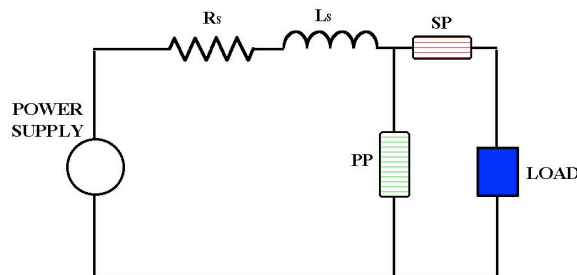


Figure 1. Protection devices implementation (parallel : PP and serial : SP).

Parallel protection

The role of this protection is to maintain the voltage within acceptable limits by the circuit to protect and to evacuate energy of the parasitic bias impulse which cause the over-voltage. Several kinds of components exist, known as « transient voltage suppressor » but none is really satisfying and circuit designers used several of them to obtain at once: short response times, efficient limitation of the voltage to the desired value, and good ability to evacuate the energy. The transient voltage suppressor component must have a very high impedance in the off-state, a low or controlled voltage drop under high current level in the on-state (V_{on}). To satisfy this role, some voltage limiter components exist such as varistor [1], junction diodes used in reverse bias, components with discontinuous characteristics (i.e. gas discharger tube [2]), and semiconductor components with “turning over” [3]. Figure 2 illustrates Current-Voltage (I-V) characteristics of parallel protective device.

Serial protection

In case of a current overload or more especially during a short circuit of the load, the role of the device is to limit the current to an adequate value. That allows faster and simpler electromechanical switching than if the current had increased up to its huge short-circuit value. Figure 3 shows the current waveforms without current limitation, and with a serial protective (controlled or not). The component can be able to interrupt itself the current flow, which is an ideal case. Serial protection is mainly performed reversibly by a circuit breaker, or irreversibly by fuses. Others devices based on polymers [4, 5] or superconductors [6, 7, 8] allows to drastically increase the resistance during the short-circuit, but only a few component or semiconductor systems operate in this manner. Because the serial limiter is connected in series with the system to protect, it must have the lower voltage drop in the on state (passive state). In the active state, it must be able to dissipate a high energy during a rather long time to allow to cut the energy sources.

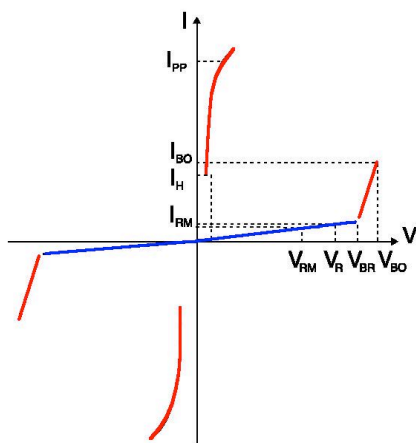


Figure 2 Current-Voltage (I-V) characteristics of parallel protective device

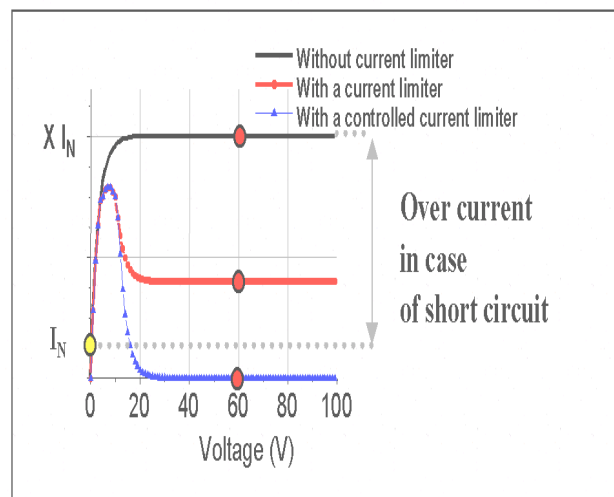


Figure 3 Current waveforms with and without current limitation.

Silicon carbide and protective components

In both serial and parallel protection, components must sustain very high energies during long times, in order to preserve their characteristics even at high temperature. They also must have very short response time to react before the system that must be protected.

Examples of ideal electrical behaviours of these components are given hereafter. For a serial protection able to work on the distribution network (240 V), the breakdown voltage must be as high as 600 V and for domestic apparatus, nominal current is in the range 1-10 A. For the parallel protection of the same kinds of apparatus, the component must limit the voltage to values in the

range of several volts to 500 V for example, and must be able to sustain a current flow in the range of several Amperes to several decades of Amperes during a few ms.

To obtain previous characteristics and a low on-state voltage drop, some trade-off are needed. SiC appears to be a good candidate to reach those requirements. It is indeed well known today that the resistance of an SiC layer is about 25 times lower than a Si layer able to block the same voltage (as shown in Fig. 4). This property is due to the high critical electric field in SiC and allows to obtain low V_{on} even under high current density.

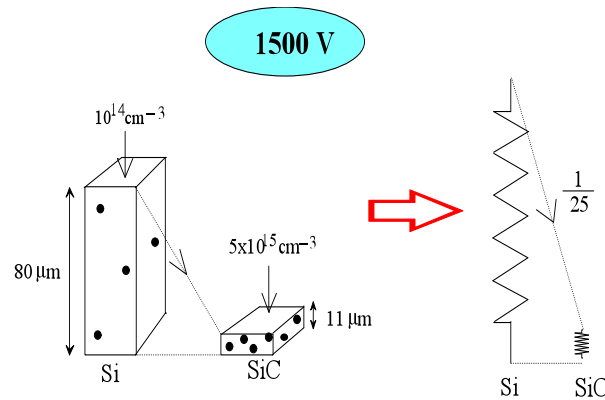


Figure 4. Schematic representation of Si and SiC layers needed to sustain 1500V.

Due to the wide band gap of SiC, which maintains a very low intrinsic carrier concentration up to ~ 1000 K, and to a high thermal conductivity, SiC components are able to correctly work even at high temperature, and subsequently to sustain high power dissipation during long times. So they are in agreement with the required properties of protection components.

Experimental check has been realized in the case of current limiters, as it is described in the following.

Serial protection by current limiters

The current limiter behaviour is preferentially obtained with normally-on components having the lowest specific resistance possible. Two kinds of components, JFET with two electrodes and JFET with gate contact have been designed and fabricated, to underline the capability of these SiC components to work under very high power densities. This choice for unipolar devices is related to the low V_{on} in such devices.

Junction Field Effect Transistor (JFET) [9, 10], without gate control.

This device should be normally-on, without gate control electrode, thereby, in opposite to a conventional MOSFET (that is normally off), a channel is pre-formed. Figure 5 shows the transistor structure similar to that of a vertical power MOSFET. A n-type layer with adequate doping level and thickness is needed on a n^+ -type substrate to sustain the required voltage 600 V. Near the surface, the active area is formed by multiple implantations of aluminium for the p^+ layer and peripheral protections, and of nitrogen for the creation of channel, as well as for n^{++} region source ohmic contact. Finally a SiO_2 layer is thermally grown above the channel.

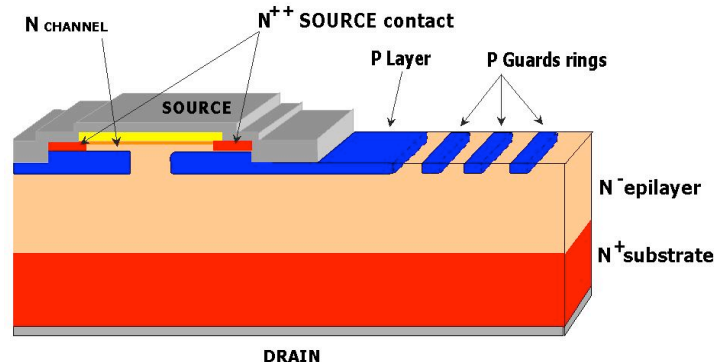


Figure 5

In the passive state, the drain-to-source voltage V_{DS} is positive, so that the current flows successively through the substrate, the epitaxial layer, the region between P^+ layers and then the

channel. When a fault current occurs, due to the increase of V_{DS} , the p^+n junction becomes reverse-biased. The space charge region (SCR) spreads and reduces the channel cross section. Therefore the channel resistance increases rapidly and the current is subsequently limited. The current flow under a high voltage involves high power dissipation in the channel region and so a high increase of the temperature. Finally due to the heating, the carrier mobility decreases, that explains the decrease of the saturation current. After having determined the main parameters such as length, depth and doping level of channel or inter-cell length, electro-thermal simulations allow to know the component behaviour as a function of time, consecutive to a short-circuit. (Figure 6).

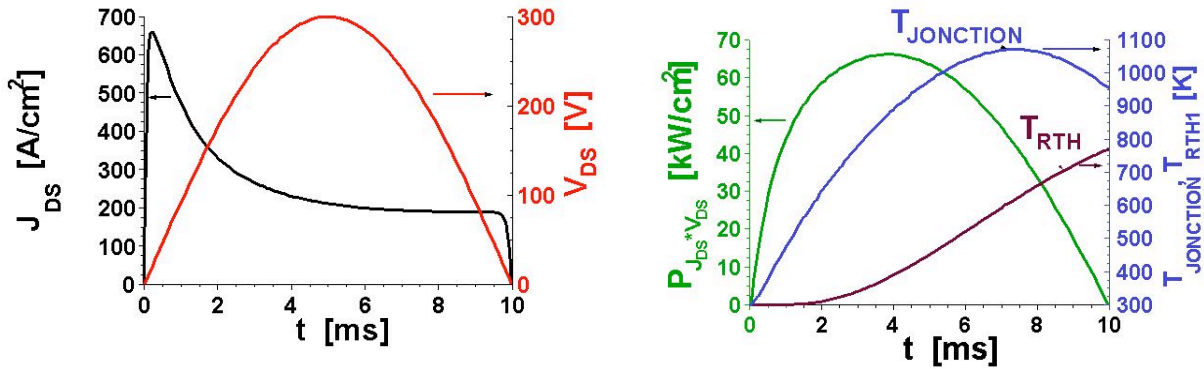


Figure 6

Figure 7 shows schematically the realized structure. Especially the periphery geometry and the center of the cell are detailed. Fabrication has been made in CNM (Centro Nacional de Microelectronica) of Barcelona but the RTA step performed at CEGELY. Figure 8 shows some experimental characteristics measured on these devices. These curves demonstrate the ability of these JFET to work under high voltage with current density as high as 800 Acm^{-2} . The specific on-resistance ($13 \text{ m}\Omega.\text{cm}^2$) is similar to the best published values [XXX].

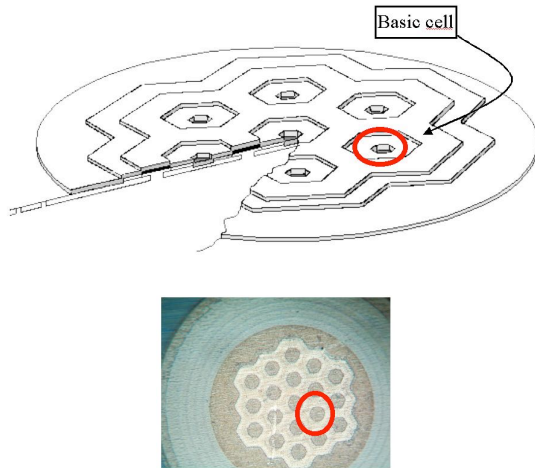


Figure 7 – Schematic and photomicrograph view of the experimental structure

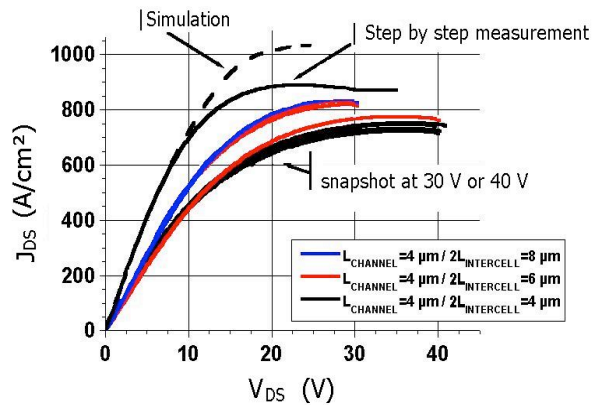


Figure 8 - Experimental $J_{DS}(V_{DS})$ characteristics

This device fully complete the requirements of current limitation but without gate control electrode. This implies the fact that the transistor is unable to control or to stop the current flow by itself. It is also impossible to modulate the epilayer resistivity (i.e. downsize the on voltage drop). A similar structure but with a different layout and p -type buried layers connection (gate and source) has therefore been designed and fabricated.

Vertical VJFET with gate control

The component must sustain 600 V, ensure a continuous current of 1 or 2 A and limit the current to $<10 \text{ A}$, i.e. to a maximum current density of 100 A/cm^2 for a active area of 10 mm^2 . To simplify the

design and mostly optimise the active area/total area ratio, a buried gate has been chosen. Figure 9 shows the geometry and the main parameters of the structure. The optimisation of parameters has been made with ISE simulator software, taking into account realistic doping profiles that were calculated with I²SiC [11], a software based on the Monte-Carlo method.

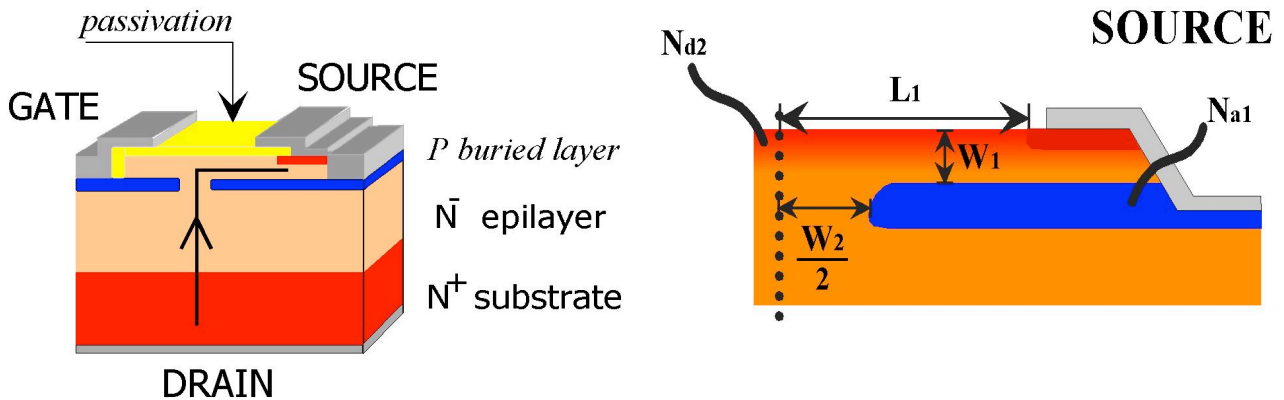


Figure 9

The principle of this component is rather simple. In the on-state, the drain bias is >0 and electrons flow from source to drain through the channel near the surface then through the vertical channel pinched between the gate p^+ contacts. They continue then through the epilayer and the substrate towards the backside contact. In the JFET working mode, a zero bias on the gate ($V_{GS} = 0$ V) gives the best current characteristics. When a fault current occurs, the subsequent increase in V_{DS} results in a high reverse bias of the p^+n junction. The spreading of the SCR due to this reverse bias, tightens the channels and leads to an increase of the resistance. When the SCR meet again, the channel is pinched and the current is limited to a value which decreases in time due to the decrease of the mobility subsequent to the increase of the temperature. The p^+n junction is reversed biased if $V_{GS} < 0$. That allows to control the maximum value of the limitation current and to decrease the dissipated power within the component. On the contrary, a low value of $V_{GS} > 0$ biases the junction in forward direction and the hole injection modulates the n^- layer resistivity and decreases the specific resistance of the component in the passive state. The gate command thus allows to decrease the nominal losses and to control the maximum value of the fault current.

Figure 10 shows one of the geometry among the transistor fabricated by CNM. The active area is 0.006 cm^2 . Experimental static characteristics are given in Figure 11 and underline the capacity to limit the current under high voltage. The other important property of the component is the response time. Figure 12 gives the waveforms of current and voltage when a short-circuit occurs and shows that the continuous regime of limited current is obtained in less than $1 \mu\text{s}$.

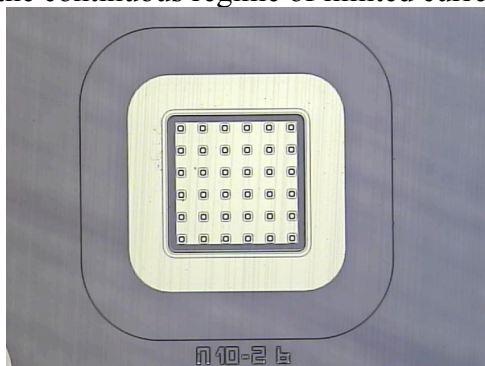


Figure 10

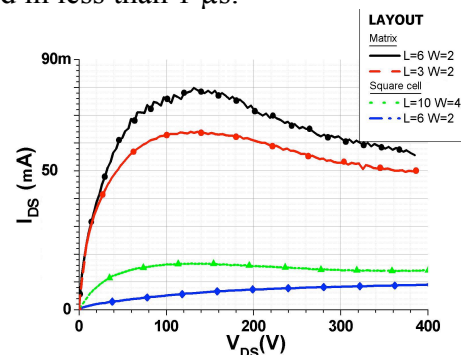


Figure 11

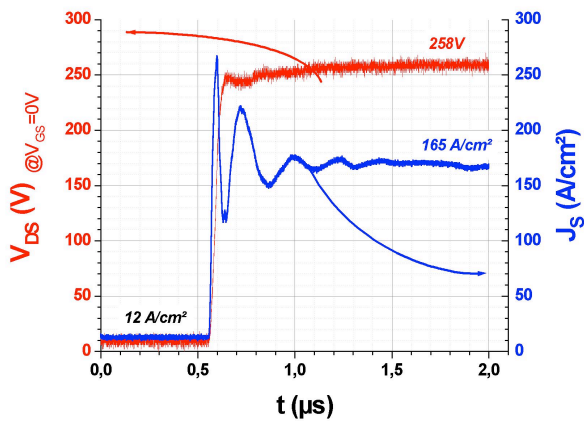


Figure 12

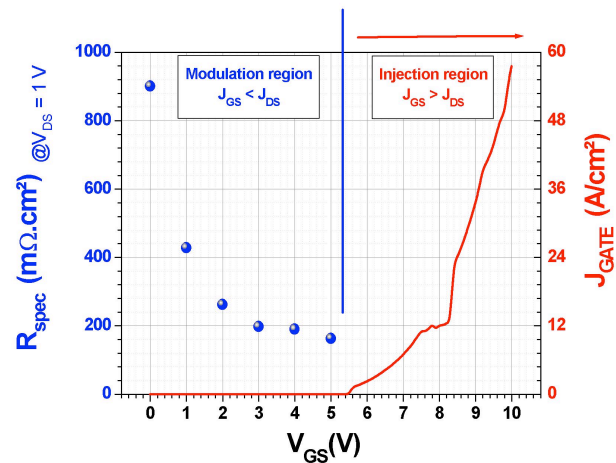


Figure 13

Finally, Figure 13 shows the evolution of the specific resistance in the on-state as a function of the gate bias. As above mentioned, this voltage drop is divided by a factor 4 as soon as $V_{GS} > 5$ V. In these conditions, the hole injection remains weak and the gate current keeps a reasonable value.

Conclusion

Thanks to the properties of SiC, current limiter devices have been fabricated. These devices show a breakdown voltage > 800 V and are able to work in a steady state mode under 400 V, at current density of ~ 150 A.cm⁻², corresponding to a power density of 60 kW.cm⁻². SiC-based current limiters are therefore able to open new future prospects for this material.

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