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Topical Review

Thermal management and packaging of wide and ultra-wide bandgap power devices: a review and perspective

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Abstract

Power semiconductor devices are fundamental drivers for advances in power electronics, the technology for electric energy conversion. Power devices based on wide-bandgap (WBG) and ultra-wide bandgap (UWBG) semiconductors allow for a smaller chip size, lower loss and higher frequency compared with their silicon (Si) counterparts, thus enabling a higher system efficiency and smaller form factor. Amongst the challenges for the development and deployment of WBG and UWBG devices is the efficient dissipation of heat, an unavoidable by-product of the higher power density. To mitigate the performance limitations and reliability issues caused by self-heating, thermal management is required at both device and package levels. Packaging in particular is a crucial milestone for the development of any power device technology; WBG and UWBG devices have both reached this milestone recently. This paper provides a timely review of the thermal management of WBG and UWBG power devices with an emphasis on packaged devices. Additionally, emerging UWBG devices hold good promise for high-temperature applications due to their low intrinsic carrier density and increased dopant ionization at elevated temperatures. The fulfillment of this promise in system applications, in conjunction with overcoming the thermal limitations of some UWBG materials, requires new thermal management and packaging technologies. To this end, we provide perspectives on the relevant challenges, potential solutions and research opportunities, highlighting the pressing needs for device–package electrothermal co-design and high-temperature packages that can withstand the high electric fields expected in UWBG devices.

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Keywords: power electronics, power semiconductor devices, thermal management, packaging, co-design, wide-bandgap, ultra-wide bandgap

(Some figures may appear in colour only in the online journal)

1. Introduction

Power electronics is the technology for electrical energy conversion using solid-state electronics. It is ubiquitously deployed in electric vehicles, data centers, motor drives, electric grids and renewable energy integration. At the heart of power electronics are power semiconductor devices, which are used as solid-state switches in circuits. The global market for power semiconductors reached $40 billion in 2021 and is growing fast [1]. Functioning as solid-state switches, ideal power devices should have minimal resistance when passing an ON-state current, block high voltage in the OFF-state and produce minimal loss during turn-ON/OFF switching.

Conduction and switching losses appear in real-world power devices due to the non-zero ON-resistance (R_{ON}) and the need to extract or supply charges in switching, respectively. These energy losses dissipate as heat, elevating the temperature of the device active junction and the package housing the device. The elevated junction temperature (T_j) could adversely impact the device characteristics as well as the device and package reliability. T_j of commercial power devices is usually limited to below 125 °C–175 °C for long-term, reliable operation [2]. Thermal management, which dictates the heat removal in a device and its package, is thereby a key limiting factor for power device performance and reliability.

In the last two decades, power electronics has witnessed revolutionary advances enabled by devices made of wide-bandgap (WBG) semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN) [3–8]. Owing to their superior material properties such as high critical electric field (E_C), WBG devices can achieve a much lower specific ON-resistance ($R_{ON,SP} = R_{ON}A$, where A is the device area) for the same breakdown voltage (BV), thereby allowing for smaller areas, capacitances, charges and switching losses, as well as higher operating frequencies, compared with similar voltage- and current-rated silicon (Si) devices [9]. The higher frequency and lower losses further enable miniaturization of passive components in power electronics systems, reduce system size, boost power density and enhance efficiency. On the horizon there are power devices made of ultrawide bandgap (UWBG) semiconductors such as gallium oxide (Ga_2O_3), aluminum nitride (AlN), and diamond [10–13]. UWBG devices promise a theoretical $R_{ON,SP}$–BV trade-off superior to their WBG counterparts and are excellent candidates for the next generation of power electronics.

Despite their superior electrical performance, thermal management of (U)WBG devices is more challenging than that of their Si counterparts for three main reasons: (a) since these devices are expected to handle very high power densities while minimizing areal footprint, the combination of high power and small area leads to extremely high heat fluxes which are incredibly difficult to manage; (b) the concurrence of higher current density and electric field (E-field) produces very high local heat fluxes, which can lead to non-uniform temperature distributions and local thermal runaway; (c) for some device structures and materials, there are inherent thermal limitations, which further complicate and exacerbate the problem. For example, in high-electron-mobility transistors (HEMTs), the device active region consists of an extremely thin (∼5 nm) quantum well current channel, i.e. the two-dimensional electron gas channel, where heat generation is spatially confined [14], further increasing the demand for thermal management. Another example is Ga_2O_3, which suffers from a very low thermal conductivity (k_T) of 11–27 W m^{-1} K^{-1} [15, 16] (table 1). This is an order of magnitude lower than that of Si.

Due to these challenges, heat removal has become a key roadblock to exploiting the electrical performance of (U)WBG devices in systems. For instance, the insufficient thermal management requires a larger A for heat dissipation, which compromises the device switching frequency and system efficiency [18]. The thermal issues can also result in de-rating of power devices, i.e. reducing the continuous operating current.

Thermal management in power devices is a multi-dimensional problem. As shown in figure 1, the heat generated at the device junction is usually removed through the package to an area where it can be further dissipated, typically via convection (e.g. air and liquid cooling). The micron- and submicron- sized device structures in the junction area, semiconductor materials and their interfaces, package architectures, packaging materials and cooling techniques all play vital roles in determining the thermal resistance (R_{th}) along the flow of heat, i.e. the junction-to-ambient thermal resistance ($R_{th,j–a}$). Moreover, their roles are usually interdependent. For instance, the cooling and package designs can alter the major heat flow towards the top or bottom side of the chip, under which circumstances $R_{th,j–a}$ would be sensitive to different device structures and material properties within the same device. Hence, thermal management of power devices must holistically account for the package and cooling as well as the internal structures and materials.

The demonstration of large-current, packaged devices is an indispensable milestone for any power device technology towards being deployed in power electronics, as no industrial devices can be used in converters without packaging. While WBG packaging has been researched for years [19, 20], the good news is that the emerging UWBG technologies also reached this milestone very recently [10, 21, 22]. Despite this fast progress, papers that provide a global overview of

Table 1. Thermal conductivity of WBG and UWBG materials [17] ($x = 0.4$–0.8 for $Al_xGa_{1-x}N$).

Material	Thermal conductivity (W m^{-1} K^{-1})	Material	Thermal conductivity (W m^{-1} K^{-1})
Si	150	SiC	400
GaN	200	Diamond	2200
[100] Ga_2O_3	11	[010] Ga_2O_3	27
$Al_xGa_{1-x}N$	~10	AlN	319

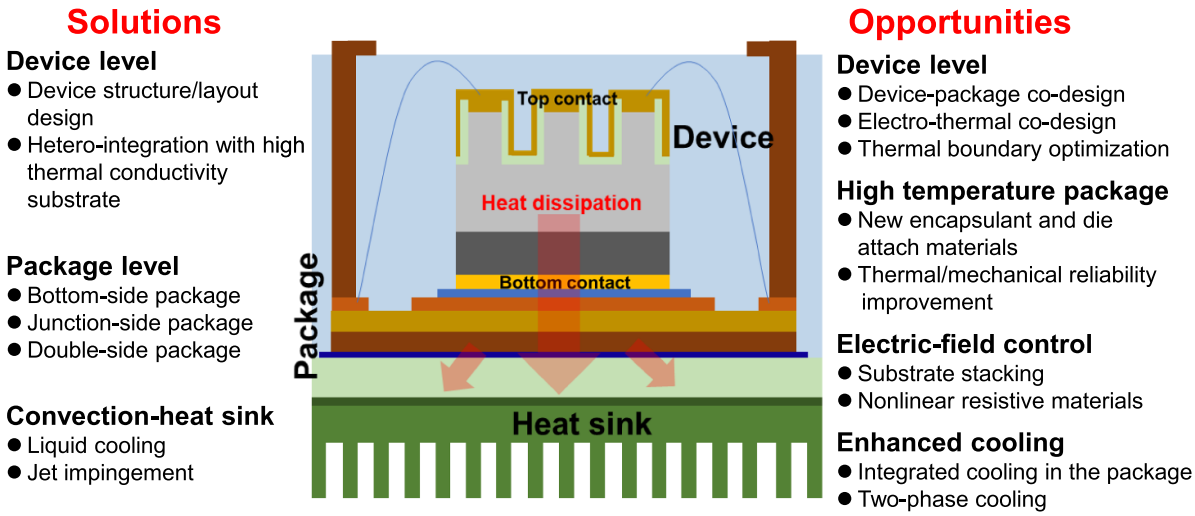

Figure 1. Schematic of heat generation and dissipation in a bottom-side-packaged power device, as well as an overview of solutions and research opportunities for the thermal management and packaging of WBG and UWBG devices presented in this paper.

WBG and UWBG device thermal management are scarce. Recently, thermal studies on lateral UWBG devices have been reviewed with a focus on the fundamentals of devices and materials [23, 24]. This article attempts to build on a material–device–package holistic viewpoint that is closely tied to power electronics applications and discusses common challenges for the thermal management of UWBG devices. To this end, we place a particular emphasis on the state-of-the-art of packaged devices and provide the perspectives both on the device- and package-level thermal management of UWBG devices.

As the literature is vast but space is limited, in this paper, we will focus on the power device and module packaging. Convection-centric cooling technologies have been nicely summarized in [19] and will not be the main focus of this article. We also note that thermal management is not the sole purpose for packaging; the packaging for (U)WBG devices must also handle high E-fields [25, 26] as well as reduce parasitics and electromagnetic interference (EMI) [27, 28]. These electrical and EMI considerations will be briefly mentioned in this article, with a focus on their relevant constraints on the thermal designs of packages.

This article is organized as follows: section 2 illustrates the significance of thermal management for power devices; section 3 describes the basic package architectures and discusses the impact of semiconductor k_T; sections 4 and 5 overview the thermal management and packaging of WBG and UWBG devices, respectively; section 6 provides future perspectives on thermal management and packaging of UWBG power devices; section 7 summarizes the paper.

2. Why does thermal management matter for power devices?

We attempt to answer this question from the viewpoint of power device operations. For a unipolar transistor, the total power loss (P_{loss}) is the sum of conduction loss (P_{con}) and switching loss (P_{sw}), which can be described by [29]

$$P_{loss} = P_{con} + P_{sw} = DR_{on,sp}\frac{I_0^2}{A} + fk_sA \tag{1}$$

where D is the duty cycle, I_0 is the conduction current, f is the switching frequency and k_s is a circuit-related switching parameter. The minimum P_{loss} can be achieved by optimizing the device area (A_{opt}) when $d(P_{loss})/d(A) = 0$:

$$A_{opt} = I_0\sqrt{DR_{on,sp}/fk_s} \tag{2}$$

$$P_{loss} \geqslant 2I_0\sqrt{DR_{on,sp}fk_s}. \tag{3}$$

Considering a 175 °C limit for T_j (the widely used limit for commercial WBG devices), and that losses are independent of T_j (an optimistic simplification), the thermal constraint for device operation at ambient temperature (T_a) is

$$T_j = R_{th,j-a}P_{loss} + T_a \leqslant 175°C. \tag{4}$$

As illustrated in section 1, the key system benefits of (U)WBG devices is their high frequency. From (3) and (4),

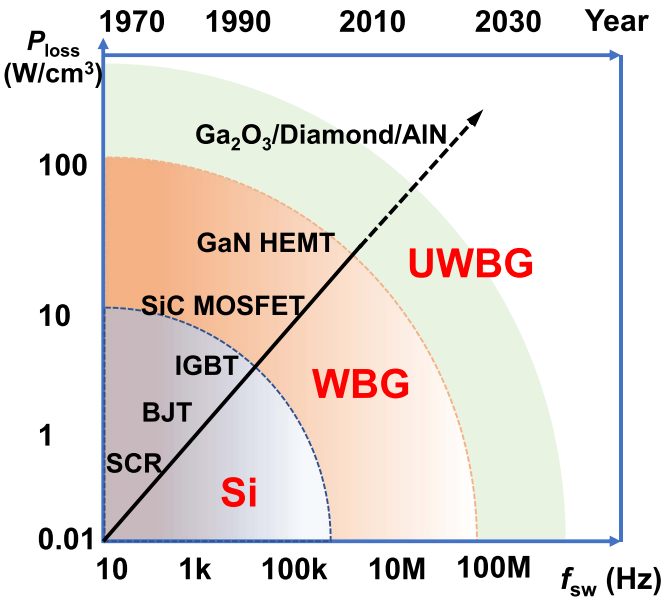

Figure 2. Power density versus switching frequency of power devices based on different materials.

the maximum frequency limited by the thermal constraint is

$$f \leqslant (175^{\circ}\mathrm{C} - T_a)^2 / D R_{on,sp} k_s (2 I_0 R_{th,j-a})^2. \quad (5)$$

As suggested by equation (5), the fulfillment of frequency upscaling in power electronics hinges not only on the inherently low $R_{on,sp}$ of (U)WBG devices but also a low $R_{th,j-a}$. To retain the $R_{on,sp}$ advantage, a $R_{th,j-a}$ at least similar to that of Si devices is preferred. This is challenging due to the much smaller A of (U)WBG devices.

Another angle for understanding the more pressing thermal requirements of (U)WBG devices is to look at the density of power to dissipate, which can be estimated using (2) and (3):

$$p_{loss} \cong 2 f k_s. \quad (6)$$

Although k_s could vary for different (U)WBG devices, (6) suggests that a higher power density is required for frequency upscaling, and this requirement is more or less independent of the underlying material. Figure 2 plots the power density versus frequency for representative Si, SiC and GaN device technologies as well as the projection for UWBG semiconductors.

A common vision is that a T_j higher than 175 °C could potentially be tolerated by UWBG devices for long-term operations, which could relax their thermal management requirements. Although high-voltage Ga_2O_3 and diamond devices have been reported to operate at temperatures up to 327 °C–427 °C [30, 31], their long-term reliability at high T_j still needs further scrutiny. Here, we outline the impacts of T_j on power devices and packages, as these impacts need to be carefully considered when determining the future T_j constraint for UWBG devices.

$R_{on,sp}$ and saturation current density (I_{sat}) are typically the first to be negatively affected by the elevated T_j. When T_j increases from 25 °C to 150 °C, $R_{on,sp}$ of commercial GaN and SiC transistors was reported to increase by 1.7–2.5 times [32], with a reduction in I_{sat} of up to 50% [33]. This will increase the device conduction loss and de-rate its current capability. Additionally, the device transconductance decreases at high T_j due to the reduced carrier mobility, resulting in a slower switching speed and higher switching loss. The increased conduction and switching losses accelerate the T_j rise, which may lead to a destructive thermal runaway [34, 35].

The reliability and robustness of power devices are also compromised at high T_j. T_j is a direct accelerator for power device wearout in switching operations [36]. For example, the lifetime of a 600 V rated GaN HEMT stressed at 640 V and 8 A hard switching was reported to decrease from 900 h at 100 °C to 250 h at 125 °C [36]. Under a similar overvoltage switching condition, the degradation of SiC metal–oxide–semiconductor field-effect transistors (MOSFETs) was reported to accelerate from tens of hours at 25 °C to tens of minutes at 100 °C [37]. Robustness is also critical for power devices to withstand surge energy, overvoltage and overcurrent in systems [33, 38]. The failure of power devices under these conditions is usually thermally triggered, suggesting a compromised robustness at a higher T_j. For example, the critical surge energy of SiC and GaN p–n junctions is generally 30%–40% lower at *a* T_j of 150 °C than at 25 °C [39].

Finally, the reliability of packaging components such as the die-attach, interconnects, substrates and encapsulants, can also be negatively impacted by high T_j. A survey on the high-temperature reliability of these components is presented in [40]. When T_j is elevated to 200 °C, cracking is seen in some widely used packaging components such as Durapot epoxy and Resbond hydro-set ceramic [40]. This suggests a need to explore new materials and structures for high-temperature packages, which will be discussed in section 6.

3. Basics of power device/package thermal management

As shown in figure 1, the thermal management of power devices can be categorized into device- and package-level designs. Examples of device-level designs are uniformly spreading heat across the device, alleviating hot spots around critical junction areas and using materials with high k_T as device substrates [41–43]. Typically, in a power transistor, the channel formed beneath the gate is the area that experiences the peak T_j. A substrate with a high k_T and reduced thickness can help to 'pull' the heat down away from the channel, particularly in the scheme of a bottom-side cooling package. An example of this would be using SiC and diamond as the substrate for GaN HEMTs [44–48]. This method is also applicable to Ga_2O_3 devices with a low k_T [24, 49–53], which will be elaborated in sections 4 and 5.

The heat generation induced by E-field crowding can also be mitigated by device design. Implementing guard rings [54–56], field plates [57–62] and junction termination extensions [63–69] can help to spread the E-field and prevent the build-up of weak electrical and thermal points in the

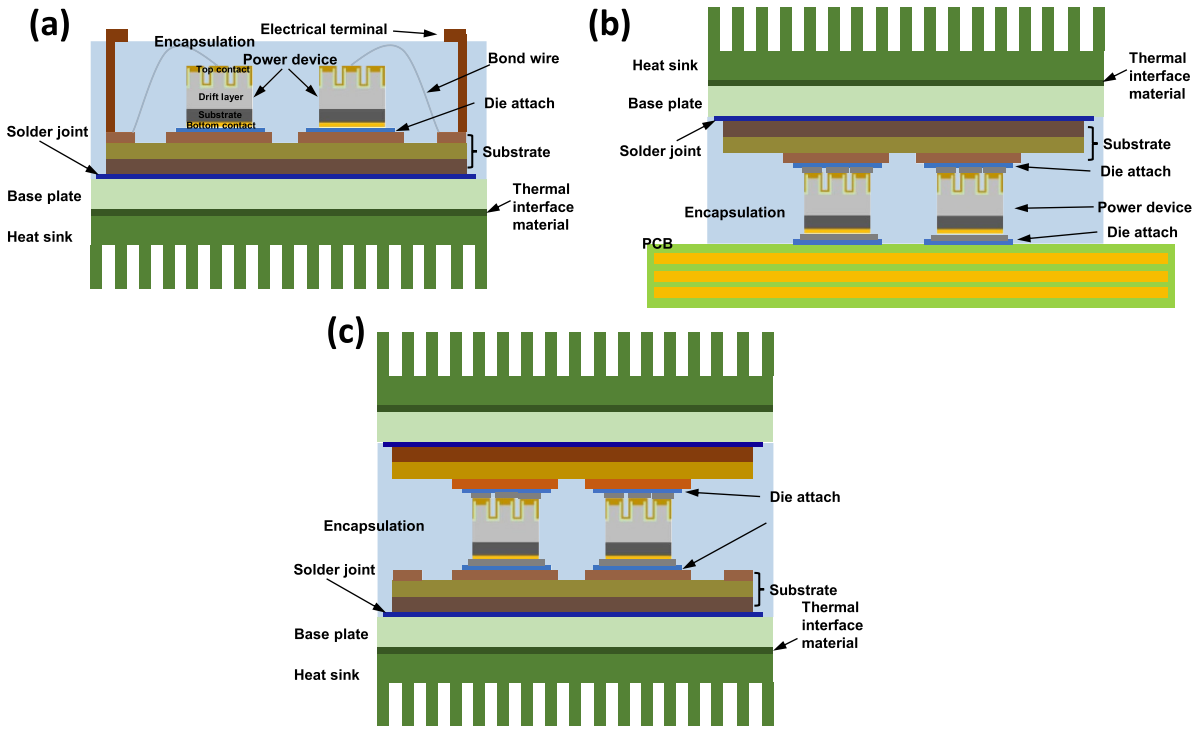

Figure 3. Schematic cross section of (a) a bottom-side cooling package, (b) a junction-side (or top-side) cooling package and (c) a double-side cooling package.

device. This can be well illustrated by a comparative thermal study of lateral and vertical GaN devices with identical material k_T: superior thermal performance is revealed in vertical GaN devices due to the alleviated E-field crowding and more uniform current distributions [2].

The device package incorporates many components, such as die-attach, interconnects (e.g. wire bonds), metal–ceramic substrates and baseplates or lead frames, encapsulants and terminals. The k_T of these materials and R_{th} of these layers and interfaces can affect heat dissipation away from critical areas of the semiconductor. The effectiveness of the overall packaging system is dependent upon the individual components and their thermal properties. For example, the defects, brittle intermetallics and thermomechanical stresses can cause the R_{th} of the die-attach layer to increase, which in turn results in an increase in local temperature and package degradation and failure [70, 71]. Cracks which may develop during operation because of thermal cycling and mismatches in the coefficient of thermal expansion (CTE) of different materials (e.g. the encapsulation material and the metal interconnects) also impede the heat flux and result in larger R_{th} [72]. It has been shown throughout the literature that device thermal performance is improved with optimization of device packaging [21, 22, 24, 73, 74].

There are generally three types of packaging and cooling schemes. Figure 3(a) shows a typical schematic of a bottom-side cooling package [75]. For multi-chip modules, the power devices are attached to a substrate which is typically a ceramic with copper metallization on the top and bottom. The substrate is then typically soldered onto a baseplate for heat spreading and mechanical support. The module is encapsulated using epoxy resin or silicone gel. The final module is mounted to a heatsink for cooling. A thermal interface material is used between the baseplate and the heatsink to reduce the thermal resistance of the interface. While a bottom-side cooling package is suitable for high-k_T semiconductors such as SiC and diamond [23, 76, 77], it may be difficult to achieve efficient heat removal for those with a low k_T.

Junction-side (or top-side) cooling can be advantageous for semiconductors with low k_T, as the heat flows from the device junction directly to the package rather than through the bulk of the device, as shown in figure 3(b) [78, 79]. For these low-k_T devices, junction-to-case thermal resistance ($R_{th,j–c}$) can be reduced compared with a bottom-side cooling package to enable higher power density [21]. However, junction-side cooling packages can also face some challenges. The chip is often directly attached onto the substrate metallization through a flip-chip method. The mismatch of CTE between the metal and the chip could result in mechanical stresses [80, 81]. The E-field distribution can also be an issue as the edge termination of the device is in close proximity to the substrate metallization, which could lead to voltage de-rating or degradation [27, 82, 83]. Further, as most of the heat is removed through the device metal contacts, the effective heat dissipation area will be smaller for a junction-side cooling package than for a bottom-side cooling package since the bottom metal contact covers the entire chip area while the top contact does not due to the edge termination, gate and passivation.

Double-side cooling packages (shown in figure 3(c)) are gaining increased attention for their superior thermal

management due to both bottom- and top-side cooling paths [21, 84, 85]. Such a package may offer the opportunity to address the thermal limitations of some WBG or UWBG materials with low k_T. However, the complexity of double-side cooled packages makes them prone to reliability and yield issues as well as high cost.

As presented in table 1, the k_T of WBG and UWBG materials varies over a wide range, among which Ga_2O_3 has the lowest value and diamond the highest [17]. Considering the device–package interplay, a natural question is whether the semiconductor k_T matters for the thermal management of packaged devices. The answer could be quite straightforward for junction-side and double-side cooling packages: for semiconductors with a low k_T, such that the R_{th} through the bottom heat flow path is very large, there is likely to be negligible difference between junction-side and double-side cooling packages. A powerful example is the Ga_2O_3 diodes reported in [21], which experimentally demonstrates that junction-side cooling enables most of the heat to be directly extracted from the package with minimal heat flowing into the Ga_2O_3 chip.

For a bottom-side cooling package, the significance of semiconductor k_T depends on the relative R_{th} of the chip and package. An analysis of WBG and UWBG devices with bottom-side cooling was presented in [17]. It was found that for $k_T < 150$ W m^{-1} K^{-1} (e.g. Ga_2O_3), the chip's R_{th} dominates $R_{th,j-a}$. For $k_T > 400$ W m^{-1} K^{-1} (e.g. SiC and diamond), the package's R_{th} dominates $R_{th,j-a}$, whereas for $150 < k_T < 400$ W m^{-1} K^{-1} (e.g. AlN and GaN), the contribution of the chip's R_{th} depends on the heat transfer coefficient (HTC) at the heatsink.

Finally, it is worth noting that the accurate measurement of peak T_j is challenging for both bare-die and packaged devices, particularly those with submicron channel/gate structures. The T_j profile measured by micro-Raman spectroscopy and thermoreflectance usually represents an average temperature within a critical area [86–88]. The actual peak T_j could be underestimated, and the measured R_{th} could be smaller than the actual value due to the delicate channel structures and E-field crowding. Besides, some techniques, such as infrared thermography, have a poor spatial resolution of ~5–10 μm [89], and many thermography approaches cannot be applied to packaged devices. For packaged devices, T_j is often monitored by measuring a thermosensitive electrical parameter (TSEP) [90]. For example, in [21] the forward voltage at 10 mA was selected as the TSEP of a packaged Ga_2O_3 diode, and showed an excellent linearity with temperature.

4. Review of WBG device thermal management technologies

Over the last two decades, GaN HEMTs and SiC MOSFETs have arguably become the two most commercially successful WBG power transistors. These devices and the constructed packages are now widely used in electric vehicles, data centers and consumer electronics. As shown in figure 4, the vertical MOSFET and lateral HEMT have fundamentally distinct device architectures and physics; both structures have also been used for several types of UWBG devices. Hence, despite the relative maturity of their thermal management and packaging technologies, a brief review could be beneficial for the emerging UWBG devices.

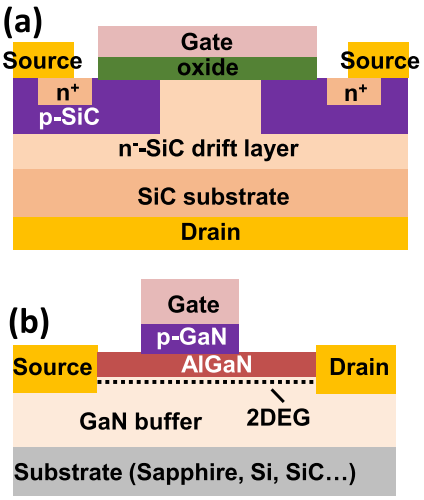

Figure 4. Schematic of (a) a SiC MOSFET and (b) a GaN HEMT.

4.1. SiC diode and MOSFET

The commercialization of SiC devices dates back to the first SiC Schottky barrier diodes (SBDs) introduced to the market by Infineon in 2001 and the first SiC MOSFETs in discrete packages by Cree and Rohm in 2010–2011 [20]. SiC devices are now commercially available in the voltage class of 650–3300 V [7]. Thanks to the high k_T of SiC and the availability of the industrial substrate thinning process, the standard bottom-side cooled packages are prevailing for SiC discrete packages and multi-chip power modules. Today, most of the commercial SiC SBDs and MOSFETs as well as Si IGBTs are packaged in transistor outline (TO) series discrete packages and multi-chip power modules with standardized footprints and wire bond interconnects. These bottom-side cooled packages are able to achieve reasonable R_{th} due to the high k_T of SiC, but, due to the higher current densities of SiC MOSFET dies associated with the smaller chip size compared with Si IGBTs, current de-rating is often needed to avoid overheating of the devices during operation [91]. Accordingly, extensive research efforts have been devoted to further reducing the R_{th} of SiC packages to enable greater heat dissipation under both steady-state and transient conditions.

Junction- and double-side cooling have been pursued for SiC devices by replacing the traditional wire bonds with interconnect methods that enable direct heat transfer from the device junction to the substrate or lead frame. Examples of such interconnect methods include soldering lead frames or substrates directly to the die topside contacts [20, 76, 92], soldering or sintering Cu, Mo or Cu–Mo posts or bumps between the die and the substrate [93–96], and drilling and electroplating Cu-filled vias for PCB-embedded packages [97–99]. As an example, the use of Cu and Mo posts in a double-side cooled

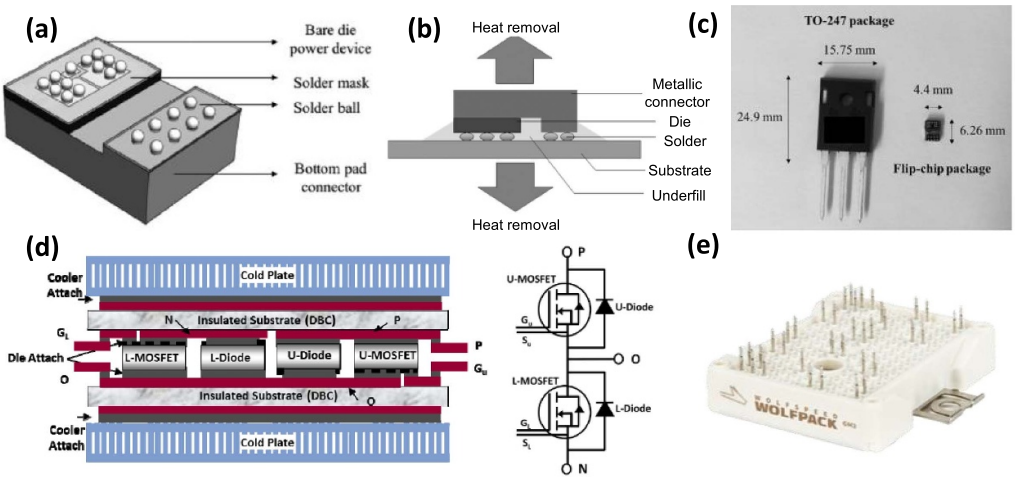

Figure 5. (a) Schematic of a bondless, flip-chip SiC chip-level package and (b) illustration of the double-side cooling based on this package. (c) Photo showing the comparison with a TO-247 MOSFET package and the prototyped flip-chip package. © 2017 IEEE. Reprinted, with permission, from [100]. (d) Schematic of the double-side cooling packaged SiC dies in the phase-leg configuration with the equivalent circuit model shown on the right. © 2015 IEEE. Reprinted, with permission, from [18]. (e) Photo of a Wolfspeed high-power full SiC module. Reproduced with permission from [101]. Used with permission of Wolfspeed Inc.

configuration was utilized to achieve an overall $R_{\text{th,j–c}}$ of just 0.17 °C W^{-1} for a 10 kV, 25 A SiC MOSFET [85].

Recently, Seal *et al* demonstrated a double-side cooled, chip-scale, wire-bondless package [100]. As shown in figures 5(a) and (b), a SiC die is assembled on a metallic connector and then is flip-chip bonded onto a substrate using solder balls, allowing heat dissipation from both sides of the die. The metallic connector translates the bottom interconnection of the device to the plane of the top contacts, making all the device terminals accessible on one side. Figure 5(c) shows its comparison with a TO-247 MOSFET package, revealing a package size that is 14 times smaller. Smaller power loop inductance and electrical R_{ON} have also been demonstrated compared with conventional wire-bonded, bottom-side cooled packages.

SiC multi-chip modules were first demonstrated by Cree/Wolfspeed in 2013 [20] and are now available from multiple vendors in standard footprints. An example of a SiC power module with a double-side cooled package is shown in figure 5(d) [18]. Wolfspeed provides SiC power modules from 1200 V to 1700 V and 20 A (six-pack, three-phase) to 600 A (half-bridge). An example of one of their 1200 V modules is shown in figure 5(e); it employs solderless pins to interface with an external PCB and removes the baseplate in the module [101]. In addition, removing the baseplate reduces the form factor of the pack and machining and material costs, and improves the reliability of the thermal interfaces such that R_{th} can be maintained for a higher number of cycles [102]. At higher voltages, 10 kV SiC MOSFET power modules have been demonstrated both in academia and industry with traditional bottom-side cooling packages [103, 104] and, more recently, double-side cooling packages [85]. A comprehensive review of SiC power module packaging is presented in [20, 76].

4.2. GaN vertical FETs and lateral HEMTs

Before detailing the more mature lateral GaN HEMTs, we briefly introduce the emerging vertical GaN transistors due to the similarity between their thermal management and that of SiC MOSFETs. Recently, several vertical GaN transistors have been demonstrated, such as current aperture vertical electron transistors [105], trench MOSFETs [106] and power fin field-effect transistors (FinFETs) [9]. The temperature-dependent characteristics and dynamic switching performance of vertical GaN transistors have also been reported [9, 107–110]. The packaging of vertical GaN transistors is similar to their SiC counterparts. For example, the TO-247 packaged vertical GaN fin junction-gate field-effect transistor (FinJFET) has been recently demonstrated [32, 33, 111], which shows good thermal performance at high temperatures as well as under avalanche and short-circuit conditions.

GaN power HEMTs are commercially available in the voltage classes of 15–900 V [4, 8] and have been recently demonstrated up to 10 kV [66] based on an emerging multi-channel structure [67–69, 112]. Thermal management is challenging for GaN HEMTs for two reasons. First, commercial GaN power HEMTs are all fabricated on low-cost Si or sapphire substrates with a multi-layer, high-dislocation-density buffer region between GaN device layers and the substrate. The relatively low k_{T} of GaN, Si and sapphire compared with SiC (see table 1), as well as the thermal boundary resistance (TBR) between multiple layers, lead to a relatively large R_{th} across the wafer structure. Second, the current in lateral GaN HEMTs is spatially confined compared with that in vertical devices, deteriorating the non-uniformity of heat generation and dissipation.

To address the thermal challenge, different packages have been developed by industry to allow for junction-side cooling, such as Infineon's dual-small-outline (DSO) packages,

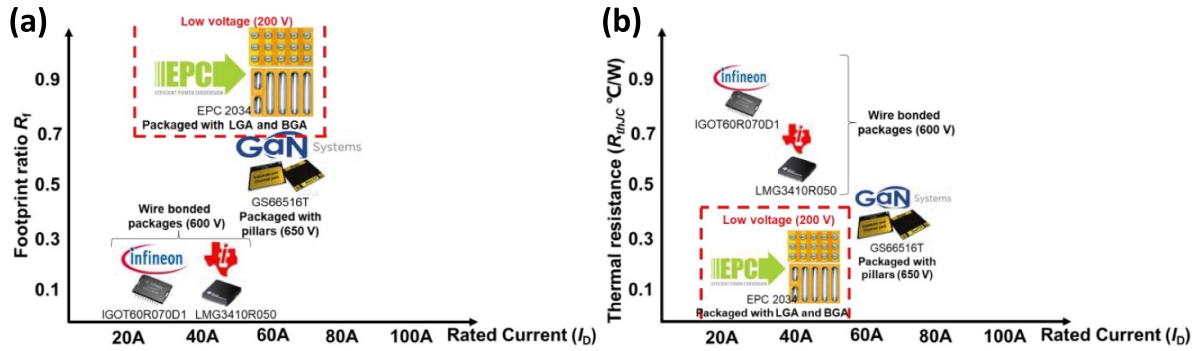

Figure 6. (a) The package footprint ratio and (b) the junction-to-case thermal resistance of commercial GaN packages as a function of device rated current. © 2020 IEEE. Reprinted, with permission, from [113].

Texas Instrument's quad-flat-no-leads (QFN) packages, GaN System's GaNpx packages and EPC's 'solder bar' and ball grid arrays (BGAs) packages. These packages are all surface mounted and obviate the long leads in the traditional TO packages to minimize parasitic inductance, which is essential to exploit the fast-switching capabilities of GaN HEMTs. While the DSO and QFN packages still have bonding wires, the GaNpx and solder bar packages eliminate leads and bonding wires. Specifically, the EPC package works for low-voltage GaN devices and consists of solder bumps to form the land grid arrays or BGAs. This flip-chip bonding using solder bumps is widely used in microwave and radio-frequency (RF) applications. Its main drawback is the limited surface area of the interconnect, which restricts the heat flow down to a small fraction of the total die area.

Figures 6(a) and (b) compare the footprint ratio and $R_{\mathrm{th,j-c}}$ of these commercial GaN packages as a function of rated current [113]. The packaging efficiency is represented by the footprint ratio, i.e. the ratio of the die footprint to the package footprint. The higher this ratio, the more efficient the package and the PCB footprint utilization.

To further reduce the package parasitic inductances and increase the footprint ratio, efforts have been devoted to embedding GaN bare dies into the PCB. PCB embedding has been demonstrated for a single GaN device, GaN integrated circuits and a full-bridge GaN module with good thermal performance [114, 115]. Additionally, Lu *et al* proposed an alternative packaging approach that combines a PCB interposer for device interconnection and a DBC substrate for heat dissipation, electrical isolation and lower CTE mismatch [113] (figure 7). A 650 V, 120 A GaN HEMT is packaged, demonstrating a $R_{\mathrm{th,j-c}}$ of 0.14 K W^{-1}, which outperforms the similarly rated commercial GaN packages.

Device-level thermal management is also being actively studied, and many demonstrations have been made in GaN RF power devices. Despite the use of low-cost Si and sapphire substrates in commercial GaN power devices, researchers have explored GaN devices fabricated on high-k_{T} substrate, starting from the integration of GaN onto SiC substrates [45]. To further alleviate the thermally limited performance, GaN on higher-k_{T} diamond substrates has also been achieved [82]. Chao *et al* demonstrated a GaN-on-diamond HEMT

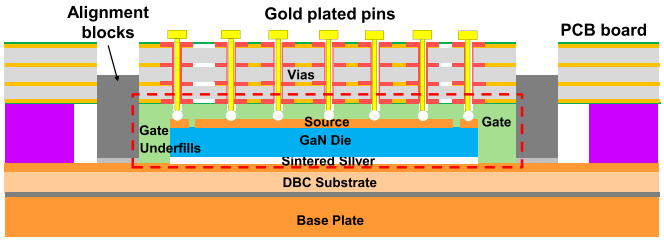

Figure 7. The schematic of the embedded package for single GaN HEMT device based on the PCB-interposer-on-DBC approach. © 2020 IEEE. Reprinted, with permission, from [113].

with power density over three times greater than that of a GaN-on-SiC HEMT with the same active area [116]. This demonstration employed a wafer bonding approach; meanwhile, chemical vapor deposition (CVD) of diamond on the N-polar side of GaN epilayers has also been investigated. From a thermal perspective, Pomeroy *et al* reported a 40% decrease in $R_{\mathrm{th,j-c}}$ of a GaN-on-diamond HEMT compared with a reference GaN-on-SiC HEMT [117]. More recently, high-quality CVD diamond/GaN interfaces have enabled the demonstration of very high power GaN-on-diamond HEMTs with reasonable temperature profiles [118]. Coating the device with high-k_{T} heat-spreading layers has been demonstrated on GaN HEMTs using nanocrystalline diamond (NCD) [119–121]. Electro-thermal simulation has shown that the peak T_{j} of NCD-capped GaN HEMTs is reduced by 30% with respect to a reference HEMT [122]. Incorporation of p-type doping in NCD can further reduce E-field crowding [123].

5. Review of UWBG device thermal management technology

Similar to section 4, we will prioritize the reported thermal management of large-area packaged devices in this section and briefly mention the device-level management reported for small-area devices. The thermal studies of UWBG devices heavily concentrate on Ga_2O_3 due to its very low k_{T}. In contrast, AlN and diamond devices have good substrate k_{T}, suggesting the applicability of housing them in the mature packages developed for GaN and SiC. However, the increased

ionization of their deep-level dopants at elevated temperature makes them suitable for high-temperature applications, which brings new challenges for packaging.

5.1. Ga_2O_3 device

Thermal management is arguably the most serious concern for Ga_2O_3 power devices. The device-level thermal management of lateral Ga_2O_3 devices has been reviewed in [23, 24]. Here we provide a brief summary of these studies and will elaborate our perspectives in the next section. Following the footsteps of its predecessors (e.g. GaN HEMTs), two aspects are being extensively explored for Ga_2O_3 device-level thermal management: (a) substrate engineering, particularly the heterogeneous wafer-epitaxy integration of Ga_2O_3 device layers onto high-k_T substrates, and (b) optimization of channel structure to reduce the peak T_j. The ultimate goal of approach (a) is to enable a bottom-side cooling package for Ga_2O_3 devices, while (b) would be beneficial to both junction-side and bottom-side cooling package schemes.

In 2019, Xu *et al* demonstrated the first wafer-scale heterogeneous integration of 2-inch Ga_2O_3 thin films onto 4-inch SiC and Si substrates by an ion-cutting process [53]. Ga_2O_3 MOSFETs fabricated on a Ga_2O_3-on-SiC wafer demonstrated improved forward and blocking characteristics up to 230 °C compared with the devices fabricated on Ga_2O_3-on-Ga_2O_3 and Ga_2O_3-on-Si wafers. This improvement can be attributed to the reduced self-heating of the Ga_2O_3-on-SiC devices. For the Ga_2O_3-on-SiC devices, a breakdown voltage of 600 V was achieved at 230 °C with a weak dependence on temperature. The same group fabricated SBDs on β-Ga_2O_3/SiC integrated heterogeneous material [124]. The thermal resistance of the SBD based on Ga_2O_3/SiC heterogeneous material is one quarter that of the β-Ga_2O_3 bulk wafer. In the same year, a smaller-size demonstration of a Ga_2O_3 substrate directly bonded to a SiC substrate was also reported [50]. Very recently, Song *et al* reported a Ga_2O_3-on-SiC composite wafer fabricated by a fusion-bonding method and subsequent Ga_2O_3 epitaxy on this composite wafer [49]. In addition to Ga_2O_3-on-SiC, Ga_2O_3 heterogeneous wafer-epitaxy integration onto diamond substrates is also being explored [125–127], but has not reached the wafer scale yet due to the small size of single-crystalline diamond substrates.

In addition to heterogeneous integration, thinning the native Ga_2O_3 substrate is a simple and effective method for thermal management, which can be easily implemented by chemical–mechanical planarization [62]. Modeling and analysis for thermal management of Ga_2O_3 devices on thinned substrates are presented in [128]. A double-side cooling package combined with a heat spreader was predicted to reduce the R_{th} of a single-finger device to as low as 11 mm °C W^{-1} with a maximum power density as high as 16 W mm^{-1} achieved for a T_j limit of 200 °C. A multi-finger transistor thermal model was also developed to show that the Ga_2O_3 transistor could work below the T_j limit by properly designing the gate pitch.

Similar to a GaN HEMT, encapsulation of Ga_2O_3 transistors with a high thermal conductivity material is also desirable. While NCD growth on Ga_2O_3 is currently under active investigation as a heat spreading layer, most recently Lundh *et al* demonstrated for the first time an AlN-capped lateral Ga_2O_3 transistor. The sputtered AlN cap was sufficiently effective to enable a DC power density in excess of 5 W mm^{-1}, exceeding that of any substrate-side thermal management approach reported to-date [129].

As the other focus of device-level thermal management, the impact of channel design on device thermal management is exemplified in the power FinFET, a new junctionless power transistor [9] first demonstrated in GaN [61, 130, 131] and subsequently in Ga_2O_3 [132, 133]. Due to the anisotropic k_T in Ga_2O_3 [134], Chatterjee *et al* predicted that a Ga_2O_3 FinFET with fins orientated to [100] could allow for a 30% reduction in peak T_j as compared to devices with fins aligned to the [010] orientation [135]. From similar considerations, in Ga_2O_3 lateral MOSFETs, Kim *et al* pointed out that the layout design could also impact the peak T_j [136].

Recently, large-area packaged Ga_2O_3 power devices have been demonstrated by a few groups [21, 22, 137–141], which allows for probing the Ga_2O_3 thermal management beyond the material and device levels. Unlike the heterogeneous integration that aims at making Ga_2O_3 chips compatible with bottom-side cooling packages, another pathway is to employ a junction-side cooling package and extract the heat from the device junction directly to the package without the need for substrate engineering. As a validation of this path, Xiao *et al* demonstrated the first large-area Ga_2O_3 SBDs packaged in bottom-side and double-side cooled configurations using nanosilver sintering as the die-attach (figures 8(a)–(c)) [22]. The packaged SBDs show a forward current over 20 A and a breakdown voltage over 600 V. The $R_{th,j-c}$ of a double-side packaged Ga_2O_3 SBD was measured to be 1.43 K W^{-1} and 0.5 K W^{-1} in the bottom-side and junction-side cooling configurations, respectively (figures 8(d) and (e)) [21]. The latter $R_{th\,j-c}$ is lower than the similarly rated commercial bottom-side cooled TO-packaged SiC SBDs. By considering different cooling approaches (as can be represented by the HTC), $R_{th,j-a}$ was analyzed for the bottom-side, junction-side and double-side cooling package schemes (figure 8(f)). It was concluded through thermal impedance measurements and simulations that junction cooling is essential for Ga_2O_3 devices, with a HTC over 10^3 W m^{-2} K being preferable [21].

Surge current is an essential ruggedness metric listed in any power diode's datasheet and the most important indicator of its transient electrothermal ruggedness [39]. It measures the device's capability of temporarily sustaining a current much higher than the rated current before the protection circuit intervenes and is usually evaluated in a 10 ms wide half-sinusoidal current waveform. Xiao *et al* found that a double-side cooled package enables a critical surge current of 70 A in Ga_2O_3 SBDs, which is nearly two times higher than for the bottom-side cooled packaged device (figures 9(a) and (b)) [22]. The former Ga_2O_3 SBD shows a ratio between the peak surge

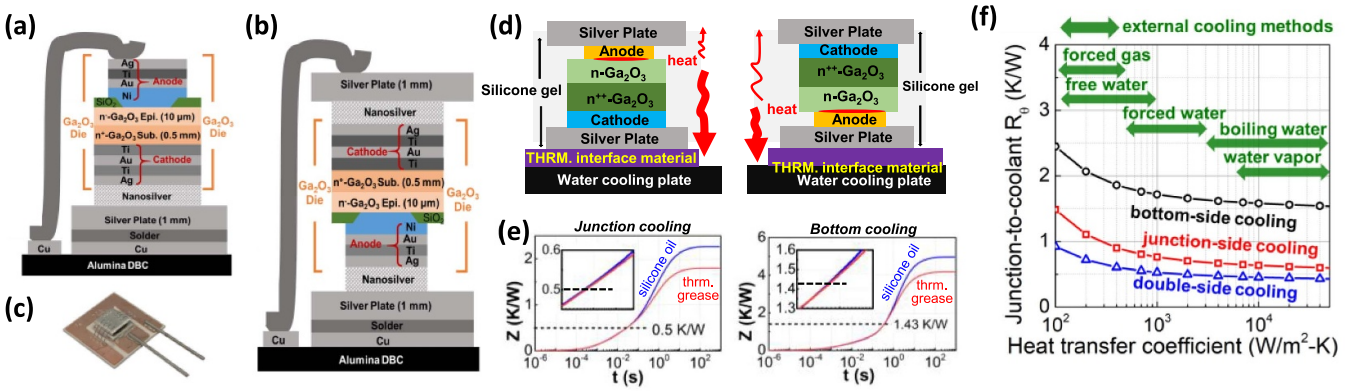

Figure 8. Schematic of the fabricated Ga_2O_3 SBD in (a) a bottom-side cooling package and (b) a double-side cooling package. (c) Photo of a double-side cooling packaged Ga_2O_3 SBD. © 2021 IEEE. Reprinted, with permission, from [22]. (d) Measurement setup for the junction-to-case thermal resistance of a double-side cooling packaged Ga_2O_3 SBD under bottom-side cooling (left) and junction-side cooling (right). The measurement results are shown in (e). (f) The simulated junction-to-ambient thermal resistance of a bottom-side, junction-side and double-side cooled Ga_2O_3 SBD with different external cooling approaches. © 2021 IEEE. Reprinted, with permission, from [21].

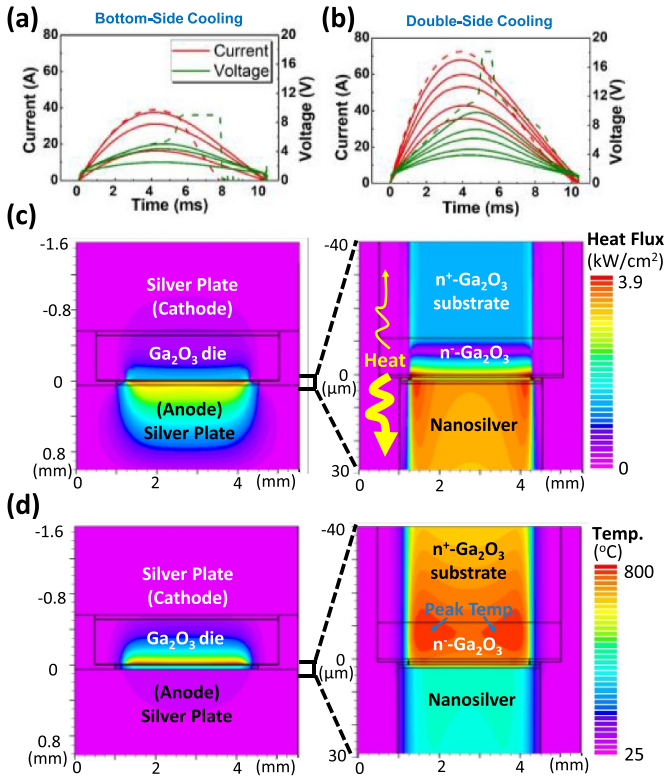

Figure 9. The experimental surge current measurement waveform of (a) a bottom-side cooled Ga_2O_3 SBD and (b) a double-side cooled Ga_2O_3 SBD. The simulated contours of (c) heat flux and (d) temperature in the double-side cooled Ga_2O_3 SBD structure (left) and the junction region (right) at the peak surge current transient. © 2021 IEEE. Reprinted, with permission, from [22].

current and the rated current higher than that of the similarly rated commercial Si and SiC SBDs. Electrothermal mixed-mode simulations revealed that with the double-side package heat is mainly extracted through the junction side in the transient condition; meanwhile, the peak T_j is moved from the Schottky contact into the bulk Ga_2O_3 during the transient heating process (figures 9(c) and (d)). These results illustrate the significance of the package design and cooling configuration on the transient thermal performance and electrothermal ruggedness of Ga_2O_3 devices [74].

The results above seem to suggest that, for a typical Ga_2O_3 chip, a double-side cooled package brings little benefit compared with a junction-side cooled package. According to the simulations in [21], this does not hold when the Ga_2O_3 substrate is thinned or replaced by high-k_T substrates. Under such configurations, the heat removal through the back side of the chip could become as effective as that through the junction side. This prediction was experimentally validated by Gong *et al* [141]. A multi-step grinding and CMP process was used to thin the substrate down to 70 μm, and the fabricated Ga_2O_3 SBD was housed in a double-side cooled package (figure 10(a)). A reference Ga_2O_3 SBD without substrate thinning (550 μm thick) was fabricated and packaged using the same process. The Ga_2O_3 SBD with the thinned substrate showed a smaller $R_{th,j-c}$ (figure 10(b)) and higher surge current capability, illustrating effective through-chip heat removal under steady-state and transient conditions. Such superior performance was further validated by performing 150 W system-level power factor correction circuit measurements, delivering a high conversion efficiency of 98.9% (figure 10(c)) and manifesting the impact of device thermal management on circuit performance.

Finally, a few other large-area Ga_2O_3 diodes have been demonstrated with TO packages, including the trench MOS Schottky diode [137] and NiO/Ga_2O_3 heterojunction p–n diodes [138–140]. Although these works did not focus on thermal management, they report excellent electrical characteristics of the packaged Ga_2O_3 devices, including high-temperature operation, minimal reverse recovery, high overvoltage ruggedness and nanosecond switching. These results retire many critical risks associated with the electrical performance of the packages for UWBG power devices.

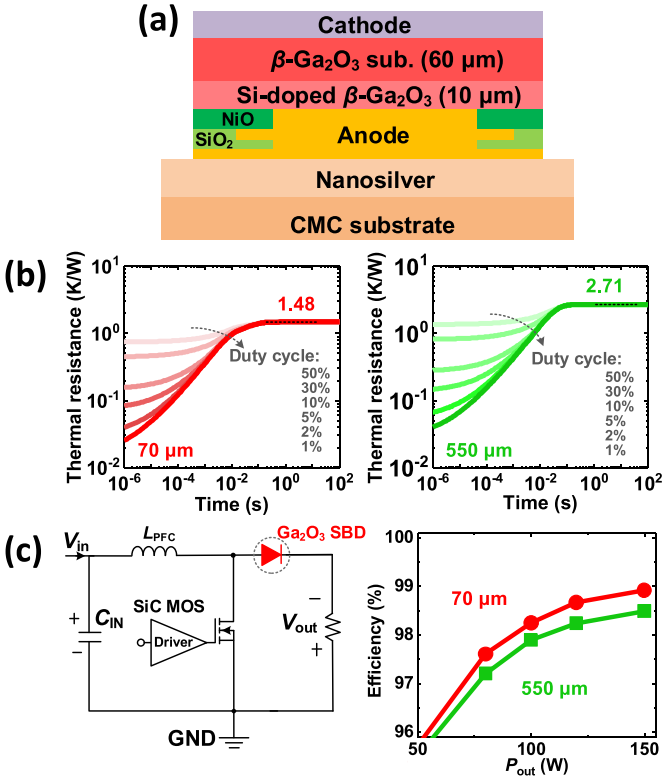

Figure 10. (a) Schematic diagram of a thin-body Ga_2O_3 SBD with flip-chip packaging. (b) Time-resolved thermal resistance curves of a 70 μm thin-body Ga_2O_3 SBD (left) and a 550 μm normal body thickness Ga_2O_3 SBD (right). (c) Circuit schematic of the boost power factor correction (PFC) circuit (left) and system efficiency as a function of the output power (P_{out}) at a switching frequency of 0.1 MHz. © 2022 IEEE. Reprinted, with permission, from [141].

5.2. Diamond and AlN devices

Among the UWBG semiconductors, diamond and AlN have the theoretical best-in-class power material figure-of-merit [142, 143]. Due to the relative immaturity of material synthesis and processing technologies, their device development is still at an early stage, although packaged diamond power devices have been recently demonstrated with bottom-side packages (figures 11(a) and (b)) [10].

UWBG devices are in general attractive for high-temperature applications due to their low intrinsic carrier concentration. An additional feature in diamond is the relatively high activation energy of dopants, which are incompletely ionized at the room temperature. At elevated temperatures, the increased ionization results in a negative temperature coefficient (NTC) of $R_{on,sp}$ in diamond devices, which prevents thermal runaway. Hitoshi *et al* demonstrated a vertical diamond SBD assembled on a metal–ceramic package (figure 11(c)) [144]. The packaged diamond SBD shows small reverse recovery at high temperatures up to 250 °C (figure 11(d)). Another high-temperature diamond SBD demonstration was reported by Sergey *et al* [145] with a forward current higher than 10 A up to 200 °C. The authors also compared the device thermal performance using silver paste and Cu–Sn solder as two different types of die-attaches. As illustrated in figures 11(e) and (f), the device mounted with Cu–Sn solder shows lower peak T_j but slightly higher forward bias drop. The $R_{th,j-c}$ and conductivity of the two packaged devices were reported to be 3.7 K W^{-1} (1.4 W cm^{-2} K) and 1.2 K W^{-1} (4.2 W cm^{-2} K) for the silver paste and Cu–Sn solder, respectively.

Perez *et al* [146] investigated the system-level benefits of the NTC effect in diamond devices (figure 12). Diamond SBDs with three different die sizes were compared with a similarly rated SiC SBD, and their heatsinks were optimized accordingly. While allowing the devices to operate at an elevated temperature (up to 500 K for SiC and 1300 K for diamond) allows the use of heatsinks with high R_{th} values, the R_{ON} of diamond devices decreases while that of SiC devices increases (figures 12(b) and (c)). Diamond devices exhibit a lower power loss and optimal operation at higher temperatures, thus easing the heatsink designs. As a result, the power loss and heatsink volume of diamond devices can both be three times smaller than those of their SiC counterpart at 450 K (figure 12(d)).

To realize the high-temperature application of diamond power devices, challenges are present in high-temperature packages. For example, the difference in CTE and stiffness between diamond and die-attach materials will lead to thermal stress and thus lifetime degradation and reliability issues. Fusté *et al* [147] simulated the thermomechanical interaction between components in a diamond module. Simulation was conducted for a custom SOT-227 power module (figure 13) with Si, SiC and diamond. A diamond die shows higher residual effective stress compared with SiC and Si dies during the high-temperature thermal cycle. This issue results from the high elastic modulus and low CTE of diamond, because of which small bending deformation causes high tension on both upper and lower die surfaces. Three different die-attach materials were then investigated for stress distribution and deformation in diamond modules. The results show a saturated stress distribution and a similar accumulated viscoplastic deformation for the three materials.

AlN power devices and high-Al $Al_xGa_{1-x}N$ channel HEMTs have been studied over the past few years with a focus on their electrical performance, for example the improvement of ohmic contact [148, 149]. Few works have been reported on their device- and package-level thermal management. Owing to the high k_T of AlN, bottom-side cooled packages are expected to work well. Besides, AlN devices also present a NTC effect in their $R_{on,sp}$, making them suitable for high-temperature applications [150].

$Al_xGa_{1-x}N$ is promising for the next generation of lateral power devices but suffers from low k_T (see table 1) due to alloying. The thermal behaviors of $Al_xGa_{1-x}N$ channel HEMTs have been rarely explored. Lundh *et al* [151, 152] performed multidimensional thermal analysis and revealed the interdependence of electronic and thermal transport in $Al_xGa_{1-x}N$ channel HEMTs. It should be noted that $Al_xGa_{1-x}N$ HEMTs can be made on either a sapphire substrate or a free-standing AlN substrate. The former substrate would make the device thermal management similar to Ga_2O_3 devices, while the latter may make it similar to bulk AlN devices.

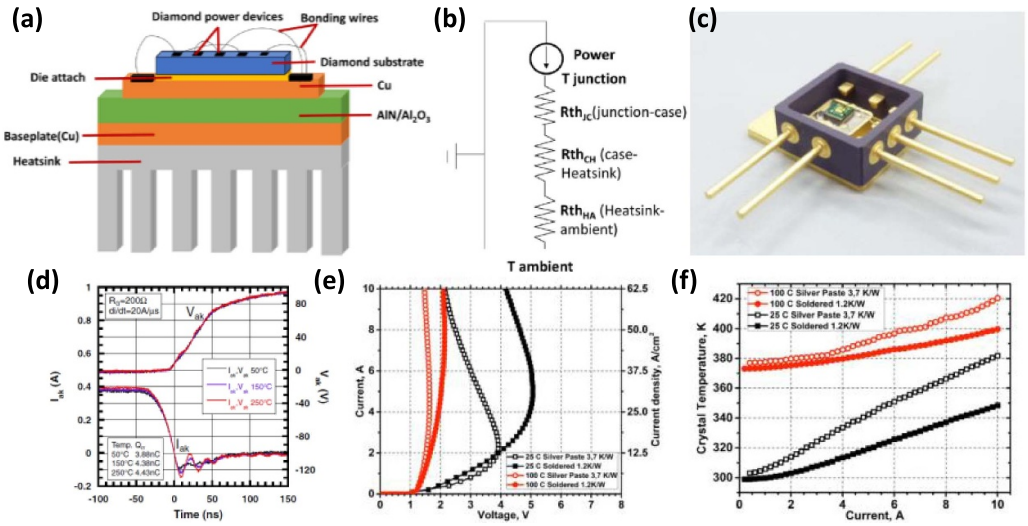

Figure 11. (a) Schematic illustration of a generally used package for diamond power devices and (b) its DC thermal equivalent circuit. Reproduced from [10]. © IOP Publishing Ltd. CC BY 3.0. (c) Photograph of a metal–ceramic package for a vertical diamond Schottky barrier diode. (d) Switching characteristics of the vertical diamond Schottky barrier diode at different temperatures. Reproduced from [144]. © 2014 The Japan Society of Applied Physics. All rights reserved. (e) Forward *I*–*V* characteristics of a diamond Schottky barrier diode with two different types of die-attaches. (f) The dependence of crystal temperature on forward current. [145] John Wiley & Sons. © 2015 WILEY-VCH Verlag GmbH & Co. KGaA, Weinheim.

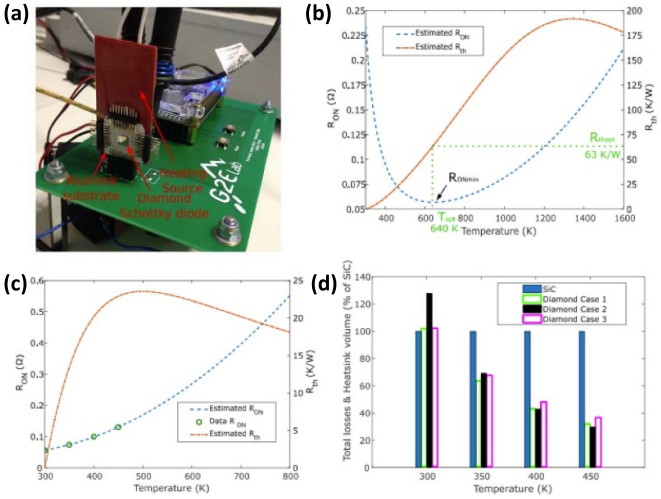

Figure 12. (a) Bulk converter prototype using a packaged diamond SBD. Temperature-dependent device ON-state resistance and heatsink thermal resistance for (b) a diamond SBD and (c) a commercial SiC SBD. (d) Estimated total loss and heatsink volume of a SiC SBD and three different sizes of diamond SBD at different temperatures. Reprinted from [146], Copyright (2020), with permission from Elsevier.

As a summary of this section, thanks to the high k_T of AlN and diamond, bottom-side cooled packages are expected to be suitable. However, due to the deep-level doping, AlN and diamond devices may deliver optimal performance at high temperatures, thereby requiring high-temperature packaging. This requirement poses challenges for package design, CTE management, package material selection and package reliability. These issues and their potential solutions will be further discussed in the next section.

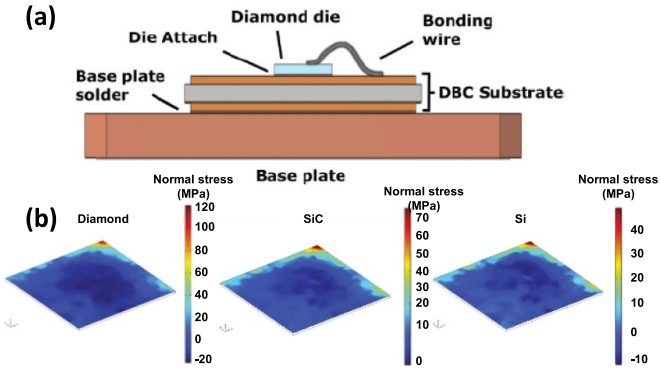

Figure 13. (a) Schematic diagram of the custom SOT-227 power module. (b) Normal stress distribution at the interface between die and die-attach for diamond, SiC and Si chips. © 2020 IEEE. Reprinted, with permission, from [147].

6. Future perspectives

6.1. Device–package co-design

The major collective push for recent thermal management efforts in the United States began with DARPA's thermal management technology program and continued with the near-junction thermal transport and intra-chip/inter-chip enhanced cooling programs [153–156]. Many results on WBG and UWBG technologies suggest a need for the co-design of power devices and their packages as well as of their electrical and thermal performances.

6.1.1. Bottom-, junction- and double-side thermal management. As illustrated in sections 4 and 5, substrate thinning and integration with high-k_T substrates is an effective

method for reducing R_{th} and dissipating heat from the active region. However, further improvements can be made by employing embedded microfluidics such as microchannel cooling and jet impingement [82, 154, 157, 158]. The high HTC in close proximity to the device can lead to significant improvements in power density. For instance, van Erp *et al* recently demonstrated a microchannel cooling structure integrated in the Si substrate of GaN-on-Si SBDs [159]. Using this technology, a GaN-on-Si full-wave bridge rectifier was demonstrated and it achieved 30 times greater power output than a natural convection (air-cooled) reference structure [159].

For junction-side thermal management, approaches including the integration of high-k_T heat spreading layers, flip-chip integration and microfluidic cooling could be utilized to dissipate heat from the active region. Junction-side thermal management is especially enticing for lateral (U)WBG transistor structures which typically have their active regions within tens of nanometers of the junction-side device surface, as is the case for structures such as GaN HEMTs, $Al_xGa_{1-x}N$ HEMTs, and lateral Ga_2O_3 MOSFETs [160–163].

Despite the effectiveness of flip-chip integration for junction- and double-side cooling packages as exemplified in sections 4 and 5, further optimization is required for successful deployment. For the junction-side package of low-k_T devices, the underfill materials surrounding the die-attach could be critical. These materials usually exhibit low k_T, making little impact on high-k_T power devices where the majority of the heat is removed through the die contact and die-attach. However, for low-k_T devices, the underfill material could become a non-negligible heat extraction path. For example, electrothermal simulation suggested that the heat dissipation of Ga_2O_3 MOSFETs is greatly limited by flip-chip bonding of the device to the carrier substrate with low-k_T epoxy. Increasing the epoxy underfill k_T from typical values of $\sim$1 W m^{-1} K^{-1} to 14 W m^{-1} K^{-1} (h-BN infused epoxy composite) leads to a 66% reduction in the peak T_j rise for the Ga_2O_3 MOSFET flip-chip integrated with a diamond carrier substrate [24].

Furthermore, the impact of the thermal design on the electrical performance must also be considered. The mismatch of the CTE between different layers and interfaces in the package may lead to considerable mechanical and reliability issues. Similar to bottom-side cooling, introducing high-HTC forced convection cooling can greatly improve the thermal performance. For example, Kwon *et al* demonstrated junction-side jet impingement cooling via additively manufactured nozzles with air as the coolant, which reduced the peak temperature rise of the tested GaN transistors by $\sim$65% [164].

More work is also needed to improve the double-side cooling of low-k_T devices, such as $Al_xGa_{1-x}N$ and Ga_2O_3. As illustrated in section 5, if substrate heat removal is inefficient, double-side cooling of low-k_T devices may have minor benefits over junction-side cooling due to the majority of the heat being dissipated through the junction rather than through the device. To realize the high current and power densities offered by these UWBG devices, further work is needed to improve the heat dissipation through low-k_T devices, such as through wafer thinning and heterogeneous integration, such that the double-sided cooling can be improved.

6.1.2. Heterogeneous integration and TBR. One highly desirable solution for device-level thermal management is to utilize monocrystalline diamond and AlN as part of the active semiconductor layer. This would position the thermal management solution directly at the source of the heat generation. Lundh *et al* reported a comparative simulated thermal analysis of lateral transistor structures based on UWBG $Al_xGa_{1-x}N$, Ga_2O_3 and diamond. It was shown that diamond transistors can have up to $\sim$50 times lower R_{th} than other UWBG-based device technologies [165]. Unfortunately, diamond-based device technologies are still plagued by doping limitations, scalability and the high cost of producing large-area single-crystal substrates [13, 166].

Because of its importance for thermal management of WBG and UWBG devices, an area of research that has been attracting increasing interest is the understanding, characterization and optimization of interfacial thermal transport [167, 168]. For GaN devices on foreign substrates, the TBR has been shown to contribute significantly to the peak T_j rise [169–171]. Typically, this TBR consists of contributions from both interfaces and interfacial layers. Manoi *et al* suggested that optimization of the AlN nucleation layer contributed to the effective TBR in GaN-on-SiC HEMTs because an additional 10%–40% temperature rise was possible with an AlN layer in GaN HEMTs depending on the composition of the nucleation layer in the GaN microstructure [172].

Likewise, for UWBG devices, the TBR at the interfaces must be minimized. Decreasing the TBR must be considered to most effectively deploy the thermal management approaches of bottom-side cooling, junction-side-cooling or double-side cooling packages discussed previously. For example, for $Al_xGa_{1-x}N$ and Ga_2O_3, the thermal conductance across the surrounding UWBG/metal contacts and UWBG/substrate interfaces becomes increasingly important for thermal transport in junction-side and bottom-side thermal management, respectively. Shi *et al* used time-domain thermoreflectance to measure the TBR of several Ga_2O_3/metal interfaces [173]. They found that Ni/Ga_2O_3 and Cr/Ga_2O_3 interfaces have the lowest TBRs for Schottky and ohmic contacts, respectively.

For bottom-side thermal management by bonding UWBG semiconductors to a high-k_T substrate, the bonding agent and technique introduce an additional R_{th} to the device. Cheng *et al* have recently reviewed the TBR across heterogeneously integrated surfaces by techniques including transfer bonding, surface-activated bonding, plasma bonding and hydrophilic bonding [174]. Physics-based modeling of interfacial thermal transport is still very much an active area of investigation as typical methods, such as the acoustic mismatch model, diffuse mismatch model and atomic Green's function, all possess inherent limitations. Therefore, these frameworks can fail to fully capture and elucidate the complex interactions occurring at and near the interface, such as the presence of local vibrational modes unique to the interfacial region [175–178]. Understanding the physical processes that dictate

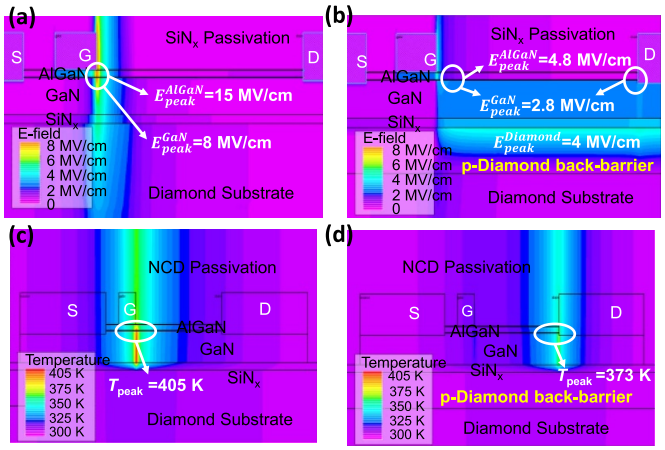

Figure 14. E-field contours of GaN HEMTs (a) without and (b) with a p-type diamond back-barrier. Lattice temperature contours of devices (c) without and (d) with a p-type diamond back-barrier, illustrating that the optimization of E-field management allows for a movement of the peak T_j location and a reduction of its magnitude. © 2016 IEEE. Reprinted, with permission, from [123].

thermal transport within/across WBG/UWBG materials and interfaces will undoubtedly provide some guidance for thermal management and package design and thus requires further research.

6.1.3. Electrothermal co-design. As mentioned in previous sections, suppression of E-field crowding is beneficial from a thermal perspective since Joule heat generation from the E-field is also reduced and more evenly redistributed in the transistor channel [2]. Therefore, advanced electrothermal co-design should be employed to enhance both electrical and thermal performance [2, 179–181]. Considering this co-design, the aforementioned heterogeneous integration can go beyond mere thermal management to electrothermal management. For example, Zhang *et al* proposed to insert p-type diamond as a cap layer or back-barrier layer above or beneath the horizontal current channel, so as to not only provide a path for near-junction heat removal but also an E-field management structure to suppress E-field crowding [123] (figure 14). By inserting a p-diamond back-barrier layer with a perfect charge balance into the n-type channel, the peak E-field is suppressed. As a result, the peak T_j location moves from the gate edge to the drain edge and its magnitude is lowered.

It is worth mentioning that electrothermal management is not only important for UWBG devices but also for their packages. The package of UWBG devices is expected to withstand a higher E-field than its WBG counterpart. Hence, E-field control itself is a pressing challenge for UWBG packaging. We will elaborate this point in section 6.2.3.

Finally, it is also pertinent to be mindful of both the device application and the thermal management strategies being employed at packaging levels. For applications involving fast-switching transients, such as solid-state circuit breakers, devices may be expected to handle high power loads in the nanosecond to microsecond regime [182]. Lundh *et al* demonstrated that for a GaN HEMT subject to submicrosecond pulsing, there is no observable temperature rise in the underlying substrate [183]. Similarly, in a millisecond pulse, Xiao *et al* revealed a small temperature rise in the Ga_2O_3 substrate of a packaged Ga_2O_3 SBD [22]. Therefore, for many transient applications, substrate engineering may have less impact and junction-side approaches will be preferable for thermal management.

To address the importance of matching the thermal design with the time scale of its application, several reviews focusing on transient thermal management have recently been published [81, 184, 185]. In addition to application-specific considerations, such as time-scale matching, the thermal design must also be tuned to match the thermal management scheme at the package level. From this perspective, Zhang and Palacios encouraged device–packaging thermal co-design and offered some practical applications [9]. For GaN FinFETs, if the package is designed to extract heat from the top-side of the device, then it is more important to optimize the fin pitch and the inter-fin material for better thermal management [9]. This would have a large impact on the switching speed and loss of FinFETs and thus require careful electrothermal co-design under switching operation conditions [186].

6.2. High-temperature packaging

The adoption of UWBG devices and an overall trend towards a higher power density amplifies the need for robust and reliable packaging. The ability and suitability of these devices to operate at much higher temperatures due to their low intrinsic carrier concentrations and deep-level dopants is compelling for many automotive, aerospace, military and downhole applications [187, 188]. However, conventional packaging materials and design in many cases are not adequately suited for operating temperatures exceeding 250 °C. This, in combination with the low k_T of some UWBG materials, emphasizes the need for rigorous thermal management design.

As illustrated in section 5, UWBG devices have demonstrated superior high-temperature stability compared with Si and WBG devices, making them inherently suitable for high-temperature applications. However, device packaging has rarely been shown to survive operating temperatures beyond 200 °C [189] with most being limited to 250 °C and below [190, 191]. Three of the limitations of a high temperature package are the stability and reliability of the encapsulation, the substrate, and the die-attach. Each of these components is critical for the operation and reliability of any packaged device and needs to be carefully selected to account for the elevated temperatures and resulting thermomechanical stresses.

6.2.1. Encapsulant. The primary limitation for the reliability of high-temperature packages is the encapsulation. The encapsulation serves as a crucial passivation layer and also provides environmental protection to the device [192]. Reliability studies suggest that the dielectric and mechanical strength of commercially available encapsulants degrades significantly before the temperature reaches 250 °C–275 °C [193]. In

Table 2. Critical properties for encapsulation [195, 196].

Property		Typical desired value
Electrical	Dielectric strength	$\geqslant$20 kV mm^{-1}
	Dielectric constant	$<$5
Thermal	Glass transition temperature (T_g)	$>$Working temperature ($^\circ$C)
	k_T	$>$1 (W m^{-1} K^{-1})
Mechanical	CTE (α)	Matched to device and substrate (ppm K^{-1})
	Elastic modulus	4–10 (GPa)
	Viscosity (η)	$<$20 Pa·s for underfill (50 for encapsulation)
	Processing temperature	$<$300 $^\circ$C
	Moisture absorption	$<$1% weight gain in 85 $^\circ$C/85% relative humidity

addition, these high temperatures result in thermomechanical stresses which can cause cracking and in turn a loss of mechanical and dielectric strength [194, 195]. The majority of commercial encapsulants also have a low k_T, which if improved upon could alleviate some induced thermal stress and strains. Thus, it is critical to examine the dielectric, mechanical and thermal stability/conductivity properties when evaluating an encapsulant for high-temperature applications. Silicone elastomers are commonly used in power module packages. They have a relatively low Young's modulus, which helps to alleviate some of the thermomechanical stresses; however, they are subject to the aforementioned degradation when exposed to temperatures above 200 °C [196]. As such, other polymeric, composite and novel encapsulation materials are of great interest. The pertinent properties for material selection are shown in table 2.

6.2.2. Packaging substrate. Metal–ceramic substrates are widely used in electronics packaging for structural support, insulation, thermal management and electrical interconnection. With temperatures potentially exceeding 250 °C, thermal cycling in the substrate can cause cracking, warping and/or delamination of the layers, all of which are severe reliability issues [197]. The substrate is also paramount for thermal management, serving as a first-level heat spreading and extraction layer, which puts a critical lens to k_T as well. For these reasons, careful consideration of the mechanical, thermal and electrical properties must be made when selecting a substrate [198]. Table 3 highlights commonly used metal/ceramic substrate technologies [198, 199].

6.2.3. Die-attach. The die-attach must provide a strong connection between the device and its associated substrate while having high electrical and thermal conductivity [200]. In addition, matching the CTE to both the substrate and the device is critical to minimize the thermomechanical stresses seen at the interface. With expected working temperatures surpassing 250 °C, conventional tin- and lead-based solders will either melt or degrade significantly, and as such other attachment methods must be utilized. Table 4 identifies the key properties of commonly used methods and potential high-temperature materials [192].

Nano-silver sintering offers a higher maximum operating temperature, good thermal performance and better electrical conductivity than conventional solder, making it a suitable choice for high-temperature applications **[**201, 202**]**. Furthermore, large-area silver sintering allows for the reliable construction of multi-layer substrates and bonding of substrates to baseplates, and enables other novel packaging configurations to assist in thermal management and mechanical reliability **[**203, 204**]**.

6.2.4. New package designs and enhanced cooling. Another tactic to alleviate some of the generated heat and in turn reduce overall thermomechanical stress is to alter the package layout and architectures. While the basic structures of bottom-, junction- and double-side cooled packaging are illustrated in figure 3, many module- and system-level designs exist and can significantly affect system performance. While this higher-level packaging and integration is not the focus of this article, these exciting research opportunities are worth a mention. For example, in a double-side cooled, multi-chip package, interposers, such as metal bricks, balls or tubes, have been used for device-top interconnection, with Cu being the most widely used interposer material due to its high electrical and thermal conductivity [85]. However, rigid Cu interconnections between the device and the substrates of the power module could bring reliability concerns. Ding *et al* demonstrated a porous interposer made of sintered silver, which reduces the thermomechanical stresses in the module by 42%–50% with a trade-off of only a 3.6% increase in T_j [205].

Lastly, second-level cooling strategies can be implemented to reduce $R_{th,j-a}$. Two-phase, jet impingement and immersion cooling, among others, can improve upon the performance of the conventional finned heatsinks and liquid cold plates [206]. Some of these cooling technologies are illustrated in figure 8(f). Recently, Gebrael *et al* demonstrated a novel cooling approach by monolithically integrating a thin insulating material and a conformal Cu coating on power devices [207]. This approach allows the copper to be in close proximity to devices, and has been validated by applications to WBG GaN power devices.

6.2.5. Electric-field control. While primarily thermal limitations and concerns have been discussed to this point, the package also provides critical support pertaining to E-field control. To fully exploit the higher E-field blocking capability of UWBG devices, the E-field strength of the package must also be higher. To prevent partial discharge and to mitigate the possible peak temperature induced by a crowded E-field and the risk of device or package electrothermal failure, several techniques can be implemented to either reduce the E-field magnitude or provide ample insulation to increase reliability [26].

Table 3. Substrate critical properties and material comparison [198, 199].

Property		DBC/Al_2O_3	DBC/AlN	DBA/Si_3N_4
Electrical	Dielectric strength (kV mm^{-1})	15	15–20	18
Mechanical	Young's modulus (GPa)	340	302–348	260–320
	Flexural strength (MPa)	350	320	900
Thermal	CTE (ppm K^{-1} at room temperature)	7.5	4.6	3.4
	Thermal conductivity (W m^{-1} $°C^{-1}$)	19–26	180	90
	Thermal cycles to failure (100 °C–350 °C)	50–75	100	>1380

Table 4. Die-attach critical properties and material comparison [192].

Material	Processing temperature (°C)	Working temperature (°C)	Electrical conductivity $(10^5\ \Omega\ cm)^{-1}$	Thermal conductivity (W cm^{-1} $°C^{-1}$)	CTE (ppm $°C^{-1}$)	Young's modulus (GPa)
$Sn_{63}Pb_{37}$	183	<130	0.59–0.7	0.51	25	16
$Pb_{95.5}Ag_{2.5}Sn_2$	300	<250	0.35	0.23	30	13.8
Sintered nano Ag	280	<600	2.6–3.9	2.4	19	9

The first method is the selection of an encapsulant with a higher dielectric strength. However, the electrical properties of many materials, especially polymers, can change significantly as temperature increases [208]. Nevertheless, the use of passivation coatings, i.e. polyimide conformal coatings, can be a way to supplement this loss of dielectric strength.

The second method is to adjust the ceramic insulating layer of the substrate. Increasing the thickness of the ceramic can reduce the E-field intensity at the triple point but would also increase $R_{th,j-c}$ [209]. Therefore, it should be used sparingly. In the vein of substrate adjustment, stacking multiple metal/ceramic bonded substrates has been demonstrated as an effective method of reducing the E-field and improving the partial discharge inception voltage (PDIV) of the package [210]. By stacking two of these substrates, depending on the material and thickness, an improvement of between 53% [28] and 94% [211] in the PDIV was observed. It should be noted that after two stacked substrates the benefits are curtailed as voltage sharing becomes uneven [211]. In addition, this method may also reduce the overall $R_{th,j-c}$.

Lastly, the application of a coating to the triple point can be an effective way to increase PDIV. A nonlinear resistive coating between the substrate and the encapsulant has been shown to provide an increase of up to 85% in PDIV [25]. This method is incredibly flexible as it can be utilized in combination with a range of architectures and packaging materials, making it a practical way to improve electrical field management. However, further evaluation is needed to understand the performance under higher operating temperatures.

In summary, the packaging for UWBG devices will play a critical role in their ability to operate at their full potential through enhanced heat dissipation, high-temperature operation, thermomechanical stress and strain reduction, and E-field control.

7. Conclusion

The last two decades have witnessed revolutionary advances in power electronics enabled by SiC and GaN power devices. Similar advances are also envisioned with the maturity of UWBG devices. These devices promise continued scaling for power electronics towards a higher frequency, smaller form factor and higher power density. An unavoidable by-product of this scaling is more heat generation in a smaller chip area, which requires increasingly advanced device- and package-level thermal management to ensure safe device operation and long-term reliability. Thus, thermal management is a critical enabler to exploit the electrical superiority of WBG and UWBG power devices.

The thermal management of practical power devices has to account for packaging and cooling. Fortunately, WBG and UWBG power device technologies have both achieved the packaging milestone, in the case of the latter very recently. This paper outlines three basic cooling architectures, followed by discussion of critical device structures and material properties for each WBG and UWBG device technology. Thermal management of packaged WBG and UWBG power devices has been comprehensively reviewed.

Thermal management and packaging of UWBG power devices are still in their infancy and face new challenges that are not present in Si and WBG devices and packages, such as the very high E-field and heat flux, very small die size and the very low k_T of some UWBG materials. Additionally, UWBG power devices offer the unique opportunity to operate at very high temperatures, but the lack of packages operational in such conditions has become a critical roadblock. The solutions to these challenges require a new level of device–package, electrothermal co-design. Additionally, breakthroughs in high-temperature, high-voltage packaging technologies are highly

desirable for expanding the application space of UWBG power electronics.

Finally, we provide perspectives on the key challenges and potential solutions to UWBG thermal management. These perspectives aim at invoking future research in materials science, physics, devices, packaging and power electronics, as well as manifesting the context for more fundamental electro-thermal studies. The exciting research in this area will greatly accelerate the development and deployment of UWBG power devices, and could make a revolutionary change in the landscape of power electronics.

Data availability statement

All data that support the findings of this study are included within the article (and any supplementary files).

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