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# Development of a high accuracy and stability test bench for ageing measurement of 16nm FinFETs based FPGA

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## Abstract

This article describes the development of a test bench so as to measure the ageing of 16nm FinFETs used in a Zynq UltraScale+ FPGA from Xilinx. The Ring Oscillator (RO) drift measurement method was chosen and implemented in the setup. However, RO is a circuit sensitive not only to ageing but also to temperature and voltage. In order to mitigate the undesired sensitivity to temperature and voltage, we installed a regulation system to control the temperature and the internal voltage of the FPGA, and we characterised the RO frequency in function of the temperature and the voltage to apply post-measurement compensations. We improved the measurement circuit by using the GPS signal as a time reference. 1000 hours test with ( $T_{FPGA} = 100^{\circ}C$ ) and ( $V_{FPGA} = V_{nom} + 25\%$ ) was performed and results show clear RO frequency drifts lower than 0.1% measured with an accuracy of  $0.9 \times 10^{-4}$ .

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## 1. Introduction

In order to get more and more efficient digital circuits, the two most important FPGA manufacturers, Xilinx and Intel, use FinFET in the Zynq Ultrascale+ 16nm [1] and Agilex 10nm [2] respectively.

Four well-known failure mechanisms damage FET-based VLSIs [3], [4] are: Time Dependent Dielectric Breakdown (TDDB), Hot Carrier Injection (HCI), Bias Temperature Instability (BTI), and ElectroMigration (EM). The main degradation mode of the failure mechanisms at the circuit scale is the increase of the signal propagation time. The FPGA's modularity and reconfigurability make it an appropriate device to measure signal propagation time degradation of latest technologies. In addition, FPGAs are available at low cost on the public market. In the literature there are four main methods for ageing measurement:

- Transition Probability (TP) [5].
- Ring Oscillator (RO) [6].
- ElectroMagnetic (EM) [7].
- UnderSampling (US) [8].

Table 1 shows the results of most published FPGA ageing tests. Drifts from 1% to 15% are observed for

voltage stress conditions from 1.8 to 2 times the nominal voltage [9, 10, 11] or a stress temperature of  $177^{\circ}C$  [12]. It is obvious that with high voltage and temperature stress, far from the operating values, it is possible to observe propagation time drift for shorter test times. However, this over-stress could result in failure mechanisms which are not representative of the real operating conditions.

In order to observe propagation time drifts with a stress close to the nominal values and for a reasonable test time, it is necessary to have a test bench with a stable environment which leads to accurate measurements. In all long tests, the temperature and voltage are fixed but unregulated except in [10, 13] where the FPGA is placed in a temperature-controlled chamber. Nevertheless, the temperature control is global compared to the local temperature variations within the FPGA. So as to remove some measurement noise, the [9, 10, 12, 14] measurements are averaged which provokes loss of information. The accuracies obtained with not averaged measurement is 0.35% [8] and 0.5% [6], however, this is not enough to observe small drifts in RO.

The objective of this publication is to introduce a high stability test bench in order to measure, with accuracy, the propagation delay drifts in an FPGA. For this we use the RO method. The new features in this paper are:

- The use of the GPS signal as a time reference in the frequency measurement of RO.

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Table 1  
Presentation of ageing test conditions and results using FPGAs

Ref.	Method	Device	T (h)	Volt. $\frac{V_{test}}{V_{nom}}$	Temp.	Max drift (%)	Accuracy (%)
[6]	RO	Cyclone III	1300	1	25°C	2.4	0.5
			360	1.5	25°C	5.5	
[8]	US	Virtex7	144	n.c	n.c	1.5	0.35
		Kintex7	168	n.c	n.c	0.2	
[9]	TP & RO	Cyclone III	1800	1.8	75°C	15	n.c
				1	25°C	0.6	
[10]	EM	Spartan6	168	1.5	80°C	5.17	n.c
[11]	RO	Spartan6	200	2	150°C	2.89	n.c
		Zynq7000			-35°C	1	
[12]	RO	Artix7	864	1	177.5°C	5.13	0.016 (average*)
[13]	RO	ZynqUS+	100	1.3	107°C	0.33	n.c
[14]	RO	Artix7	332	1	35°C	0.3	average*
					125°C	1.8	
[15]	RO	Artix7	12000	1.3	-30°C	0.6	0.072
				1.5	115°C	3.4	
This paper	RO	ZynqUS+	1000	1.25	100°C	0.5	0.009

\*Average: The result is an average of several measures

voltage of the FPGA. To remove noise from the temperature and voltage measurements, we use a sliding average of 1024 measurements, then, these measurements are concatenated with the RO measurements before sending them to the computer for accurate knowledge of the environmental parameters at the time of each RO measurement.

Every 10 minutes, measurements of the 567 ROs are sent. This transmission is divided into 21 sub-sequences of 10 seconds. Finally, each ROs is in measurement mode for 10 seconds and in stress mode the remaining time.

### 2.3. GPS as a time reference

In the measurement circuit, the frequency is measured using a reference signal. Up to now, this signal is built using the FPGA clock, which itself comes from a quartz oscillator. Quartz oscillator ageing and its sensitivity to temperature and supply voltage results in measurement instability for long time tests. In our test bench we added a GPS receiver [18] which provides a PPS (Pulse Per Second) signal. Table 2 gives the means and Standard Deviation (SD) of 3 ROs frequency measured during test presented in subsection 3.3. Table 2 shows lower SD for measurements made with PPS than with quartz signal. Nevertheless, compared to SD, the difference  $\sigma_{Quartz} - \sigma_{GPS}$  is negligible, which mean that the

PPS signal used in the circuit doesn't improve so much measurement accuracy for short term test. In contrast, the PPS signal is maintained by the GPS agency, which guarantees a long-term stable time reference unlike the ageing quartz oscillator.

Table 2  
Mean and Standard Deviation of 3 ROs frequency measured using Quartz and GPS

	$RO_1(Hz)$	$RO_2(Hz)$	$RO_3(Hz)$
$\mu_{Quartz}$	298933212	30082268	295606258
$\mu_{GPS}$	298924859	300814281	295597998
$\sigma_{Quartz}$	47804.8	49294.7	47637.8
$\sigma_{GPS}$	47800.6	49288.2	47632.4

### 2.4. Temperature regulation

In order to reduce temperature variations caused by the FPGA's power consumption or external perturbations, we have developed a regulation loop which stabilises the internal temperature of the FPGA. For this, we use the internal temperature measurement made by the SYSMON to control a Peltier module in contact with the FPGA. To design the regulator, we performed a PRBS (Pseudo Random Binary Sequence) so as to identify the behavioural model of the system. Based on this model, an RST controller [19] is developed in the Processor System (PS) which also receives the temperature

measurement. The output of the regulator is sent to the PL which provides a PWM signal to control the Peltier module.

The temperature regulation allows us to have an internal temperature stress setpoint between [15°C to 115°C] and with an internal FPGA temperature random error of 0.05°C.

### 2.5. Voltage regulation

When there are variations in the power consumption of the FPGA, we observe variations in the internal voltage of a few millivolts. So, we implemented a regulation that uses the voltage measurement from the SYSMON to control the PMIC (Power Management Integrated Circuit) on the Ultra96-V2 board. The nominal voltage supplied by the PMIC to the FPGA is 850mV. It is possible to change the FPGA voltage setpoint by writing to the PMIC registers using the I2C protocol. We designed PI (Proportional Integrated) regulator into the PS, whose output controls the setpoint of the PMIC.

The voltage regulation allows us to have an internal voltage stress setpoint between [-30% to +40%] of the nominal voltage with an accuracy limited by the resolution of the PMIC control which is 3.9mV. However, the SYSMON measurement step is  $\frac{3}{2^{16}} = 0.0458mV$ . The voltage measurement is done at the same time as the RO frequency measurement.

## 3. Measurements

### 3.1. Validation of regulations

To demonstrate the stability improvement with both regulations, we implemented a bench of 1000 ROs in the FPGA which will be switched OFF and ON in order to cause temperature and voltage perturbations. The test is divided into three phases (see Figure 3). Firstly, both regulators are off, secondly, we switch on the temperature regulation (T=30°C) and finally we switch on both regulations (T=30°C and V=850mV). The relative frequency is plotted with a reference frequency measured at T=30°C and V=850mV. Phase 3 highlights the advantage of the two controls on the relative frequency. The noise in the voltage measurement corresponds to the limited resolution of the control which has been mentioned before.

### 3.2. Compensation of measurements

Figure 3 shows that voltage fluctuations lower than the PMIC resolution (3.9mV) have a significant effect on RO frequency. However, as the voltage measurement precision of the SYSMON is quite smaller (0.0458mV),

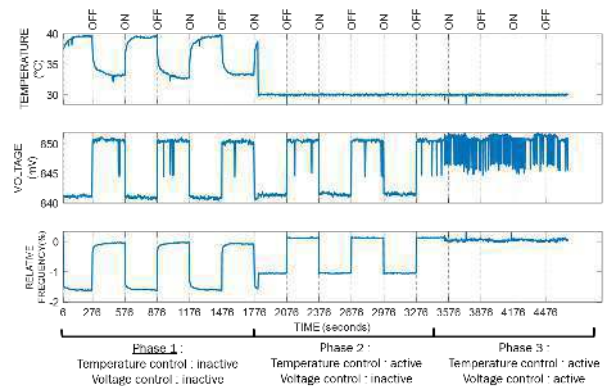


Fig. 3. Temperature and voltage regulation impact on the FPGA parameters a) Internal temperature evolution, b) Internal voltage evolution, c) Evolution of 3 ROs relative frequency average

we can use its measurements to compensate the effect of voltage fluctuation after measurements. Hence, using both regulations, we characterised the RO frequency as a function of temperature and voltage (see Figure 4).

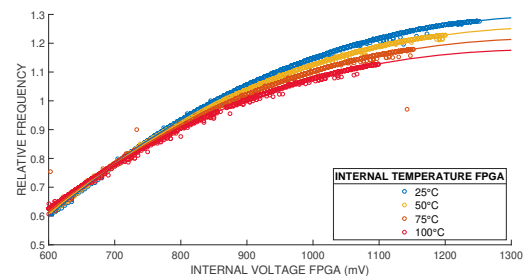


Fig. 4. Characterisation of the RO frequency as a function of temperature and voltage

The relative frequency is calculated for  $V_0 = 850mV$  and  $T_0 = 25^\circ C$ , so that:

$$f_{rc}(t) = \frac{f(V(t); T(t))}{f(V_0; T_0)} \quad (2)$$

Applying a polynomial regression to the measurements in Figure 4 we obtain:

$$f_{rc}(t) = P_{00} + P_{10}V^*(t) + P_{01}T^*(t) + P_{20}V^{*2}(t) + P_{11}V^*(t)T^*(t) + P_{30}V^{*3}(t) + P_{21}V^{*2}(t)T^*(t) \quad (3)$$

where  $V^*(t) = V(t) - V_0$  and  $T^*(t) = T(t) - T_0$ . Eq.3 models the evolution of the relative frequency as a function of temperature and voltage. Figure 4 shows the match between the function and the RO measurements ( $R^2 = 0.999$ ). This characterisation will be used in the following section to compensate measurements.

### 3.3. Use of compensation and ROs drift measurements

During a 1000 hours stress test,  $T_{FPGA}$  and  $V_{FPGA}$  were set at  $100^{\circ}C$  and  $V_{nom} + 25\%$ , respectively. To observe the drift, we evaluated the frequency relative variation such that:

$$f_r(t) = \frac{f(t) - f_{t=0}}{f_{t=0}} \quad (4)$$

where  $f(t)$  is the RO's frequency measurement at time  $t$  and  $f_{t=0}$  is the RO's average frequency on the first day.

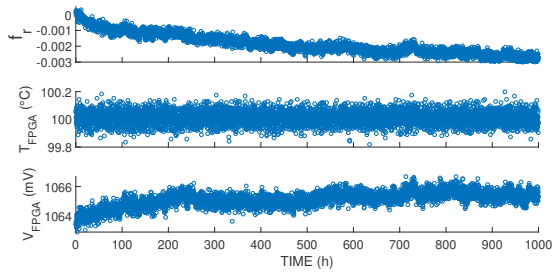


Fig. 5. Upper) Evolution of one RO relative frequency Middle) Evolution of the FPGA temperature Lower) Evolution of the FPGA voltage

In Figure 5 we can see a voltage drift which cannot be regulated because it is lower than 3.9mV.

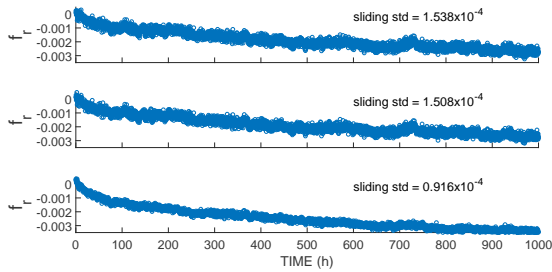
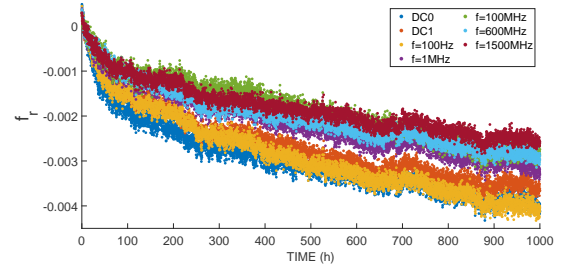


Fig. 6. Measurement of frequency relative variation Upper) Without compensation Middle) With temperature compensation Lower) With temperature and voltage compensation

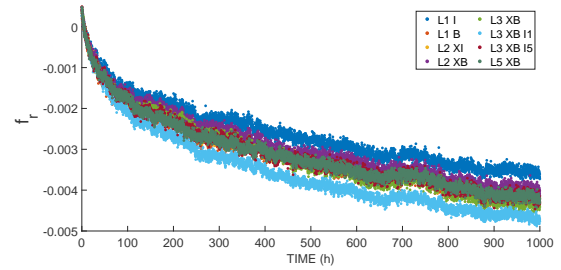
Applying the compensation introduced in section 3.2, we obtain the RO drift only caused by ageing (Figure 6). Figure 6.b shows a minor improvement in the accuracy of the result when temperature compensation is applied, confirming the quality of the regulation to stabilise the internal temperature. With the voltage compensation, (Figure 6.c) the accuracy (sliding standard deviation of the measurement) is improved. We obtained an accuracy of  $0.9 \times 10^{-4}$  against  $1.5 \times 10^{-4}$  for the uncompensated measurements.

Figure 7 shows the drift results for different ROs configurations. Thanks to the accuracy of the test bench,

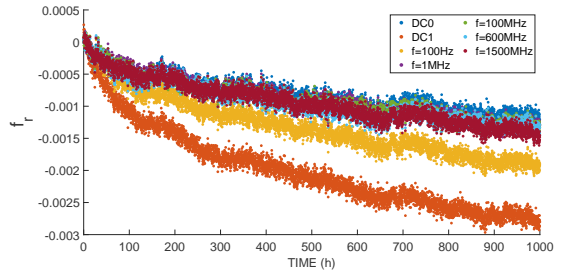
we can observe the different drifts in function of the internal stress or the architecture in a short test time and with the FPGA working close to its nominal conditions. As explained in section 2.1, the ROs in Figure 7a and Figure 7b measure mainly the degradation of LUTs and the ROs in Figure 7c measure mainly the degradation of routing. Figure 7a shows that LUT degradation is more sensitive with static stress (DC0, DC1 or low frequency) than with high frequency stress. Figure 7b shows the influence of RO architecture (cf. Figure 2). Finally, for long paths RO, Figure 7c shows a maximum degradation for high static stress (DC1) and a minimum degradation for low static stress (DC0).



(a) RO : L1 B ; stress frequency : variable ; stress duty cycle : 0.5



(b) RO : variable ; stress frequency : 0 ; stress duty cycle : 1



(c) RO : LP ; stress frequency : variable ; stress duty cycle : 0.5.

Fig. 7. ROs variations with different parameters of internal stress or architecture

Using nonlinear least squares algorithm we fit data from Figure 7a with power model. We plotted module of those data with power model in log-log scale (Figure 8) so as to extract degradation parameters. First

of all, we remind that stress conditions are  $100^{\circ}\text{C}$  and  $V_{nom} + 25\%$  during 1000 hours. Those stress conditions are well known to accelerate degradation due to BTI. From power model we can extract the time exponent which is between 0.28 – 0.35. Those results are slightly higher than what is found in the literature concerning BTI time exponent [20] but sufficiently close to associate this degradation with BTI. Indeed, we have not an usual BTI ageing measurement setup (isolated transistors) : the circuit is made of PMOS and NMOS which are both stressed for any stress signal (static and dynamic) and are subject to recovery at least during measurement phase.

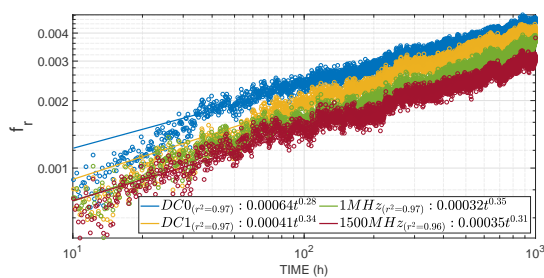


Fig. 8. 4 ROs drift plot in log-log for several internal stress conditions

#### 4. Conclusion

In this work, a test bench based on Ring Oscillator methodology for high precision and stability ageing measurements has been developed and applied to a 16nm FinFET based FPGA. To improve the measurements accuracy and stability, a GPS signal has been used as a time reference. In addition, FPGA internal temperature and voltage regulation has been achieved with an accuracy of  $0.05^{\circ}\text{C}$  and  $3.9\text{mV}$ . Furthermore, a  $f(T;V)$  characterisation has been performed for post-measurement compensations. Performances of the test bench have been tested on a preliminary ageing study of 1000h. The standard deviation of  $1.5 \times 10^{-4}$  has been obtained without compensation and  $0.9 \times 10^{-4}$  with compensation. Such accuracy has made it possible to observe clear drifts of less than 0.1% under temperature and voltage stress conditions close to the nominal conditions ( $T_{FPGA} = 100^{\circ}\text{C}$  and  $V_{FPGA} = V_{nom} + 25\%$ ) for a relatively short test time.

#### 5. Acknowledgements

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