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Influence of process parameters on electrical properties of PiN diodes fabricated with a highly p-type doped layer selectively grown by VLS transport.

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The quality of 4H-SiC bulk and epilayer material is day after day improving and several unipolar devices such as Schottky and JBS rectifiers, JFETs and MOSFETs are commercially available. Nevertheless, some technological barriers still persist like the local and in depth doping into the SiC top epilayer. Indeed, a defect-free area with high doping level is very difficult to obtain by ion implantation. Furthermore, the depth of the implanted area is limited to several hundred of nanometers using standard ion implanters.

SiC Selective Epitaxial Growth (SEG) by Vapor-Liquid-Solid (VLS) transport on a bowl-shaped geometry appears to be a promising solution to perform deep, highly doped and high quality p-type doped area. Such SEG-VLS growth of highly p-doped ($> 5 \times 10^{19} \text{ cm}^{-3}$) SiC layer was successfully demonstrated recently on large and small areas fabricated by Reactive Ion Etching (RIE) [1]. Moreover, a high quality P⁺⁺(VLS)-N junction can be achieved by using this technique that offer new prospects for the achievement of new power electronics devices, including deeply buried peripheral protection zones such as guard-rings or JBS structures [2].

This work presents the influence of some process parameters and crystal orientation on both forward and reverse characteristics of PiN diodes composed of p⁺⁺-layers emitter and guard-rings peripheral protection fabricated by SEG-VLS. Fig. 1 reports a picture of a typical processed PiN diode. Spacing between two adjacent guard-rings has been optimized by Sentaurus TCAD finite elements simulation. Simulated breakdown voltages of a diode without and with optimized 3 guard-rings peripheral protection are $V_{br} \sim 500 \text{ V}$ and $V_{br} \sim 1200 \text{ V}$ respectively. Different configurations of guard-ring spacing were tested on the fabricated devices and will be detailed in the final paper.

The processed samples were composed of a 15 μm thick, $N_d = 5 \times 10^{15} \text{ cm}^{-3}$ doped n⁺ layer, grown in a hot-wall CVD reactor on commercial n⁺ 4H-SiC wafers. The Emitter and guard-ring have been defined together by RIE. Then an Al(1.5 μm)/Si(1.1 μm) stacking were deposited and selectively etched in order to fill the patterns only. After performing the VLS growth as described in [1], the 500 nm SiO₂ passivation layer was deposited by PECVD. Finally cathode and anode ohmic contacts were formed by annealing e-beam deposited Ni based and Ni/Ti/Al based metallic stacking. The final result is showed in fig. 1 and the targeted structure is described in fig. 2. The detail of process variations is reported on Table I.

Fig. 3 reports forward current-voltage characteristics recorded at various temperatures of three diodes fabricated with different processes. One can see that the static forward behaviors of diodes change dramatically as a function of the process. For example, “process A” diodes have a Schottky like behavior, “process B” diodes have a bipolar behavior and “process C” diodes exhibits both Schottky and bipolar characteristics in the same time.

Changes on the reverse characteristics has also been observed and, in particular, on the breakdown voltage (V_{br}). For example a maximum of $V_{br} = 900 \text{ V}$ is observed for “process A” diodes when a maximum of $V_{br} = 100 \text{ V}$ has been observed for “process B” diodes. Since the maximum V_{br} value of

“process A” diodes is higher than simulated V_{br} without guard-rings, we can conclude that p^{++} SEG-VLS layers are really promising for the fabrication of deep guard-rings peripheral protection.

In order to explain the large variation of V_{br} and forward static electrical properties, we performed active degradation characterizations (AD), Photo-Emission Microscopy (PEM) and Transmission Electron Microscopy Observations (TEM). Fig. 4 reports TEM pictures of the VLS layer and demonstrates that some processes generate a lot of defects and poly-typism (“Process D”) while some generate almost defect free layers (“process E”). These differences directly affect the properties of the diode.

In the final paper, we will correlate electrical measurements to TEM and PEM observations in order to model the diode behavior and propose improvements of the VLS growth.

[1] D. Carole *et al*, Materials Science Forum 717-720, 169 (2012)

[2] N. Thierry-Jebali *et al*, Material Science Forum, 740-742, 911 (2013)

Table I. Process variations of fabricated diodes

Process name	A	B	C	D	E
Substrate orientation	On-axis		8°-off		
Al/Si deposition technique	e-beam		sputtering	e-beam	
Post VLS annealing	No	1700°C, Ar, 30 min		No	1700°C, Ar, 30 min

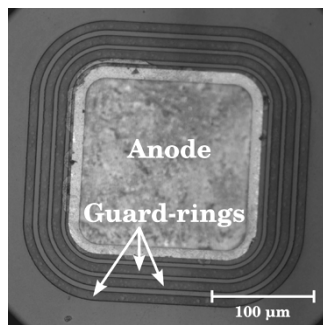


Fig. 1. Optical image of a typical processed PiN diode

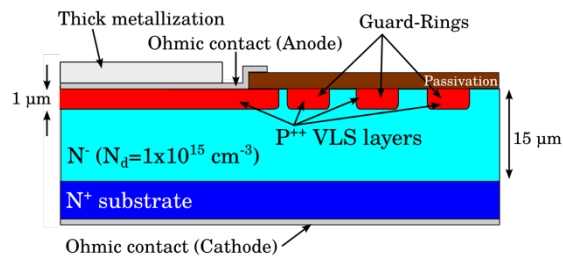


Fig. 2. Cross section of the fabricated diodes.

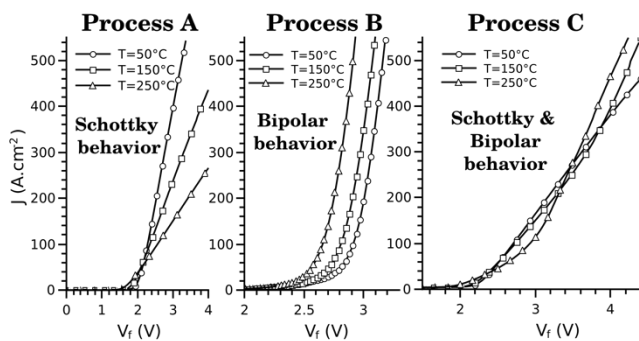


Fig. 3. Forward J-V behavior at 50 °C, 150 °C and 250 °C of 3 different diodes

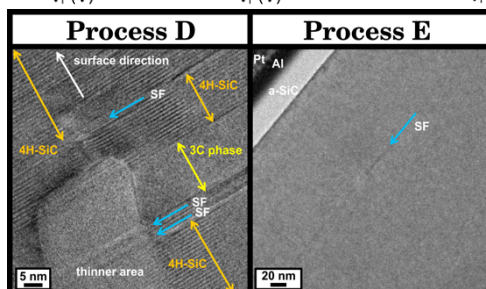


Fig. 4. High Resolution Bright Field Transmission Electron Microscopy pictures of VLS layers after two different processes.