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# Modeling of carrier lifetime based on deep-Level transient spectroscopy for power PIN diodes

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Abstract—The dynamic performances of PIN diodes are very difficult to predict with Technology Computer-Aided Design (TCAD) simulation tools, especially when the carrier lifetime is adjusted. The standard simulation model used in TCAD tools for carrier lifetime is based on Shockley-Read-Hall (SRH) recombination theory. This model is not sufficient as it considers the presence of only one deep energy level located at the material mid-gap. Used as a lifetime killer, **Platinum doping introduces** several deep energy levels facilitating the minority carrier recombination. Thus, a new approach based on trap physical description is performed using Deep Level Transient Spectroscopy (DLTS) measurement technique. This approach has significantly reduced the large mismatch observed between the PIN diode turn-off measurements and the standard simulation model results.

Keywords— Power PIN diode, Turn-off transient characteristics, Platinum diffusion, carrier lifetime control, traps simulation model, Deep Level Transient Spectroscopy (DLTS)

#### I. INTRODUCTION

Nowadays, various lifetime control techniques are used in the industry to make semiconductor power devices much faster, especially when operating in switching mode. The reduction of carrier lifetime can be made by the diffusion of metallic impurities such as Gold and Platinum, or by high energy irradiation [1].

Metallic atoms are intentionally introduced into Silicon in order to generate deep levels in the band gap. Those levels act as intermediate levels in the band gap and facilitate the carrier mobility between the conduction band and the valence band. Thus, this can reduce the minority carrier lifetime allowing an important improvement in the electrical characteristics of power devices. Actually, this reduces the switching time delay of the power devices making them faster. On the other hand, the carrier lifetime reduction generates an increase in the onstate voltage drop ( $V_f$ ). As a consequence, a trade-off between the static and the dynamic performances of power devices is required [1,2].

The location of defect levels in the band gap is important insofar as it impacts the leakage current. Indeed, a defect level located at the mid gap generates a higher leakage current than level located far from the mid gap. For this reason, Platinum is used as an alternative to Gold despite of its efficiency in lifetime control. Studies have shown that Gold generates much higher leakage current than Platinum [1,3].

TCAD tools have always been essential in the research field to model and predict realistic behavior of new technologies allowing industrial developments with a lower cost. The good TCAD simulation predictivity is based on the models chosen to represent real phenomena occurring into the device. In special cases, simulation models need to be calibrated to reduce prediction errors.

Platinum introduces electrically active levels in the Silicon band gap. Nevertheless, Platinum modeling does not exist in TCAD tools like it does for Boron and Phosphorus. The simulation model usually used in TCAD Sentaurus tools to describe the recombination through deep levels is Shockley-Read-Hall recombination model (SRH). SRH considers the presence of only one deep level located in the middle of the material band gap [4]. Currently, several deep Platinum related levels are observed into the Silicon band gap using Deep Level Transient Spectroscopy (DLTS) measurement technique. In order to take into account the presence of these levels in the simulation model, SRH recombination model was replaced with a new approach. This approach is based on the DLTS measurements of traps characteristics such as the traps energy levels  $E_T$ , the capture cross-sections  $\sigma_T$ , and the traps concentrations N<sub>T</sub>. Finally, an advanced measurement method is conducted to determine the Platinum concentration profile in the Silicon bulk for each deep level, based on both DLTS measurements and current-capacitance measurements.

#### **II. EXPERIMENTAL RESULTS**

#### A. Sample properties

In this part, samples which are modeled with TCAD Sentaurus tools and measured by DLTS techniques will be presented. The diodes designed and manufactured by STMicroelectronics, are P+N-N+ structure from an epitaxial Czochralski-grown N-type Silicon substrate.

Fig. 1 shows the diode structure composed of a lightly N-doped layer (N-) in between a heavily P-doped anode layer

(P+) and a heavily N-doped cathode layer (N+). The N- layer has a doping concentration of approximately  $10^{14}$  at.cm<sup>-3</sup>.

The thickness of the central region is designed in order to support 750V breakdown voltage. The edge termination of the diode structure is composed of a P-doped guard ring and N+ regions. It is designed in order to protect the diode from a premature destruction which can occur when the diode is reverse biased, by avoiding tightening of the equipotential bonding at the edge of the component.

At the end of the manufacturing process and before the metallization step, the diode is intentionally doped with Platinum atoms from a Pt-silicide layer on the front side. Platinum is then thermally annealed during few hours, at a temperature above 800°C. This step is required in order to reduce the switching rate of the diode when operating in the dynamic mode. In fact, it reduces the lifetime of the minority charge carriers stored during the ON-state that needs to be evacuated when switching to the OFF-state.



Fig. 1. The P+N-N+ diode cross section view.

#### B. Deep Level transient Spectroscopy measurements

The DLTS is a non-destructive measurement technique, proposed by Lang in 1974 [5], to characterize traps in semiconductors. It is based on measuring the emission rate of carriers captured by a deep level (trap) as a function of the temperature. A temperature scan ranging from 80K up to 300K is needed in order to activate all the traps present in the Silicon gap.

DLTS measurements are first performed on P+N-N+ diodes without Platinum (reference diode) and compared with measurements performed on Platinum-doped diode in order to detect any non-Platinum contamination.

A reverse voltage  $V_R$  of -10V is applied to the diodes, in order to empty all present traps from carriers, followed by a filling pulse  $V_P$  of +1V. The pulse voltage is maintained during 0.1ms to fill all the traps present in the Silicon gap. The diode is then reverse biased again in order to emit (reject) all carriers captured by traps during the previous phase.

DLTS measurements performed on the Platinum-doped diode showed the presence of three different deep levels in the Silicon gap. Note that the DLTS spectrum of the reference diode shows no defects. This confirms that defects detected are exclusively Platinum-related defects (Fig. 2).

The DLTS software is configurated to give positive peaks for majority carriers and negative peaks for minority carriers. As the drift layer expands mainly in the lightly doped region (N-), the two positive peaks detected at 105K and 265K, are identified as electron traps. A negative peak is also detected at 170K, and is identified as a hole trap.



Fig. 2. DLTS measurement on the P+N-N+ Platinum doped diode.

The first trap  $E_{T1}$  is an acceptor level located at 0.22eV from the conduction band. The second trap  $E_{T2}$  is a donor level located at 0.32eV from the valence band. The third trap  $E_{T3}$  is an acceptor level located at 0.50eV from the conduction band.

Referring to the literature,  $E_{T1}$  and  $E_{T2}$  are identified as substitutional Platinum defect (Pt<sub>s</sub>), and the  $E_{T3}$  is identified as a Pt-X defect complex. Regarding its very low amplitude at the surface compared to the two other defects, this mid-gap defect is not systematically detected and not taken into consideration in all defect studies. In some studies, it is considered as a Platinum-Hydrogen (Pt-H) defect complex [6,7]. while others consider that it is Platinum-Oxygen (Pt-O) defect complex [8]. As the Pt-H complexes can be dissociated at an annealing temperature above 450°C [3], the  $E_{T3}$  level is probably a Platinum-Oxygen defect complex.

Our experimental results obtained by DLTS measurements are in a good agreement with at least three studies : Prohinig *et al.* [6] present three levels located at  $E_{C}$ -0.23eV,  $E_{V}$ +0.36eV, and  $E_{C}$ -0.50Ev, Kwon *et al.* [8] present three levels located at  $E_{C}$ -0.23eV,  $E_{V}$ +0.36eV, and  $E_{C}$ -0.52eV, and Gill *et al.* [9] present three levels located at  $E_{C}$ -0.23eV,  $E_{V}$ +0.36eV, and  $E_{C}$ -0.23eV,  $E_{V}$ +0.32eV, and  $E_{C}$ -0.55eV.

The DLTS measurements allow to determine the physical characteristics of traps such as the trap type, the energy level, the concentration, and the capture cross section, near the diode junction. All of these parameters will be integrated in the trap simulation model (Table 1).

	Energy level [eV]	Concentratio n [at.cm <sup>-3</sup> ]	Capture cross section [cm <sup>2</sup> ]
Ет1	E <sub>C</sub> -0.22	$1.14 \times 10^{+14}$	5.38×10 <sup>-14</sup>
E <sub>T2</sub>	Ev+0.32	4.34×10 <sup>+12</sup>	2.69×10 <sup>-12</sup>
E <sub>T3</sub>	E <sub>C</sub> -0.50	$3.89 \times 10^{+10}$	1.00×10 <sup>-15</sup>

TABLE 1. PHYSICAL CHARACTERISTICS OF TRAPS OBSERVED WITH DLTS MEASUREMENT

#### **III. SIMULATION MODEL**

Traps play an important role in simulation model when introduced intentionally into the device like Platinum in our case. They significantly impact the device conductivity by enhancing recombination. As mentioned earlier, the Shockley-Read-Hall recombination model consider a single mid-gap. It is based on the value of electrons and holes lifetime which is used as a calibration parameter to control the switching rate. Thus, the new approach based on DLTS measurements describes more precisely the physical phenomena involved.

#### A. Methodology

To overcome the SRH recombination model limitations, the SRH model is disabled in the simulation and a traps model is introduced.

For that, DLTS measurements performed on the PIN diode are used such as the traps type, the energy level, and the capture cross section (Table 1). The Traps concentration obtained by DLTS measurements is not sufficient to describe the Platinum concentration profile. The given value is measured near the diode junction. However, the Platinum concentration is not homogeneous in the whole device volume. It varies as a function of the intrinsic zone thickness of the PIN diode [3]. To obtain a complete trap concentration profile, several DLTS measurements are performed with varying the reverse voltage applied to the PIN diode. Measurement equipment is limited to -35V. This allows to determine the real trap concentration profile up to about twenty micrometers from the diode junction. To complete the concentration profile, the starting DLTS profile is extrapolated with respect to a simulated Platinum profile based on Vervisch et al. study [10]. This method is used only for  $E_{T1}$  and  $E_{T2}$  traps. The concentration of the third trap  $E_{T3}$  is very low and hard to measure. Thus, its concentration profile determined by capacitance and reverse current is measurement based on Prohinig et al. study [6].

The complete Platinum concentration profile obtained for each trap is then implemented in TCAD Sentaurus tools. Finally, electrical simulations are made in order to evaluate the diode simulation model in the switching mode.

#### B. Trap model parameters

#### a) The type:

The carrier type of traps is determined from the DLTS spectrum. The software configuration is fixed to give a positive peak for electrons traps and a negative peak for holes traps in the case of a P+N-N+ diode [11]. Thus, two acceptor and one donor levels are introduced in the trap simulation model.

#### b) The energy level:

The trap energy level is determined from the Arrhenius plot of the emission rate as a function of temperature.

The following expression denotes the Arrhenius-equation in the case of an N type region [11].

$$\ln(\tau_e V_{th,n} N_C) = \frac{E_C - E_T}{k} \frac{1}{T} - \ln(\chi_n \sigma_n)$$
(1)

 $\tau_e$  denotes the emission time constant,  $V_{th}$  the thermal velocity, and N<sub>C</sub> the state density.  $\chi_n$  is the enthalpy factor, and  $\sigma_n$  is the electron capture cross section.

The thermal velocity  $V_{th}$  and the state density  $N_{C}$  expressions are represented by the following equations.

$$V_{\rm th} = \sqrt{\frac{3kT}{m_n^*}} \tag{2}$$

$$N_{\rm C} = \left(\frac{2\pi m_{\rm n}^* k T}{h^2}\right)^{\frac{3}{2}}$$
(3)

 $m_n^*$  is the effective mass for electrons, k is Boltzmann constant, and h is Planck constant.

The energy level  $(E_C-E_T)$  is then obtained from the slope of (1).

#### c) The concentration:

The trap concentration is obtained from the amplitudes of DLTS signal made of discrete Fourier coefficients (Fig. 2). The DLTS measurement gives a single value of trap concentration, whereas the concentration is not constant through the device volume. In fact, several studies show that Platinum concentration has a symmetrical distribution [8,10, 12,13,14]. It increases near the surface, decreases in the middle of the wafer volume, and then increases to reach the wafer backside surface. Then, it forms a symmetrical shape about the center line of the wafer. A half profile is sufficient in our case to cover the entire intrinsic zone of the diode.

In our work, the Platinum concentration profile of each trap level is obtained by varying the reverse voltage applied to the PIN diode from -1V to -35V with a step of 1V (equipment limitation). Indeed, the thickness of the probed area depends on the reverse voltage applied. It increases as |VR| applied increases. With a maximum of -35V, the probed area is about twenty micrometers from the diode junction. This allows to determine the trap concentration profile near the surface.

The trap concentration sum forms the substitutional Platinum concentration. Fig. 3 represents the Badr *et al.* work results [12] compared to our  $Pt_s$  concentration measured by DLTS. The authors presented the measured Platinum depth profile compared to simulated Platinum depth profile. The concentration profile is obtained from DLTS measurement techniques by etching the sample surface progressively. The sample is Platinum diffused at 830°C during 2h with a cooling rate of 4.6K/min. The simulation model is based on Jacob *et al.* study [13,14]. A slower cooling rate is used for the simulation curve in order to show its effect on the Platinum profile within about 10 micrometers from the surface. With a lower cooling rate, Platinum profile changes from U-shape to M-shape, sach as the case of our samples.



Fig. 3. Comparison between Badr and Jacob's  $Pt_s$  concentration profile and the measured  $Pt_s$  concentration profile of this work, as a function of the sample depth.

It is totally coherent that the  $Pt_s$  concentration profile measured near the surface, in this work, is higher than Badr and Jacob studies, due to the mismatch of the temperature and diffusion time.

In order to obtain the complete depth profile, the concentration profile of each trap is developed with different approaches. The measured profile of  $E_{T1}$  is not sufficient to be extrapolated as a function of the depth. A simulated Platinum profile based on Vervisch model [10] is used which allow to predict the global substitutional Platinum profile. As the  $E_{T1}$ 

Platinum profile is the most consequent in term of amplitude (Table1), its concentration profile is proportional to the simulated substitutional Platinum profile (Fig. 4).

The measured profile of  $E_{T2}$  is sufficient to be extrapolated mathematically as a function of the depth as shown in Fig. 5.



Fig. 4.  $E_{T1}$  trap depth profile obtained by DLTS measurements and extrapolation.



Fig. 5.  $E_{T2}$  trap depth profile obtained by DLTS measurements and extrapolation.

The concentration of the third trap  $E_{T3}$  is very low and hard to measure. For that reason, some authors neglect it [8,9]. A method based on reverse current voltage (I-V) and capacitance voltage (C-V) characteristics allow to determine the Platinum concentration profile of traps located near the Silicon mid gap [6,15,16].

The depth profile is calculated from the generation current density  $J_{gen}$  as a function of the depletion width, as expressed in (4).

$$N_{\rm T}({\rm x}) = \frac{1}{q\xi} \frac{dJ_{\rm gen}}{d{\rm x}} \tag{4}$$

With q the elementary charge,  $\xi$  the trap emissivity, and x the depletion width.

The generation current density is obtained from the reverse current density  $J_R$ . Indeed, in a PN junction which obeys the SRH theory, the reverse current density  $J_R$  is the sum of the generation current density  $J_{gen}$  and the diffusion current density  $J_{diff}$  (5).

$$J_{\rm R} = J_{\rm gen} + J_{\rm diff} \tag{5}$$

Indeed, the generation current is created by the carrier generation in the depletion region. The diffusion current is created by the carrier generation which occurs in the intrinsic zone (out of the depletion region) followed by the diffusion of these carriers towards the depletion region. However, a nonnegligible part of the current can appear when the diode is reverse biased with a very high voltage close to the avalanche voltage, called the impact generation current (Fig. 6).



Fig. 6. Reverse current density curve as a function of the depletion region depth

Currents are then separated by the method proposed by Murakami *et al.* [17]. It consists of plotting the reverse current density as a function of the depletion width calculated from the C-V characteristics. This leads to a linear dependence of the reverse current density on the depletion width. The linear part of the reverse current density is the generation current density which is defined by (6). It starts at a reverse voltage of -5V to about -700V (Fig. 7). The slope of this line gives information about the generation lifetime ( $\tau_g = 8 \times 10^{-4}$ s). The current diffusion is given by the y-intercept ( $J_{diff} = 1 \times 10^{-9}$  A/cm<sup>2</sup>).

$$J_{gen} = \frac{qn_iW}{\tau_g} \tag{6}$$



Fig. 7. The linear part of the reverse current curve as a function of the space charge region.

The trap emissivity is defined as a function of the  $E_{T3}$  concentration measured by DLTS near the junction, and the generation lifetime.

$$\xi = \frac{qn_i}{N_{T3}\tau_g} \tag{8}$$

n<sub>i</sub> is the intrinsic carrier density.

With an emissivity of  $394s^{-1}$ , the variation of the generation current density as a function of the depletion width gives the depth profile of the third trap labeled  $E_{T3}$  shown in Fig. 8. This value is consistent with the trap emissivity calculated by Prohinig *et al.* [6] and Rasinger *et.al* [15] respectively  $470s^{-1}$  et  $450s^{-1}$ .



Fig. 8.  $E_{T3}$  trap depth profile obtained by DLTS measurement and I-V and C-V measurements.

#### d) The capture cross section

The capture cross section of the trap is the intersection of the Arrhenius plot of (1) with the y-axis giving the product  $\chi_n \sigma_n$ .  $\chi_n$  is the enthalpy factor.

#### IV. RESULTS AND DISCUSSIONS

To validate the diode simulation, the diode electrical behavior is investigated under the dynamic mode. The key parameters which allow to evaluate the carrier lifetime control are the reverse recovery time delay  $(t_{rr})$ , the maximum reverse current (I<sub>RM</sub>), and the reverse recovery charges (Q<sub>rr</sub>).

In this part, simulation results obtained with the SRH recombination model and those achieved with the new approach are compared with the electrical measurements results performed on the ultrafast power diode in the dynamic mode at room temperature.

Fig. 9 presents a simplified schematic of the electrical switching circuit used in simulation to operate the diode in the dynamic mode. It is composed of an IGBT to act as a switch, and the diode under test placed in parallel with an inductor. That way, the diode will be reverse-biased when a direct voltage is applied, and the switch is ON. When the switch is OFF, the diode is forward biased. The transition between ON and OFF state is softened by the presence of the inductor. In addition, parasitic inductors are considered in order to include the IGBT and the diode packaging loses.



Fig. 9. A simplified schematic of the electrical switching circuit used to operate the diode in the dynamic mode.

The simulation curve of the reverse current in the switching mode, made with the standard simulation model (SRH), is plotted and superposed on the measurement curve in order to demonstrate the large gap between simulation results and measurements (Fig. 10).



Fig. 10. Simulated reverse current curve with SRH model compared to the measured reverse current curve, in the switching mode.

The simulation curve of the reverse current based on trap model is also superposed to the measurement (Fig. 11).



Fig. 11. Simulated reverse current curve with traps model compared to the measured reverse current curve, in the switching mode.

The comparison between measurement and simulation results is also made by calculating the percentage deviation between measurement and simulation results.

Table 2 presents the simulation results performed at room temperature performed with the standard SRH model and the new approach based on trap description. Simulation results performed with SRH model show an important gap between the simulation and the experimental results. Simulation results performed by trap model improve significantly the simulation performances. In term of I<sub>RM</sub>, the simulation results performed with the new approach are in a good agreement with the measurements with a percentage deviation about 5.0%. A less good result in terms of t<sub>rr</sub> and Q<sub>rr</sub> but still acceptable compared to the initial gap obtained with SRH recombination model.

TABLE 2. THE PERCENTAGE DEVIATION OF SIMULATION RESULTS FROM MEASUREMENTS IN THE DYNAMIC MODE AT ROOM TEMPERATURE

	I <sub>RM</sub>	t <sub>rr</sub>	Qrr
SRH model	+51.8%	+33.1%	+79.5%
Trap model	+5.0%	+16.5%	+13.8%

#### V. CONCLUSION

Electrical simulation results of the PIN diode performed with the standard SRH recombination model showed a big difference with the measurements in the dynamic mode. To improve the obtained results, a new approach based on traps description is performed and gives a better agreement with the measurements. This new approach is based on DLTS measurements which allows to detect the presence of three different traps Platinum-related against a single trap considered in the SRH recombination model. In addition, another measurement technique based on DLTS is used in order to determine the Platinum depth profile for each trap level by varying the reverse voltage applied to the PIN diode. Thus, the new simulation model presented allows not only to predict the electrical behavior of Platinum doped diodes in the dynamic mode, but also to better predict the trade-off required between the static mode and the dynamic mode, and to investigate the phenomena occurring during the diode Turnoff

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#### NOTATION

- TCAD Technology Computer-Aided Design
- SRH Shockley-Read-Hall
- DLTS Deep Level Transient Spectroscopy
- Si Silicon
- Pt Platinum
- Pts substitutional Platinum
- Pt-X unknown defect complex associated to Platinum
- Pt-H Platinum Hydrogen complex
- Pt-O Platinum oxygen complex
- VF diode drop voltage
- trap energy level Ет
- Nt trap concentration
- trap capture cross section ( $\sigma_n$ ,  $\sigma_p$ ) σт
- Ec conduction band energy level
- Ev valance band energy level
- VR reverse voltage
- VP pulse voltage
- time pulse tp
- electron capture cross section  $\sigma_n$
- $\sigma_p$ hole capture cross section
- enthalpy factor χn
- emission time delay  $\tau_{e}$
- ξ Vth,n trap emissivity
- electron thermal velocity
- Nc state density
- electron effective mass m<sub>n</sub>\*
- Boltzmann constant k
- Planck constant h Т
- temperature reverse current  $J_R$
- generation current Jgen
- diffusion current  $J_{\text{diff}}$
- generation lifetime
- $\tau_{g}$ trr
- reverse recovery time delay  $Q_{rr}$ reverse recovery charges
- Irm maximum reverse current
- IGBT Insulated Gate Bipolar Transistor

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