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► **To cite this version:**

Madeleine Abernot, Thierry Gil, Aida Todri-Sanial. ONN-Based On-chip Learning for Obstacle Avoidance on Mobile Robot. SSI 2023 - Smart System Integration Conference, Mar 2023, Bruges, Belgium. <hal-04007886>

HAL Id: hal-04007886

<https://hal.science/hal-04007886v1>

Submitted on 2 Mar 2023

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ONN-Based On-chip Learning for Obstacle Avoidance on Mobile Robot

Madeleine Abernot^a, Thierry Gil^a, and Aida Todri-Sania^{a,b}

^a *LIRMM, University of Montpellier, CNRS, 161 rue Ada, Montpellier, France*

^b *Electrical Engineering Department, Eindhoven Technical University, Eindhoven, Netherlands*
aida.todri@lirmm.fr

The amount of data available to process at the edge has increased drastically in the last decades with the emergence of edge devices in numerous domains. Moreover, the increasing amount of data requires powerful artificial intelligence (AI) algorithms, such as deep learning algorithms to process the data, and they are very power-hungry. Thus, there is a lot of ongoing research on how to train and compute on edge devices. Current hardware architectures based on von Neumann are not adapted for AI algorithms due to the processing to memory transfer bottleneck [1]. Recently, neuromorphic computing, which proposes brain-inspired hardware-based paradigms, has emerged as a suitable solution to edge computing, removing the von Neumann bottleneck [1].

Oscillatory Neural Network (ONN) is a promising neuromorphic computing paradigm for AI at the edge. ONNs [2,3,4] are networks of coupled oscillators using the natural synchronization behavior of oscillators to compute. Information is encoded in the phase relationship among oscillators to reduce the voltage amplitude and limit power consumption [5]. In state-of-the-art, ONN is configured with a fully-connected recurrent architecture, and trained with unsupervised learning to solve auto-associative memory tasks, like pattern recognition. In the framework of the EU H2020 NEURONN [6] project, we explore ONN architectures, learning algorithms, and applications to showcase ONN advantages for edge computing. We developed a fully-connected recurrent ONN in digital to implement it on FPGA to explore ONN edge applications and on-chip learning capabilities [7]. For example, using the ONN auto-associative memory properties, we demonstrated it can efficiently solve real-time obstacle avoidance application on mobile robots equipped with proximity sensors [8,9]. In this case, we cascade two ONNs, one trained to detect obstacles and the second trained to define the novel robot direction. Later, we updated the system with an all-in-one architecture based on a Xilinx Zynq processor to have an ONN-based System-on-Chip (SoC) capable of reading, conditioning, and treating sensory data [9]. In parallel, we also explore ONN on-chip learning capabilities with the digital design. Recently, we proposed a novel architecture, also based on the Zynq processor, to allow ONN on-chip learning for auto-associative memory tasks [10].

In this work, we combine both the obstacle avoidance application with the on-chip learning capability. We propose an architecture that incorporates the on-chip learning in the ONN-based SoC architecture configured for robot obstacle avoidance, see Fig. 1. In particular, we propose to have a pre-trained ONN to detect obstacles, and a non-trained or half-trained ONN to define direction. The training of the second ONN is done by using an additional post-processing from the first ONN output to define a direction. This computed direction is then compared with the direction given by the second ONN output. A difference between the two activates the training of a novel pattern. After numerous cycles without any difference, we consider the second ONN trained, and we remove the post-processing algorithm. Results from [9] and [10] are encouraging to perform real-time on-chip learning with ONN for mobile robot obstacle avoidance application.

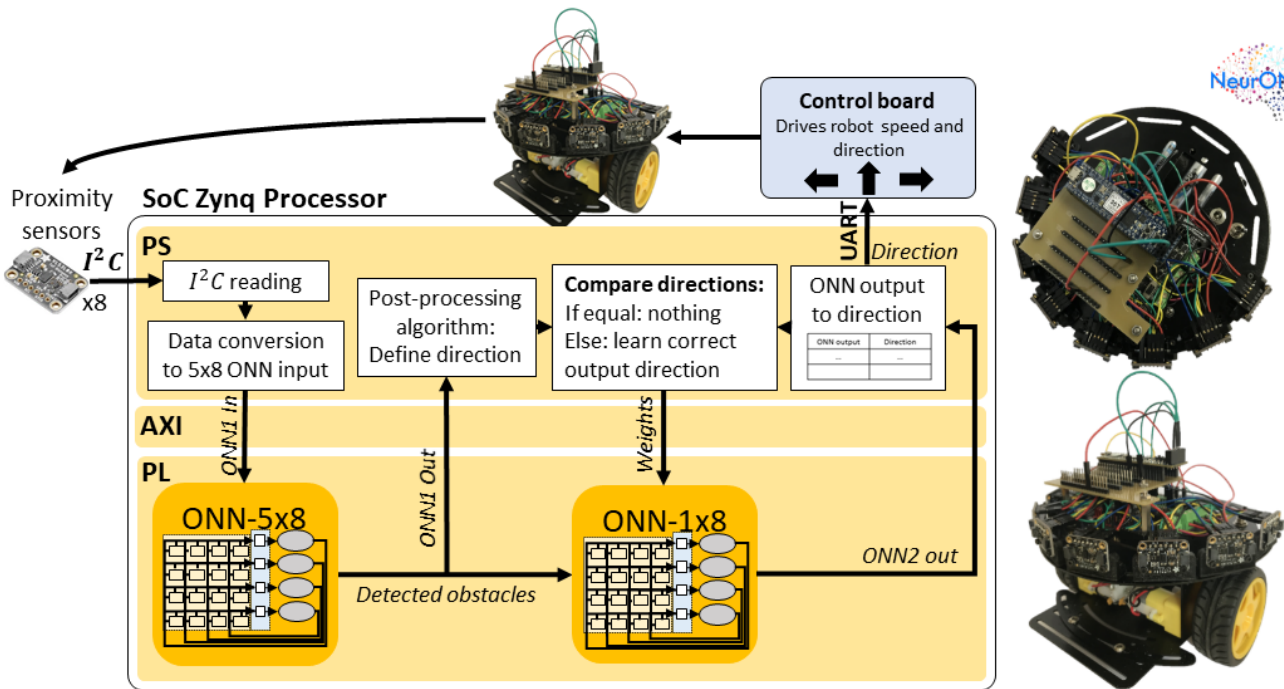


Fig. 1: Schematic of the architecture to perform ONN on-chip learning for obstacle avoidance.

Acknowledgment

This work was supported by the European Union's Horizon 2020 research and innovation program, EU H2020 NEURONN (www.neuronn.eu) project under Grant 871501.

We thank CNRS, CSIC, and AIM collaborators for the fruitful exchanges with members of the project.

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