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# A study on the challenges in GaN HEMT-based designs from component to board development level

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**Abstract**—This paper presents a study on a few main challenges in GaN-based designs from component to board development level. Transistors in parallel in a switch are more critical in designing power cells due to the high sensitivity to parasitic components in both power and gate control circuits. Further, the changes in switching behaviour on the discrepancies in device parameters are yet to be realized. In this study, both experimental and simulation based approaches are used for the verification of parasitic effects. The large signal modeling with LTSpice simulation is used for the prediction of effect due to parametric variation of devices in parallel.

**Index Terms**—GaN HEMTs, paralleling, parasitic components, device characteristics, high speed switching

## I. INTRODUCTION

The wideband-gap semiconductors such as GaN and SiC are capable of applying in high switching frequencies (over 200kHz) which can improve the power density and efficiency of converters. However, high frequencies increase vulnerability to parasitic elements in both the power and gate control circuits. Due to those frequency dependent parasitics, high current and voltage spikes can be generated during switching transitions.

GaN power transistors have (i) the rigorously limited gate voltage ranges (very low safe margins) with high electron mobility, and (ii) low threshold voltages that highly sensitive to fast voltage/current transients which cause spurious turn-on. Further, the switching transient spikes can permanently damage the sensitive gate structure. Further, the switching behaviour of many GaN devices in parallel can be effect by the variations in device parameters. However, this phenomenon has not been investigated extensively.

In this study, those issues of the GaN HEMTs in parallel will be investigated. The results can be used to establish more appropriate strategies for driving the GaN transistors to ensure the safety and robustness of the devices.

## II. COMPONENT LEVEL ISSUES

Most GaN HEMT manufacturers are yet to confirm the reliability of their products to implement confidently in commercial applications. Thorough parametric tests and circuit evaluation are required to guarantee the device reliability.

A theoretical analysis has been conducted to investigate the effect on the current distribution through two parallel GaN transistors due to the variation in device parameters. The commercially available GaN devices (GS66508T from GaN Systems Inc.) have been considered for the analysis.

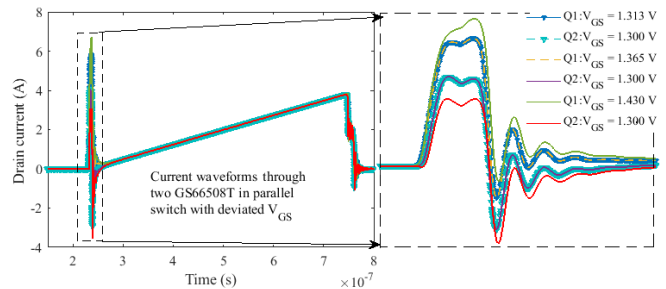


Fig. 1. A comparison of current through two parallel GaN HEMTs devices in a switch.

Fig. 1 shows the effect on threshold voltage variation in two parallel devices (i.e. Q1 and Q2). As depicted in Fig. 1, the change in the peak current due to the change in threshold voltage is approximately 28 A/V for GS66508T transistors in parallel. More details about different parasitic elements will be presented in the full paper.

## III. BOARD LEVEL ISSUES

PCB parasitic components in GaN HEMTs in parallel and their effect in current and voltages have been explained in detail in [1]. In this study, these parasitic effects are studied in single layer boards with different transistor layouts.

The ideal method to evaluate the current distribution among transistors in parallel is to monitor the current in each device. These current waveforms have very high frequency harmonics (hundred of megahertz) which requires appropriate current sensors. For current measurements, a wide bandwidth, fast responding sensors are required [3,4]. From the bandwidth perspective, current sensing shunt resistors (current viewing resistors—CVR) and magnetoresistive (MR) sensors found to be the potential solutions. Compared to MR, the shunt-based resistors have extremely flat frequency response from DC to 2 GHz. In [2], a study on CVR based drain current measurements for fast switching GaN HEMTs is presented. As seen in Fig. 3, CVR introduce considerably oscillations during the on-transients [3].

## IV. EXPERIMENTAL VERIFICATION

The main objective of this task is to investigate current distribution of four GaN HEMTs in parallel in two different layouts. Moreover, the consequences of adding CVRs in the power path are to be identified. For the basic experimental

prototype, a high frequency power cell (i.e. a half-bridge converter) was designed as the schematic illustrated in Fig. 2. The device under test (i.e. four GaN HEMTs in parallel) constituted the low-side switch.

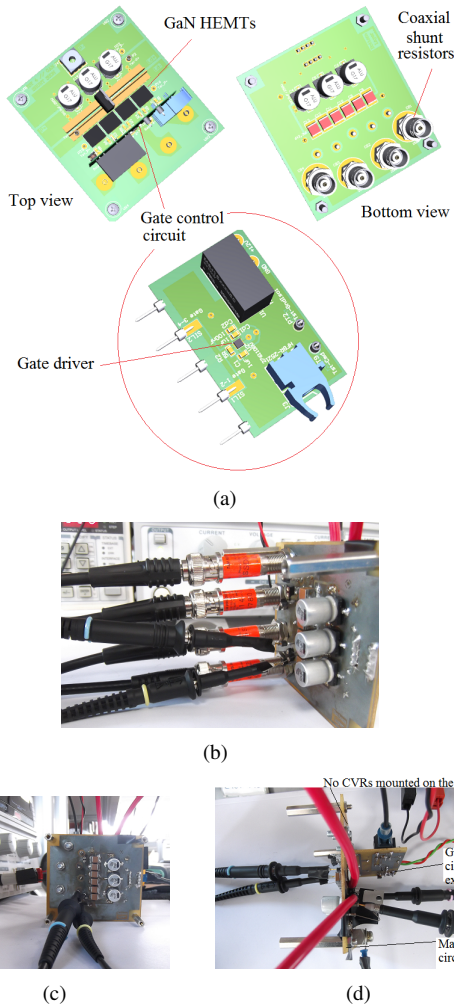


Fig. 2. Four GaN HEMTs in line laid configuration: (a) the design, (b) and (c) top side and bottom views of the PCB, (d) CVR mounted circuit.

Current through each GaN HEMT is measured using stud-type, high bandwidth, coaxial shunt current sensors. Thermal images are used to evaluate the power dissipation balance between the four HEMTs and to correlate them with the current measurements. The same circuit is further investigated by removing the current sensors. A second circuit is built by eliminating the CVRs as to achieve low parasitics. The circuit is tested up to 27 A/80 V. Here, only the voltage measurements and thermal images are obtained. Thermal images are used to evaluate the power dissipation between the four HEMTs and to correlate them with the current measurements.

Circuit simulation is another approach to predict the current waveforms, providing that the simulation is reliable and the circuit model is accurate. By implementing a fairly precise simulation model, the effect of adding CVR in the power path is observed. More details will be presented in the full paper.

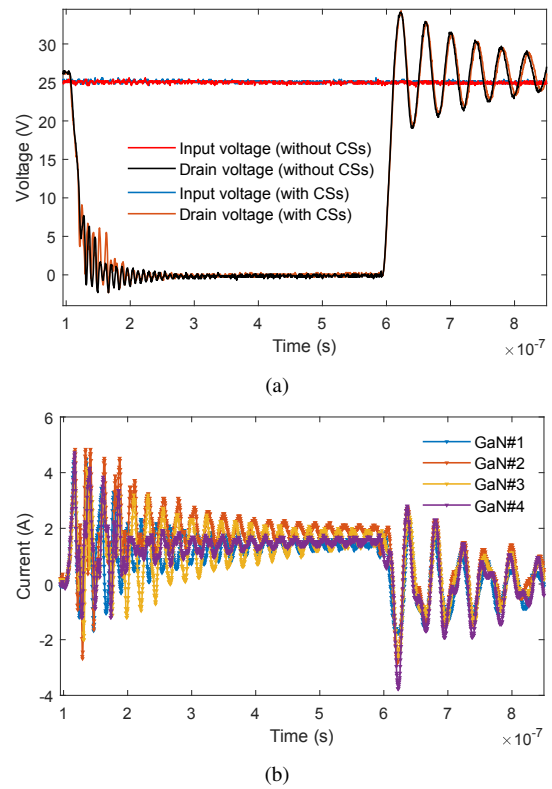


Fig. 3. A comparison of results with and without connecting CVRs: (a) drain and input voltages, (b) Coaxial shunt based current measurements.

## V. CONCLUSION

A fairly equal current distribution is observed among the components in both circuits during the switching operations, resulting in a stable thermal equilibrium. As per the results, more clean and reliable measurements can be obtained by optimizing the PCB design (to reduce the copper-track related parasitic components) and eliminating inline sensors that add more parasitics to the circuit. Despite an optimized circuit design, the discrepancies in threshold voltages of parallel GaN HEMTs can lead to unbalanced current sharing among devices during switching transients.

## VI. ACKNOWLEDGMENT

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