Technical Design Report for the ATLAS inner Tracker pixel detector

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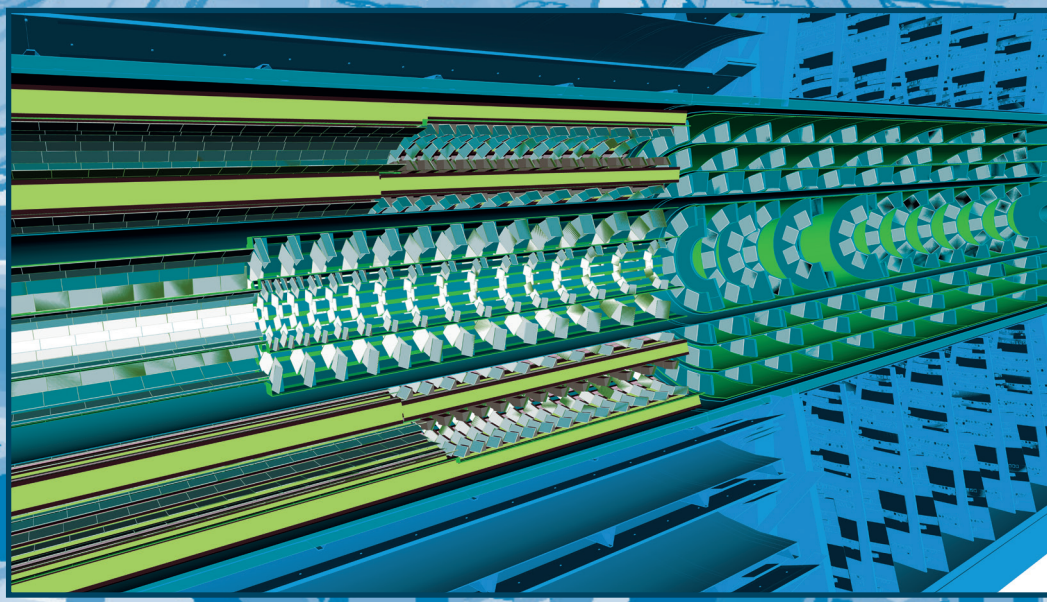
ATL-TDR-030 · LHCC-2017-021

ATLAS

Inner Tracker Pixel Detector



Technical Design Report

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Reference: CERN-LHCC-2017-021
ATLAS-TDR-030
Created: 15th June 2018
Prepared by: The ATLAS Collaboration

Abstract
This is the second of two Technical Design Report documents that describe the upgrade of the central tracking system for the ATLAS experiment for the operation at the High Luminosity LHC (HL-LHC) starting in the middle of 2026. At that time the LHC will have been upgraded to reach a peak instantaneous luminosity of 7.5×10^{34} cm^{-2}s^{-1}, which corresponds to an average of about 200 inelastic proton-proton collisions per beam-crossing. The new Inner Tracker (ITk) will be operational for more than ten years, during which time ATLAS aims to accumulate a total data set of 4000 fb^{-1}. Many of the features of the tracker have already been presented in the first Technical Design Report that detailed the construction of the ITk Strip Tracker. That report was published in April 2017. This document focuses on the ITk Pixel Detector. A baseline design is described in detail, and the motivations for the chosen technologies are illustrated. In some cases, alternative solutions are also illustrated. In this case, we indicate the advantage in pursuing the other designs, and describe the time line for a decision. The design, construction and expected performance are set out in detail. When considering performance we pay particular attention to those parameters that are determined by the performance of the Pixel Detector. We describe in detail the design and construction of the Pixel Detector, including the results of measurements of prototype modules and associated support structures and we explain the status of the plans for their mass production. We present details of the decommissioning of the existing tracking detector and the replacement of the inner layers of the ITk Pixel Detector part way through the lifetime of the High Luminosity LHC. Finally, we describe: the costing and schedule, including major milestones, to construct the detector.

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1 Introduction

This is the second of two Technical Design Reports that describe the upgrade of the central tracking system for the ATLAS experiment (Inner Tracker, ITk) as part of the preparation for the operation at the High Luminosity Large Hadron Collider (HL-LHC) that will start in the middle of 2026. In the first report, published in April 2017, the design, development and plans for the production of the ITk Strip Detector were presented [1]. In this document, the design, development, results of measurements on prototypes and plans for the production of the ITk Pixel Detector are presented, together with updates of the design of the common ITk mechanics and electronics systems.

Meeting all of the requirements of a charged particle tracking detector close to the beam-line at the HL-LHC presents a unique challenge for the design of an all-silicon system that consists of a Pixel Detector at small radius and a large area Strip Detector surrounding it. The design of the ITk benefits from the enormous amount of experience gained over more than two decades in the construction and operation of the existing inner tracking detector that has been highly successful for the exploitation of LHC physics up to and well beyond its original design requirements. This is particularly true of the existing Pixel system that was upgraded in 2015 during the first Long Shutdown (LS1) of the LHC with the insertion of an additional pixel layer within 3.4 cm of the beam line. This so called Insertable b-Layer (IBL) uses a combination of sensor technologies, including high-resistivity, planar and 3D, silicon detectors [2, 3]. These technologies are also proposed for the ITk Pixel Detector.

The design of the ITk Pixel Detector proposed in this document is based on the highly successful concept of "Hybrid Pixel Detector" developed for and implemented in the present ATLAS Pixel Detector [4] and in the IBL. However, it is clear that the very particular requirements imposed for a Pixel Detector operating at HL-LHC demand the development and implementation of new technical solutions. The HL-LHC will operate at an instantaneous luminosity up to $\mathcal{L} = 7.5 \times 10^{34}$ cm^{-2}s^{-1} which corresponds to an average of approximately 200 inelastic proton-proton collisions per beam crossing. The ITk will have to operate over the entire LHC Phase II program, delivering an integrated luminosity of 4000 fb^{-1}. In order to cope with these requirements, and to maintain the same tracking performance as the present ATLAS Inner Detector, the layout of the ITk required a careful optimization that is described in detail in Chapters 2 and 3. Also the implementation of the Hybrid Pixel Detector concept required several adaptations and in some case the use of novel technologies to adapt to the HL-LHC conditions. The most significant improvements and novel solutions are summarized in Chapter 4 and analysed in detail in Chapters 5 to 18. Most of the technical decisions have been made. For those cases where options are unresolved, the

relative merits of the different solutions are discussed and the decision making process and timeline for the decision are presented.

In designing the ITk, the aim has been to be able to reuse many of the existing services that are in place for the current Inner Detector. Many of the existing high and low voltage cables can be re-used over most of their length between the side-caverns and patch panels close to the detector. It will also be possible to reuse the cable cooling plant and the dry gas system which provides dry gas to the existing Inner Detector. The design of the services was illustrated in the Strip TDR and in this document only updates are given in Chapter 14.

The ITk will be installed as a single monolithic unit into the centre of ATLAS. Particular care has been taken to reduce the time on the beam line and rapid connection techniques are being prototyped so that the detector can be ready for operation a few months after installation. The safe decommissioning and disposal of the existing tracking detector and the plans for the insertion and connection of the ITk have been have been presented in the Strip TDR and will be updated here.

As well as the numerous technical challenges, the construction of a Pixel Detector of the scale that is proposed demands a new approach to the organization of the bulk component production. The active surface of the new tracker is more than 10 times larger than in the existing silicon Inner Detector and it will be constructed over just three years.

The infrastructure for tracking the production of parts of sufficiently high quality, on time and to agreed costs will require significant development and more oversight than was used in the past. A comprehensive set of quality assurance and quality control procedures will have to be developed and included from the beginning in the production plan. Particular attention will be devoted to the monitoring of the rate and quality of the module production.

The various aspects of the project management, in particular the details of the production model and the production schedule are outlined in Chapter 19. The management and internal organisation of the ITk, including its interaction with the rest of the experiment were discussed in the Strip TDR (Chapter 23) and will not be repeated here. Chapter 20 covers an analysis of the preliminary cost estimate of the Pixel Detector and of the ITk Common Electronics and Common Mechanics work packages. The assumptions that form the construction plan and the mitigation strategies that will aid successful delivery are captured in the Risk Management Plan and Risk Register (see Chapter 21).

2 The Pixel Detector Layout and Simulation

The layout presented in this chapter is the baseline for the ITk Pixel Detector and is used as a reference throughout the rest of the document. The layout is an evolution of the concepts developed in the ITk Strip Technical Design Report [1] and follows the same guiding principles of an extended barrel stave with inclined sensors in the forward region of pseudorapidity[1]. It represents a major step towards a fully engineered detector design, taking into account the engineering constraints and benefiting from recent developments in pixel module design to achieve optimal detector performance for a fully efficient tracker covering $|\eta| < 4$, and simultaneously achieving all other performance goals as outlined in the Strip TDR. In the second part of this chapter the Geant4 simulation [5] of the ATLAS ITk is presented. The description of the Pixel Detector has been improved and, compared to the ITk Strip TDR, takes into account more of the engineering detail. In particular, the simulation results presented in this document are based on a more detailed description of the detector including stave supports and services. This allows for an improved description of the Pixel Detector material and a better understanding of how the material affects the tracking performance. Radiation dose and fluence results are also presented, using an equivalent ITk simulation model implemented in the FLUKA [6] framework.

2.1 Description of the ITk Layout

The layout presented in this chapter is based on one of the candidate layouts described in the Strip TDR called "Inclined Layout". This layout is shown in Figure 2.1 taken from Reference [1]. The Inclined Layout represents a significant evolution compared to the layouts discussed in the ATLAS Phase-II Upgrade Letter of Intent [7] and in the Phase-II Upgrade Scoping document [8]. Like the reference detector layout from the Phase-II Upgrade Scoping document, the detector design presented in the Strip TDR combines precision central tracking in the presence of an average of 200 pile-up events with the ability to extend the tracking coverage to a pseudorapidity of 4 while maintaining excellent tracking efficiency and performance. The ITk comprises two subsystems: a Strip Detector surrounding a Pixel Detector. The Strip Detector has four barrel layers and six end-cap petal-design

[1] ATLAS uses a right-handed coordinate system with its origin at the nominal interaction point (IP) in the centre of the detector and the z-axis along the beam pipe. The x-axis points from the IP to the centre of the LHC ring, and the y-axis points upward. Cylindrical coordinates (r, ϕ) are used in the transverse plane, ϕ being the azimuthal angle around the z-axis. The pseudorapidity is defined in terms of the polar angle θ as $\eta = -\ln\tan(\theta/2)$.

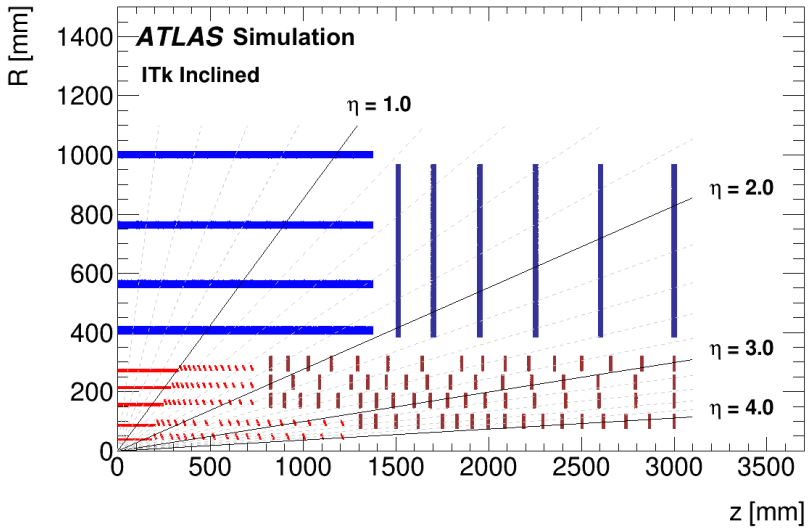


Figure 2.1: Schematic layout of the ITk for the HL-LHC phase of ATLAS as presented in the Strip TDR [1]. The active elements of the barrel and end-cap Strip Detector are shown in blue, for the Pixel Detector the sensors are shown in red for the barrel layers and in dark red for the end-cap rings. Here only one quadrant and only active detector elements are shown. The horizontal axis is the axis along the beam line with zero being the interaction point. The vertical axis is the radius measured from the interaction region. The outer radius is set by the inner radius of the barrel cryostat that houses the solenoid and the electromagnetic calorimeter.

disks, both having double modules each with a small stereo angle to add $z(R)$ resolution in the barrel(end-caps), respectively. The Strip Detector, covering $|\eta| < 2.7$, is complemented by a 5 layer Pixel Detector extending the coverage to $|\eta| < 4$. The Pixel and Strip Detector volumes are separated by a Pixel Support Tube (PST). In addition, and because of the harsh radiation environment expected for the HL-LHC, the inner two layers of the Pixel Detector are replaceable. The inner two pixel layers are separated from the outer three layers by an Inner Support Tube (IST), that facilitates a replacement of the inner layers. The combined Strip plus Pixel Detectors provide a total of 13 hits for $|\eta| < 2.7$, with the exception of the barrel/end-cap transition of the Strip Detector, where the hit count is 11 hits. The Pixel Detector presented in the Strip TDR [1] was designed to supply a minimum of at least 13 hits from the end of the strip coverage in pseudorapidity to $|\eta|$ of 4. While the Strip Detector remains unchanged and is described in detail in Reference [1], the Pixel Detector layout has evolved to further improve the performance, reduce cost and incorporate engineering constraints. In the following, an overview is given on the methods used to optimise the detector layout, starting from the original Letter of Intent and Scoping Document studies, followed by a detailed description of the optimisations and changes to the Pixel Detector design since the Strip TDR.

2.1.1 Methods used to optimised the ITk Detector Layout

Designing a tracking detector for the Phase-II upgrade of the ATLAS experiment is a challenging task. The detector will have to cope with the Phase-II operational conditions with an average of up to 200 pile-up events, the corresponding data rates and an unprecedented radiation environment. At the same time the ITk Detector will have to provide the required tracking performance to enable the physics programme as outlined in the ATLAS Phase-II Upgrade Letter of Intent [7]. The development of the ITk Detector layout is carried with the following set of goals:

- Design a tracking detector that provides the required tracking performance to the ATLAS Phase-II physics programme, in events with an average pile-up of up to 200 simultaneous interactions.
- The detector should provide robust tracking in presence of detector defects, like sensor inefficiencies due to expected radiation effects, as well as dead modules due to eventual component failures.
- Aim to minimise cost by reducing as much as possible the total silicon surface necessary to achieve the required hit coverage and by choosing less complex solutions whenever possible.
- At the same time, try to choose layout options that allow to minimise the CPU time needed for reconstruction, which is one of the cost drivers for the computing budget for the ATLAS Phase-II programme.

An iterative design approached is followed for the layout optimisation. A design tool called "idres" [9] is used to optimise the position of pixel and strip sensors in radius and z-position along the beam direction. The tool allows to very quickly compute the hit coverage for a given layout as a function of η. It uses a 2-dimensional magnetic field map of the ATLAS solenoid, a simplified 2-dimensional model of the passive detector material and the individual precision of the pixel and strip sensors to estimate the track parameter resolutions as a function of η and transverse momentum. For candidate layouts a Geant4 [5] geometry model is implemented to allow in depths simulation and reconstruction studies of the hermeticity, tracking performance and CPU requirements to reconstruct events. The basis of the Geant4 models are engineering drawings of the detector components to ensure that realistic assumptions are used in the layout design work.

The design of the ITk layout benefits from the experience gained in controlling Run-1 and Run-2 levels of pile-up in the current ATLAS track reconstruction. Effective cuts to reduce the level of fake tracks and to reduce the CPU needed to reconstruct high pile-up events are either an increased requirement on number of hits and cut harder on holes (sensors crossed by the track without a hit found). Figure 2.2 from the ATLAS Phase-II Upgrade Letter of Intent [7] the ratio of the number of reconstructed to generated tracks for $t\bar{t}$ events, as a function of pile-up. Requiring 9 hits and not more than 1 hole in the Pixel Detector

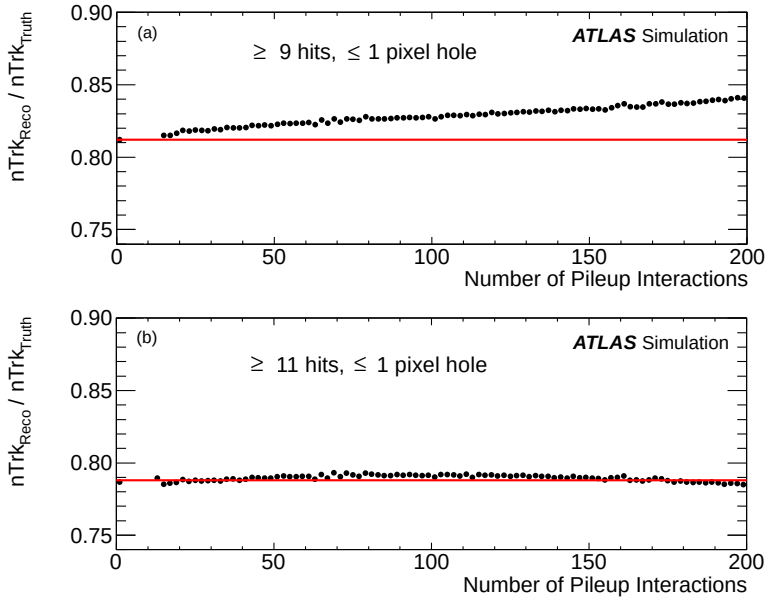


Figure 2.2: Ratio of reconstructed to generated tracks for $t\bar{t}$ events at various levels of pile-up. Two different track selections are studied: requiring track reconstruction with at least 9 hits per track (a), and with at least 11 hits per track (b). The plot is taken from Reference [7].

results in significant fake component at Phase-II pile-up levels, while requiring 11 hits instead is removing this additional component. For a minimal hit requirement of 11 hits one needs to allow for at least one additional layer, since the individual sensors will have a finite inefficiency. In order to ensure robustness against detector defects, ATLAS requires a redundancy of at least 2 additional hits. The resulting hit requirement of at least 14 hits for the ITk is used for the layouts presented in the ATLAS Phase-II Upgrade Letter of Intent [7] and Phase-II Upgrade Scoping document [8], which has 4 pixel layers and 5 double layers of Strip Detectors with a small stereo angle.

The ITk layouts studies in preparation for the Strip TDR aimed at improving on the Phase-II Upgrade Scoping document layout, for a detector that covers the extended η range of 4. Studies with full ITk granularity pixel and strip sensors implemented in Geant4 indicated that a reduced hit requirement of 12-13 hits is sufficient to control fakes and to ensure robust tracking. This resulted in an opportunity to replace a double strip layer with an additional pixel layer in the barrel region, which reduces the total strip sensor surface needed and improves the tracking performance in the core of high-p_{T} jets and for τ 3-prong topologies, because of the better double-track resolution of high-granularity pixel sensors. In addition, the barrel part of the Strip Detector was extended in length, which allowed to reduce the number of strip disks from 7 to 6 and to drop the barrel strip stub-layer.

The Pixel Detector layouts studied for the Strip TDR are based novel ideas for the local

stave support structures[2], compared to previous generations of experiments. One is the inclined barrel stave design, where the flat barrel stave is prolonged with a section with inclined modules. This allows the end-of-stave material to be shifted further out in z and hence minimises the material-induced performance degeneration in the barrel to end-cap transition of a classical pixel design. In addition, this concept minimises the amount of silicon needed as inclined modules have a larger angular coverage in this region. The second novel concept is the end-cap ring system, where layers of pixel rings extend the coverage in z and allow routing of the service separately along each ring layer. As is the case for the inclined module sections, each ring can be individually placed to optimise the coverage. Doubling the number of pixel rings in the layer allows additional hits to be added where needed to keep the hit counts stable as a function of η. In particular the inclined stave design for the inner barrel layers is the key to achieve good tracking performance with an extended coverage to η of 4. It allows for 2 or more hits in layer 0 in the inclined section close to the interaction point. This adds redundancy in the number of hits for good pattern recognition performance. Furthermore, having the first hit close to the beam pipe in radius improves the impact parameter and vertex resolution.

The result of this layout design process is the Inclined Layout shown in Figure 2.1, as presented in the Strip TDR [1]. This layout required 15% less silicon for the Strip Detector and featured a 5 layer Pixel Detector designed with the same total silicon surface as required for the 4 pixel layer layout presented in the Phase-II Upgrade Scoping document.

2.1.2 Description of the Inclined Duals Layout

The Pixel Detector design presented in this document is based on the Strip TDR layout, the new layout is referred to as the "Inclined Duals" layout. The same design ideas of barrel stave with sections of inclined modules and end-cap ring systems are used. The following design optimisations for the Pixel Detector were implemented to further improve the detector performance and to reduce costs as well as complexity:

- The hit requirement for $|\eta| > 2.7$ was reduced from 13 pixel hits to 9.
- The active size of the pixel read-out chip was increased to 19.2 mm $\times$ 20 mm, which is turn leads to larger sensors when combining them into modules with 2 (*duals*) and 4 (*quads*) read-out chips. This required a reduction in the number of module rows per layer at given radii and the number of modules on the end-cap rings.
- The inner envelope for the IST was decreased to a radius 145 mm, requiring changes in the radii of the inner and outer end-cap systems, as well as the barrel layer radii, in order to avoid hermeticity holes in the barrel/end-cap transition region.

[2] The detailed description of the barrel longeron structures and its rows of flat and inclined modules, the end-cap ring design, etc., can be found in Section 4.7.

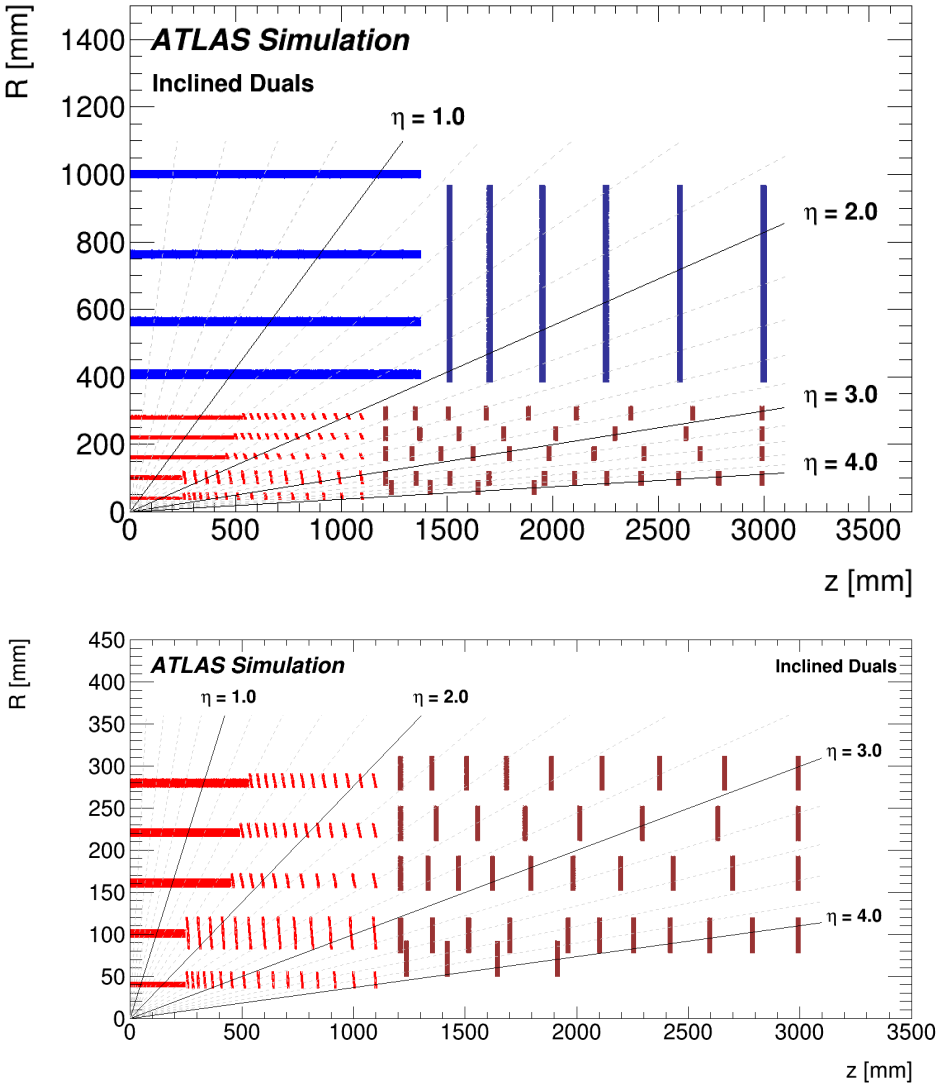


Figure 2.3: **Top**: A schematic layout of the ITk Inclined Duals layout for the HL-LHC phase with the pixel layout as presented in this document. **Bottom**: A zoom into the Pixel Detector. In each case, only one quadrant and only active detector elements are shown for both diagrams. The active elements of the barrel and end-cap Strip Detector are shown in blue, for the Pixel Detector the sensors are shown in red for the barrel layers and in dark red for the end-cap rings. The horizontal axis is along the beam line with zero being the interaction point. The vertical axis is the radius measured from the interaction region.

- For the inner barrel Pixel Detector the longeron solution, which coupled layers 0 and 1, was dropped in favour of a dual shell structure. As a result the mechanical stability is improved and 2 module rows could be added to barrel layer 1 to increase the radius of flat section to better space out the inner two layers in radius.
- The inner radius of the inclined modules in barrel layer 0 was decreased from 39 to 36 mm to improve the hermeticity in the barrel flat/inclined transition region. In addition, this change allows for the shortening of the barrel section in z to 110 cm while still covering the full η range.
- An important improvement in the layout presented in this document is the simplified geometrical solution to keep the number of hits stable as a function of η. In particular, using inclined quad modules in barrel layer 1 allows more hits to be added in this region, significantly simplifying the design of the outer end-caps and barrel layer 2 and reducing the total pixel surface needed.
- For the baseline layout the inclination angle in barrel layers 0 and 1 was changed to 75 degrees, reducing the material crossed by particles and increasing the angular coverage of the inclined modules in this region.
- A further inner ring layer was added to the inner pixel end-cap system to improve the coverage close to $|\eta|$ of 4 and to reduce the extrapolation distance between the end of the barrel and the first hit in the end-caps.
- The length of the outer barrel inclined section has been extended to $z = 110$ cm in order not to line up in η the barrel/end-cap transitions regions of the Pixel and Strip Detectors. This avoids any buildup of pattern recognition problems in this very complicated geometrical region.
- The length of the flat sections in the outer layers 2–4 is chosen so as to avoid the lining up of the flat/inclined transitions in η and to extend the coverage of the flat (quad) modules before the tilted modules take over, such that one minimises the total number of modules on the staves.
- In the outer barrel layers the flat section has been increased in radius by 5 mm w.r.t. the inclined sections to increase the lever arm in the central Pixel Detector and to reduce the complexity of engineering the flat/inclined transition on the stave, in particular the bending of the cooling pipes.
- The end-cap ring system is now correctly modelled as 2 half shells with half rings staggered by 10 mm in z between their centres, leading to a maximum distance of 16 mm between adjacent modules in ϕ in the overlap region.

After these changes the exact layer radii and sensor positions have been re-optimised to ensure full hermeticity for particles originating from a luminous region extending up to ± 15 cm in z. The resulting layout is shown in Figure 2.3, with both the overall layout of the ITk and the zoom into the pixel system.

Table 2.1: Main layout parameters for the pixel flat barrel. The number of sensors per row refers to a half-row ($z > 0$ mm) in the central, flat part of the barrel where sensors are placed parallel to the beam line. The number of hits indicates how many hits are expected in the layer for particles originating from $z = 15$ cm. The total length in z of the inner and outer barrel sections (flat and inclined) is 110 cm.

Barrel Layer	Radius [mm]	Rows of Sensors	Sensors per Row	Type	Hits
0	39	16	6	duals	1
1	99	20	6	quads	1
2	160	30	11	quads	1
3	220	40	12	quads	1
4	279	50	13	quads	1

Table 2.2: Main layout parameters for the pixel inclined section. The number of rows of sensors is the same per-layer as in Table 2.1. The radii of the inclined sections refer to the innermost point of the sensors. The number of hits indicates how many hits are expected in the layer for particles originating from $z = 15$ cm. The total length in z of the inner and outer barrel sections (flat and inclined) is 110 cm.

Barrel Layer	Radius [mm]	Sensors per Row	Type	Hits	Angle [deg]
0	36	16	singles	2–3	75
1	80	13	quads	2–3	75
2	155	11	duals	1	56
3	215	13	duals	1	56
4	274	13	duals	1	56

Table 2.3: Main layout parameters for the pixel end-caps. The radii refer to the innermost point of the sensors on a ring. The number of hits indicates how many hits are expected in the layer for particles originating from $z = 15$ cm.

End-cap Layer	Radius [mm]	Rings	Sensors per Ring	Type	Hits
0	50	4	16	quads	3
1	78	11	22	quads	3–4
2	152	10	32	quads	2
3	211	8	44	quads	1
4	271	9	52	quads	1

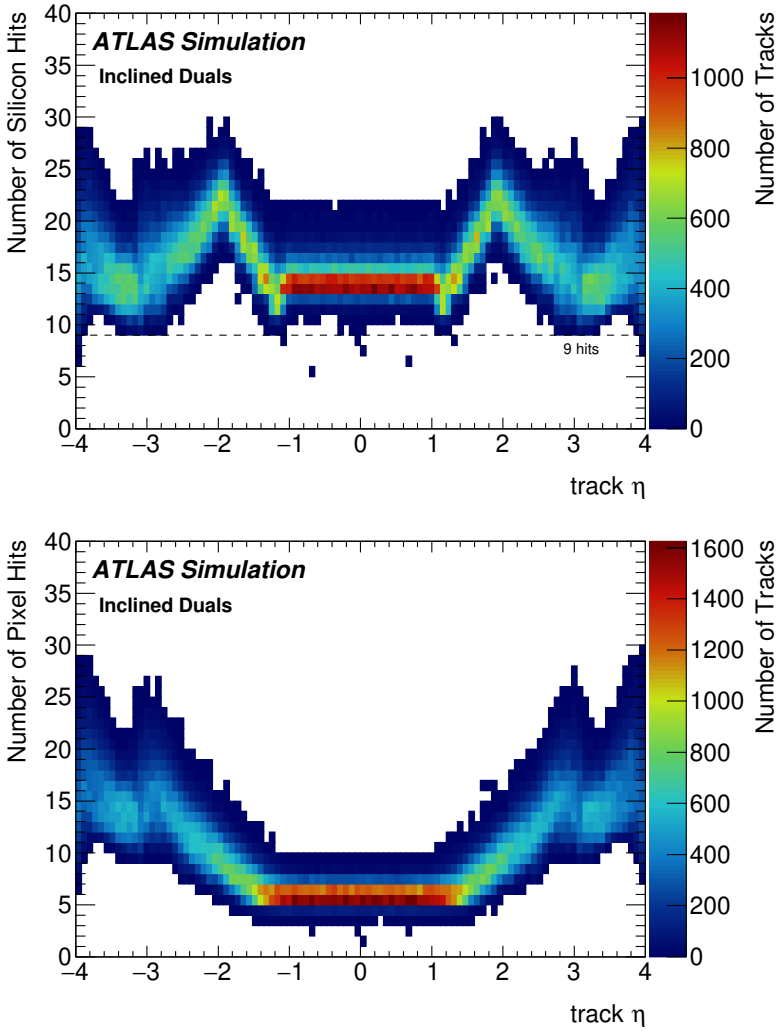


Figure 2.4: **Top**: The total number of strip plus pixel measurements (hits) on track as a function of η. **Bottom**: Number of pixel measurements (hits) on track as a function of η. For this figure a sample of single muon events with $p_{\mathrm{T}} = 1$ GeV is used. The muons are produced with a flat distribution between -15 to 15 cm in z and between 0 to 2 cm in R, respectively.

Table 2.4: Summary of the pixel surface needed for the different parts of the detector. The results of the Inclined Duals layout are compared to the corresponding numbers for the layout presented in the Strip TDR [1].

Detector Part	Layout	
	Inclined Layout [m^2]	Inclined Duals [m^2]
Inner Barrel Flat	0.35	0.52
Inner Barrel Inclined	0.82	1.00
Inner Barrel Total	1.17	1.51
End-cap Inner Rings	1.10	0.94
Outer Barrel Flat	2.51	4.49
Outer Barrel Inclined	2.75	2.30
Outer Barrel Total	5.26	6.79
End-cap Outer Rings	6.48	3.50
Barrel Total	**6.43**	**8.30**
End-cap Rings Total	**7.58**	**4.44**
Total	**14.01**	**12.74**

Tables 2.1, 2.2 and 2.3 detail the main design parameters of the Inclined Duals layout. Three types of sensor are used: single read-out chip modules of 19.2×20 mm^2 in size in the inclined section of barrel layer 0, dual modules with two read-out chips for the flat section of barrel layer 0 and the inclined section in barrel layers 2 to 4, and quad modules with four read-out chips for the remaining parts of the detector. The number of hits in each layer and each part of the detector refers to straight trajectories originating from $z = 15$ cm, which is the hermeticity requirement used to design the layout. Figure 2.4 shows the total number of pixel plus strip measurements on track, demonstrating that the number of hits is above 9 at all η except very close to $|\eta|$ of 4. Also shown is the number of pixel measurements as a function of η. The number of hits on average exceeds the minimum requirement due to primary vertex z spread and the sensor overlaps. Table 2.4 summarises the total silicon surface needed for the different parts of the detector. In total the pixel surface is reduced from 14.01 m^2 in the Inclined Layout [1] to 12.55 m^2 in the Inclined Duals layout, mainly because of the reduced hit requirement for $|\eta| > 2.7$.

2.2 Simulation of the ITk Detector

Like the pixel layout, the simulation description of the detector design has significantly evolved since the Strip TDR. In this section the details of the simulation implementation of the pixel layout are described, in particular focussing on the improvements. The full simulation of the ITk layouts under consideration is performed using a software release dedicated to the ATLAS Upgrade program. The production of simulated samples follows the same steps as regular ATLAS simulation based on the Run 2 offline software chain:

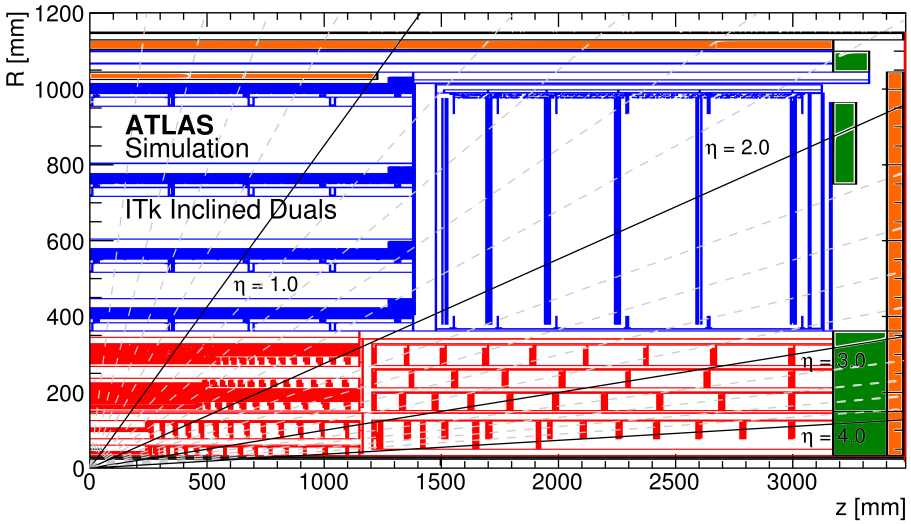


Figure 2.5: Location of the materials for one quadrant of the Inclined Duals layout. Shown is the Pixel Detector surrounded by the Strip Detector. The Patch-Panel 1 regions (green) and the moderators (orange) in front of the barrel solenoid and the end-cap calorimeters are also shown.

event generation, detector simulation using Geant4 [5], digitisation of simulated energy deposits into the actual detector read-out data format, and event reconstruction starting from the digitised data. This offline software chain has been adapted for the upgrade ITk Detector, including a dedicated tuning of the track reconstruction software.

The distribution of material within the detector volume has a large impact on the tracking performance, electron and photon measurements, and the fluence levels and total ionising radiation doses. Particular care was taken to describe the material with an improved level of detail compared to Reference [1]. The dimensions, location and material of all detector elements were implemented in the simulation framework based on the technical design of the detector as discussed in the following chapters. In Figure 2.5 the location of the materials is shown for one quadrant of the ITk Detector volume. Most materials in the volume are defined in terms of their chemical compound (or mixture of chemicals) and density. For the different components the relevant physical design was detailed by the ITk pixel mechanics groups and the most recent engineering estimates available at the time have been used to build the simulation model.

The Strip and Pixel Detectors are separated by the Pixel Support Tube (PST), which is modelled as a 20.75 mm thick cylinder, with carbon fibre as material and with an inner radius of 341 mm. The inner two layers of the Pixel Detector are separated from the outer pixel layers by the Inner Support Tube (IST), which is modelled as a 0.455 mm thick carbon fibre cylinder with an inner radius of 145 mm.

The Pixel Patch-Panel 1 (PP1) (see Section 4.5 and Figure 2.5) is modelled as a solid, homo-

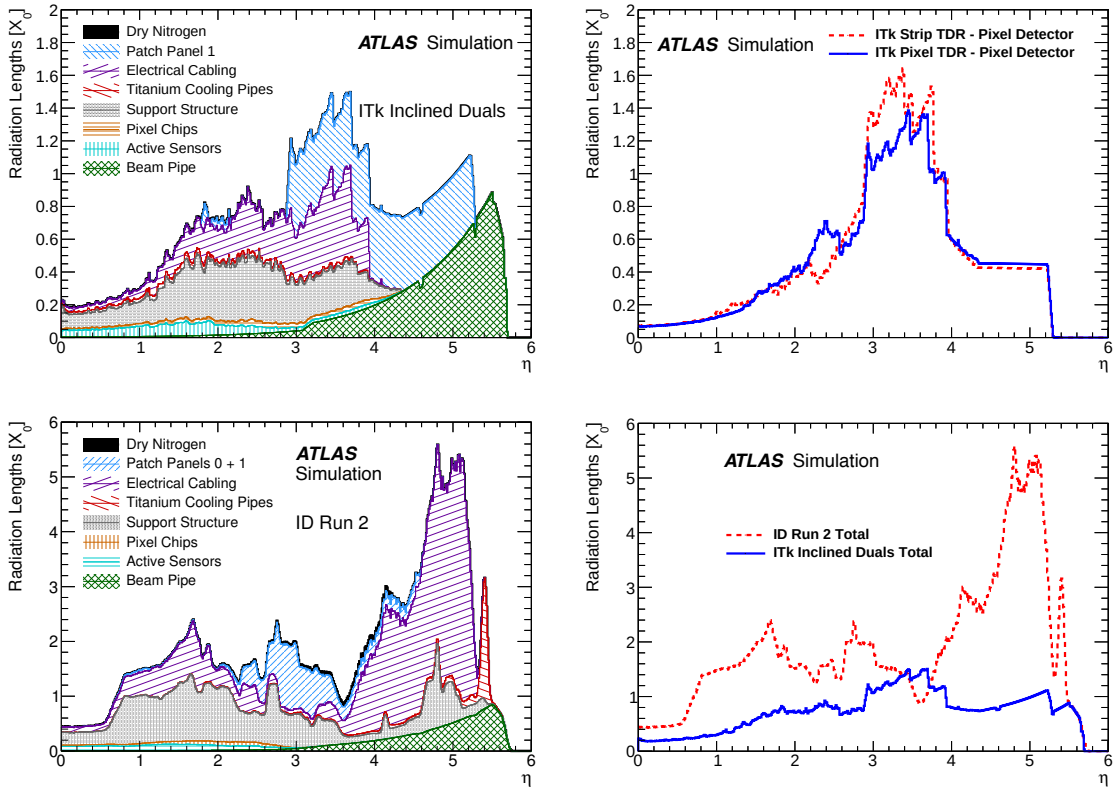


Figure 2.6: **Top**: Radiation length X_0 versus the pseudorapidity η (left) and a comparison of the Pixel Detector from the Inclined Duals layout presented in this TDR with the layout presented in the Strip TDR (right). The figures only show positive η; negative η is expected to look the same. **Bottom**: The radiation length X_0 versus η for the current ATLAS Inner Detector (left) and a comparison of the ITk and the current ATLAS Inner Detector (right).

geneous 40 kg cylinder at each end of the ITk Pixel Detector. The PP1 for the Strip Detector is modelled as 20 kg for each barrel end, and each end-cap end (two separate annuli at each end), filled with the same generic material as used for end-cap substructures. The mass and the materials to model the PP1 region are chosen conservatively, based on engineering estimates. The poly-moderator is modelled as a cylinder along the outer part of the cryostat bore, 25 mm thick. A second piece, 20 mm thick, is modelled inside the outer support cylinder, slightly shorter than the Strip barrel staves. Poly-moderator disks with thickness 70 mm are placed in front of the forward calorimeter volume. The current Run 2 beam pipe will be retained for the Phase-II detector. Thus for ITk simulations considered in this document, existing Run 2 beam-pipe simulation models were used. This beam-pipe is 28.3 mm in radius, and 0.0038 X_0 in radiation lengths, at $z = 0$ mm.

A summary of the material distribution of X_0 versus η is shown in Figure 2.6 for the Inclined Duals layout, based on the detailed modelling of the Pixel and Strip Detectors as described below. Shown as well is a comparison of the Pixel Detector for the Inclined Duals

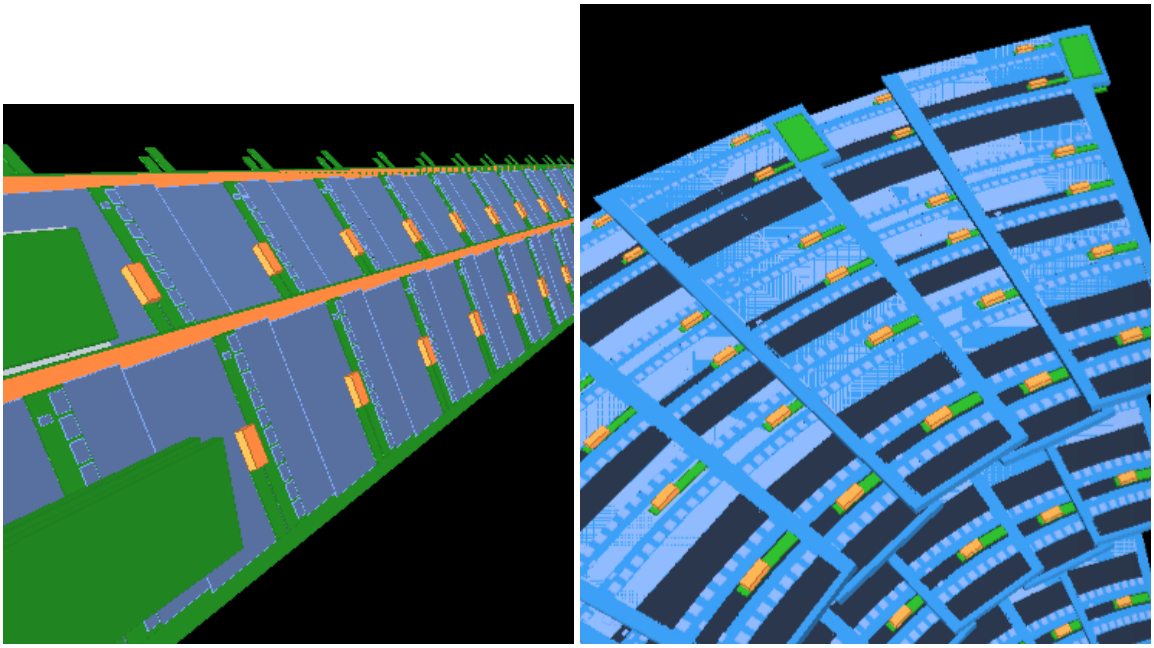


Figure 2.7: Geometry displays of the Geant4 model of (**left**) the strip barrel staves and (**right**) end-cap petals, illustrating the level of detail of the modelling.

layout and the layout as presented in the Strip TDR. The description of the Inclined Duals layout uses a much improved geometry model, which is better accounting for the different detector materials. The reduction in the forward is a consequence of the layout improvements described about. For comparison the same radiation length distribution is shown for the current ATLAS Inner Detector. As for the Inclined Duals layout, the contribution of the moderator in front of the calorimeters is not shown. Comparing the ITk to the current ID, the material of the new detector will be significantly less for nearly all η.

2.2.1 Description of the Strip Detector in Geant4

The Strip Detector is simulated as described in the Strip TDR [1]. The strip barrel detector is described with individual parts modelled separately. Masses and material compositions reflect the mechanical designs. The strip end-caps are modelled in detail as well, but with some materials merged: some materials/objects that sit next to each other are not individually described, but instead one homogeneous block is modelled, and is adjusted to have the correct radiation length as calculated from the engineering designs. Figure 2.7 shows examples of geometry displays of the Geant4 model of the Strip Detector. Shown are displays for strip barrel staves and end-cap petals, illustrating the different level of detail in the modelling.

For the Strip Detector global supports, both barrel and end-cap are described in detail. The stave components including cooling pipe, carbon foam, face-sheets, cable bus, hybrids,

frond-end ASICs etc. are implemented in the model. All of these components have their own Geant4 volume. However, in the end-caps, each silicon sensor is described individually, but the remaining components of the substructure are modelled as a single wedge-shaped object placed between the two silicon layers, and uniformly filled with a generic material. The density of this material is adjusted to give a radiation length of 0.02 X_0 per substructure.

The service volumes between the barrel and end-cap sub-detectors are modelled as an annulus, followed by service volume cylinders along the end-caps. Build-up of materials along these structures is allowed for; for example there are more services from strip barrel layer 2 to layer 3 than from layer 0 to layer 1. Cable cross-sections are used to get the mass per unit length of each material and by the length needed to route the cables out. A factor of 1.3 is applied to account for indirect routing, clips, supports, etc., which are not covered by the above description. The resulting total mass of a given material is smeared evenly over the volume. Cables beyond η of 2 are folded into the modelling of PP1.

2.2.2 Description of the Pixel Detector in Geant4

In the following the modelling of the Pixel Detector is discussed in detail, starting from the description of the modules.

Each pixel module is implemented as an active sensor volume and a front-end chip. The front-end chip is modelled as a 150 μm thick silicon wafer, with a 1 μm thick copper layer to model its circuitry, and one 20 μm diameter Sn-Ag bump-bond per pixel channel. The materials of each chip are homogeneously distributed throughout their corresponding volume. 3D pixel sensors are emulated in the innermost pixel layer (layer 0) in both the barrel and end-caps. They are modelled as a 150 μm thick layer of silicon for the active sensor and a 100 μm thick layer of inactive silicon for the support wafer. Planar pixel sensors are modelled in the other pixel layers as 100 μm thick active silicon in layer 1 and 150 μm thick active silicon in layers 2 to 4, respectively. The pixel modules are then placed on the different support structures to describe the outer and inner Pixel Detector parts, barrel and end-caps.

The outer pixel barrel is modelled in simulation on realistic engineering designs of the longeron support structures as shown in Figure 2.8. Barrel layers 2 and 3 are coupled by a common longeron structure, where in layer 2 adjacent staves alternate with one or two cooling lines on a single longeron, while for layer 3 it is always two cooling lines, thus giving in this combination the total number of cooling lines per layer. Layer 4 is modelled with longerons on the outside that each have two cooling lines. The longeron truss structures are approximated by modelling them as thin sheets of carbon fibre. The four main rails that support the longeron truss, and which account for some 80% of the mass, are modelled separately using a denser material. The simulated longeron therefore has the same total mass as the physical support structure, and provides a good approximation of the mass distribution.

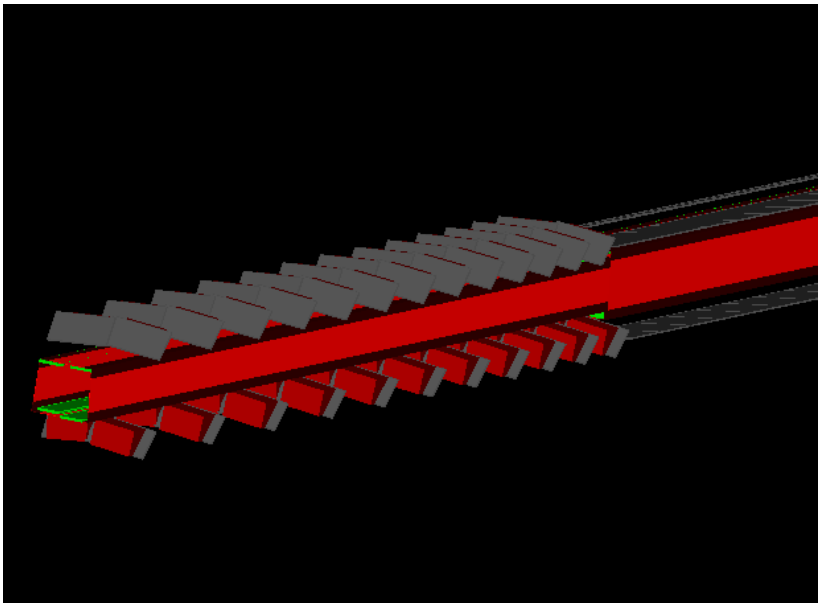


Figure 2.8: A display of the Geant4 geometry model of the outer barrel longeron stave with inclined and flat modules mounted and services running inside.

Services are running inside the longeron. The flat barrel sensors are quad modules, while the inclined sensors are dual modules. Sensor supports in the inclined section for dual modules are individually modelled as 0.6 g/cm^3 carbon foam wedges. The density of the modelled supports correspond to the prototypes that provide the best thermal performance for a 56° inclination angle.

The inner barrel support structure is modelled as carbon fibre truss double shells (see Section 13.2.4 for details), with one shell per layer. The truss shells are approximated by one sheet of carbon fibre behind each row (akin to a stave) of modules. Adjacent sheets overlap in ϕ, reproducing the ϕ modularity of the truss structure with its longitudinal support rails. For each pixel layer, the total mass of the support structure is adjusted to match the corresponding engineering estimates. The layer 1 barrel sensors are quads, with quad sensors mounted at 75° in the inclined section. Since larger sensors and a steeper inclined sensor angle are more challenging to cool, the inclined-sensor supports are modelled as cooling blocks in simulation, which are represented with a more conservative material budget, matching the corresponding engineering design for such steeply-angled inclined-sensor supports. In layer 0 the flat section has dual modules, while in the inclined section single chip modules are mounted at 75° on the same type of carbon foam cooling blocks used in the outer barrel.

The outer pixel end-caps are modelled as rings. Each layer of rings is supported by a 0.4 mm carbon fibre cylinder "shell", along which services for the rings are routed. Each "ring" is constructed from two half-rings, each covering just over half of the ϕ coverage of the entire ring. The two half rings in a pair are separated in z by 10 mm, to allow them to overlap

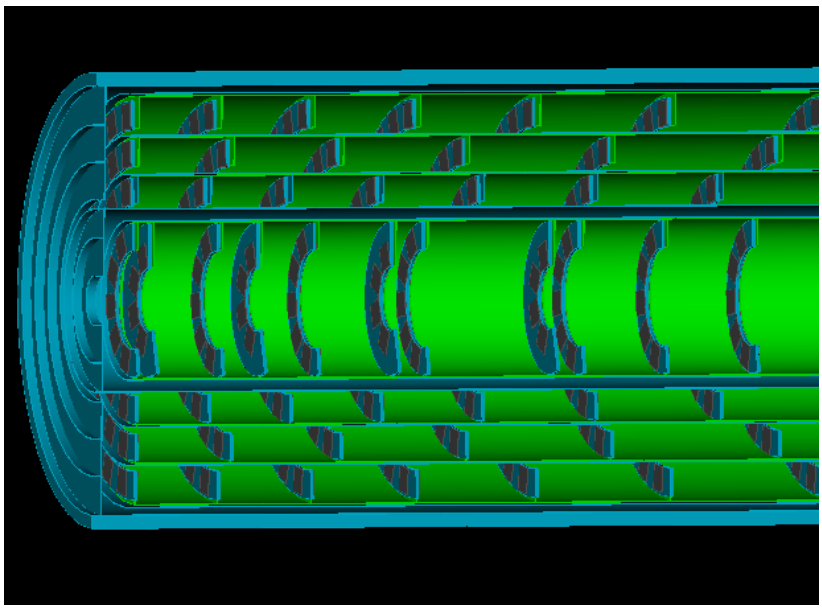


Figure 2.9: A display of the Geant4 geometry model of the inner and outer end-cap shell structures with its ring supports for modules.

in ϕ such that each ring is hermetic for $p_{\mathrm{T}} = 1$ GeV primary particles. For the inner pixel end-caps the same ring structures are used to model the detector. Figure 2.9 shows the geometry model of the inner and outer end-cap ring layers.

Great care was taken to accurately describe the material in services and cooling pipes. Detailed engineering estimates (see Chapter 14) for cable types, masses and chemical composition are used whenever possible and the corresponding multiplicities in terms of number of cables are calculated to construct the material model as implemented in Geant4. In particular, Twin-axial (AWG30) cable material was used for data lines. Services in the pixel barrel model are described according to their actual geometry. Their mass and material is smeared out across the width of each longeron. The number of cables at different z positions is modelled separately, such that at any z position along a stave the correct number of wires corresponding to the number of modules is modelled. Services in the pixel end-caps are modelled in the same way. Pixel services are modelled as continuous wires, routed from their sources out to Pixel Patch-Panel 1 (PP1), along the routes defined in engineering envelope models. The masses and materials of all services correspond to engineering descriptions. These estimates are based on a 1 MHz trigger read-out rate in the inner two pixel layers, and a 4 MHz trigger read-out rate in the outer three pixel layers, as this is the most conservative option in terms of material. The total mass of all pixel services in simulation has been computed, and is 135 kg, which is consistent with engineering estimates to within 1.5%. Figure 2.10 shows a display of the overall ATLAS Phase-II tracker ITk with the Strip and Pixel Detectors as described here.

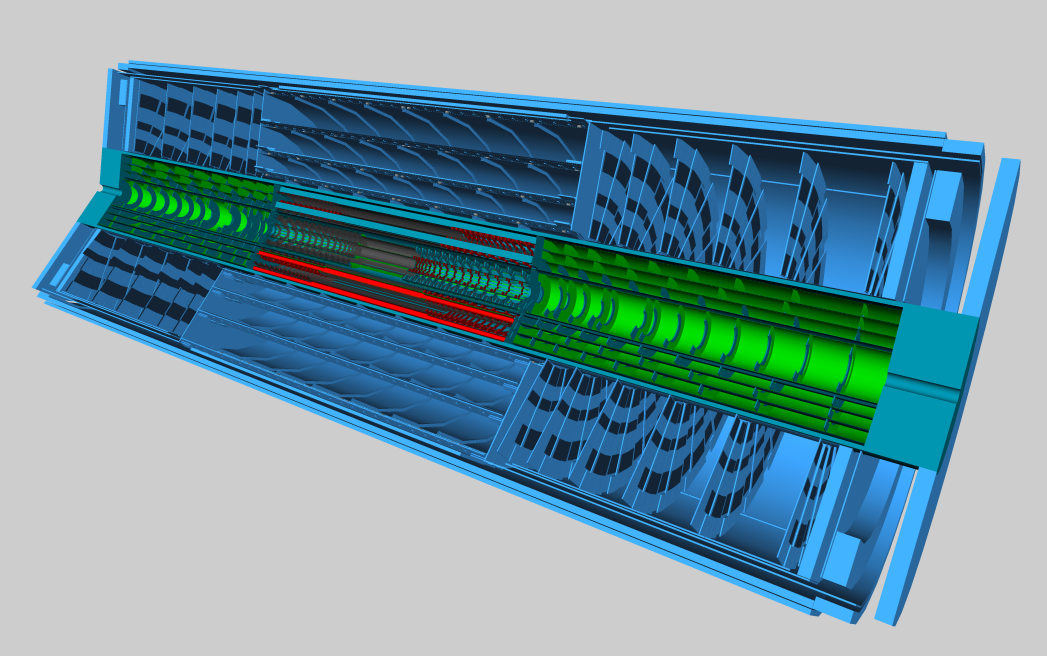


Figure 2.10: Display of the ATLAS Phase-II Inner Tracker ITk with the Inclined Duals detector layout.

2.2.3 The Digitisation, Clustering and Track Reconstruction Chain

The digitisation software for ITk strips and pixels is based on the ATLAS SCT and IBL offline software, respectively. ITk strips are modelled using n-in-p sensors with electron carriers. Here the channel efficiency is set to 99.5%, and no defects are simulated for the main results. ITk pixel sensors are simulated as planar n-in-p with electron carriers. The channel efficiency is simulated as perfect for hits above threshold, also without simulated defects. For the pixel sensor two different pitch sizes are considered for performance studies, either 50×50 μm^2 or 25×100 μm^2 as both options are still considered. For the pixel size of 50×50 μm^2, the front-end electronics in-time threshold is set to 600 electrons, with an intrinsic standard deviation of 40 electrons added in quadrature with a noise standard deviation of 75 electrons. For 25×100 μm^2 pixels the in-time threshold, intrinsic standard deviation and noise standard deviation values are all multiplied by 1.5 owing to the larger capacitance of such rectangular pixels. Most studies presented in this document are based on simulating 50×50 μm^2 pixel sensors. For some studies results are compared to simulation using 25×100 μm^2 pixel sensors. Further studies are needed to fully assess the performance implications of the different options for the pixel pitch.

The first step of event reconstruction in ITk is the formation of clusters from individual channels with a hit for the Strip and Pixel Detectors, respectively. In the following, this is illustrated using a sample of single muons with $p_{\mathrm{T}} = 100$ GeV. For the Pixel Detector, the cluster formation starts from grouping hits in adjacent pixels to form clusters. Figure 2.11

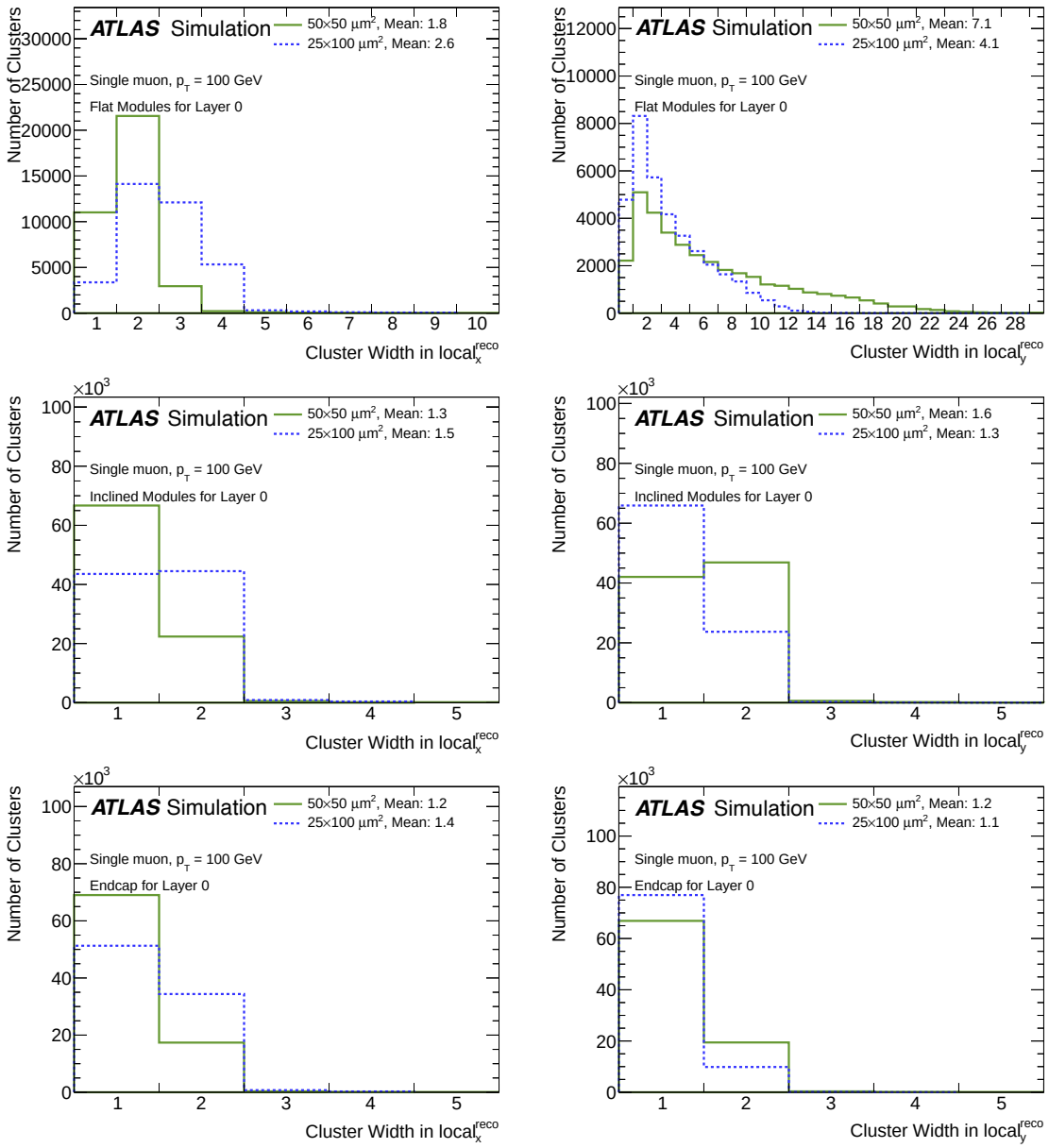


Figure 2.11: Comparison of cluster sizes in *local-X* and *local-Y* for 50×50 μm^2 and 25×100 μm^2 pitch sensors, for different parts of the detector. **Top to bottom:** Resolution for clusters in the flat and inclined section in layer 0 and in the end-cap.

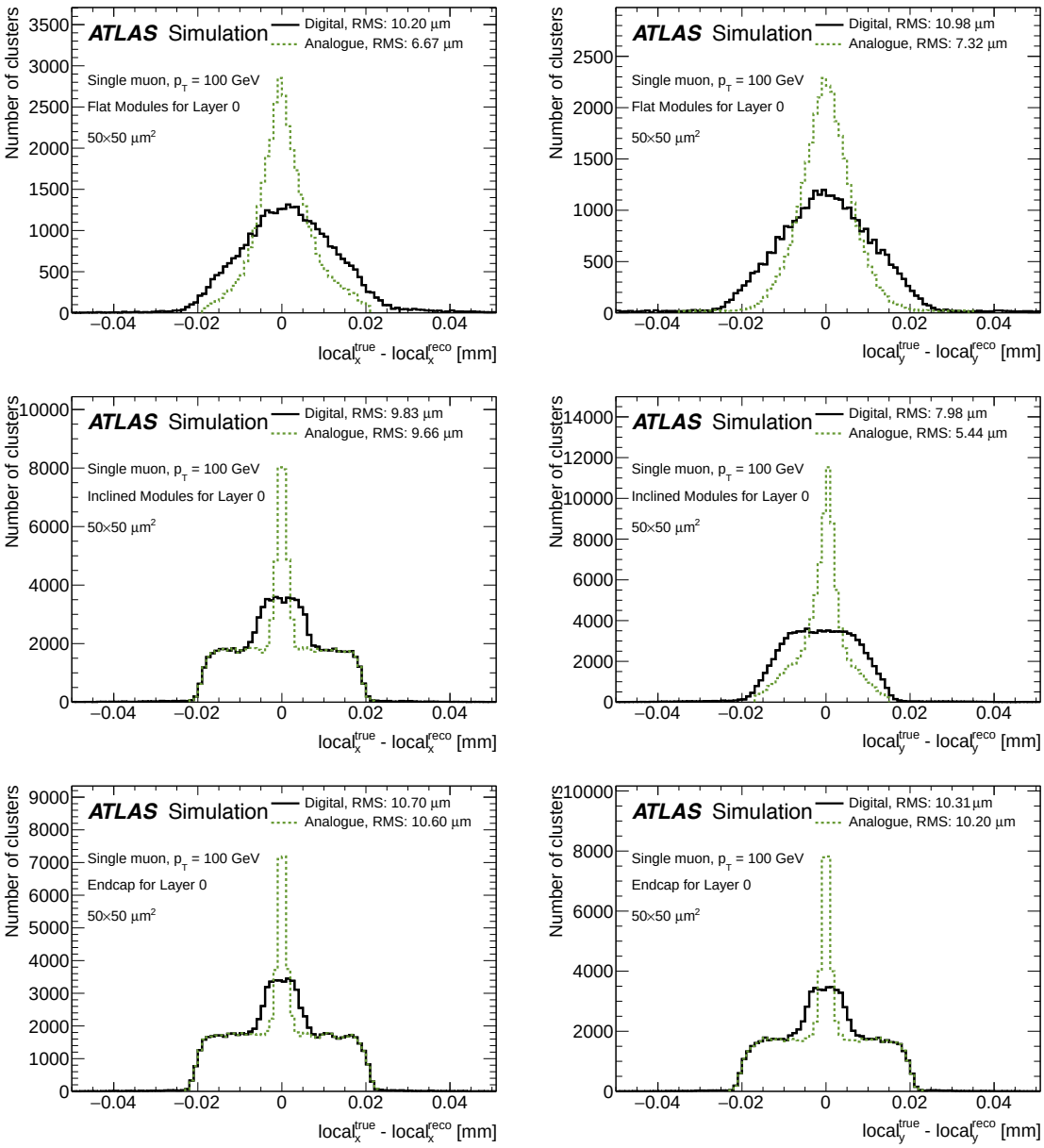


Figure 2.12: Comparison of the residuals in *local-X* and *local-Y* using digital and analogue clustering techniques with 50×50 μm^2 sensors for different parts of the detector. **Top to bottom:** Resolution for clusters in the flat and inclined section in layer 0 and in the end-cap.

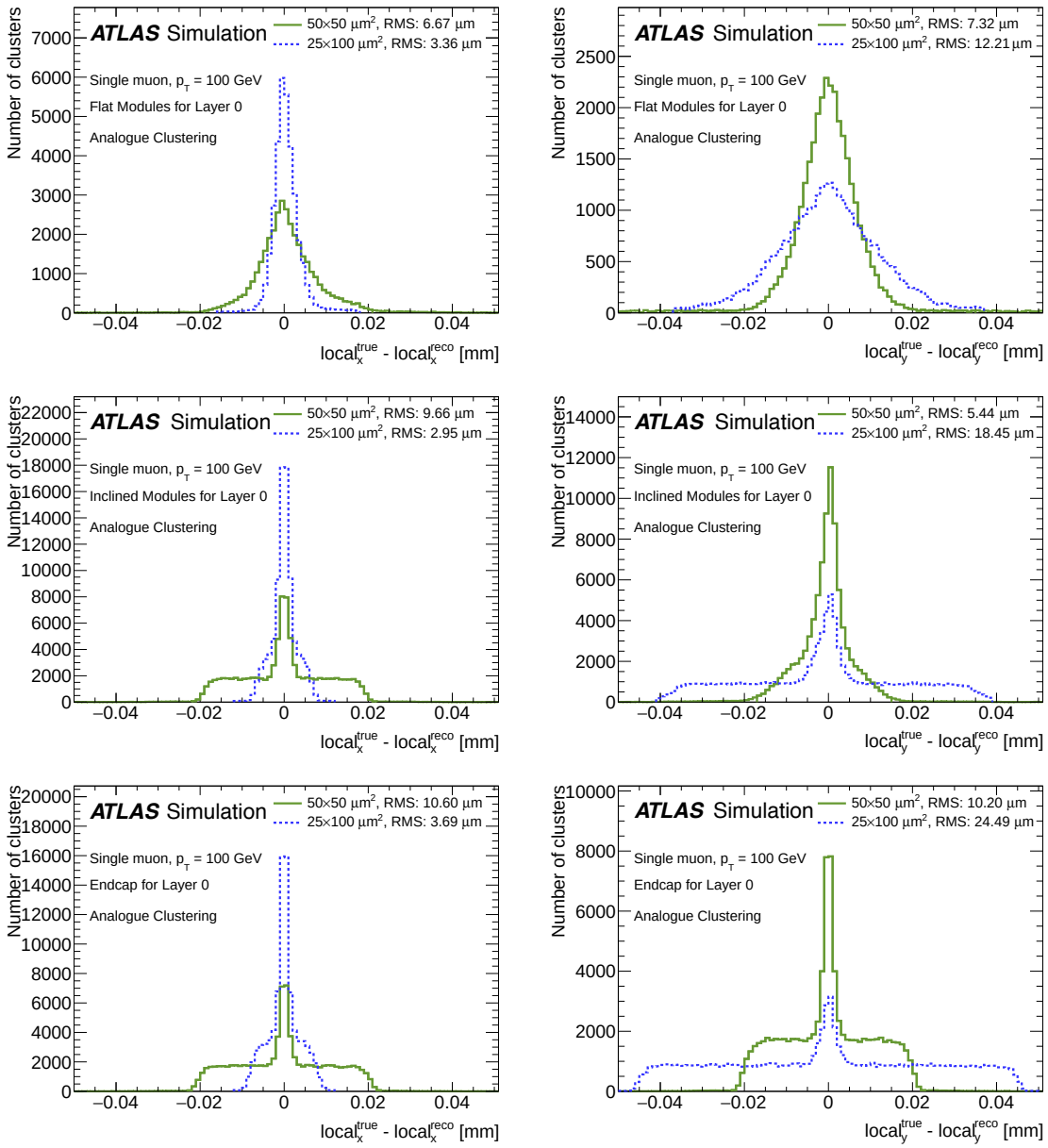


Figure 2.13: Comparison of the residuals in *local-X* and *local-Y* using analogue clustering techniques 25×100 μm^2 and 50×50 μm^2 pitch sensor for different parts of the detector. **Top to bottom:** Resolution for clusters in the flat and inclined section in layer 0 and in the end-cap.

Table 2.5: Set of cuts applied during the track reconstruction depending on the pseudorapidity interval. Holes are counted if track candidates cross active sensors on which no hit was found, double holes are two consecutive active sensors crossed without a hit found. Here d_0 and z_0 are defined with respect to the mean position of the beam spot.

Requirement	Pseudorapidity interval		
	$\lvert\eta\rvert < 2.0$	$2.0 < \lvert\eta\rvert < 2.6$	$2.6 < \lvert\eta\rvert < 4.0$
Pixel+Strip hits	≥ 9	≥ 8	≥ 7
Pixel hits	≥ 1	≥ 1	≥ 1
Holes	< 2	< 2	< 2
Double holes	≤ 1	≤ 1	≤ 1
Pixel holes	< 2	< 2	< 2
Strip holes	< 2	< 2	< 2
p_T [MeV]	> 900	> 400	> 400
$\lvert d_0\rvert$	≤ 2 mm	≤ 2 mm	≤ 10 mm
$\lvert z_0\rvert$	≤ 20 cm	≤ 20 cm	≤ 20 cm

shows the resulting cluster sizes in *local-X* and *local-Y* [3]. The cluster sizes vary with the average inclination angle of particles hitting the sensors, as can be seen for the flat and inclined barrel sensors and for the end-cap sensors. Two algorithms are used to determine the cluster position. The first algorithm (digital clustering) only uses the information that a pixel has a hit to determine the cluster position, while the second algorithm (analogue clustering) makes use of the analogue information capabilities of the read-out chip to further refine the precision of the cluster position, interpolating the charge measurement of the first and last pixel hit in both directions. Figure 2.12 shows the residual between the measured and the true position in *local-X* and *local-Y* using digital and analogue clustering for single muon events and 50×50 μm^2 pitch sensors, for different regions of the detector. Significant gains in resolution are obtained by means of charge interpolation, in particular in *local-Y* for the flat and inclined barrel sensors. The shape of the distribution reflects the average incident angles of particles hitting the sensors and the resulting rate of clusters with a width of 1 pixel or larger than 1 pixel in *local-X* or *local-Y*, respectively.

Figure 2.13 shows a comparison of analogue clustering results for 25×100 μm^2 and 50×50 μm^2 sensors in the flat barrel and inclined sections in layer 0 and for end-cap sensors. As expected, while with 50×50 μm^2 the analogue clustering significantly improves the *local-Y* resolutions, with 25×100 μm^2 the *local-X* benefits most. In the flat section the loss in *local-Y* is smaller compared to the inclined and end-cap sections, as in those sections the clusters width with 25×100 μm^2 ends up being mostly 1 pixel.

The next step after the clustering is the space point formation. Here, the strip cluster inform-

[3] The *local-X* and *local-Y* coordinates represent the two coordinates along the pixel sensor grid. Depending on how the sensor is mounted those local coordinates translate into global directions. *local-X* is in the $R\phi$ plane perpendicular to the beam line. For a flat barrel module *local-Y* points in the z direction, for an end-cap module it points radially in R and accordingly in Rz for inclined modules.

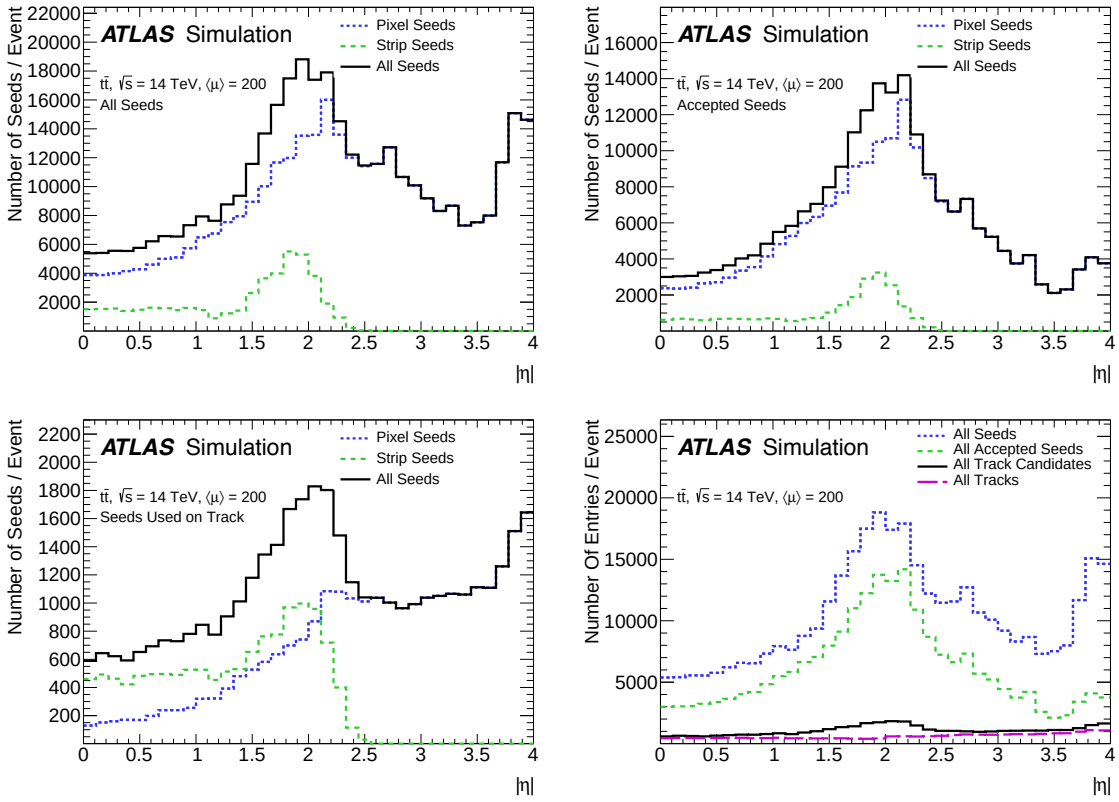


Figure 2.14: **Top left:** The number of all space point triplet track seed combinations found when searching in the Strip and Pixel Detectors, respectively. **Top right:** Number of accepted seeds after duplicate removal, used to start the combinatorial Kalman Filter track finder. **Botton left:** Number of strip and pixel seeds that result in a track candidate before final ambiguity resolution. **Bottom right:** Summary of all seeds, selected seeds, track candidates and final tracks after ambiguity resolution, as a function of η. All results are shown for $t\bar{t}$ Monte Carlo simulation events with an average of 200 pile-up events.

Table 2.6: The CPU required in HS06×seconds to reconstruct $t\bar{t}$ Monte Carlo events with an average of 200 pile-up events in the ITk, for the different reconstruction steps. Shown as well are the results for the current Run 2 Inner Detector for $t\bar{t}$ events with an average of 20 pile-up events. The studies were done on an Intel Xenon 7210, 1.3 GHz, 64 core CPU, 116 GB RAM. The CPU time is multiplied with the HS06 factor of 3.5.

Detector, Pile-up	Cluster Finding	Space Points	Si Track Finding	Ambiguity Resolution	TRT+Back Tracking	Primary Vertex	Total ITk/ID
ITk, 200	26	24	124	96	-	6	283
Run 2, 20	1.5	0.7	23	15	19	0.5	64

ation from both sides of a barrel stave or end-cap petal is used to construct strip combinations, exploiting the small stereo angle to obtain precise information in *local-Y*. The pixel and strip space points are then used in the seeding stage of the track finding. The track finding used for reconstruction of the ITk is based on the same code used for the current ATLAS Inner Detector for Run 2, tuned for the ITk geometry and with a first optimisation for 200 pile-up. The technique applied is an iterative, combinatorial Kalman filter that is seeded from triplet space point combinations. For the ITk, the track seeding starts with strip space point triplet combinations in the first iteration and then makes use of the pixel information to find additional track candidates. For each triplet combination, all space points are required to be on a straight line in Rz. They form a circle in $R\phi$, allowing an estimate of the initial helix parameters. After applying initial p_{T} and impact parameter cuts, a confirmation of the seed in a 4th layer is done to further reject fake combinations. Finally, seeds are accepted after a duplicate removal. For each accepted seed, a search road is defined, in which a combinatorial Kalman filter is used to find one or more track candidates. Those candidates are subject to an ambiguity resolution stage, with the aim of rejecting incomplete and duplicate tracks, resolving situations with shared clusters between several tracks, and removing fake tracks. This is achieved by scoring the track candidates based on the presence or absence of hits when crossing the sensor layers. Each track candidate considered is fitted using the Global-χ^2 track fit. The procedure is repeated iteratively, attributing shared clusters to the higher scoring track candidate, and refitting candidates that got modified, to obtain the final set of tracks. As part of the ambiguity selection the track selection criteria listed in Table 2.5 are applied to all tracks entering the final list of selected good tracks.

The behaviour of the reconstruction flow is illustrated in Figure 2.14, which in the top left, shows the rate of all strip or pixel seeds for $t\bar{t}$ Monte Carlo events with 200 pile-up. Shown as well in the Figure (top right) is the rate of accepted seeds, that pass a duplicate filter rejecting triplets of space points already used before to find a track candidate. Accepted seeds are used to start the combinatorial Kalman track finder, which is the most time consuming component of the pattern recognition. The lower, left plot shows the rate of good track candidates that are found using strip or pixel seeds. The lower, right plot shows the summary of all seeds, selected seeds, candidates and final tracks after ambiguity resolution.

The Phase-II environment with an average of up to 200 pile-up events also presents a chal-

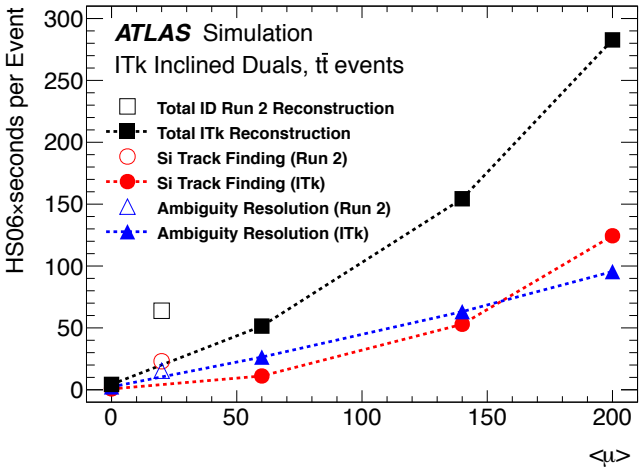


Figure 2.15: The CPU required in HS06×seconds to reconstruct a $t\bar{t}$ event in the ITk as a function of the average pile-up. Shown is the total CPU required to reconstruct the ITk, the CPU spend for the silicon track finding and for the ambiguity resolution. For comparison the corresponding CPU requirements for reconstructing the current Run 2 detector are shown, for an average pile-up of 20 events.

lenge in terms of CPU time needed for reconstruction. From the very beginning the CPU performance was taken into account in the layout optimisation process, aiming to minimise the combinatorial complexity and hence the CPU requirement for the ITk. Table 2.6 compares the CPU requirements in terms of HS06×seconds [10] for each reconstruction step for $t\bar{t}$ Monte Carlo events with 200 pile-up for the ITk and 20 pile-up for the current Run 2 Inner Detector, respectively. Figure 2.15 shows the CPU required to reconstruct a $t\bar{t}$ event in the ITk with different levels of average pile-up. Even with the preliminary tuning of the ITk reconstruction, the total CPU time spent in tracking is significantly less than 10 times slower at an average of 200 pile-up events than the time spend in reconstructing events with an average of 20 pile-up events in the current Run 2 detector, despite the 10 times higher average pile-up. It illustrates that the ITk meets the design goal of a layout optimised also for the technical performance of the reconstruction of high pile-up events.

More results on the tracking behaviour and performance are detailed in the Chapter 3.

2.2.4 Occupancies in Pixels from Simulation Studies

Presented here are hit density and chip occupancies in the Inclined Dual layout as predicted using the Geant4 simulation. These occupancies determine the bandwidth required for the front-end chips and read-out. Low hit densities are as well important to reduce pattern recognition mistakes due to wrong hit associations.

Table 2.7: Average hits per chip per event for 50×50 μm^2 pixels using $t\bar{t}$ events with 200 pile-up. Listed are results layer by layer for the flat and inclined barrel regions and the end-caps.

(Ring) Layer	Flat Barrel	Inclined Barrel	End-cap
0	223.0	136.7	80.9
1	26.6	27.8	37.7
2	19.3	20.1	21.0
3	12.9	12.7	13.3
4	9.9	9.1	9.3

Hit occupancy is defined as the number of hit pixels per chip and per event. These were calculated per chip and event, then averaged over chips sharing the same z position. Each pixel sensor is divided into an array of 1×4 $(\phi - \eta)$ pixel regions (see Section 4.3.1 for details). This replicates the read-out structure of the chips, where only hit regions are read out, along with sub-region pixel information, in order to limit the read-out data rate from long (η) clusters. Hence a region occupancy, i.e. the number of hit regions per chip, and a regional occupancy, i.e. the number of hit pixels per region (maximum of 4), were also calculated.

Figure 2.16 shows the average channel occupancy, the average number of hits per chip, the average number of regions with a hit per chip and the average occupancy per region with at least one hit, for the Inclined Dual layout, for the barrel and end-cap regions, respectively. Simulated samples of $t\bar{t}$ events were used with an average of 200 pile-up events superimposed. The results shown are for a pixel size of 50×50 μm^2. In the flat barrel section the average hit and regional occupancies increase rapidly with z, while the number of hit regions per chip decreases with the change in phase-space covered by each flat module. In the inclined section the average hit and regional occupancies drop as the incident angle becomes more orthogonal, then increases slowly with z. At extremes of the inclined barrel the hit occupancy is comparable to the inner flat region, especially for the outermost layers. The end-cap section shows similar behaviour to the inclined barrel region, with relatively slow increases in occupancy over z.

Table 2.7 shows the average number of hits per chip across z in the flat and inclined barrel sections, as well as for the end-cap, as a function of pixel layer. The central z (flat) region of layer 0 dominates in occupancy. This is due to the proximity to the collision region and to the relatively large thickness of the 3D sensors in barrel layer 0.

Figure 2.17 shows the distribution of the chip hit occupancy over the event sample for barrel and end-cap regions. Ring 0 in the end-cap section also shows relatively high number of hit chips per event compared to other ring layers. The right shoulder in the ring 0 distribution comes from the chips with smallest radii, which have a higher occupancy.

Table 2.8 shows the maximum occupancy per barrel layer and end-cap ring along with hit densities and channel occupancies. The highest average occupancy across z in the barrel is

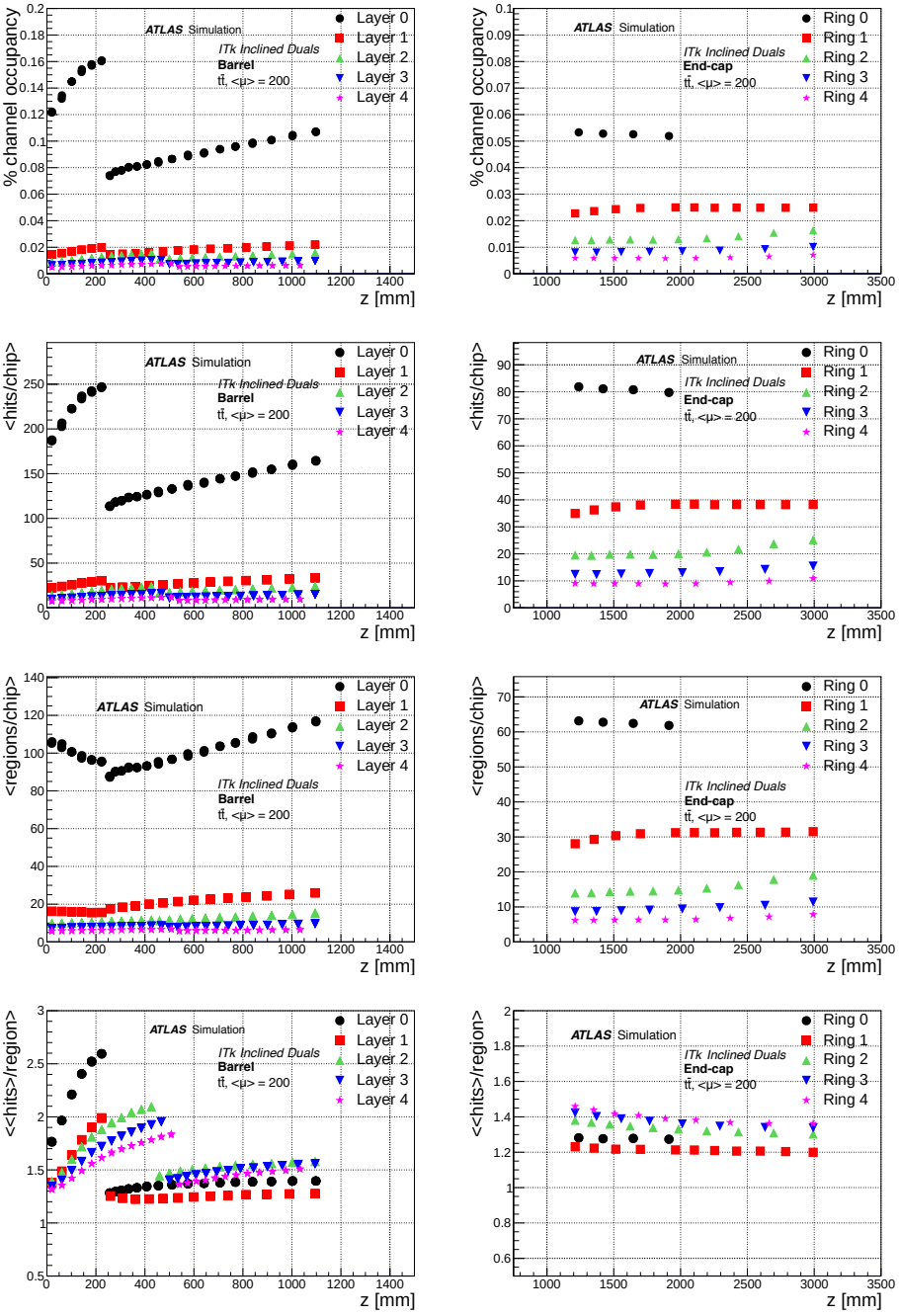


Figure 2.16: Average occupancy for the Inclined Dual layout, separated for (**left**) barrel and (**right**) end-caps. Results are for sensors with 50×50 μm^2 pixel pitch and $t\bar{t}$ events with 200 pile-up. **Top**: Channel occupancy in percent. **Second row:** Hit occupancy per chip. **Third row:** Region occupancy. **Bottom**: Average regional occupancy.

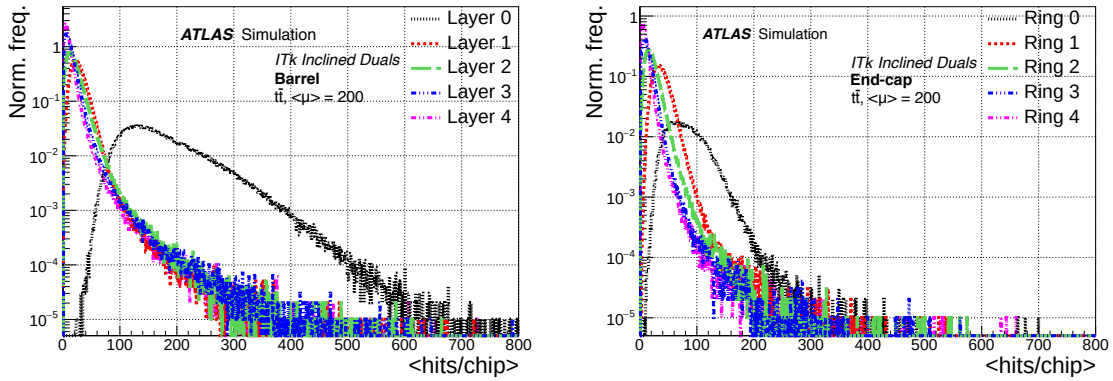


Figure 2.17: Distribution of chip occupancies over all events (minimum single hit) for the Inclined Dual layout, separated for barrel and end-caps. **Left**: Barrel **Right**: End-cap.

Table 2.8: Maximum hits per chip per event in each layer for 50×50 μm^2 pixels flat and inclined barrel regions and the end-caps. Results are for $t\bar{t}$ events with an average of 200 pile-up events.

Barrel Layer	$< hits/chip >$	$< chan.Occ. >$ [%]	$< density >$ [mm^{-2}]
0	247.1	0.161	0.643
1	33.7	0.022	0.088
2	24.3	0.016	0.063
3	16.0	0.010	0.042
4	12.2	0.008	0.032
Ring Layer			
0	81.9	0.053	0.213
1	38.4	0.025	0.100
2	25.2	0.016	0.066
3	15.5	0.010	0.040
4	10.9	0.007	0.028

247 pixels, which translates to a maximum channel occupancy of 0.16 % and maximum hit density of 0.64 mm^{-2}.

2.3 Fluence and Radiation Dose Studies

Due to the increased luminosity and the associated increase in the rate of proton-proton collisions, the expected radiation levels in the ATLAS ITk will increase by roughly an order of magnitude compared to the present Inner Detector. Radiation background simulations have been performed for the ITk using the PYTHIA8 [11] event generator and the FLUKA [6] particle transport code. The predictions of particle fluences and ionising doses for the ITk layout assume an integrated luminosity of 4000 fb^{-1} and an inelastic proton-proton cross-section of 79.3 mb at a centre-of-mass energy $\sqrt{s} = 14$ TeV. In Figure 2.18 the fluence and dose distributions for the Pixel Detector are shown. Plots of 1 MeV neutron equivalent fluences and dose are normalised to 4000 fb^{-1}; the other plots are per event. It is important to emphasise that accurate fluence and dose predictions require precise modelling of the entire ATLAS geometry in FLUKA. While fluences in the innermost layers of the ITk pixel barrel region are dominated by particles coming directly from the interaction point, the fluences in the outer barrel layers and the pixel end-cap region are increasingly dominated by particles coming from secondary interactions in the calorimeter, beam-line and pixel service material. The pixel services are routed out radially away from the beam-line as soon as feasible as this is beneficial in reducing radiation backgrounds, including the activation of detector components. Hadron fluences for energies greater than 20 MeV are also calculated to allow estimates of Single Event Upsets (SEU), as well as charged particle fluences which can be used for occupancy estimates.

In the baseline scenario, the outer pixel barrel and end-cap detector will be operated to collect a total integrated luminosity of up to 4000 fb^{-1}, while the inner barrel and end-caps are replaced after 2000 fb^{-1}. A summary of the maximum 1 MeV neutron equivalent fluences and the ionising dose are given in Table 2.9. For these results the values have been multiplied by a safety factor of 1.5. Within the baseline replacement scenario the maximal fluences and total ionising doses are within sensor specifications as described in Chapter 5.

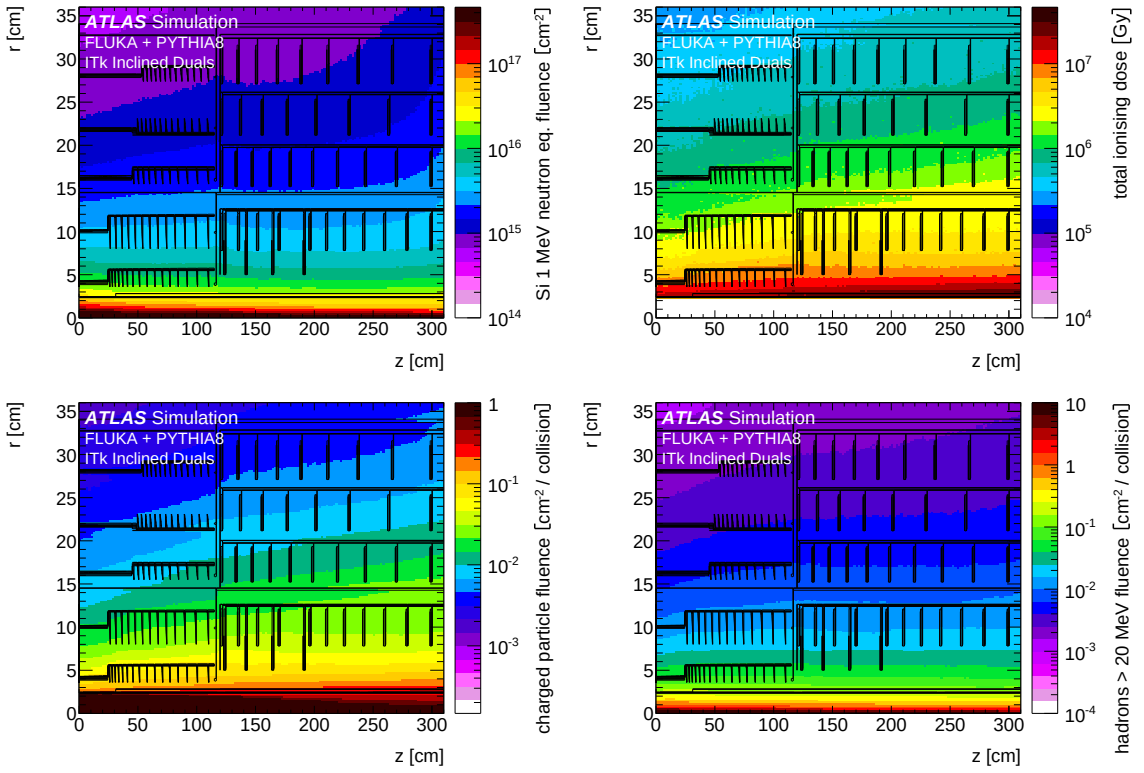


Figure 2.18: The fluence and dose distributions for the Pixel Detector. **Top left**: 1 MeV neutron equivalent fluence. **Top right**: Total ionising dose. **Bottom left**: Charged particle fluence. **Bottom right**: Hadron fluence for energies greater than 20 MeV. The top two lots are normalised to 4000 fb^{-1}. No safety factors are taken into account for this Figure.

Table 2.9: The maximal 1 MeV neutron equivalent fluences and total ionising dose for different parts of the Pixel Detector, for the baseline replacement scenario for the inner section. All values have been multiplied by a safety factor of 1.5.

Luminosity	Layer	Location	R (cm)	z (cm)	Fluence (10^{14} n_{eq}/cm^2)	Dose (MGy)
2000 fb^{-1}	0	flat barrel	3.9	0.0	131	-
			4.0	24.3	-	7.2
		inclined barrel	3.7	25.9	123	-
			3.7	110.0	-	9.9
		end-cap	5.1	123.8	68	6.3
2000 fb^{-1}	1	flat barrel	9.9	24.3	27	1.5
		inclined barrel	8.1	110.0	35	2.9
		end-cap	7.9	299.2	38	3.2
4000 fb^{-1}	2-4	flat barrel	16.0	44.6	28	1.6
		inclined barrel	15.6	110.0	30	2.0
		end-cap	15.3	299.2	38	3.5

2.3.1 Pixel Sensor Radiation Damage Simulation

Non-ionising energy losses introduce defects in the silicon band gap which increase the leakage current, deform the electric field, and result in the trapping of mobile charge carriers. Changes in the electric field increase the depletion voltage. Defects decay over time through the process of annealing that depends on the thermal history of the sensors. The current simulation of the ITk does not account for bulk radiation damage effects. This section briefly introduces a new simulation [12] that includes such effects, has been validated with Run 2 collision data and test beam data, and will be incorporated into the ATLAS simulation framework in the future.

One of the most critical inputs to the simulation is the electric field profile after irradiation. Figures 2.19 and 2.20 show the field profiles for planar and 3D sensors, respectively. The electric field is computed with Technology Computer Aided Design (TCAD) using models with effective energy levels in the silicon band gap. All models agree that for a fixed bias voltage, the field becomes more non-uniform with increasing fluence. However, there are significant disagreements between models for the exact form of the profile, as indicated for two planar sensor models in Figure 2.19. Each model is validated in some way with test beam data and over time, the spread in predictions will close as additional high-quality data are acquired. The double-peak structure observed in the New Delhi model [13] in Figure 2.19 is characteristic of n-on-n sensors at moderate fluences (up to 10^{15} n_{eq}/cm^2) used in the current ATLAS Pixel Detector, but may not be appropriate for n-on-p at high fluences where the Perugia 2017 models predicts a linear field [14]. Studying the field-dependence of highly irradiated sensors is an active area of research (see e.g. Reference [16]); the spread

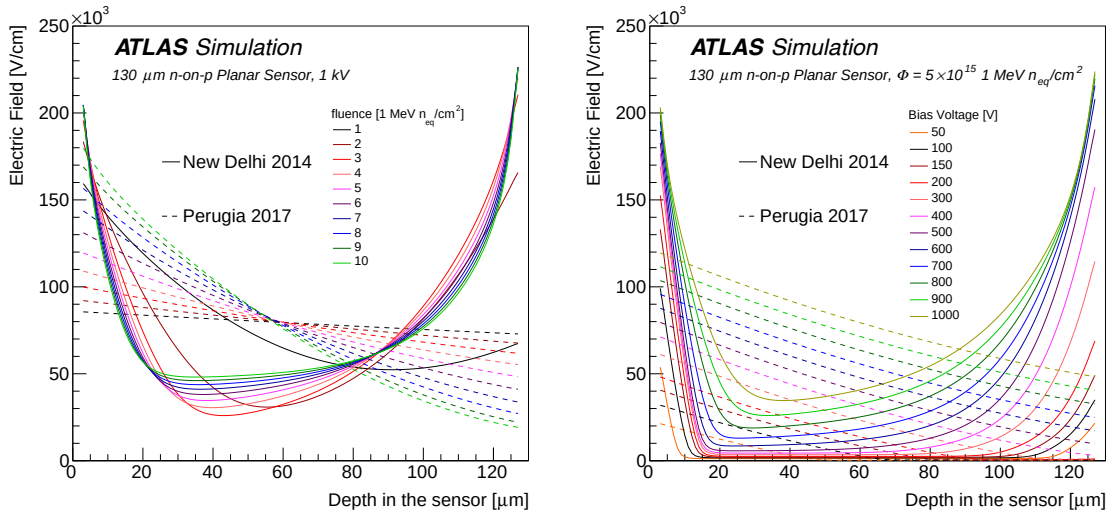


Figure 2.19: Electric field profile along the depth direction for 130 μm planar sensors at 1 kV for different fluences (**left**) and a scan of bias voltages for a fluence of 5×10^{15} n_{eq}/cm^2 (**right**), using the New Delhi 2014 [13] and Perugia 2017 models [14].

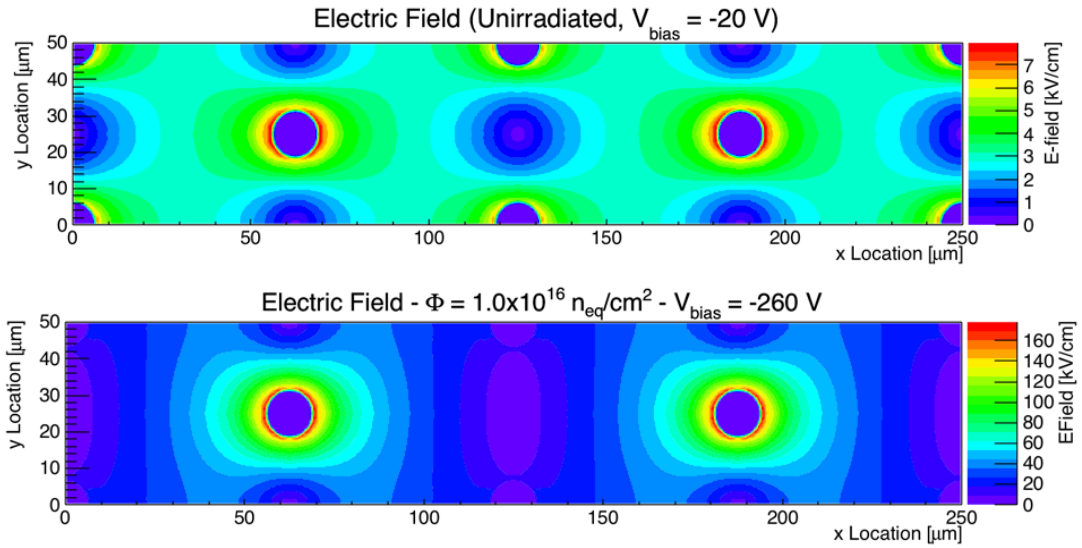


Figure 2.20: The electric field profile along the directions transverse to the depth for the unirradiated case and bias voltage of 20 V (**top**) and for a fluence of 1×10^{16} n_{eq}/cm^2 at 260 V bias voltage (**bottom**) using the Perugia model [15].

in predictions from the two models shown in Figure 2.19 is an indication of the current uncertainty.

The most important quantity for assessing the impact of radiation damage on tracking performance is the charge collection efficiency (CCE). Figure 2.21 shows the CCE for planar and 3D sensors using the New Delhi and Perugia models, respectively. The CCE is computed by extrapolating the electric field up to a desired fluence, producing a time-over-threshold distribution and fitting this to a Landau convolved with a Gaussian, and then taking the most probable value divided by the corresponding zero-fluence value. The bias voltage is set to 600 V for planar sensors and for 3D sensors to -20, -20, -30, -50, -50, -160, -190, and -260 V for 0, 1, 2, 5, 10, 50, 60, and 100 $\times 10^{14}$ n_{eq}/cm^2, respectively. Table 2.10 uses the information in Figure 2.21 combined with the predicted fluence on the five pixel layers after 2000 fb^{-1} for the innermost two layers and 4000 fb^{-1} for the outer layers to predict the CCE for planar and 3D sensors. The model predictions for the CCE is similar for the all layers. These predictions are in agreement with test beam data, as discussed in Reference [17]. Test beam results for planar and 3D sensors foreseen for the ITk are discussed in Chapter 5, illustrating the hit efficiencies and operational parameters for irradiated sensors.

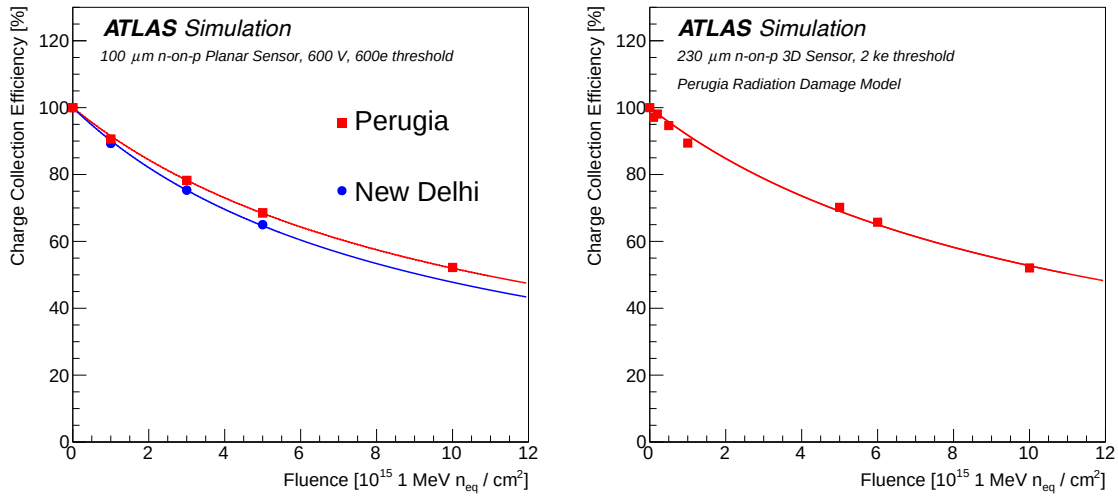


Figure 2.21: The charge collection efficiency (CCE) as a function of fluence for planar (**left**) and 3D sensors (**right**). The points indicate the fluences at which the CCE has been calculated. The New Delhi model is used for the planar sensor up to 1×10^{15} n_{eq}/cm^2; beyond that, the electrical field is extrapolated from the previous points and the CCE is then calculated using the extrapolated field. The Perugia model is used for 3D sensors. Annealing is not included.

Location	Fluence [10^{15} n_{eq}/cm^2]	Planar CCE [%]	3D CCE [%]
Layer 0	13.1	41	45
Layer 1	2.6	77	80
Layer 2	2.7	76	79
Layer 3	1.6	84	87
Layer 4	1.2	88	90

Table 2.10: The charge collection efficiency for planar and 3D sensors on the five pixel barrel layers using the fluence-dependence shown in Figure 2.21 after 2000 fb^{-1} for the innermost two layers and 4000 fb^{-1} for the outer layers, taking a safety factor of 1.5 into account. See Figure 2.21 for the high voltages and thresholds.

2.3.2 Implications of a High Granularity Timing Detector on the ITk

The High Granularity Timing Detector (HGTD) [18] adds precision timing in the very forward region ($2.4 < |\eta| < 4.2$) to complement the ITk and to further enhance the pile-up mitigation at the HL-LHC. The addition of the HGTD has two direct consequences on the ITk itself. One is a necessary change in the overall ITk envelope to free space for the HGTD itself, the other are the implications of the HGTD on the radiation environment for the ITk.

In the configuration without a HGTD detector (Figure 2.22(a)), the ITk side of the end-cap calorimeters is covered by a 50 mm borated polyethylene (BPE) moderator which reduces the neutron albedo from the end-cap calorimeter to the ITk. The replacement of this moderator with the HGTD detector ('plain HGTD', shown in Figure 2.22(b)) would increase the neutron fluence in the large-z part of the ITk by about 50 %. When the HGTD is covered by an additional layer of 50 mm BPE (Figure 2.22(c)), the shielding performance is restored. Since the HGTD consists of very light material, very similar to the ITk itself, it is not a significant additional source of neutrons by itself. Therefore the baseline is to place the HGTD on the ITk side of the moderator on the end-cap calorimeter ('optimised layout', shown in Figure 2.22(d)), in which case the latter also protects the HGTD sensors. In this configuration the envelope available to the ITk is shortened by the thickness of the HGTD assembly, which in its current design would amount to ∼75 mm.

Figure 2.23 shows the fluence (in n_{eq}/cm^2) divided into neutron and "other particles" components as a function of the radius. Only the neutron component is affected by the moderators. At small radii, in the inner pixel and for the inner part of the outer pixel volumes, the "other particles" (mostly $\pi^{\pm}$) component dominates. In the central regions of the ITk the HGTD and moderator configuration is practically irrelevant. A clear reduction of the neutron component is only observed at the end of the ITk volume, close to the end-cap.

Figure 2.24 gives a summary of the HGTD and moderator configuration studies. The solid blue symbols represent different configurations between the extremes shown in Figures 2.22(b) and 2.22(c), i.e. a moderator thickness varied from 0 top 100 mm between the HGTD and the ITk. The horizontal line is the baseline level without any HGTD. The other points at 50 mm thickness are variations of Figure 2.22(d). The open triangle corresponds to the optimised layout.

The details of the ITk layout are affected by a necessary envelope reduction of ∼75 mm in z to accommodate an HGTD. For both the Pixel Detector and the Strip Detector, the positions of all the end-cap rings and disks, respectively, would be adjusted to shorten the overall system in z while keeping optimal coverage. These adjustments would not affect the overall design of both sub-detectors.

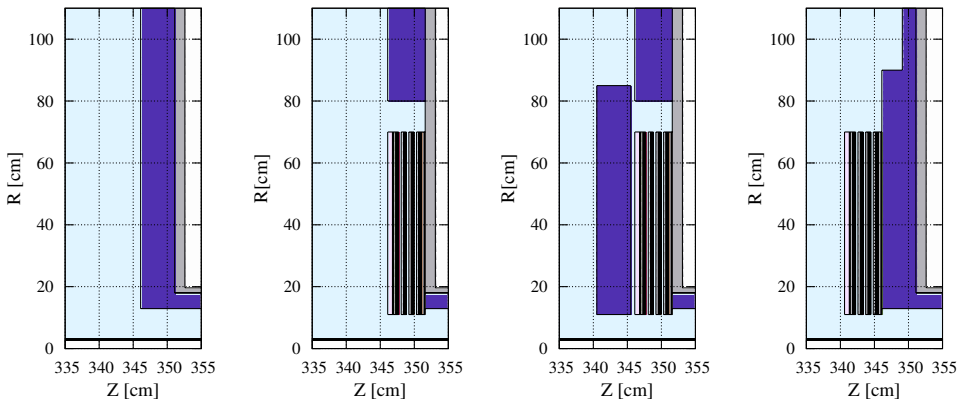


Figure 2.22: Different moderator configurations explored during the optimisation. (**a**) The *baseline* without the HGTD and a Run 2 like moderator configuration. (**b**) The *plain HGTD*, where the HGTD replaces the Run 2 moderator at $r < 80\,\text{cm}$. (**c**) The HGTD fixed on the end-cap, but covered with a moderator layer. For option (c) the thickness of the moderator layer is varied from 0 to 10 cm in order to find an optimal balance between space consumption and 1 MeV-neutron equivalent fluence reduction. (**d**) In configuration the HGTD is placed on the ITk side of the moderator. For this configuration the moderator thickness at $r > 70\,\text{cm}$ has been varied in order to create space for services. The geometry shown in (d) is referred to as *optimised layout*.

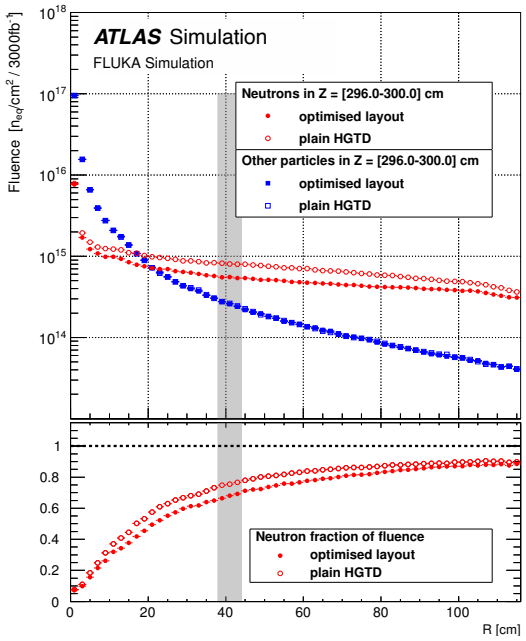


Figure 2.23: **Top**: Fluence in n_{eq}/cm^2 separated into neutron and "other" components in the region close the the HGTD. The values for two different moderator configurations are compared. The 'plain HGTD' corresponds to Figure 2.22(b) while the 'optimised layout' refers to Figure 2.22(d). The 'hot spot' radial range, used in Figure 2.24, is indicated by the shaded band. **Bottom**: Fraction of total fluences.

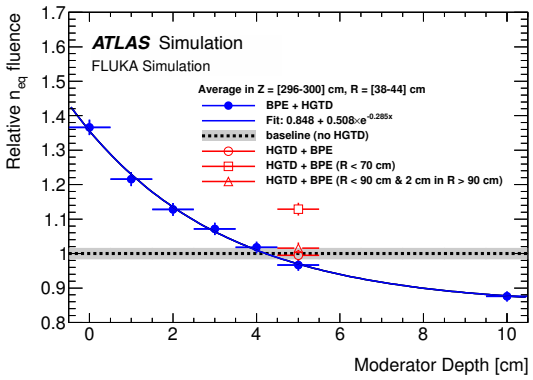


Figure 2.24: Relative 1 MeV neutron equivalent (n_{eq}) fluence in the hottest spot of the outermost ITk Strip end-cap relative to the baseline without a HGTD. The horizontal line, showing the baseline configuration with 50 mm moderator and no HGTD, is considered the target level for the shielding optimisation. The solid blue circles and the fit show the fluence reduction as a function of the moderator thickness between the ITk and the HGTD. The other symbols at 50 mm thickness correspond to configurations in which the HGTD is on the ITk side of the moderator. They differ only in terms of moderator thickness at $r > 70$ cm.

3 Tracking and Physics Performance

In this chapter, the expected performance of the ITk Detector, described in Chapter 2, is presented. The detector layout is based on the requirement of identifying charged particles with high efficiency and purity and measuring their properties with high precision in the presence of an average of up to 200 pile-up events expected at the HL-LHC. The upgraded detector should preserve and, if possible, exceed the physics performance of the current Run 2 detector, under the Phase-II operational conditions. The results presented here update those presented in the Strip TDR [1].

In Section 3.1, the tracking and vertexing performance of the ITk Detector is compared to the performance of the current (Run 2) Inner Detector (ID). Results are presented on tracking efficiency, fake rates at different levels of pile-up, track parameter resolutions, robustness of tracking with respect to detector defects and tracking performance in dense environments, such as for high-p_{T} jets or τ-leptons. The performance of the primary vertex reconstruction is also shown. In Section 3.2, results are presented for b-tagging and for the pile-up mitigation for jet and $E_{\mathrm{T}}^{\mathrm{miss}}$ reconstruction using the ITk Detector, followed by results on lepton identification and isolation studies. In the final section of this chapter, results are presented for physics studies exploring the potential of the upgraded detector at the HL-LHC.

All performance studies presented in this chapter are done using Monte Carlo events based on a full Geant4 simulation as described in Section 2.2. For most studies, samples are used where an average of 200 pile-up interactions are overlaid[1] on the hard-scattering event. The reconstruction software used is adapted from Run 2 to reflect the new geometry, and take advantage of further improvements discussed in Chapter 2. The default track selection cuts listed in Table 2.5 are used. While the reconstruction software is not yet fully optimal for the ITk, it is sufficiently tuned to build confidence that an adequate performance can be achieved for the goals of the HL-LHC physics programme.

[1] The average pile-up $\langle\mu\rangle = 200$ is in practice simulated as a uniform distribution between 190 and 210, from which for a given event a value of $\langle\mu\rangle$ is chosen and then the actual number of pile-up events is selected from a Poisson distribution. The interaction vertices are distributed along a Gaussian shaped beam spot region with a length of $\sigma(z) = 5$ cm, and a width of 12 μm in x and y.

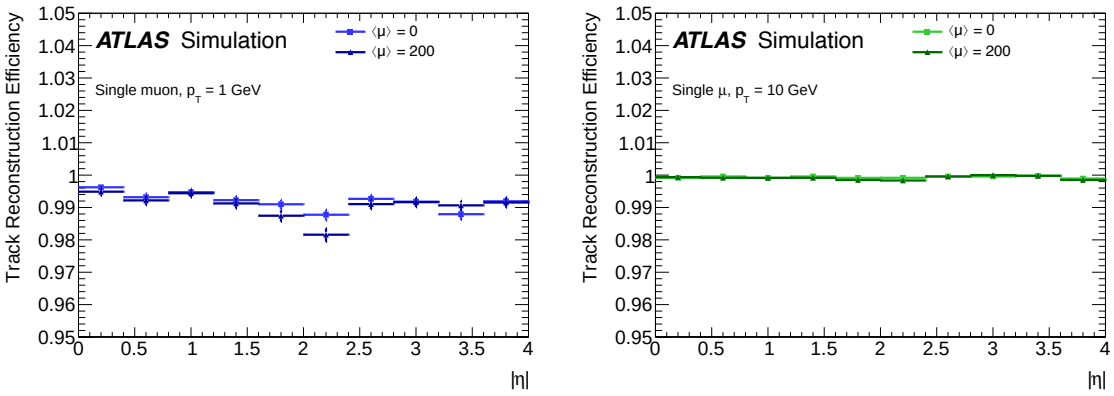


Figure 3.1: Tracking efficiency for muons without pile-up ($\langle\mu\rangle = 0$) and with an average of 200 pile-up events ($\langle\mu\rangle = 200$). **Left**: for $p_{\mathrm{T}} = 1$ GeV muons. **Right**: for $p_{\mathrm{T}} = 10$ GeV muons.

3.1 Tracking and Vertexing Performance

The basic tracking and vertexing performance using the ITk Detector is described in this section. Results are compared to the Run 2 detector. Results on clustering, local detector occupancies and technical aspects of the track reconstruction can be found in Sections 2.2.3 and 2.2.4.

3.1.1 Tracking Efficiency and Fake Rate

Two of the most important performance criteria for a tracking detector are efficiency and the rate at which "fake" tracks are reconstructed. Fake tracks are constructed from random associations of genuine clusters from tracks and (to a much smaller extent) noise hits. In particular, the large number of pile-up events at the HL-LHC could result in a reduced tracking efficiency or a significant increase in background contributions arising from these fake tracks.

The tracking efficiency is defined as the fraction of prompt particles which are associated with tracks passing a track quality selection. The particles considered must satisfy $p_{\mathrm{T}} > 1$ GeV and $|\eta| < 4.0$, and be produced by the primary interactions. Secondary particles produced in the Geant4 simulation are excluded.

For the efficiency calculation, tracks are required to have a high "probability" of matching to a truth particle satisfying the above cuts. The matching "probability", P_{match}, takes into account that a single track can have clusters that are generated by different particles, and is

defined [2] as:

$$P_{\text{match}} = \frac{2N_{\text{common}}^{\text{pix}} + N_{\text{common}}^{\text{strip}}}{2N_{\text{track}}^{\text{pix}} + N_{\text{track}}^{\text{strip}}} \tag{3.1}$$

where $N_{\text{common}}^{\text{pix/strip}}$ is the number of Pixel/Strip Detector clusters common[3] to both the track and the particle to which it is being matched, and $N_{\text{track}}^{\text{pix/strip}}$ is the number of Pixel/Strip Detector hits assigned to the track. The factor of 2 included for N^{pix} is a relative weight that takes into account that each pixel layer provides one 2D measurement of the track whereas a double sided strip layer provides two 1D measurements. A P_{match} value of 1.0 is found if all clusters of the reconstructed track are associated with the same truth particle, while a value of 50% implies that half the clusters are associated with a given truth particle while the other clusters are associated with one or more other truth particles. The tracking efficiency, ϵ_{track}, is defined as the number of selected reconstructed tracks matched to a selected truth particle (satisfying the above cuts) with $P_{\text{match}} > 0.5$, divided by the number of selected truth particles:

$$\epsilon_{\text{track}} = \frac{N_{\text{reco}}(\text{selected, matched})}{N_{\text{truth}}(\text{selected})} \tag{3.2}$$

Muons are not affected by hadronic interactions and hence their reconstruction efficiency is expected to be close to 100% over the full η range, provided the detector is hermetic and provides enough measurements to disentangle the tracking ambiguities. Figure 3.1 shows the efficiency ϵ_{track} for single particle simulation of muons with $p_{\text{T}} = 1$ and 10 GeV without and with an average of 200 pile-up events. As expected, the efficiency is very high without pile-up - this is merely a technical validation of the detector layout and the reconstruction chain. With an average of 200 pile-up collisions the additional combinatorial confusion in the track reconstruction stage results in only a very small degradation in ϵ_{track}, illustrating that the detector provides enough redundancy and precision to resolve the dense Phase-II event environment.

The efficiency to reconstruct pions and electrons is, unlike muons, limited by interactions of the particles with the detector material, leading to inelastic hadronic interactions or Bremsstrahlung, respectively. Hence, a reduction in detector material leads to a better efficiency to reconstruct pions and electrons. Figure 3.2 illustrates the number of nuclear interaction lengths traversed by a particle before reaching the reconstruction hit requirement in the ITk. For comparison the corresponding number of interaction lengths is also shown for the current Run 2 Inner Detector. After the upgrade, particles will have to traverse significantly less material, leading to a significantly better reconstruction efficiency, as shown in Figure 3.3. On the left, the efficiencies for single muons, pions and electrons

[2] Clusters without any truth information (noise hits and very low momentum particles from secondary interactions failing the truth cuts applied in Geant4) enter in $N_{\text{track}}^{\text{pix}}$ or $N_{\text{track}}^{\text{strip}}$ with a weigh factor of 0.5.

[3] That is the information in the simulation is used to ensure the hit is the same for the truth particle and the reconstructed track, i.e. the hit (truth) is common to the truth and reconstruction.

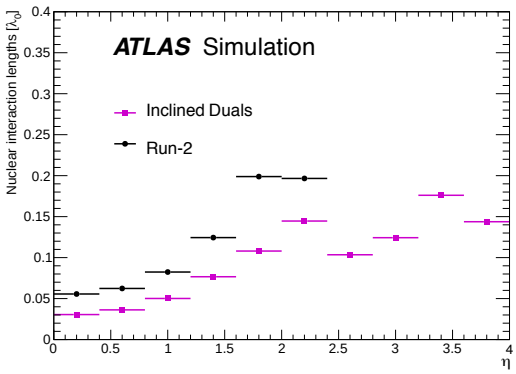


Figure 3.2: Number of nuclear interaction lengths seen by a particle as a function of pseudorapidity upto the position where sufficiently many detector layers have been crossed such that the reconstruction hit requirements are met.

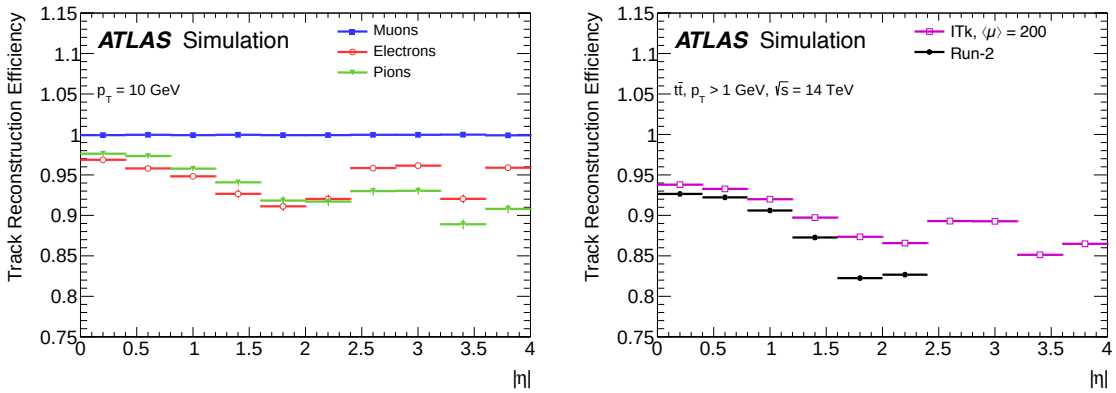


Figure 3.3: **Left**: Track reconstruction efficiency for single muons, pions and electrons with a constant transverse momentum of $p_{\mathrm{T}} = 10$ GeV. **Right**: Track reconstruction efficiency for a top-pair sample with an average of 200 pile-up events. Overlaid are the results for the current Run 2 detector.

of $p_{\mathrm{T}} = 10$ GeV are given. Shown on the right side of the figure is the reconstruction efficiency for $t\bar{t}$ events with an average of 200 pile-up events, compared to the current detector performance on Run 2 Monte Carlo. For the results shown in the figure, the electrons are reconstructed using the recovery technique for Bremsstrahlung in the pattern recognition and in track fitting [19].

The track reconstruction efficiency in the ITk is found to be stable to better than 1% for $t\bar{t}$ events with 40 to 250 pile-up, as shown on the left side of Figure 3.4 for different regions in η. For a fixed tracking efficiency, it is important to control the rate of fake or mis-reconstructed tracks. An inclusive measure for the rate of such fake or mis-reconstructed tracks is the ratio of the number of reconstructed tracks to the number of generated true particles. At a fixed tracking efficiency, problems in the track reconstruction would result

in an increase in this ratio as a function of pile-up. As can be seen on the right side of Figure 3.4, the ratio does not vary over the full range of pile-up studied between 40 and 250 by more than 1% for all η regions. The ratio is in general higher than the tracking efficiency itself, indicating that additional tracks are reconstructed with a p_{T} above 1 GeV. Several of these additional tracks are due to secondaries from particles interacting in the material of the tracker. Because of the limited momentum resolution, the dominant contribution to the additional reconstructed tracks in the forward region is due to mis-measured low-p_{T} tracks that have a reconstructed transverse momentum above 1 GeV.

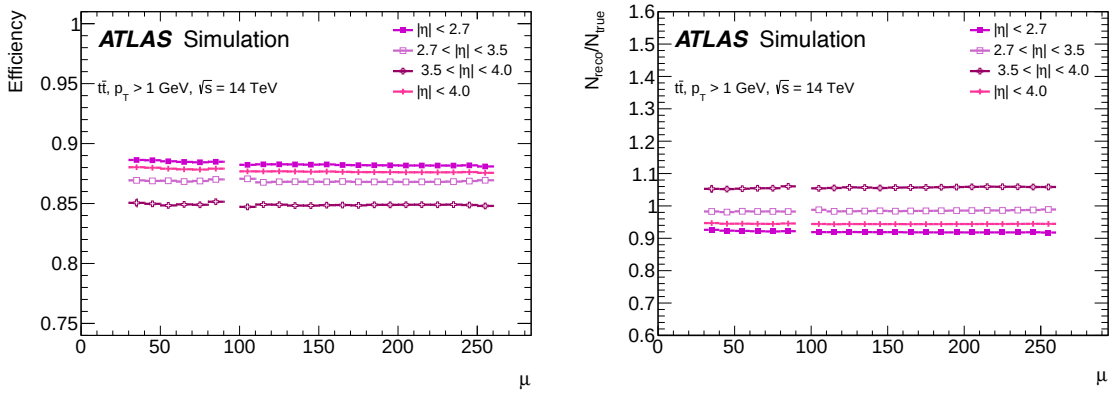


Figure 3.4: **Left**: Tracking efficiency. **Right**: Ratio of reconstructed tracks to generated charged particles. In both cases, the results are shown as a function of pile-up for $t\bar{t}$ events for pile-up μ between 40 and 250, for different regions in η.

Figure 3.5 shows a second measure of a "fake rate", this time defined using the Geant4 truth. The rate of tracks without a matching truth particle using the P_{match} criterion is shown. The ITk results are compared to the Run 2 detector performance with the standard "loose" and "tight" track selection [20]. Despite a factor 10 more in average pile-up, the ITk is outperforming the Run 2 detector in terms of fake rates; this is due to the enlarged lever arm and higher granularity on the Pixel and Strip Detectors. In addition, increasing the hit requirement in reconstruction in the central pseudorapidity region from 7 (loose selection for the Run 2 detector) to 9 hits (for the ITk and for the tight selection for Run 2 detector) allows more fakes to be removed.

Based on the above studies, it was concluded that within the pseudorapidity acceptance of the Strip Detector, a minimum of 9 pixel or strip hits is required to ensure the pattern recognition is robust against pile-up for a fully efficient detector (without any simulated defects or irradiation effects), and to ensure fake tracks are well controlled. In the forward region this requirement is loosened to 7 hits (all pixels), see Table 2.5.

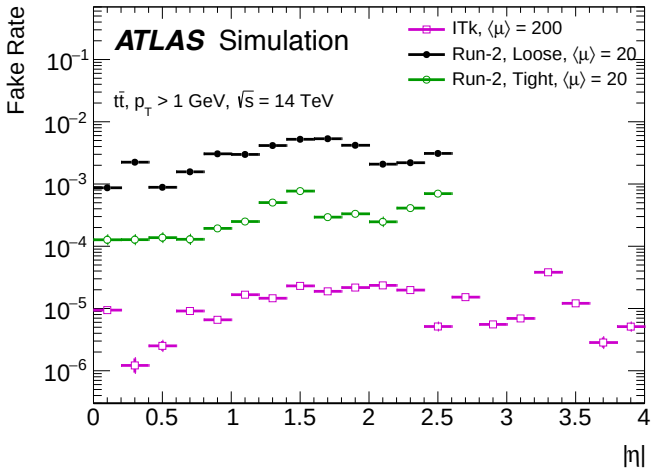


Figure 3.5: Fake rate for reconstructed tracks in $t\bar{t}$ events with $\langle\mu\rangle = 200$ using the truth particle matching criterion P_{match} as define in the text. ITk is compared to the Run 2 detector results for two different levels of track selection (loose and tight, see text for details).

3.1.2 Track Parameter Resolutions

The precise measurements provided by the Pixel Detector define the transverse (d_0) and longitudinal (z_0) impact parameter resolutions of tracks with respect to the primary interaction vertex position (see Section 3.1.6) and the polar (θ) and azimuthal angles ϕ at the vertex. The Pixel Detector adds significantly to the lever-arm for measuring the transverse particle momentum p_{T} from the curvature of the track. The resolutions of these parameters directly determine the performance of the detector in terms of its capability for b-tagging and lepton or jet reconstruction. The resolutions for these parameters are obtained from simulation by comparing their reconstructed values for a given particle with the truth value. The tracks used to calculate the resolution are required to pass the same selection criterion as for the efficiency calculation. Tracks must be matched to a truth particle with $P_{\text{match}} > 0.5$. The resolutions on the track parameters are obtained from the RMS of the core of the distribution of the difference between the reconstructed and true values of the parameters.

Figure 3.6 shows the track parameter resolutions for a detector with 50×50 μm^2 pixels and digital clustering. These are shown for single muons with different p_{T} values. For tracks with p_{T} of 100 GeV, the intrinsic d_0 resolution of the detector dominates over the multiple scattering term, and a resolution of around 10 μm is achieved for $|\eta| < 3.0$. It is worse than the resolution of the Run 2 detector, for which analogue clustering is used and which has a smaller radius of the first pixel layer compared to the ITk (necessary due to the harsh radiation environment in Phase-II, as discussed in Section 2.3). For lower p_{T} values, multiple scattering contributes significantly and the values for the ITk are very comparable to the Run 2 detector for the d_0 resolution for $|\eta| < 2.5$. At large η, the resolution remains good, indicating that useful information will be provided by these tracks, e.g., for pile-up

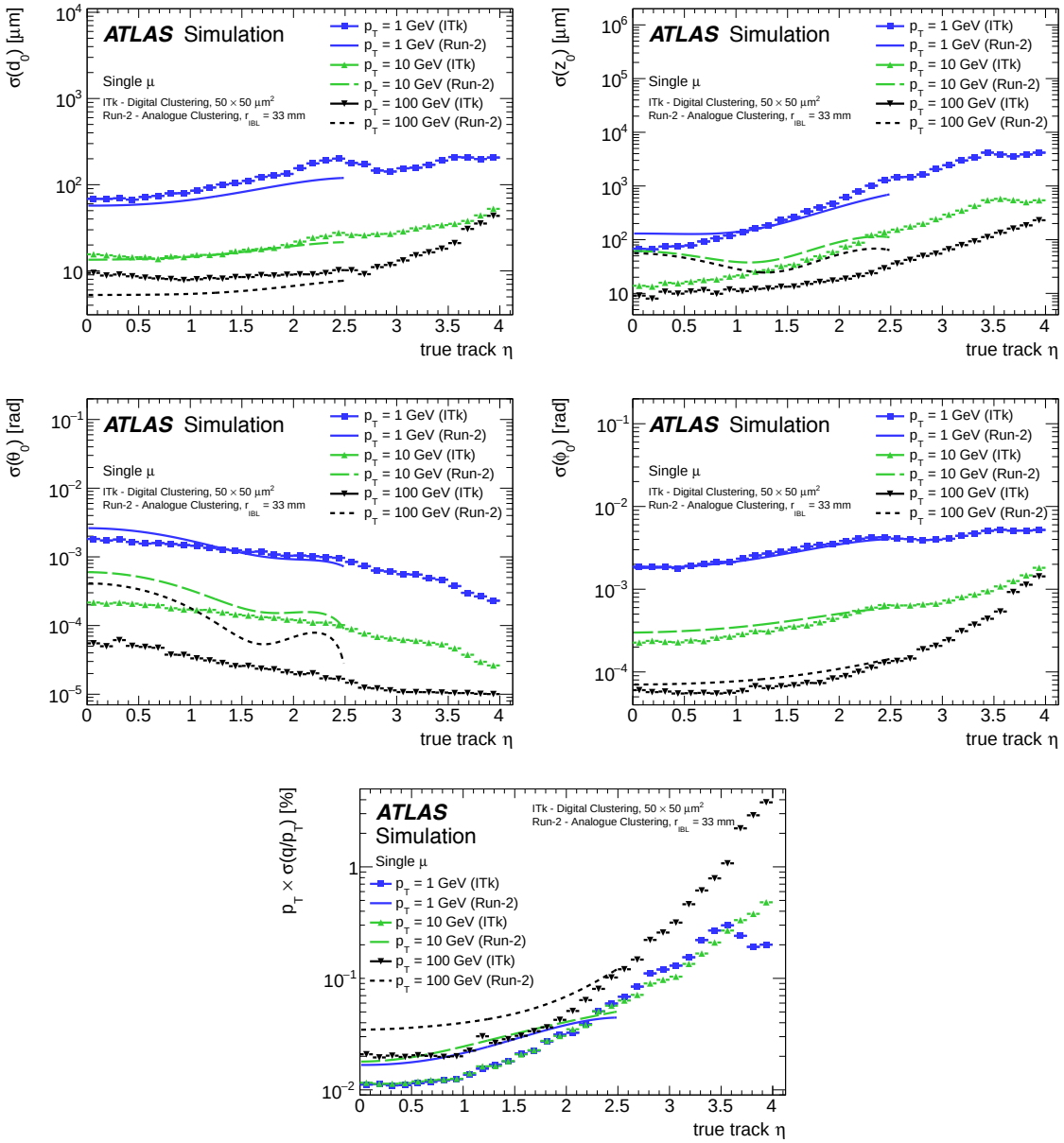


Figure 3.6: Track parameter resolution in d_0, z_0, θ, ϕ and p_{T} as a function of η for an ITk Pixel Detector with 50×50 $\mu\mathrm{m}^2$ pixels. Results are shown for single muons of 1, 10 and 100 GeV in p_{T}. The reconstruction uses digital clustering information. For comparison, the resolutions for the current Run 2 Inner Detector are also shown.

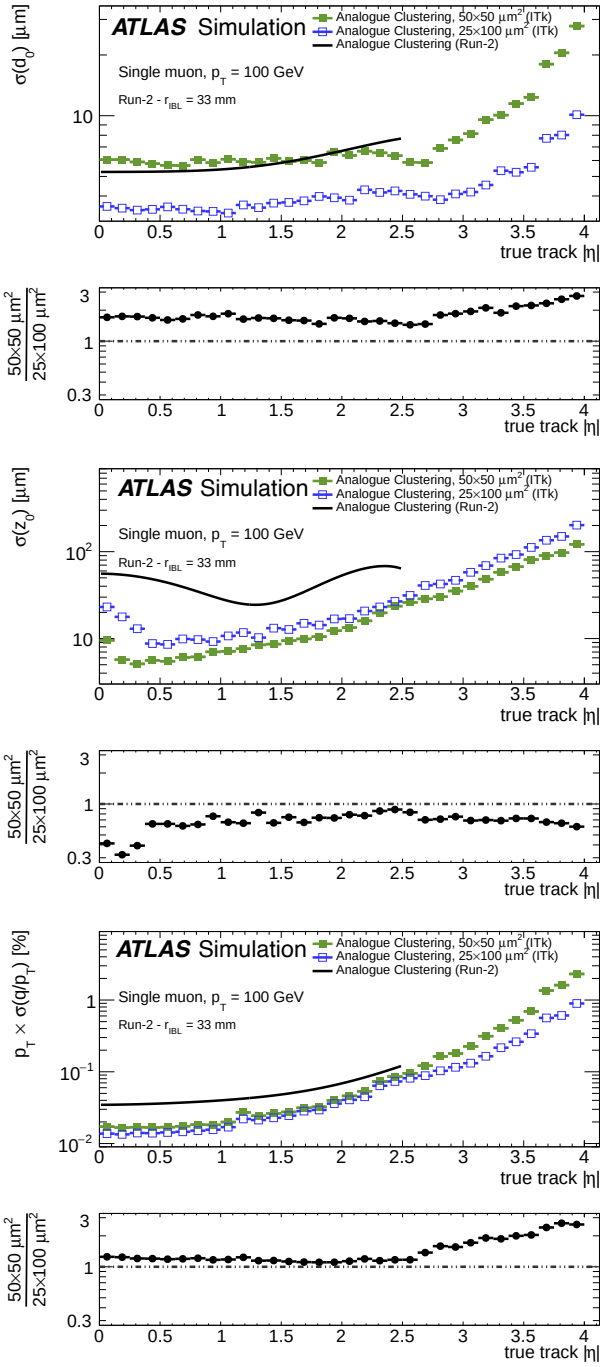


Figure 3.7: Track resolutions achieved with analogue clustering and different pixel pitches. Track parameter resolution in (**top**) d_0 and (**middle**) z_0 as a function of η for the ITk for muons with 100 GeV in p_{T}. **Bottom**: Relative p_{T} resolution with 50×50 $\mu\mathrm{m}^2$ and 25×100 $\mu\mathrm{m}^2$ pixels for 100 GeV muons. For comparison, the resolutions for the current Run 2 Inner Detector are shown. The ratio in the lower part of the plots is defined as the results using 50×50 $\mu\mathrm{m}^2$ pixels over those obtained using 25×100 $\mu\mathrm{m}^2$ pixels.

jet rejection and b-tagging purposes. The z_0 resolution is significantly better for ITk than for the Run 2 detector at all values of p_T, primarily due to the decreased pixel pitch in the z direction. In particular in the central region, the current pitch of 250 μm in the inner pixel layer (IBL) limits the resolution. This improvement is motivated by the necessity to improve the pile-up rejection capabilities of the tracker for Phase-II by identifying the primary vertex. The momentum resolution is nearly a factor 2 better in the ITk than in the Run 2 Inner Detector, primarily due to the higher precision of the strip tracker compared to the TRT, and due to the reduced material. It degrades towards the forward region, mostly due to the fact that the solenoid field in this region is weaker and the transverse path length of the tracks gets shorter.

Resolutions using analogue clustering described in Section 2.2.3 are shown in Figure 3.7. The top and middle plots illustrate the effect of different pixel sizes on the d_0 and z_0 impact parameter resolution, respectively, as a function of η for single muons at 100 GeV. As can be seen in the figure, the ITk with both 50×50 μm^2 and 25×100 μm^2 pixel sensors outperforms the current detector. The d_0 resolution with 25×100 μm^2 pixels is improved by nearly a factor 2 over the full η range, at the cost of about 35% loss in z_0 resolution. The bottom plot in Figure 3.7 shows the corresponding comparison for the p_T resolution obtained using analogue clustering and the two pixel sizes. With 25×100 μm^2 pixel sensors the momentum resolution in the barrel region is improved by 20%, while in the forward region an improvement of more than a factor 2 can be achieved.

The results presented in the following sections are based on Monte Carlo samples produced using 50×50 μm^2 pixels and digital clustering.

3.1.3 Alignment Studies

The resolution studies presented in the previous section have assumed perfect detector alignment. However, in reality, module and structural misalignment will degrade the measurement accuracy and have to be considered. Misalignments can appear on different levels, from large structural misplacements, to mis-positioning of assemblies or component deformation, to individual module placements. Additionally, sensor deformations can be regarded as misalignments as they cause a degradation of the resolution. The ATLAS Inner Detector alignment procedure is an iterative track alignment using tracks to minimise a global multidimensional χ^2 function and has shown great performance throughout the data taking campaign [21]. For Run 2 data taking, the time-dependent change of the IBL during a single fill required a dedicated alignment procedure that is able to correct for short-term detector movements within a run of the LHC.

Global placements are corrected for by the alignment procedure, while short-term detector instabilities within a data taking run are more difficult to correct for and remaining uncertainties may affect detector resolutions. Two types of instabilities are studied here: First, a

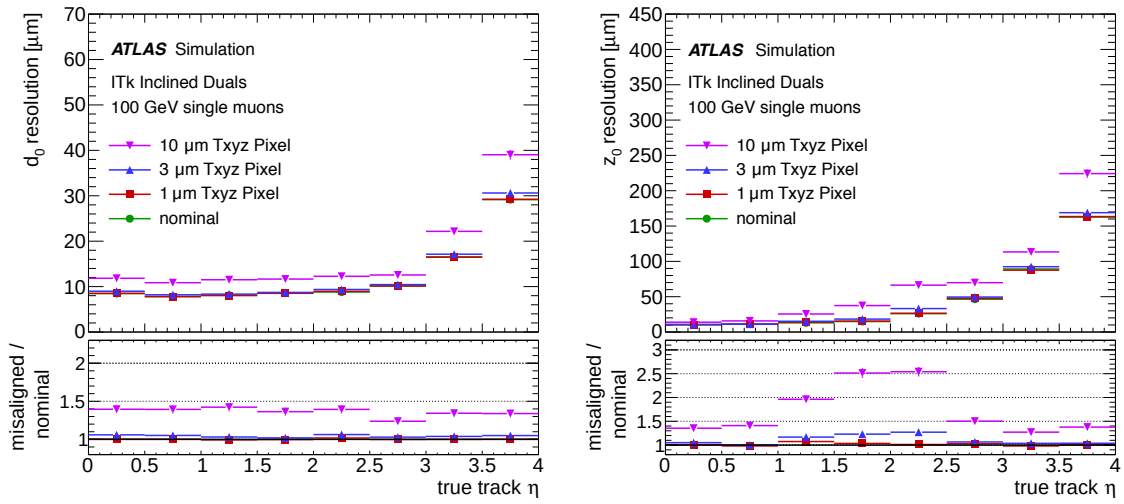


Figure 3.8: Change in impact parameter resolution for single muons with $p_{\mathrm{T}} = 100$ GeV, applying a random misalignment of 1, 3, and 10 μm RMS to all pixel modules in all three local module dimensions. **Left**: Change of transverse impact parameter resolution $\sigma(d_0)$. **Right**: Change in longitudinal impact parameter resolution $\sigma(z_0)$.

random local misalignment at the module level, and second, a global deformation of the entire inner barrel structure.

Figure 3.8 shows the effect of 1, 3, and 10 μm (RMS) random displacements of all modules in all three directions on the d_0 and z_0 impact parameter resolutions. No tilt or twist to the original module orientation has been applied. As these misalignments are small compared to the uncertainty from multiple scattering in the low momentum region, the resolution for low-momentum particles is little affected. Therefore, in the figure, results are shown only for muons with $p_{\mathrm{T}} = 100$ GeV. Misplacements of 3 μm do not lead to a significant degradation in the resolution, while 10 μm misplacements lead to a loss of resolution by a factor 1.4 in d_0 and up to a factor 2.5 in z_0 at $\eta = 2$, respectively.

The z_0 resolution is sensitive to misalignments in the tilt angle of the inclined modules, as shown in Figure 3.9. In this study the inclined modules are rotated around the R_x axis by randomly drawing tilt angles from a Gaussian distribution with $\mu = 0$ mrad and $\sigma = 1, 3, 10$ mrad. Similar to the random misalignments, tilts up to 3 mrad do not alter the resolution significantly, while 10 mrad degrade the resolution in the forward region by up to a factor 1.4 in z_0. The d_0 resolution is not affected significantly by the tilt changes studied here.

Both global deformations and misplacements of the detector affect the impact parameter resolution. Figure 3.10 shows the resulting changes in the resolution caused by deforming the long pixel barrel staves. The staves have been bent upwards at the ends by 10, 20, 30 μm, while leaving the positions at $z = 0$ cm unchanged. As expected, the resolutions at

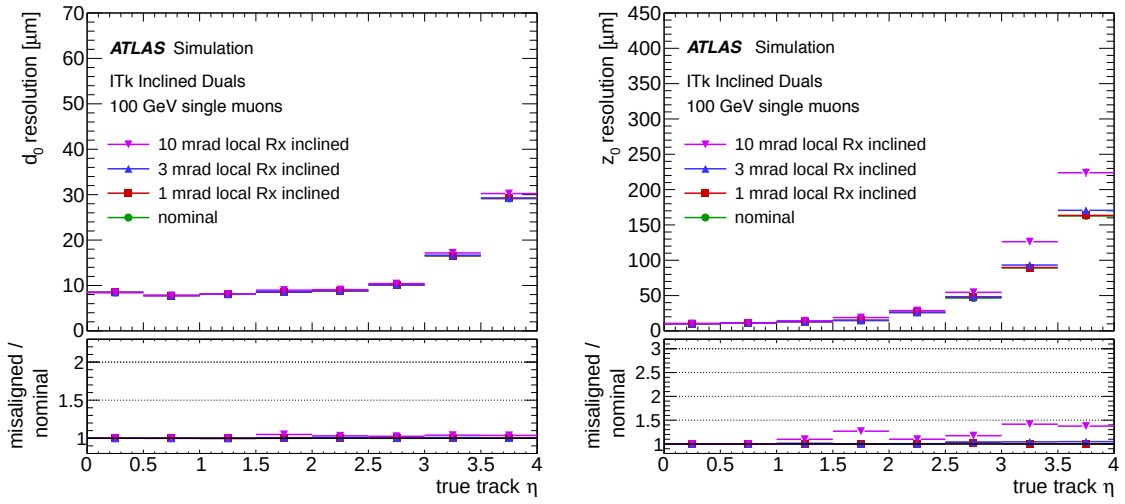


Figure 3.9: Change in impact parameter resolution compared to perfect alignment for single muons with $p_{\mathrm{T}} = 100$ GeV when randomly changing the module tilt angles (R_x) of all inclined pixel modules by 1, 3, 10 mrad RMS. **Left**: Change of transverse impact parameter resolution $\sigma(d_0)$. **Right**: Change in longitudinal impact parameter resolution $\sigma(z_0)$.

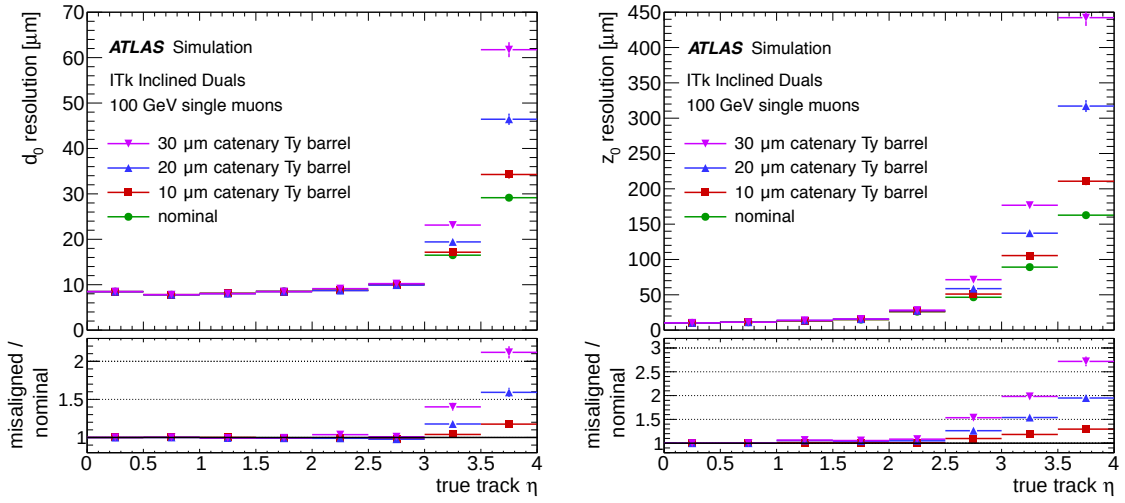


Figure 3.10: Change in impact parameter resolution for single muons with $p_{\mathrm{T}} = 100$ GeV when bowing the ends of the pixel staves outwards by 10, 20, 30 μm. **Left**: Change of transverse impact parameter resolution $\sigma(d_0)$. **Right**: Change in longitudinal impact parameter resolution $\sigma(z_0)$.

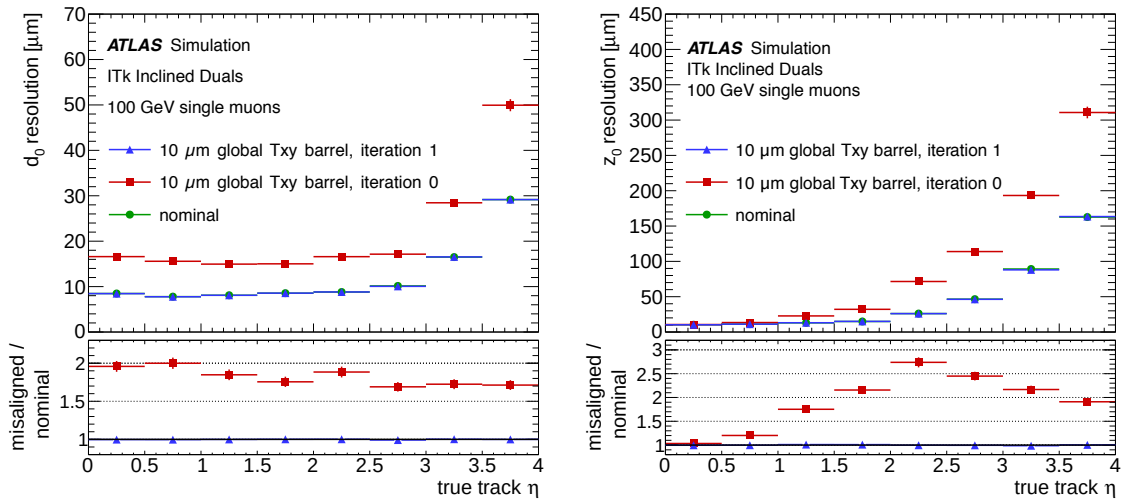


Figure 3.11: Alignment study, showing the effect of a global 10 μm displacement of the pixel system in x and y on the impact parameter resolution for single muons with $p_{\mathrm{T}} = 100$ GeV, before (iteration 0) and after (iteration 1) realignment. **Left**: Change of transverse impact parameter resolution $\sigma(d_0)$. **Right**: Change in longitudinal impact parameter resolution $\sigma(z_0)$.

high η are significantly degraded by such distortions, illustrating that these need to be well controlled by the alignment procedure. Figure 3.11 shows the results of an alignment study for a global 10 μm displacement of the pixel system in x and y, illustrating the effect of such a misplacement on the impact parameter resolution and how the alignment procedure can completely recover the nominal resolution.

3.1.4 Detector Performance Stability with Ageing and Component Failures

A goal of the ITk Detector layout design is to provide robust tracking in presence of eventual detector defects. Two types of detector defects that affect track reconstruction performance have to be considered:

- Component failures during operations, that lead to inactive modules, are known and can be described in the conditions database of the detector. They are referred to as "known detector inefficiencies".
- Detector inefficiencies leading to loss of hits, in particular due to irradiation that affects single channels, are referred to as "unknown inefficiencies".

Depending on the size of a cluster, detector channel inefficiencies can result in loosing a measurement or in biasing the position estimate in the clustering. From point of view of track reconstruction, both effects are decremental to performance. Biases in position estimates affect the track resolution and the can result in flagging clusters as outliers in the

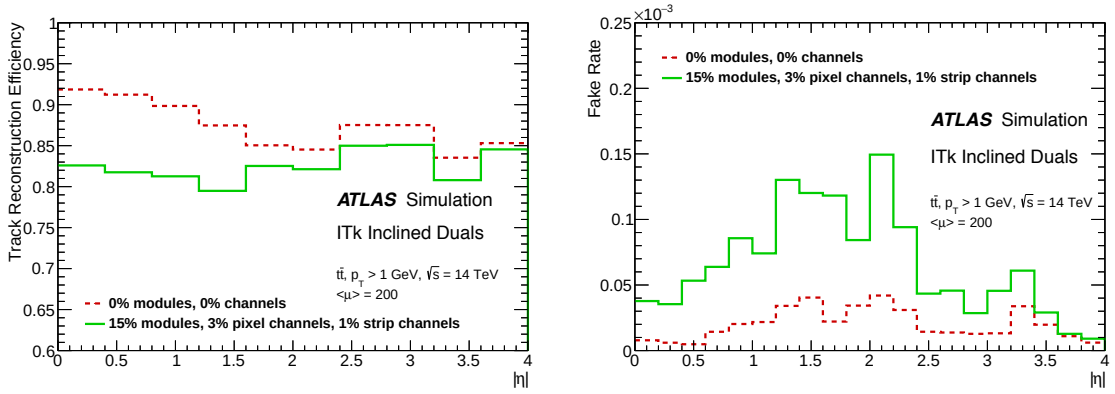


Figure 3.12: **Left**: Track reconstruction efficiency for ITk with and without 15% inactive modules and a rate of 3% and 1% random channel inefficiencies for pixel and strip sensors, respectively. **Right**: Fake rate for a detector with and without defects. Show are results as a function of η for $t\bar{t}$ events with an average of 200 pile-up events.

track fit. A lost cluster results in a hole on the track, an active module where no hit is found during reconstruction. Such a loss of a measurement in the innermost layers is particularly harmful, as the process noise from multiple scattering and energy loos still affects the impact parameter resolution. Lost clusters change the measurement arrangement and therefore influence the track reconstruction performance. They eventually lead to inefficiencies, because the pattern recognition can not explicitly allow for the effect of randomly lost clusters and track candidates may fail the selection cuts.

Inactive modules are rather easy to treat in track finding to limit the detrimental effects on performance. Permanent or temporary component failures are flagged in the conditions database and this information is used at reconstruction time. When a track candidate is built and crosses an inactive module, the missed measurement is not counted as a hole, but rather as a valid measurement on the track. The strategy to count an inactive module as a fully efficient measurement has been chosen in order not to penalise tracks in detector regions where many inactive modules are present. However, it can only be applied in a robust way to modules between the first and the last actual measurements on a track in order to avoid biases in the track length. Loosing measurements on inactive modules as well results in a worse resolution for the trajectory following, that can lead to an increase rate of pattern recognition mistakes, negatively affecting the tracking performance. For the Strip Detector, the space points used for track seeding are computed from the measurements from the modules on both sides of a barrel stave or end-cap petal. Loosing a module on one side will result in loosing the space point and therefore affects the seeding efficiency for track finding.

A case study is done to demonstrate the robustness of the track reconstruction against detector defects. For this study, both types of detector defects are considered. The efficiency of irradiated pixel and strip sensors is expected to be above 97% (see Section 5) and 99% [1],

respectively. This inefficiency is modelled as a random dead channel inefficiency in simulation. The design criteria for the detector layout is that tracking should be robust against loosing up to two measurements due to component failures. Hence, 15% of the pixel and strip modules are marked as inactive in reconstruction, corresponding to an average loss of two measurements. The same track reconstruction software is used for the samples with and without detector defects. Figure 3.12 shows the effect of the detector defects implemented for this case study on the track reconstruction efficiency and the fake rate for $t\bar{t}$ events with an average of 200 pile-up interactions. A loss of up to 10% in tracking efficiency is observed in the central region of the detector, while in the forward region the reconstruction is found to be less sensitive. As expected, the rate of fake tracks is increasing in the sample with detector defects.

3.1.5 Tracking in Dense Environments

The reconstruction of particle trajectories proves particularly difficult in dense environments. Boosted jets or decay particles from boosted objects create a higher local hit density than caused by general pile-up activity, ultimately resulting in a situation where distances between particles on the innermost measurement layers become smaller than the channel size and measurements become merged. These merged clusters usually appear as shared measurements on more than one track candidate, which is penalised by the ambiguity solving method which attempts to suppress track duplicates and minimise track mis-measurements. When they are correctly identified as a cluster created by more than one particle, these measurements can still be used to find close-by tracks and thus increase the double-track resolution. In Run 1 and Run 2, neural networks have been successfully used to identify and eventually refine the cluster information from merged clusters [22, 23]. The ability to recover analogue information from the individual pixels is critical in refining the information about the charged particle trajectories adding to a merged cluster. For the studies presented here, a digitisation model is not yet available and the performance of the neural network is emulated using truth information constructed under the assumption that an ITk pixel behaves in the same way as a pixel in the ATLAS IBL, as both have a 4-bit read-out for the time-over-threshold information.

Figure 3.13 shows the efficiency for reconstructing the three tracks in the τ 3-prong decay channel, versus the momentum of the τ. Compared are the results when allowing cluster splitting on different subsets of layers. The efficiency to reconstruct τ decays at high-p_{T} will be significantly improved by benefiting from the high pixel granularity and the analogue cluster information on all pixel layers.

The track reconstruction efficiency for tracks in jets is shown for five ranges in $|\eta|$ in Figure 3.14, for which $Z'(5\ \mathrm{TeV}) \rightarrow t\bar{t}$ events with a average of 200 pile-up events have been used. The top two plots show the track reconstruction efficiency as a function of the jet transverse momentum and pseudorapidity, comparing ITk and the current detector performance. While the current detector shows a significant loss of efficiency for high-p_{T} jets

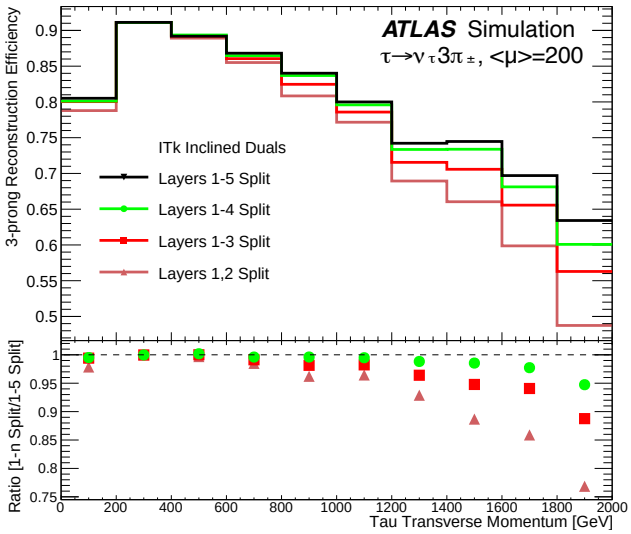


Figure 3.13: τ reconstruction performance versus τ momentum in the 3-prong decay channel. Different read-out scenarios are shown. "Layers 1,2 Split" denotes cluster splitting in the two innermost layers, "Layers 1-3 Split" in the inner three and so on. Results are obtained for a 50×50 μm^2 pixel size.

in this boosted topology, a similar degradation is not observed for the ITk, thanks to the improved sensor granularity and the enlarged lever arm of the 5 pixel layers. The bottom plots of Figure 3.14 illustrate how the tracking efficiency depends on the local track density. Here the efficiency is shown as a function of the distance ΔR in η and ϕ with respect to the jet axis for jets with a minimum p_{T} of 500 GeV from $Z'(5\ \mathrm{TeV}) \rightarrow t\bar{t}$ events with 200 pile-up. While for the Run 2 detector there is a significant degradation in the core of the jets, the efficiency for ITk remains stable over the full range of ΔR shown on the plots.

The rate of wrong associations of hits to tracks depends on the local hit density. In particular in the core of high-p_{T} jets this density is expected to increase rapidly, leading to a higher rate of tracks with a bad track matching "probability" $0.5 < P_{\mathrm{match}} < 0.8$ calculated from the simulation truth of the associated hits. In Figure 3.15 the rate of bad matching tracks is shown for high-p_{T} jets in $Z \rightarrow t\bar{t}$ events. As shown in the top left plot, for the ITk the rate of bad matching tracks is dominated by the hit density from the jet itself, receiving only small additional component due to pile-up, even up to an average pile-up of 200 events. The top right plot shows the bad match rate as a function of η for the ITk, compared to the results for the current Run 2 detector. The bottom plot shows the results as a function of ΔR for the ITk and for the current Run 2 detector, illustrating the expected dependence of the bad matched rate depends strongly on the distance of the track from the core of the jet. The ITk is able to resolve such dense hit topologies in the core of jets with a much reduced rate of pattern recognition mistakes, thanks to its increased granularity and the longer lever arm of the Pixel and Strip Detectors, compared to the current ATLAS Inner Detector.

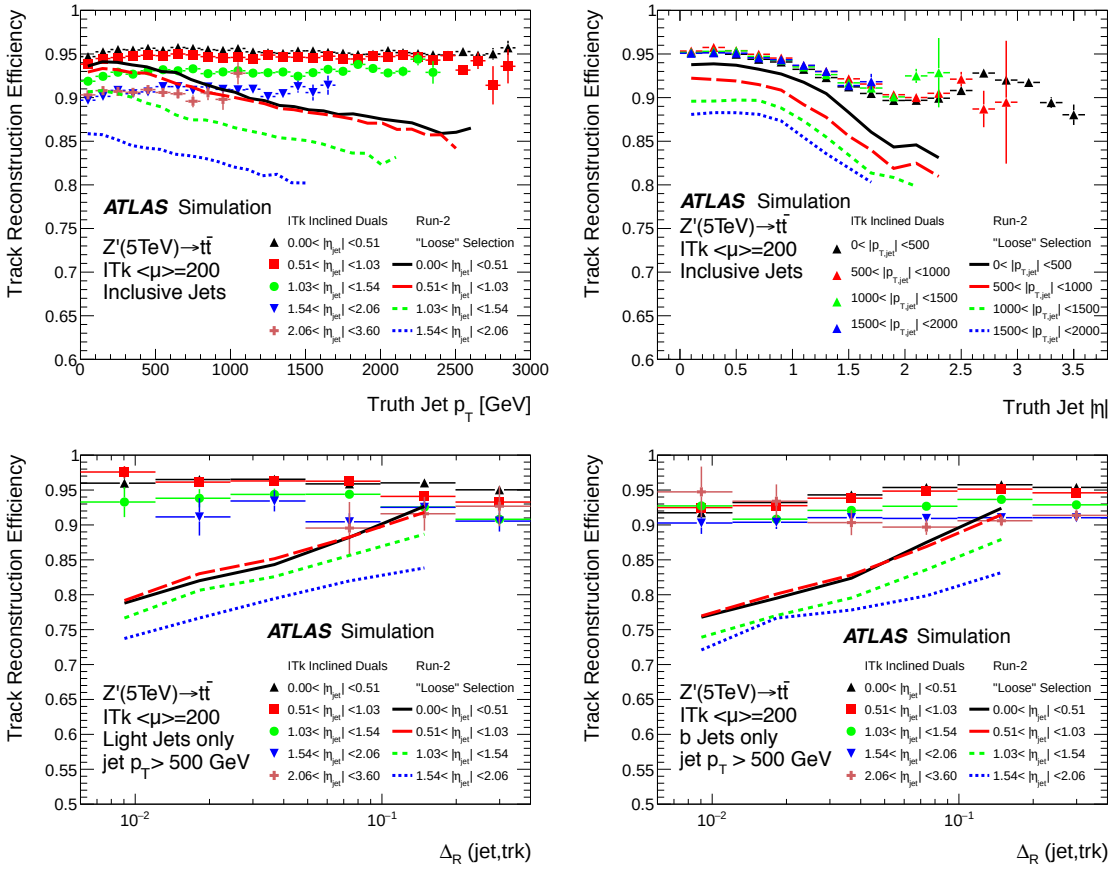


Figure 3.14: Reconstruction efficiency for tracks in jets from $Z'(5\text{ TeV}) \rightarrow t\bar{t}$ events with an average of 200 pile-up events. The results are shown for different regions in η and 50×50 μm^2 pixel size. **Top**: Track efficiency as a function of jet p_{T} (**left**) and $|\eta|$ (**right**). **Bottom**: Efficiency as a function of the distance ΔR in η and Φ of the track from the jet core for jets above 500 GeV in p_{T}, for light (**left**) and b jets (**right**), respectively.

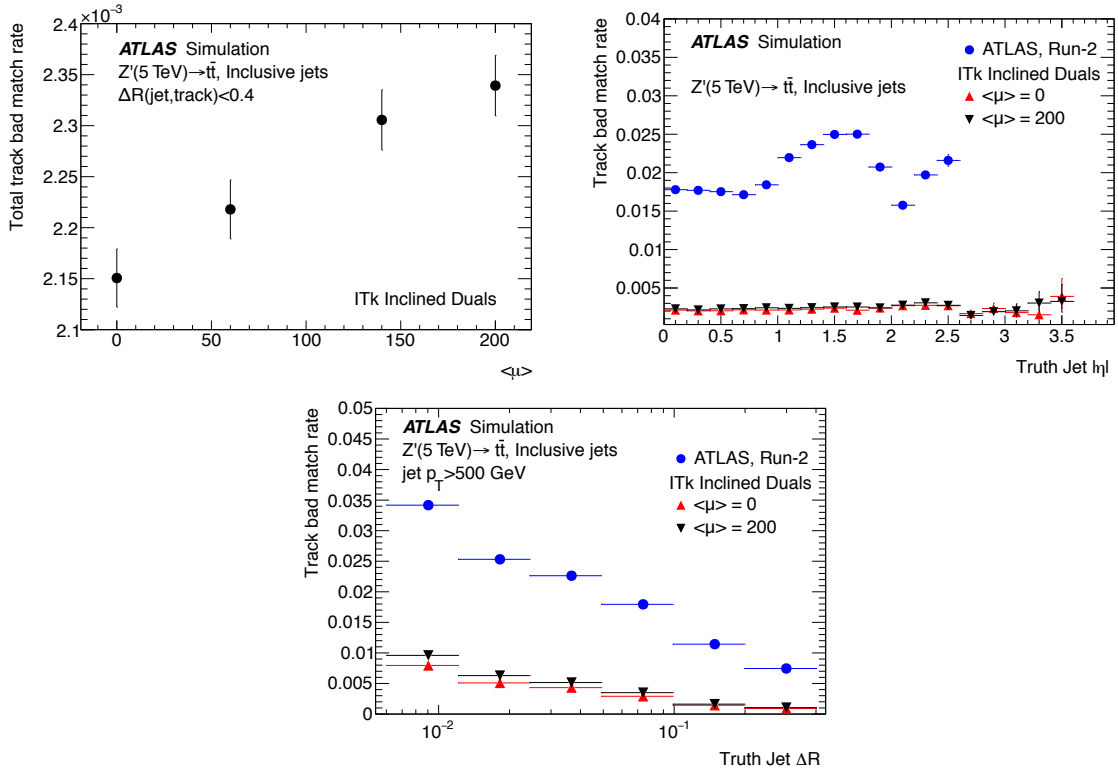


Figure 3.15: Rate of wrong associations of hits to tracks in high-p_{T} jets, leading to bad matching probabilities ($0.5 < P_{\mathrm{match}} < 0.8$). Results are for jets in $Z' \to t\bar{t}$ events. Shown is the rate of bad match tracks as a function of the average pile-up (**top left**) and as a function of $|\eta|$ (**top right**) for all tracks with a $\Delta R < 0.4$. The dependence of the bad match rate on ΔR is shown in the **bottom** plot for different average pile-up. The Run 2 result are for a sample with an average pile-up of 23.

3.1.6 Primary Vertex Reconstruction

The tasks of the primary vertex reconstruction are to find and to determine the positions of the hard-scatter and pile-up interaction vertices in collision event. Input to the primary vertex finding are the reconstructed tracks, the beam spot position and shape for each period in an LHC run. This strongly constrains the vertex positions in the transverse plane. For this study, a Gaussian shaped beam spot is assumed with a sigma of 12 μm in x and y and of 5 cm in z.

For Run 2, the primary vertex reconstruction is performed using the so-called Iterative Vertex Finder procedure which calls an Adaptive Vertex Fit as a robust fitter to determine the vertex position from a list of tracks for a given vertex candidate [24]. For the studies discussed in this section, the Adaptive Multi-Vertex Finder (AMVF) [25] was used, which deploys the same adaptive vertex fitting technique, but fits for N vertices in parallel to take into account the vertex structure of the event and to allow for tracks being compatible with multiple vertices. The AMVF was found to significantly improve the primary vertex

reconstruction performance at the high pile-up environment expected at Phase-II and is therefore used as the baseline for ITk.

Only a subset of all reconstructed tracks are input to the primary vertex finding. In addition to the track selection cuts applied in reconstruction (see Table 2.5), the following cuts are applied to ensure good impact parameter resolution:

- The impact parameter resolution in the forward region is limited by multiple scattering. A minimal p_{T} cut of 0.9 GeV is applied for tracks at all η to reject soft forward tracks.
- Each track is required to have at least 3 pixel clusters.
- Tracks are required to have $\sigma(d_0) < 0.3$ mm and $\sigma(z_0) < 0.5$ mm in order to ensure good precision. This cut effectively removes low-p_{T} forward tracks because of their limited resolution.

The AMVF uses a vertex seed finder to identify candidate vertices along the beam-line in z:

- In an iterative procedure, a new candidate vertex is added to the pool of vertex candidates handled by the adaptive Kalman filter multi-vertex fit, together with all tracks matching the vertex candidate.
- All vertices are refitted by means of the adaptive Kalman filter multi-vertex fit, where each track can contribute to several vertices. Tracks with a low adaptive weight in the fit are removed from the fit of a given vertex.
- The new vertex candidate is retained, if the vertex is found with more than 2 tracks, the sum of the adaptive weights is not too low and the new vertex is more than 3 sigma way from any other candidate.
- The procedure is repeated, until there are no more vertex candidates or the maximum number of iterations is exceeded.

The number of reconstructed vertices as a function of pile-up is shown in Figure 3.16 for $t\bar{t}$ events with a pile-up values μ between 30 and 270. At a constant efficiency, the number of reconstructed vertices is expected to depend linearly on pile-up, while vertex merging (and splitting) effects need to be taken into account. As an illustration, a linear fit to the number of vertices for pile-up values between 40 and 100 is superimposed on the figure and extrapolated to higher pile-up values. At typical Phase-II pile-up levels there is a significant deviation from a linear dependence, indicating that vertex merging effects are present in the result. Shown as well are the results for the Run 2 sample using the Run 2 vertex finding software, which has a lower pile-up vertex efficiency, as can be seen from the different slope vs μ.

Figure 3.17 shows the transverse ($r = \sqrt{x^2 + y^2}$) and longitudinal (z) primary vertex resolution for $t\bar{t}$ events with an average pile-up of 200 events as a function of the true local

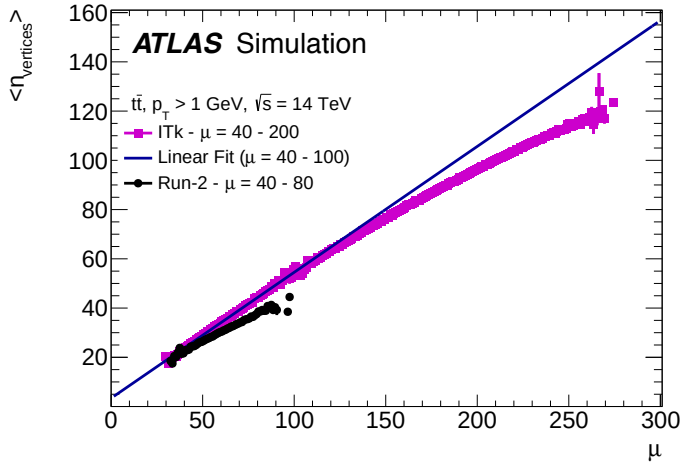


Figure 3.16: The number of reconstructed primary vertices as a function of pile-up for $t\bar{t}$ events with a pile-up between 30 and 270. Results are shown for a pixel size of 50×50 μm^2. As an illustration a linear fit to the number of vertices for pile-up values between 40 and 100 is shown, extrapolated up to 270 pile-up. Shown as well are results for a Run 2 simulation sample using the Run 2 primary vertex reconstruction code.

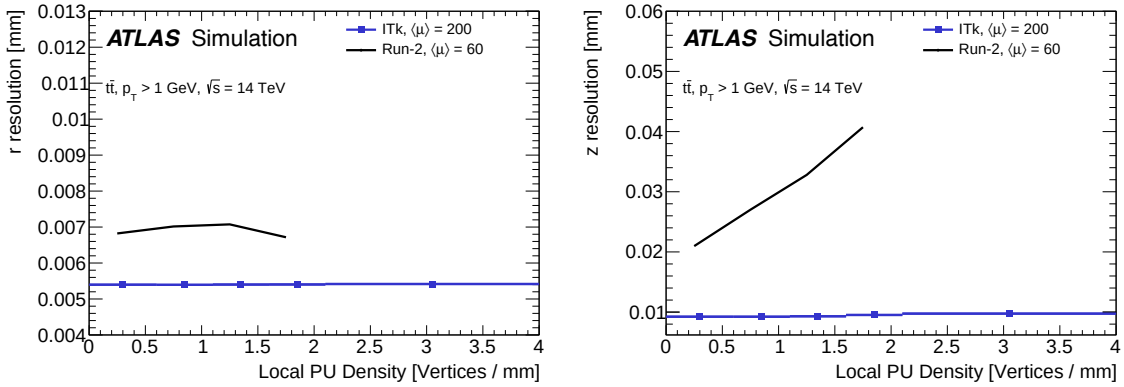


Figure 3.17: The transverse and longitudinal primary vertex resolution calculated as the difference between the reconstructed position coordinates (**left**) r and (**right**) z and their generator-level values, as a function of the pile-up density. Results are shown for $t\bar{t}$ events, a pixel size of 50×50 μm^2 and digital clustering. The radial position coordinate is $r = \sqrt{x^2 + y^2}$. Only hard-scatter vertices are considered. Shown as well are results for a Run 2 simulation sample using the Run 2 primary vertex reconstruction code.

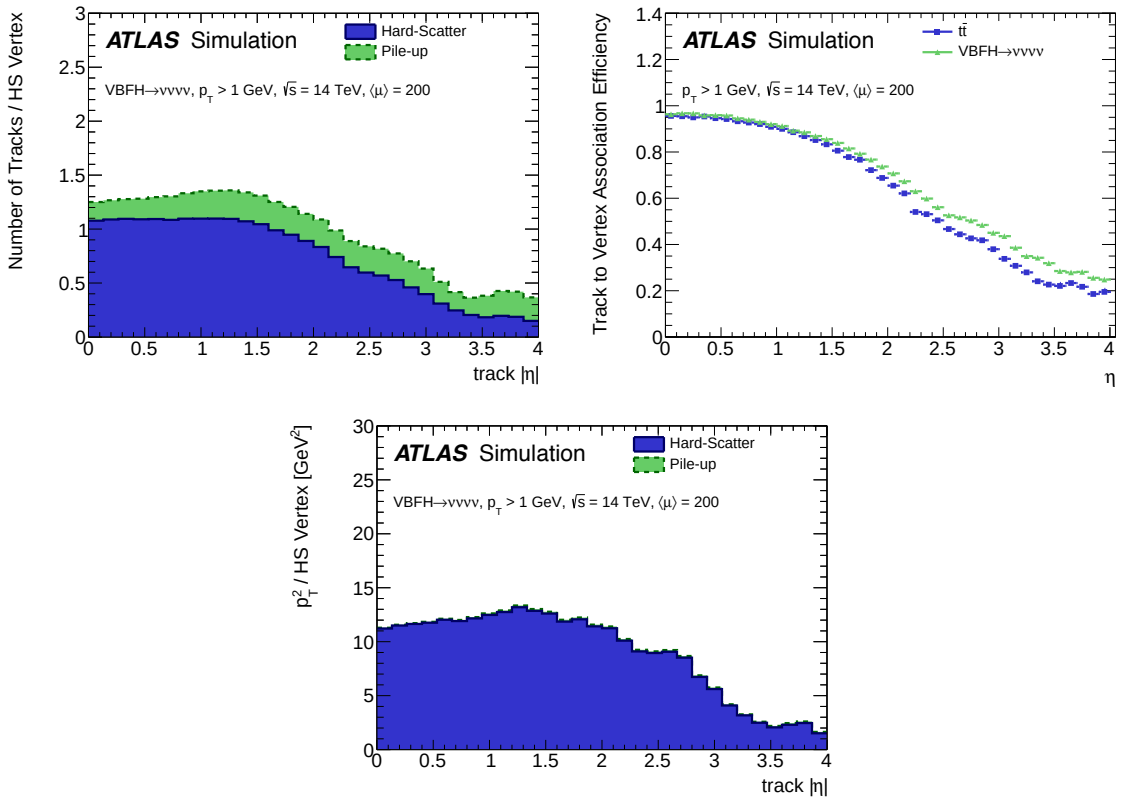


Figure 3.18: **Left**: The number of tracks in VBF $H \to \nu\nu\nu\nu$ events as a function of $|\eta|$ that are associated in the fit to the hard-scattering vertex in the AMVF fit. The tracks from the hard-scattering and pile-up interactions are shown separately, normalised to the number of events. **Right**: The efficiency to associate tracks in the fit to the hard-scattering vertex, for VBF $H \to \nu\nu\nu\nu$ and $t\bar{t}$ events. **Bottom**: The sum of the p_{T}^2 as a function of $|\eta|$ for the tracks associated to the hard-scattering vertex in VBF $H \to \nu\nu\nu\nu$ events. Results are shown for 50×50 $\mu\mathrm{m}^2$ pixels and digital clustering.

pile-up density in a ± 2 mm window around the primary interaction. There is nearly no local pile-up dependency in the resolution of the primary vertex for the ITk reconstructed with the AMVF, despite an increased probability for merging nearby pile-up vertices into the primary vertex. For the Run 2 detector, and using the Run 2 vertexing code, the resolution degrades at high local pile-up densities.

To illustrate the level of pile-up rejection for the vertex finding, the number of tracks associated to the hard scattering vertex is shown in Figure 3.18 for the more difficult case of vector boson fusion (VBF) $H \to \nu\nu\nu\nu$ events, separated by the hard scattering and the pile-up components. The results are shown as a function of $|\eta|$ of the tracks, normalised to the number of events. At all η, the ITk is able to efficiently control the contributions from pile-up in the AMVF results. At $|\eta|$ close to 4, less than half of the primary tracks are used to fit the vertex, as soft tracks have a poor z resolution and therefore are not considered by the current AMVF tuning. The remaining pile-up tracks that contribute to the vertex fit are

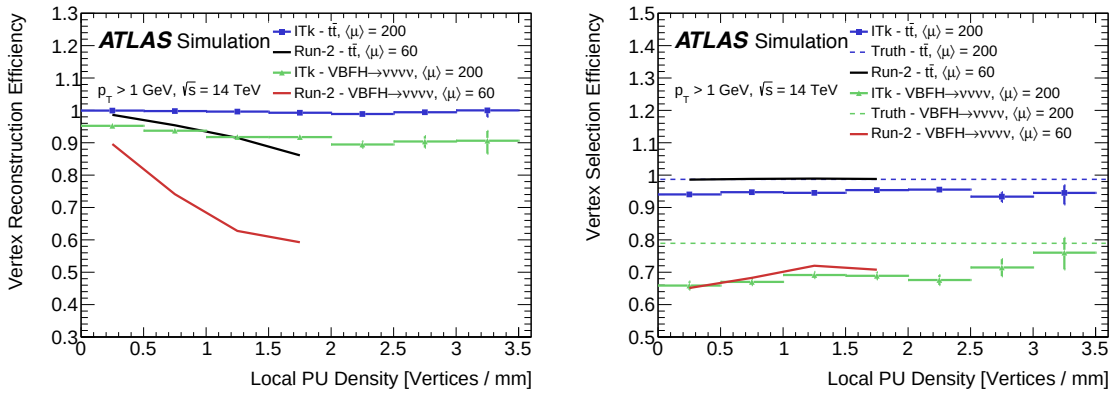


Figure 3.19: The primary vertex reconstruction (**left**) and identification (**right**) efficiency for $t\bar{t}$ and vector boson fusion $H \to \nu\nu\nu\nu$ interactions as a function of local pile-up density in events with an average pile-up of 200. Results use digital clustering and a pixel size of 50×50 μm^2. The vertex identification is done using the $\sum p_{\mathrm{T}}^2$ criterion based on the tracks used in the vertex fit, as described in the text. The dotted lines on the right plot indicate the rate of events for the ITk where the true primary interaction vertex actually has the highest true $\sum p_{\mathrm{T}}^2$. Shown as well are results for a Run 2 simulation sample using the Run 2 primary vertex reconstruction code.

comparably soft and do not contribute significantly to the $\sum p_{\mathrm{T}}^2$ of all tracks associated to the primary vertex, as can be seen in the bottom plot of Figure 3.18.

The vertex reconstruction efficiency for $t\bar{t}$ events with an average of 200 pile-up events is close to 100%, as can be seen in Figure 3.19, where the efficiency is shown as a function of local pile-up density in a 2 mm window around the primary interaction. Results are also presented for VBF $H \to \nu\nu\nu\nu$ events, which are characterised by the neutrinos leaving the detector undetected and two forward jets. For $t\bar{t}$, no significant local pile-up dependency is found. For the more difficult case of VBF $H \to \nu\nu\nu\nu$, there is small pile-up dependency on top of a few percent vertex reconstruction inefficiency. Shown as well are the Run 2 results, which show a larger local pile-up dependency.

In most of the analyses of the current Run 2 data, the hard-scattering (primary) vertex is identified based on the $\sum p_{\mathrm{T}}^2$ of the tracks associated to the vertices. This strategy yields good results for most of the high-p_{T} physics signatures for the Run 2 levels of pile-up. Figure 3.19 also shows the identification efficiency for $t\bar{t}$ and vector boson fusion $H \to \nu\nu\nu\nu$ events in the ITk as a function of local pile-up density in events with an average pile-up of 200. As can be seen for both event topologies, a very high identification efficiency is achieved even at Phase-II levels of pile-up for the ITk and for Run 2. The rate of events for which the true primary interaction vertex actually has the highest true $\sum p_{\mathrm{T}}^2$ is shown as well for comparison, for Phase-II events with an average of 200 pile-up events. For Run 2, with its low level of pile-up, this rate is comparably higher. No effects due to a large density of pile-up vertices are seen in this study. For analyses with no central high p_{T} tracks a different strategy will need to be developed to find the hard scattering vertex, e.g. by using the tracks

associated to the highest p_{T} forward jets.

3.2 Physics Object Performance

In this section, the performance of the ITk Detector is characterised in terms of physics object reconstruction. In particular, the conversion reconstruction and the b-tagging performance in the presence of an average of 200 pile-up events, and the pile-up suppression for tracks in jets and for $E_{\mathrm{T}}^{\mathrm{miss}}$ is discussed. The results here update the results presented in the Strip TDR [1]. The ATLAS performance for muon reconstruction at HL-LHC is described in Reference [26], electron reconstruction with the ITk is described in Reference [27].

3.2.1 Photon Conversion Reconstruction Studies

Excellent photon reconstruction efficiency and photon energy resolution are top priorities for physics channels like $H \rightarrow \gamma\gamma$. Both the efficiency and the energy calibrations are affected by the number of photons that interacts with the material inside the tracker volume and are converted into electron positron pairs. The top left plot of Figure 3.20 shows that the probability of a photon to convert inside the ITk volume is 10% for $|\eta| < 0.5$ and rising to 45% for $2.0 < |\eta| < 2.5$. This is a reduction by up to a factor 2.5 compared to the current detector comes from the much-reduced material budget of the ITk.

For the current detector a dedicated track reconstruction chain [28] has been introduced in order to recover the photon reconstruction performance lost due to photon conversions. This dedicated pass of the track reconstruction runs with relaxed requirements on the impact parameters and the number of hits in order to be more efficient for secondary tracks. Only regions of interest (ROI) defined by high-p_{T} electromagnetic showers in the calorimeter are considered. TRT track segments not associated to reconstructed tracks by the standard algorithms are extended inwards to the silicon detector to form secondary tracks, followed by a conversion vertex search. Identified conversions are then used to increase the photon reconstruction efficiency and to improve the energy resolution.

A similar approach has been studied for the ITk to explore the potential to reconstruct secondary tracks originating from photon conversions. In this case, the secondary tracks are formed from strip seeds within the ROI, rather than TRT segments. The top right plot of Figure 3.20 shows for a $H \rightarrow \gamma\gamma$ sample without pile-up the significant gain in the reconstruction efficiency at radii greater than 250 mm employing the ROI seeded conversion finding in addition to the standard track reconstruction. Results here are for photons with $|\eta| < 2$. The bottom left plot in the figure illustrates that the efficiency is slightly reduced after adding an average of 200 pile-up events to the $H \rightarrow \gamma\gamma$ signal. The conversion reconstruction efficiency using the two ROI seeded approaches is shown for ITk and the Run 2 detector in the bottom right plot. Further developments are needed to fully established the

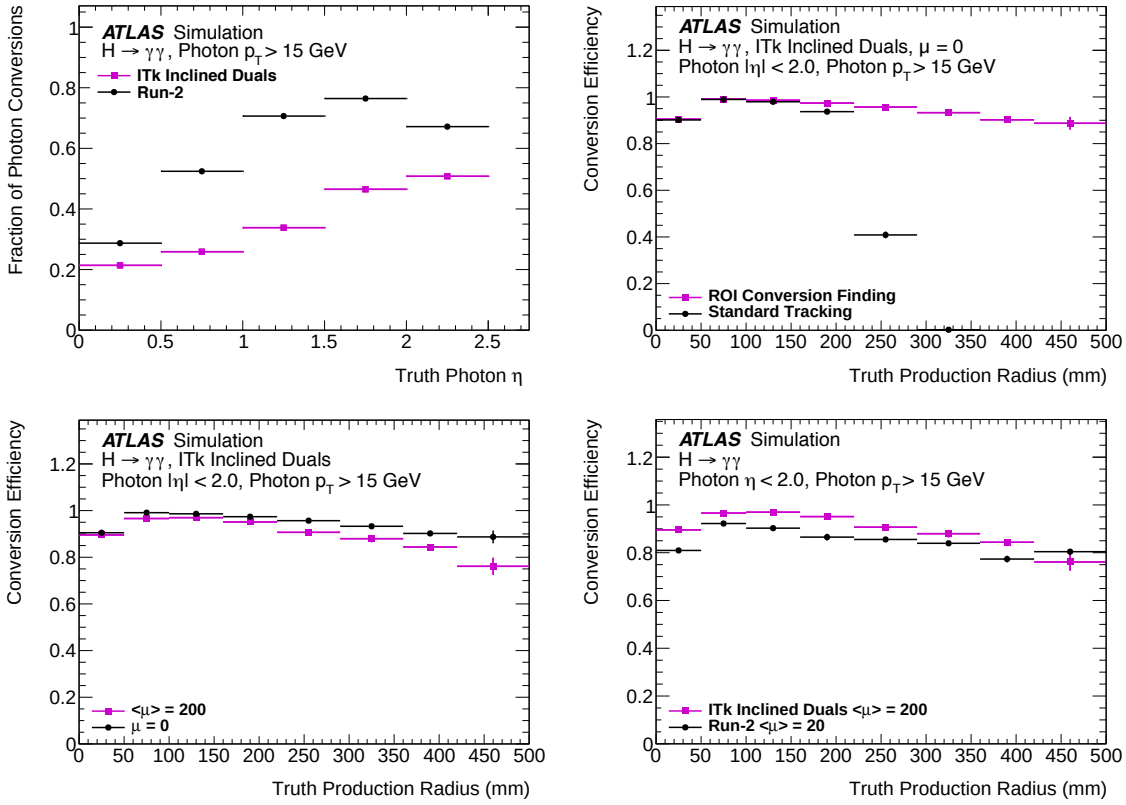


Figure 3.20: Results of a conversion reconstruction study using a sample of $H \rightarrow \gamma\gamma$ events for photons with $|\eta| < 2$. **Top left:** Probability for a photon to covert when traversing the detector. **Top right:** Efficiency to reconstruct conversions in the ITk material just using the standard track reconstruction as input, for events without pile-up, compared to the results using a dedicated reconstruction in regions of interest (ROI) defined by high-p_{T} electromagnetic showers. **Bottom left:** Effect of adding an average of 200 pile-up interactions on the conversion reconstruction in the ITk. **Bottom right:** Conversion efficiency using the ITk compared to the result for the current Run 2 detector reconstruction.

region of interest driven conversion reconstruction for the HL-LHC software chain in the ITk.

3.2.2 Flavour Tagging Performance

One of the primary roles of the Pixel Detector is to provide precise track measurements required for the impact parameter measurement. The impact parameter precision directly translates into the b-tagging performance. The goal for the design of the ITk Pixel Detector is to preserve, and if possible improve, the current Run 2 b-tagging performance in the presence of an average of up to 200 pile-up events and to significantly extend the η range for which the b-tagging information can be used for physics analyses.

The b-tagging performance is characterised by the probability to identify jets containing a b-hadron decay and by the rejection of jets not containing a b- or c-hadron as a b-jet ("light-jet rejection"). The b-tagging algorithms used in ATLAS are based on multivariate techniques, combining different sensitive observables. For each jet, these algorithms provide a "b-tag weight" that is used to discriminate between b-, c- and light-flavour jets. The following results were obtained using $t\bar{t}$ events for jets matched to partons from the top quark decays. The jets are labelled b or c based on the presence of b- or c-hadrons within a cone

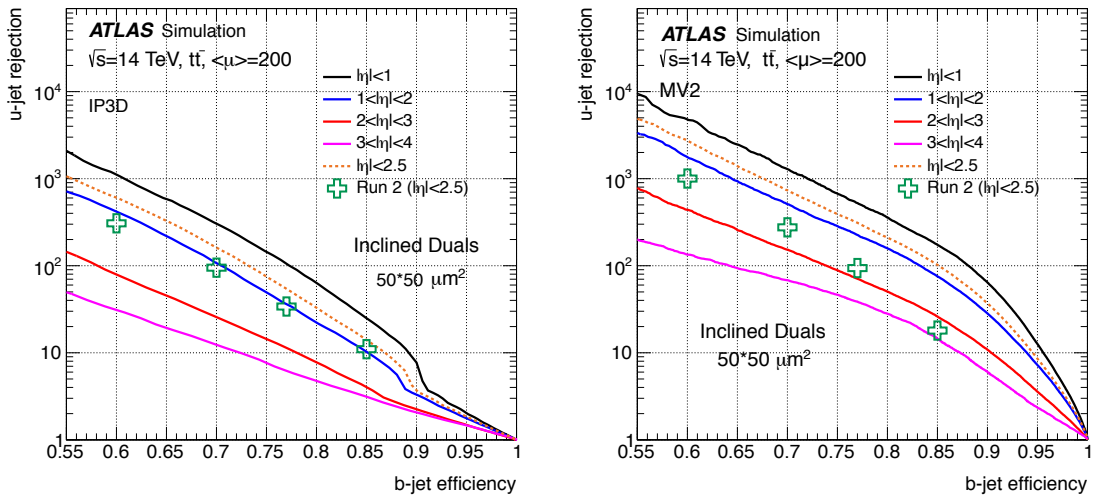


Figure 3.21: Performance of the IP3D (**left**) and MV2 (**right**) b-tagging algorithms in $t\bar{t}$ events with 200 pile-up for the ITk layout. The rejection of light jets for different η regions is shown as a function of b-jet efficiency. Results are shown for 50×50 μm^2 pixels, using digital clustering in the reconstruction. For comparison purposes, the performance for ATLAS during Run 2 with an average of 30 pile-up events is shown as crosses.

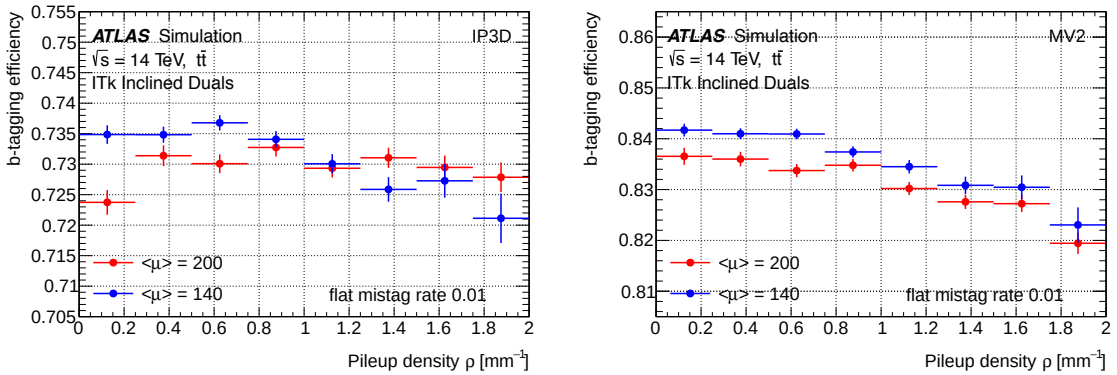


Figure 3.22: Efficiency of the IP3D (**left**) and MV2 (**right**) b-tagging algorithms in $t\bar{t}$ events as a function of local pile-up density, for events with an average of 140 and 200 pile-up. A working point of 1% is used for the light jet mistag rate.

of $R = 0.3$ around the jet axis [29]. In the absence of heavy-flavour hadrons, the jets are labelled "light". For the results presented here, tracks are subdivided into 17 categories that were defined to model the ITk resolution for tracks, depending on their η, p_{T} and hit pattern. The categories for $|\eta| > 2$ take into account the p_{T} and η dependence of the multiple scattering in the forward region. The b-tagging resolution functions have been determined using a $t\bar{t}$ sample.

Figure 3.21 shows the light-jet rejection versus the b-tagging efficiency obtained for two different b-tagging algorithms, namely IP3D and MV2 [30]. Both algorithms explore primarily the consistency of all individual tracks in a jet with coming from the primary hard-scattering vertex. IP3D is a pure impact parameter tagger which combine the single track information in $R\phi$ and in Rz, while MV2 is a multi-variant tagger that combines two secondary vertex finding algorithms with IP3D and kinematic information to obtain a better performance. Typical b-tagging working points used in analyses are for b-jet efficiencies greater than 70% to 85%, depending on the tagger used. For the results presented in the figure, $t\bar{t}$ events with an average of 200 pile-up events were used. For comparison purposes, the performance of the Run 2 detector for $|\eta| < 2.5$ for events with an average of 30 pile-up events is also shown. As can be seen from the figure, for both algorithms, the ITk performs better than the current detector for Run 2, even at pile-up levels of HL-LHC. Even in the very forward region, the ITk provides significant discrimination power between b- and light-jets. The performance gains compared to the results presented in [1] are attributed to the retraining of the IP3D and MV2 algorithms, and to the better tracking performance in jets obtained with the ITk Inclined Duals layout.

Figure 3.22 shows the b-tagging efficiency in $t\bar{t}$ events as a function of the local density of pile-up vertices around the hard scatting vertex, for the IP3D and MV2 algorithms with a working point for the light jet mistag rate of 1%. Results are presented for an average of 140 and 200 pile-up interactions. A small degradation of the b-tagging performance is

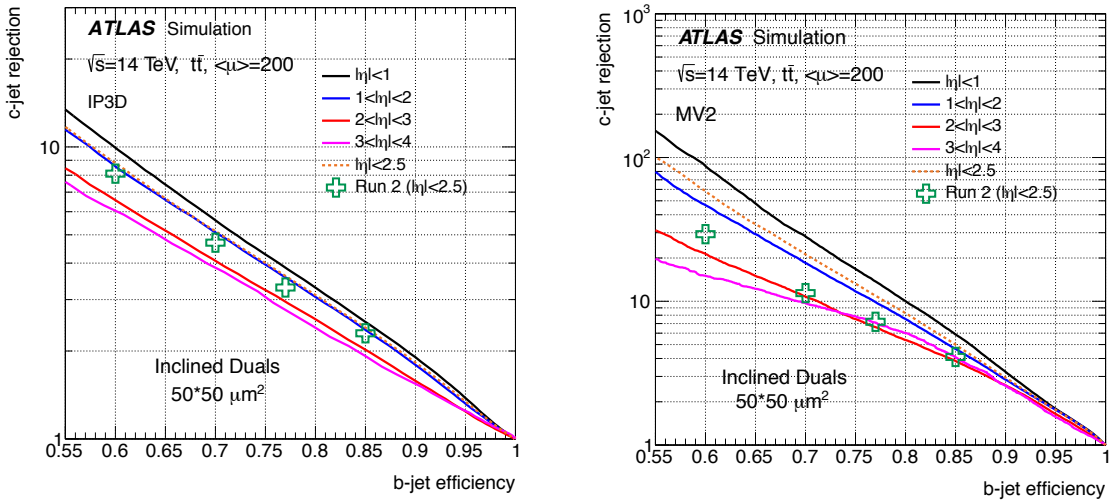


Figure 3.23: Performance of the IP3D (**left**) and MV2 (**right**) b-tagging algorithms in $t\bar{t}$ events with 200 pile-up for the ITk layout. The rejection of c-jets for different η regions is shown as a function of b-jet efficiency. Results are shown for 50×50 μm^2 pixels, using digital clustering in the reconstruction. For comparison purposes, the performance for ATLAS during Run 2 with an average of 30 pile-up events is shown as crosses.

found at high local pile-up densities, with only a limited dependence on the average pile-up levels.

Figure 3.23 shows the c-jet rejection versus the b-tagging efficiency obtained for the same two b-tagging algorithms, for $t\bar{t}$ events with an average of 200 pile-up events. As for the light-jet rejection, the ITk outperforms the Run 2 detector in terms of c-jet rejection, despite the very different levels of pile-up.

The robustness of the response of the b-tagging algorithms has been assessed on a $t\bar{t}$ sample with 10% dead pixel modules. Without a dedicated retuning, a significant drop in background rejection is observed for the IP3D algorithm, which can be as large as a 40% degradation in light-jet rejection for a 70% b-tagging efficiency working point, concentrated in the region $|\eta| < 2$ where the hit pattern information associated to tracks is used to build the template histograms. No such drop is seen in the region $|\eta| > 2$ where IP3D does not exploit hit information in the definition of the templates for the extraction of the log-likelihood ratio. The effect of pixel dead modules on the MV2 algorithm is also significant, resulting in an up to 70% degradation in light-jet rejection for a 70% b-tagging efficiency working point. A dedicated retuning of the IP3D template input histograms and a subsequent retraining of the MV2 algorithm, to allow for the presence of pixel defects, largely mitigates the degradation in b-tagging performance to be less than 15% in light-jet rejection for both algorithms.

3.2.3 Pile-up Jet Rejection and $E_{\mathrm{T}}^{\mathrm{miss}}$ Performance

Another important design goal for the ITk Pixel Detector is to maximise its ability to help rejecting pile-up contributions to jet and missing transverse energy ($E_{\mathrm{T}}^{\mathrm{miss}}$) reconstruction. This can be achieved using the separation along z of primary and pile-up vertices. Here again, extending the η range over which this information can be used is vital to maximise the physics performance of the experiment for Phase-II.

During Run 1 and Run 2 ATLAS developed several jet-vertex tagging methods to identify and remove pile-up contributions to jet reconstruction [31, 32]. In addition, ATLAS is further developing a particle flow algorithm [33] to improve the combination of calorimetric and tracking information for the jet and $E_{\mathrm{T}}^{\mathrm{miss}}$ reconstruction. A major limitation of the current detector is that track-based pile-up suppression is only possible for jets inside the Inner Detector acceptance of $|\eta| < 2.5$. The ITk Pixel Detector will significantly extend the tracker acceptance to $|\eta| < 4$.

Pile-Up Jet tagging

Among the several techniques developed in Run 1 and Run 2, to tag and suppress pile-up jets, this section considers the simplest discriminant R_{pT}, defined as the scalar p_{T} sum of the tracks that are associated with the jet and originate from the hard-scatter vertex PV_0 divided by the fully calibrated jet p_{T}:

$$R_{pT} = \frac{\Sigma_k p_{\mathrm{T}}^{\mathrm{trk}_k}(\mathrm{PV}_0)}{p_{\mathrm{T}}^{\mathrm{jet}}} \tag{3.3}$$

Small values of R_{pT} correspond to jets with a small fraction of the p_{T} carried by charged particles originating from the hard scatter vertex PV_0 and which are therefore very likely to be pile-up jets. The performance in pile-up jet suppression of the detector is highly correlated to the z_0 impact parameter resolution, which determines the track-to-vertex association efficiency and the p_{T} resolution of the tracks. The jets used in this analysis are reconstructed from three-dimensional topo-clusters [34] calibrated at the electromagnetic scale using the anti-k_t algorithm with radius parameter $R = 0.4$. The energy of the jets is corrected using pile-up subtraction followed by a jet energy scale response correction [35, 36].

The reconstructed tracks used for the R_{pT} calculation are required to pass quality criteria defined in Table 2.5 and to have $p_{\mathrm{T}}^{\mathrm{trk}} > 1$ GeV and $|\eta^{\mathrm{trk}}| < 4$. Tracks are then associated to the hard-scatter vertex as defined in Section 3.1.6, requiring the z_0 impact parameter of the track to the hard-scatter vertex to be within a window. The window is defined by the track resolution in z_0 as a function of η and p_{T} for $|\eta| > 2.2$. The resolutions are evaluated for the relevant $p_{\mathrm{T}}^{\mathrm{trk}}$ range and covering the full η acceptance using the method described in

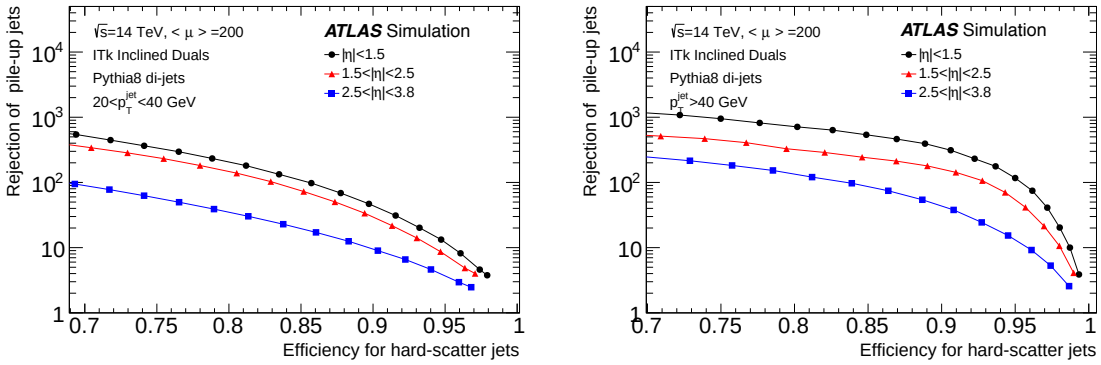


Figure 3.24: The rejection of pile-up jets as a function of the efficiency for hard-scatter jets with $20 < p_{\mathrm{T}} < 40$ GeV p_{T} (**left**) and $p_{\mathrm{T}} > 40$ GeV (**right**) using the R_{pT} discriminant in di-jet events with an average of 200 pile-up events. Results are shown for 50×50 μm^2 pixels and digital clustering.

Section 3.1.2. Below $|\eta|$ of 2.2 a constant z_0 window is used, set to the corresponding track resolution at $|\eta| = 2.2$.

In the following, reconstructed jets are defined as hard-scatter jets if a truth jet associated with the hard-scatter vertex has $p_{\mathrm{T}}^{\mathrm{true}} > 10$ GeV and is found within $\Delta R = 0.3$ of the reconstructed jet. Reconstructed jets which are separated by more than $\Delta R = 0.6$ from any true jet with $p_{\mathrm{T}} > 4$ GeV, are labelled as pile-up jets. The reconstructed hard-scatter vertex is required to be within 0.1 mm of the true hard-scatter vertex.

The rejection of pile-up using R_{pT} as a function of the efficiency for hard-scatter jets is shown in Figure 3.24, for $t\bar{t}$ events with an average of 200 pile-up events and different jet-p_{T} intervals. Each curve is obtained by varying the R_{pT} cut for jets in the given range of $|\eta|$. The efficiency of the R_{pT} cut for hard-scatter (pile-up) jets is defined as the fraction of hard-scatter (pile-up) jets surviving the R_{pT} cut. Good efficiency is obtained at all η for a typical working point of 50 in pile-up jet rejection, even for the most forward η bin.

$E_{\mathrm{T}}^{\mathrm{miss}}$ Performance

In ATLAS, the $E_{\mathrm{T}}^{\mathrm{miss}}$ information is computed as the negative value of the vector momentum sum of high p_{T} physics objects in the event, plus the soft-term from particles which do not belongs to high-p_{T} objects. The soft term in ATLAS is computed using charged tracks assigned to the hard-scatter vertex [37]. Jet vertex tagging techniques, aimed at removing jets originating from pile-up vertices, are crucial to maintain good $E_{\mathrm{T}}^{\mathrm{miss}}$ resolution in the high pile-up conditions expected at HL-LHC.

The $E_{\mathrm{T}}^{\mathrm{miss}}$ used in this analysis is a simplified version of $E_{\mathrm{T}}^{\mathrm{miss}}$ recommended for Run 2 [37]. It is reconstructed using muons selected to have $p_{\mathrm{T}} > 2.5$ GeV or $p > 4$ GeV, electrons

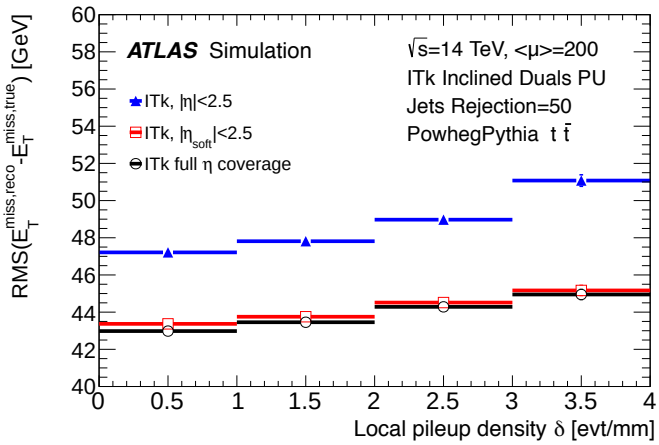


Figure 3.25: The resolutions of $E_{\mathrm{T}}^{\mathrm{miss}}$ in Monte Carlo $t\bar{t}$ events with an average of 200 pile-up events. The resolutions are shown as a function of the local pile-up vertex density around the hard-scattering vertex, for three different $E_{\mathrm{T}}^{\mathrm{miss}}$ definitions. The first considers only tracks in the region $|\eta| < 2.5$ for both pile-up jet rejection and $E_{\mathrm{T}}^{\mathrm{miss}}$ soft term. The second uses tracks for pile-up jet rejection up to $|\eta|$ of 4. The third uses tracks for pile-up jet rejection and $E_{\mathrm{T}}^{\mathrm{miss}}$ soft term down to $|\eta|$ of 4. Results are for 50×50 $\mu\mathrm{m}^2$ pixels and digital clustering.

with $p_{\mathrm{T}} > 10$ GeV, and jets with $p_{\mathrm{T}} > 20$ GeV. A working point with a factor 50 pile-up jet rejection is used for applying the R_{pT} discriminant to the selected jets, as shown in Figure 3.24. Tracks coming from the hard-scatter vertex, with $p_{\mathrm{T}}^{\mathrm{trk}} > 1$ GeV and $|\eta^{\mathrm{trk}}| < 4$, and that are not associated to muons, electrons, or jets, are used to reconstruct the soft-term of the $E_{\mathrm{T}}^{\mathrm{miss}}$.

The $E_{\mathrm{T}}^{\mathrm{miss}}$ resolution, derived in simulated $t\bar{t}$ events with $\langle\mu\rangle = 200$ as a function of the local pile-up vertex density, is shown in Figure 3.25. Compared are the results for using forward tracking for different aspects of the $E_{\mathrm{T}}^{\mathrm{miss}}$ calculation: First, tracks within $|\eta| < 2.5$ are used for both the pile-up jet rejection using the R_{pT} cut and the track soft term; second, tracks are used for the full η coverage to reject pile-up jets; and third, forward tracks are used for both the pile-up jet rejection and the track soft term. The $E_{\mathrm{T}}^{\mathrm{miss}}$ reconstruction significantly benefits from the increased tracker acceptance that enables pile-up jet rejection in the forward region. The additional gain in the soft term using tracks between $|\eta|$ of 2.5 and 4 is small. Overall the $E_{\mathrm{T}}^{\mathrm{miss}}$ performance even at an average of 200 pile-up events benefits from the excellent pile-up control using the ITk.

3.2.4 Electron and Muon Reconstruction and Identification

Electron and muon reconstruction and identification with the upgraded Phase-II detector are summarised in the Strip and Muon Spectrometer Technical Design Reports [1, 26]. The detailed results are not repeated here. Figure 3.26 (left plot) from reference [26] illustrates

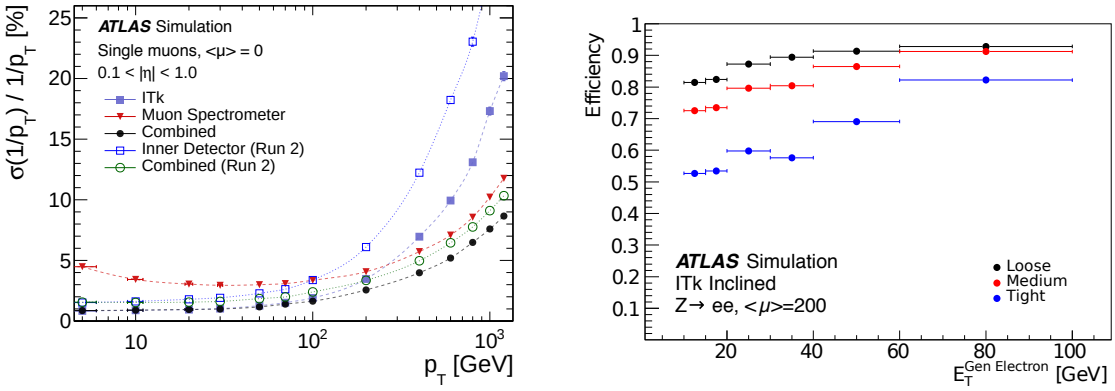


Figure 3.26: **Left**: Combined muon momentum measurement and the individual contributions from the ITk and the upgraded Muon Spectrometer [26]. For comparison the Run 2 results are shown as well. **Right**: Efficiency for electron reconstruction and identification at different selection levels for electrons from Z decays with 200 pile-up [1].

the effect of the better ITk momentum resolution that improves the combined muon momentum measurement in the central region, compared to the resolution of the Run 2 detector. The right plot [1] shows the combined electron reconstruction and identification efficiency for electrons from Z decays in events with an average of 200 pile-up events.

Study of Electron Charge Mis-Identification

Electron charge mis-identification is a major background in Run 2 ATLAS analyses such as same-sign WW [38], or Z' [39] searches. The charge of an electron is determined from the curvature of the track matched to the cluster in the electromagnetic calorimeter corresponding to the electron. The algorithm used for finding the best track candidate for a given cluster is described in detail in Reference [40]. For the current detector electron charge mis-identification is caused predominantly by Bremsstrahlung. The emitted photon can either convert to an electron–positron pair or traverse the first few layers of the detector without creating a track pair. In the first case, the electromagnetic cluster corresponding to the initial electron can be matched to the wrong-charge track from the conversion leptons. In case of photon emission without subsequent pair production, the electron track might fail the tracking recovery for Bremsstrahlung, leading to a poorly measured short track which in turn can result in a mis-measured charge sign. The size of both effects is proportional to the amount of detector material crossed.

In Figure 3.27 shows the charge mis-identification using $Z \to e^+e^-$ simulated events with pile-up. The results for ITk and current Run 2 detector are compared. The charge mis-identification probability is defined as the ratio of the number of electrons with incorrectly reconstructed charge to the number of all electrons, $P(\text{flip}) = N(\text{flipped})/N(\text{all})$. Electrons

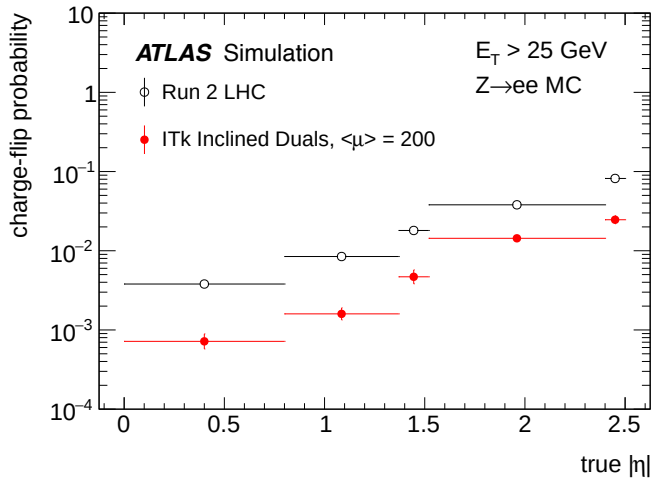


Figure 3.27: Electron charge mis-identification probability as a function of the true $|\eta|$. The charge mis-identification probability for the ITk is studied in $Z \rightarrow e^+e^-$ events with different levels of pile-up. For reference, the Run 2 result is also shown.

are required to have a minimal transverse energy $E_{\mathrm{T}} > 25$ GeV. No further commonly used identification criterion like a tight cuts on $z_0 \sin\theta$ or σ_{d_0} are required in order to keep the results more comparable. Because of the large reduction in material budget of the ITk, the probability to mis-identify the electron charge is reduced by at least a factor of 3 compared to the current detector. The magnitude of improvement depends on η of the electron in the detector. Furthermore, no significant effects due to the increased levels of pile-up are observed.

Track based Lepton Isolation

In physics analyses using primary leptons in the final-states, one crucial tool to ensure the purity of the sample is the so-called lepton isolation, requiring that the lepton is far from any jet activity in the event. Using tracks, the isolation of a given lepton is defined as the scalar sum of the transverse momenta of all charged particle tracks that fall in an angular cone of given size around the lepton trajectory and pass a set of selection requirements. For the most common configuration used during Run 2, called $p_{\mathrm{T}}^{\mathrm{VarCone,30}}$, the cone size ΔR is defined as a function of the transverse momentum of the lepton under study, $p_{\mathrm{T}}^{\mathrm{lepton}}$:

$$\Delta R\left(p_{\mathrm{T}}^{\mathrm{lepton}}\right) = \min\left(\frac{10\ \mathrm{GeV}}{p_{\mathrm{T}}^{\mathrm{lepton}}}, 0.3\right). \tag{3.4}$$

For this isolation definition, tracks entering the cone are required to have a transverse momentum of $p_{\mathrm{T}} > 1$ GeV and a longitudinal impact parameter with respect to the hard scattering vertex $|z_0 \times \sin(\theta)| < 3$ mm in order to be used in the isolation.

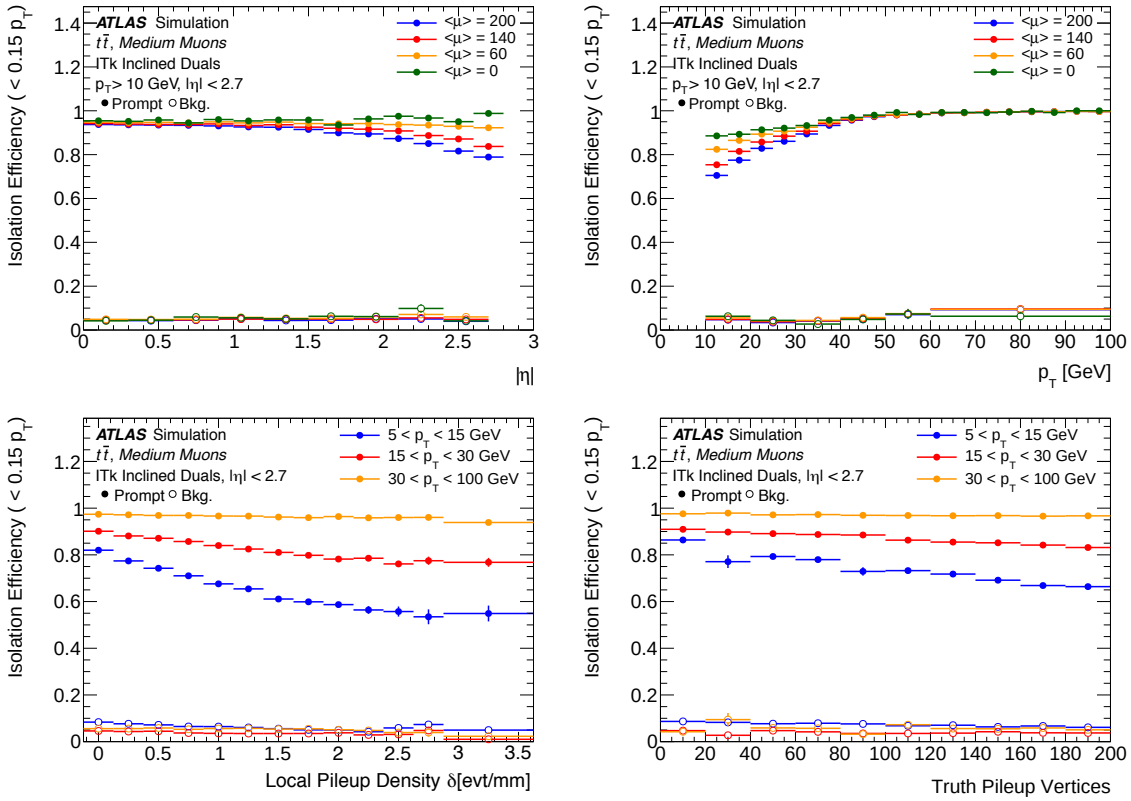


Figure 3.28: Efficiency for the track based isolation requirement $p_{\mathrm{T}}^{\mathrm{VarCone,30}} < 0.15 \times p_{\mathrm{T}}$ for muons within $|\eta| < 2.7$. The efficiency for prompt muons and secondary backgrounds is shown as a function of $|\eta|$ (**top left**) and p_{T} (**top right**), for four values of average pile-up. The efficiency for prompt muons and secondary backgrounds is shown for different p_{T} intervals as a function of pile-up density (**bottom left**) and the number of truth vertices present in the event (**bottom right**).

The impact of the demanding HL-LHC running conditions on the track isolation performance is evaluated using muons satisfying the "Medium" quality criteria [41] reconstructed in simulated $t\bar{t}$ events within the Muon Spectrometer acceptance of $|\eta| < 2.7$. To decouple this study from the challenge of primary vertex identification, events are only considered for which the reconstructed primary vertex candidate is within $|\Delta z| < 0.5$ mm of the simulation truth location of the hard scatter interaction. The primary quantity under study is the isolation efficiency, defined as the fraction of muons originating from generator-level semi-leptonic top quark decays which satisfy an isolation requirement of $p_{\mathrm{T}}^{\mathrm{VarCone,30}} < 0.15 \times p_{\mathrm{T}}$.

Figure 3.28 shows the isolation efficiency as a function of the transverse momentum and the pseudorapidity of the muon, for four running scenarios with an increasing average pile-up. The efficiency is observed to be very stable against increasing pile-up density for transverse momenta above $p_{\mathrm{T}} > 50$ GeV. At lower muon transverse momenta, a decrease with increasing pile-up is observed. The isolation cone size increases for low-momentum

muons, increasing the probability for tracks from pile-up interactions to enter the cone. In addition, the momentum of pile-up tracks is more comparable to low-p_{T} muons and hence may more easily cause inefficiencies in applying the isolation criteria. The isolation efficiency decreases with increasing absolute values of the lepton pseudorapidity, because more pile-up tracks pass the impact parameter selection at large $|\eta|$. At the same time, the fraction of the reconstructed muons from secondary decays ($\pi^{\pm}, K^{\pm}$ as well as b, c-quarks) rejected by the isolation criterion remains stable. At an average of 200 pile-up events the efficiency for background from secondaries is found to be 4.6%.

3.2.5 Study of τ Identification using the ITk

An important part of the ATLAS HL-LHC physics programme uses τ-leptons for Standard Model measurements and searches for new phenomena. τ-leptons decay hadronically 65% of the time and 35% leptonically into an electron or muon, plus neutrinos. This section will focus on hadronic τ decay modes into one or three charged pions, plus neutral particles.

The hadronic decays of τ-leptons, denoted here as τ_{had}, are reconstructed using the anti-k_t algorithm seeded by jets with $p_{\mathrm{T}} > 10$ GeV. τ_{had} candidates are required to have $p_{\mathrm{T}} > 20$ GeV, to contain one or three associated tracks (prongs) with a total charge of ± 1, and to be within the full ITk acceptance of $|\eta| < 4.0$. A Boosted Decision Tree (BDT) identification procedure, based on calorimetric shower shapes and tracking information, is used to reject backgrounds from jets. It is similar to the procedure described in References [42, 43], but it

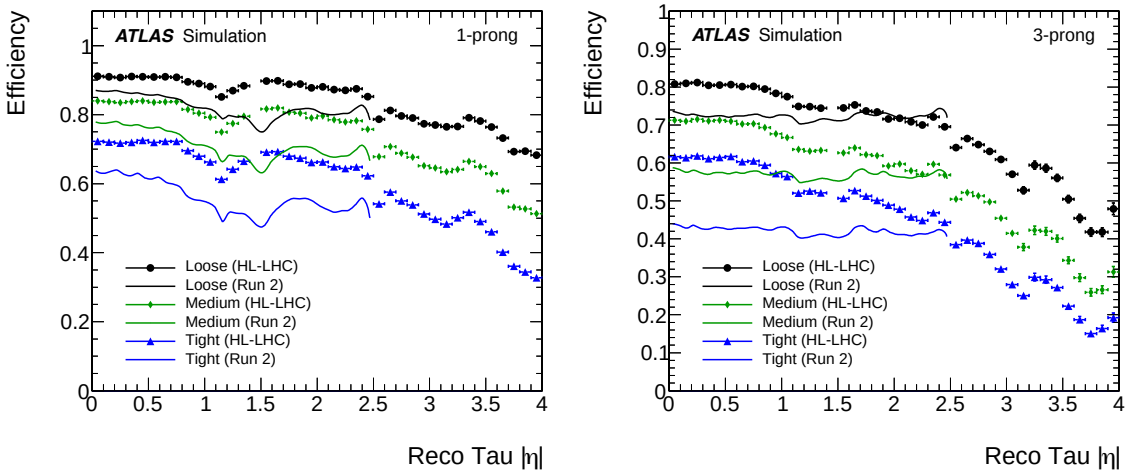


Figure 3.29: τ identification efficiency as a function of $|\eta|$ for the algorithm tuned for HL-LHC detector and pile-up conditions ("HL-LHC tuning"). Shown are the results for ITk and the current detector. The "Loose", "Medium" and "Tight" working points for ITk are chosen to reproduce the Run 2 rejections. **Left**: Efficiency for 1-prong taus. **Right**: Efficiency for 3-prong taus.

has been re-tuned for Run 2 data since. The algorithm presented here has been trained for the upgraded detector and conditions envisaged for the HL-LHC. A Drell-Yan sample was used for training, with the goal of minimising the dependence of the τ identification on both the number of interactions per bunch crossing and the τ_{had} p_{T}. The hadronic τ identification efficiency is defined as the ratio of the number of reconstructed τ candidates passing a given BDT selection cut to total number of reconstructed τ candidates. Three efficiency working points are evaluated as benchmark working points for one-prong (three-prong) τ candidates to reproduce the Run 2 rejections for the "Loose", "Medium" and "Tight" cut selections. These selections correspond to identification efficiencies of 85% (75%), 75% (60%) and 60% (45%) respectively for one-prong (three-prong) taus.

A plot of the identification efficiency vs $|\eta|$ is shown in Figure 3.29. For each of the three cut levels the average rejection under HL-LHC conditions, with an average of 200 pile-up, is chosen to be the same as for the Run 2 working points, with an average of 25 pile-up interactions. For all τ selection working points the efficiency is improved using the ITk for events with an average pile-up of 200 events, compared to the current Run-2 performance. With the ITk good τ identification performance is also preserved for the forward extension of the tracker coverage below $|\eta|$ of 2.5.

3.3 Physics Benchmark Studies

In this section the impact of the expected performance of physics objects is propagated to a selected set of physics measurements and searches. The excellent track parameter resolution and the forward tracking extension are essential ingredients to keep the effects of pile-up under control, expand the acceptance, and ultimately allow full exploitation of the physics potential of the HL-LHC dataset. It is seen that in all aspects the ITk at least matches but in most cases improves the performance compared to that achieved in Run 2. The studies for physics measurements and searches presented in this chapter are selected to highlight the capabilities of the Pixel Detector (and the inner tracker in general), and are at the same time milestones in the physics program for HL-LHC.

The effects of an upgraded ATLAS Detector are taken into account using energy smearing, efficiencies and fake rates that are applied to truth level quantities. These are applied following parameterisations based on detector performance studies, shown earlier in Section 3.1 and Section 3.2, with full simulation and HL-LHC conditions. Such an approach allows the flexibility of fully exploring optimal selections that apply for the much larger integrated luminosity expected to be delivered during HL-LHC. Extrapolations from present analyses are also used when appropriate, for instance when data-driven background estimates play a vital role in the physics analysis. The projections presented assume an integrated luminosity of 3000 fb^{-1}, corresponding to what is expected to be available towards the end of the HL-LHC physics program.

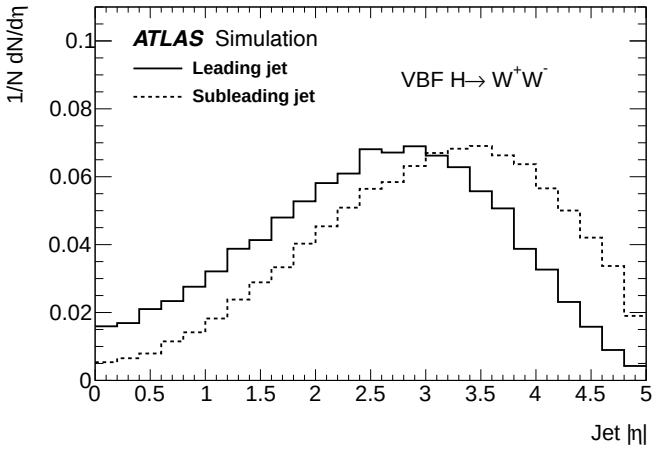


Figure 3.30: Leading and subleading jet η for the VBF production of the $H \rightarrow WW$ channel, for events with two jets with p_{T} above 20 GeV and $m(jj) > 500$ GeV

Precise measurements of Higgs properties play a central role in the HL-LHC physics program. Accurate measurements of differential cross-sections for Higgs production in the four muon decay channel strongly rely on good momentum measurement, which at the transverse momentum range relevant for this final state is heavily dependent on the ITk performance. A good momentum resolution translates into a good mass resolution which in turn yields a high signal to background ratio, allowing the extension of differential cross-section measurements to more extreme phase spaces as well as probing rare Higgs decays such as to two muons. The sensitivity for a differential cross-section measurement in the $H \rightarrow ZZ \rightarrow 4\ell$ decay channel and the expected accuracy for the $H \rightarrow \mu\mu$ cross-section measurement was studied in Reference [26]; Section 3.3.1 presents updated numbers for the expected mass resolution in these decay channels. For the overall Higgs precision measurement program, the improved b-tagging performance, improved tagging of pile-up jets and improved τ and photon identification will also benefit many other channels such as $W/ZH \rightarrow W/Zb\bar{b}$, $t\bar{t}H$, VBF $H \rightarrow WW$, $H \rightarrow \gamma\gamma$ and $H \rightarrow \tau^{+}\tau^{-}$ production, all of which are critical for the precision Higgs physics programme at the LHC. For instance, for VBF production modes the ability to correctly tag forward jets from the hard-scattering interaction significantly improves background rejection in this channel. Figure 3.30 shows for illustration the leading and sub-leading jet $|\eta|$ for the VBF production of the $H \rightarrow WW$ channel, for events with two jets with p_{T} above 20 GeV and $m(jj) > 500$ GeV. The previous study [1] has been revised using the re-optimised jet rejection and b-tagging algorithm presented in this document. The uncertainty on the $H \rightarrow WW$ cross-section is reduced from about 20% to 11% with the usage of the forward tracker extension, using the same cut-based analysis presented before. Using a multivariate analysis [44] the uncertainties in the $H \rightarrow WW$ cross-section measurement improve from 12% to 9%.

The measurement of the Higgs self-coupling strength, with any sensitivity to the Standard Model expectation, is only accessible with the full HL-LHC dataset. One of the most prom-

Physics Channel	$\|\eta\| = 2.7$	$\|\eta\| = 4.0$	Reference
VBF $H \to WW*$	22%	12%	Ref.[1]
Same-sign WW Scattering	4.5%	4.0%	Ref.[45]
$\sin^2\theta_{\text{eff}}$ in $Z \to e^+e^-$	25×10^{-5}	19×10^{-5}	Section 3.3.4

Table 3.1: Measurement precision for three benchmark physics channels without and with the Pixel Detector extension from $|\eta| = 2.7$ to $|\eta| = 4.0$.

ising channels $HH \to b\bar{b}\gamma\gamma$ is studied in Section 3.3.2, where the impact of b-tagging, in both the central and forward region, is critical in suppressing backgrounds. The $HH \to b\bar{b}b\bar{b}$ decay mode is another promising channel to study di-Higgs production for which the b-tagging performance plays a vital role. It is described in Section 3.3.3. The decay channel $HH \to b\bar{b}\tau^+\tau^-$ also has a good sensitivity and has been studied in the context of the TDAQ TDR [44].

Measurements of vector boson fusion and vector boson scattering processes are powerful probes to investigate the nature of electroweak symmetry breaking. The golden channel for vector boson scattering measurements is the production of two same-charge W bosons decaying leptonically, in association with two forward jets. The sensitivity for accurately measuring such a process has been investigated in previous TDRs [1, 26]; the forward extension of the inner tracker is fundamental to tag forward jets from the hard-scattering interaction and reject background from processes where a third lepton is present but not detected because of being out of acceptance without such extension.

Precision Standard Model measurements are also of great importance to indirectly constrain contributions of physics beyond the Standard Model. The sensitivity of a measurement of the weak mixing angle using the forward-backward asymmetry in Z/γ^* events is studied in Section 3.3.4. In this measurement forward electrons bring most of the sensitivity and backgrounds can only be kept under control thanks to the ability of associating a track to the electron energy cluster and using tracks to place isolation requirements.

The significant improvements in the measurement precision from the forward tracker extension in the benchmark physics channels mentioned above are summarised in Table 3.1. For all three channels, the measurement precision is limited by systematic uncertainties, for instance on the background normalisation or on the knowledge of parton distribution functions. Significant improvements are obtained from signal improvements and from better constraining systematic uncertainties with the extended tracking coverage. A similar improvement in the precision can therefore not be achieved by simply increasing the integrated luminosity in case the forward extension is not realised.

Low-p_{T} physics will also benefit from the new Pixel Detector, thanks to its superb impact parameter resolution. The expected mass resolution and accuracy for lifetime measurements of the B_s meson decays are presented in Section 3.3.5.

Another major objective of the HL-LHC is to search for new particles, extending the reach of the LHC both in mass as well as in coupling strength. Many of these searches rely on efficient identification of leptons and/or b-jets and on accurate measurements of jets, leptons, photons and $E_{\mathrm{T}}^{\mathrm{miss}}$ in a wide energy range. Since it was shown that the performance of the upgraded detector with ITk is as good or better than the Run 2 detector, it will still be possible to perform such searches with high sensitivity. An example of a search for exotic resonances that decay into $t\bar{t}$ pairs was presented in the Strip TDR [1]. It highlights the importance of separating highly collimated particles that arise due to the very boosted jet topologies present in such final states.

Another particularly interesting case are searches for long-lived particles which decay inside the volume of the tracking detectors, as these pose different challenges on the layout of the tracking detector. Section 3.3.6 and Section 3.3.7 explore the capabilities of direct detection of meta-stable massive long-lived particles, that within the ITk volume either decay invisibly or into Standard Model particles.

3.3.1 Higgs Boson Production in $\mu\mu$ and 4μ Final States

The impact of the ITk and muon detector upgrades on the mass resolution for the $H \to ZZ^{(*)} \to 4\mu$ and $H \to \mu\mu$ decay channels has been assessed using simulated pp collisions at $\sqrt{s} = 14$ TeV. Both channels profit from the improvements in momentum resolution, when combining the ITk with the Muon Spectrometer measurements. In particular the $H \to ZZ^{(*)} \to 4\mu$ also profits from the increase in rapidity coverage of the ITk and Muon Spectrometer detectors up to $|\eta| = 4$. Results on these channels with the upgraded detector are reported in References [44] and [26]. In the following, updated results for the Higgs boson mass resolution are shown based on the Inclined Duals layout for the ITk presented in this document.

For this study the gluon-gluon fusion (ggF) Higgs sample, as described in Reference [26], was used. The event selection used is similar to the Run 2 analyses. In the case of the $H \to ZZ^{(*)} \to 4\mu$ channel [46], the event must contain four muons and their transverse momenta, ordered in p_{T} are required to be greater than 20 GeV, 15 GeV, 10 GeV, and 5 GeV. The separation in η-ϕ (ΔR) between any of the muons must be greater than 0.1. The pair of opposite-sign muons with an invariant mass m_{12} closest to the Z boson mass is required to have 50 GeV $< m_{12} <$ 106 GeV, with at least one of the muons from this pair being within $|\eta| < 2.7$ to ensure that the mass is well measured. The other opposite-sign muon pair is required to have 12 GeV $< m_{34} <$ 115 GeV. An additional cut, $m(\mu_i, \mu_j) > 5$ GeV, is applied to all pairs. A Z boson mass constraint, similar to the one used in Run 2, is applied to m_{12}. $H \to \mu\mu$ events [47] are selected requiring exactly one pair of reconstructed opposite-sign muons with $|\eta| < 2.7$. The leading muon has $p_{\mathrm{T}} > 20$ GeV and the other muon $p_{\mathrm{T}} > 15$ GeV. Muons overlapping with jets with $p_{\mathrm{T}} > 30$ GeV within a cone of radius $\Delta R = 0.4$ are ignored.

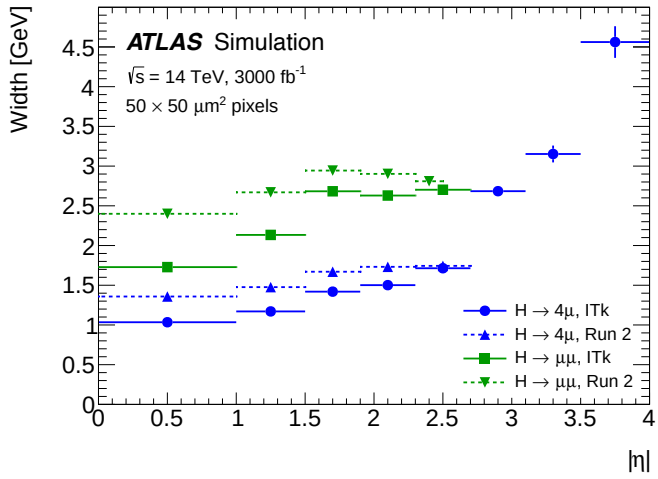


Figure 3.31: The width of the $H \to ZZ^{(*)} \to 4\mu$ (blue marker) and $H \to \mu\mu$ (green marker) invariant mass signal as a function of the $|\eta|$ of the muon with the largest $|\eta|$ value. For comparison also the width of the Run 2 analysis, based on the current detector performance, is shown.

For both channels, the width of the reconstructed Higgs boson mass distribution is determined via Gaussian fits to the mass peak. It is shown as a function of the rapidity of the muon with the largest $|\eta|$ value in Figure 3.31 for the two channels. The improved momentum resolution of the ITk results for both channels in a significantly better mass resolution compared to the current Run 2 detector, in particular in the barrel region. At the same time, the resolution of the reconstructed Higgs boson mass degrades with increasing $|\eta|$ of the muon with the largest $|\eta|$ value, because of the reduced radial extent where the track is measured. For the $H \to \mu\mu$ sample results are only shown for the central region, due to the limited statistics of muons in the forward region.

3.3.2 Higgs Self-Coupling Measurement using the $HH \to b\bar{b}\gamma\gamma$ Channel

One of the most promising channels to measure the self-coupling is the $HH \to b\bar{b}\gamma\gamma$ final state. This channel profits from a clean HH signal extraction thanks to the narrow mass peak of the $H \to \gamma\gamma$ decay and two isolated b-jets in the final state. This process has a very low Standard Model cross-section of 0.103 fb [27] due to the small branching ratio (0.26%) of this channel. Together with a low selection efficiency of below 5%, it is required that the full HL-LHC statistics is analysed to reach a significance better than 1σ. The present analysis is based on truth level particles convoluted with the detector resolution and efficiencies and fake rates computed for $\langle\mu\rangle = 200$ which were extracted using full simulations. This analysis is an update of the results presented in References [48, 27]. The main update in the study presented in Reference [27] was the reevaluation of the photon energy resolution which resulted in a narrower $H \to \gamma\gamma$ mass peak. The following results are based on

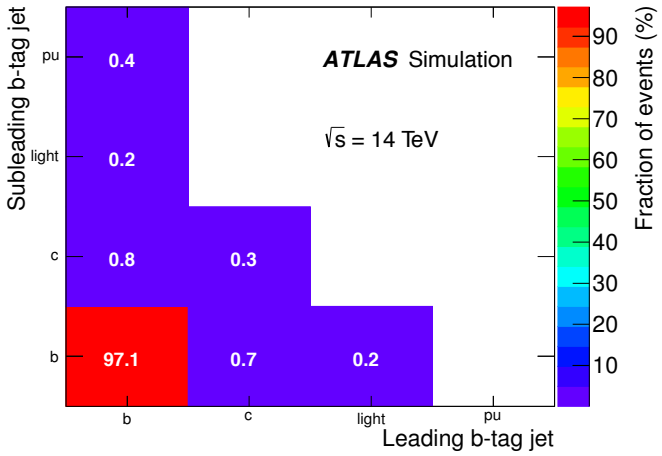


Figure 3.32: Source of b-tagged jets combining all background channels for $\langle\mu\rangle = 200$ and 70% b-tagging efficiency. Shown are the fraction of events. The sources considered are b-jets (b), c-jets (c), jets arising from light quarks (light) or from pile-up (pu).

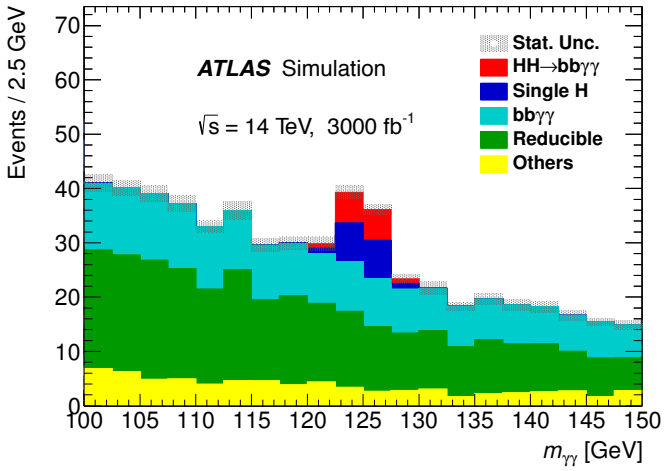


Figure 3.33: Di-photon invariant mass distributions after all the selection cuts except for the cuts on the di-photon invariant mass for $\langle\mu\rangle = 200$. The shaded area corresponds to the MC statistical uncertainty.

the so-called 'Baseline' approach of the photon energy resolution. The results presented in this section are based on the improved b-tagging performance (see Section 3.2.2) benefiting from using the more powerful MV2 algorithm and its dedicated tuning for the ITk, as well as from the improved tracking performance that came with changing to ITk Inclined Duals layout presented in this document.

The event selection criteria are identical to the ones used in the previous studies. Photons and jets are required to have $p_{\mathrm{T}} > 30$ GeV. The events are required to contain a pair of

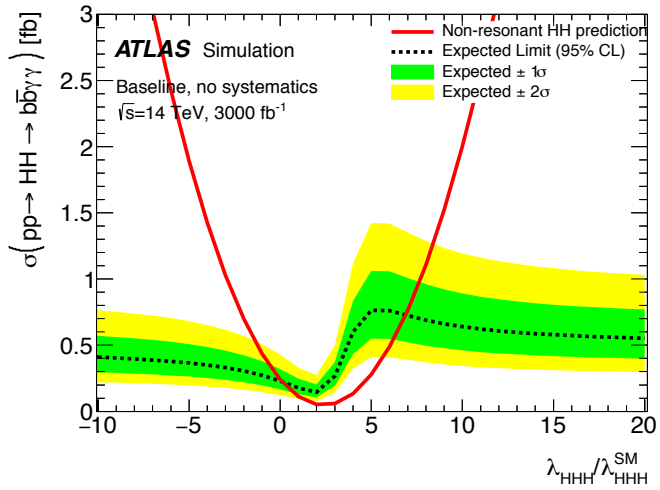


Figure 3.34: Expected 95% CL upper limit on the cross-section $\sigma(HH \rightarrow b\bar{b}\gamma\gamma)$ with 3000 fb^{-1} of data and neglecting systematic uncertainties, as a function of the Higgs self-coupling constant λ in units of λ_{SM}. The $\pm 1\ \sigma$ and $\pm 2\ \sigma$ uncertainty bands are shown in green and yellow. The non-resonant HH prediction shows the theoretical cross-section for di-Higgs production as function of $\lambda_{HHH}/\lambda^{SM}_{HHH}$.

photons and a pair of jets identified as b-jets with a 70% b-jet tagging efficiency. Isolation and angular cuts are applied to select the di-Higgs topology. The photon and the b-jet pairs must both have invariant masses compatible with the Higgs boson mass. Finally, events are categorised depending on the rapidities of the two photons. Figure 3.32 displays the source of the b-tagged jets after the selection cuts. It can be seen that the purity of the b-jet pair exceeds 97%. A 3.6% selection efficiency for a Standard Model Higgs boson is found, leading to 11 signal events for an integrated luminosity of 3000 fb^{-1} with an expected background from single $H \rightarrow \gamma\gamma$ production processes (ttH, ggH, ZH) and the continuum background ($b\bar{b}\gamma\gamma$, $b\bar{b}j\gamma$, $cc\gamma\gamma$, $jj\gamma\gamma$,...) of around 14 and 51 events, respectively. Figure 3.33 displays the di-photon invariant mass. Compared to the results presented in the LAr TDR [27], the expected numbers of events from the continuum background and single Higgs production are reduced by 14% and 19%, respectively, because of the improved b-tagging performance. As a result, a 1.5 σ significance is now expected corresponding to a gain of 17% compared to the LAr TDR [27]. Systematic effects are expected to be small and if they are neglected, the Higgs boson self-coupling would be constrained at 95% CL to $0.2 < \lambda_{HHH}/\lambda^{SM}_{HHH} < 6.9$ as shown in Figure 3.34.

3.3.3 Higgs Self-Coupling Measurement using the $HH \rightarrow b\bar{b}b\bar{b}$ Channel

Another promising channel to measure the Higgs self-coupling is the $HH \rightarrow b\bar{b}b\bar{b}$ final state. This channel profits from the large Higgs boson branching ratio to b-quarks, with a predicted $HH \rightarrow b\bar{b}b\bar{b}$ cross-section of 13.2 fb in the Standard Model. Compared to the $\gamma\gamma b\bar{b}$

channel the background is significantly higher in this channel and the systematic uncertainties associated with it are not negligible. The study presented here updates the analysis in Reference [49], in particular taking benefit from the improved b-tagging performance as described in Section 3.2.2. The trigger selection for the $4b$ final state is discussed in the TDAQ TDR [44].

The analysis selection is based on the Run 2 analysis of 24.3 fb^{-1} of 13 TeV data collected in 2016 [50]. Events are required to contain four jets with $p_{\mathrm{T}} > 40$ GeV and $|\eta| < 2.5$. Each jet is identified as a b-jet using a 76% b-tagging efficiency working point. Jets are paired to form two Higgs boson candidates that both are required to have an invariant mass consistent with the mass of the Higgs boson. Additional kinematic and angular cuts are applied to suppress background and enhance the sensitivity to di-Higgs boson production. The expected background in the signal region is dominated by QCD multi-jet production (∼90%), with a sub-leading contribution from top quark decays (∼10%). The expected yields in the signal region are then extrapolated to $\sqrt{s} = 14$ TeV and 3000 fb^{-1} following the strategy documented in Reference [49].

Figure 3.35 shows the expected upper limit on the $HH \to b\bar{b}b\bar{b}$ cross-section as a function of the Higgs self-coupling for 3000 fb^{-1}. Two projections are shown; the first neglects systematic uncertainties, and the second assumes that the level of systematic uncertainties remains the same as the for the current analysis of 2016 data. The largest source of systemic uncertainty comes from the ability to model the QCD multi-jet background using control regions in data. With 3000 fb^{-1}, the improved ITk b-tagging results in a 20% (10%) gain in sensitivity assuming no (current) systematic uncertainties. The allowed range at 95% CL

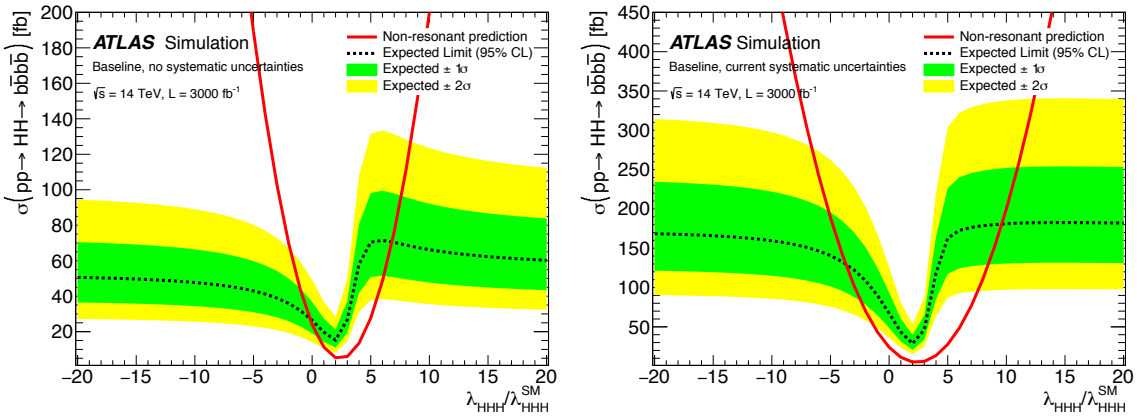


Figure 3.35: Expected 95% CL upper limit on the cross-section $\sigma(HH \to b\bar{b}b\bar{b})$ with 3000 fb^{-1} of data as a function of the Higgs self-coupling constant λ_{HHH} in units of $\lambda^{\mathrm{SM}}_{\mathrm{HHH}}$. The $\pm 1\sigma$ and $\pm 2\sigma$ uncertainty bands are shown in green and yellow. **Left**: Results evaluated without systematic uncertainties. **Right**: Results assuming that the systematic uncertainties remain as they are in the 2016 analysis. The non-resonant HH prediction shows the theoretical cross-section for di-Higgs production as function of $\lambda_{HHH}/\lambda^{SM}_{HHH}$.

for $\lambda_{HHH}/\lambda_{HHH}^{SM}$ with 3000 fb^{-1} including (without) systematic uncertainties is -4.1 – 8.7 (-1.2 – 8.0).

3.3.4 Prospects for a Precision Measurement of the Weak Mixing Angle

In the Standard Model (SM), the Z boson is a mix of the neutral states associated to the U(1) and SU(2) gauge groups, which results to different Z-couplings to left- and right-handed fermions. This difference leads to an asymmetry in the angular distribution of positively and negatively charged leptons produced in Z boson decays. Experimentally this asymmetry can be expressed simply as:

$$A_{\mathrm{FB}} = \frac{N(cos\theta^* > 0) - N(cos\theta^* < 0)}{N(cos\theta^* > 0) + N(cos\theta^* < 0)}, \tag{3.5}$$

where θ^* is the angle between the negatively charged lepton and the quark in the Collins-Soper frame [51] of the di-lepton system. This asymmetry is enhanced by Z/γ^* interference and exhibits a significant dependence on the di-lepton mass. The size of the asymmetry at the Z pole depends on the weak mixing angle, $\sin^2\theta_{\mathrm{eff}}$ [52]. In the SM the weak mixing angle can be expressed as a function of the Z mass, fine-structure constant α and the Fermi-coupling constant G_{F}. It receives radiative corrections involving in particular terms proportional to m_{top}^2 and $\log(m_h)$. Many models of new physics predict modifications to those radiative corrections.

Several measurements of $\sin^2\theta_{\mathrm{eff}}$ have been made at previous and current colliders. The current world average is dominated by the combination of measurements at LEP and at SLD, which give $\sin^2\theta_{\mathrm{eff}} = 0.23153 \pm 0.00016$ [52]. At the LHC, the best sensitivity to $\sin^2\theta_{\mathrm{eff}}$ is at high Z boson rapidities when at least one lepton is present in the forward region [53]. Only Z bosons decaying to di-electron pairs are considered in this analysis since this final state provides the best experimental precision within the largest acceptance with the upgraded ATLAS Detector for HL-LHC.

The resolutions for the simulated $pp \to Z/\gamma^* \to e^+e^-$ signal at $\sqrt{s} = 14$ TeV are smeared to match the expected detector response. The $pp \to Z/\gamma^* \to e^+e^-$ events are categorised into three independent classes according to the electron $|\eta|$: CC, CF, FF when C represents electron reconstructed in the central region ($|\eta| < 2.5$) and F represents electron reconstructed in the forward region ($2.5 < |\eta| < 4.2$). Both electrons are required to have $p_{\mathrm{T}} > 25$ GeV. The invariant mass of the opposite-charge electron pair, m_{ee}, is required to be 60 GeV $< m_{ee} <$ 200 GeV and the events are further categorised in 10 equally-spaced bins in absolute di-lepton rapidity up to $|y_{ee}| = 4.0$.

The contribution of jets mis-identified as electrons is suppressed using a tight electron identification and a track isolation requirement. The extended η coverage of the ITk allows to further reject of hadronic jets misidentified as electrons applying a track to cluster matching

and a track-based isolation requirement also in the forward region. Only electron candidates with no tracks with $p_T > 1$ GeV other than the electron track within a cone of radius of 0.2 are selected. A 40% improvement on the signal significance for the CF class is observed by including the track isolation requirement for electrons in the forward region.

After the final selection, the purity of the candidate sample is determined with simulation, and is found to be greater than 99% for the CC class, between 90 and 98% in the CF, and between 60 and 90% for the FF class. A_{FB} is calculated from the selected di-electron candidates, and unfolded to particle level to correct for detector effects and migrations in m_{ee} and $|y_{ee}|$ bins. For the CF and FF classes migrations in the reconstructed mass m_{ee} are up to 50 and 60%, respectively. Various sources of uncertainty are considered. Those associated with background are mostly relevant for CF and FF classes and are estimated to be 5% on the background yield and considered uncorrelated for each m_{ee} and $|y_{ee}|$ bin. Significant uncertainties arise from knowledge of the electron energy scale and resolution. Systematic uncertainty of 0.5% (0.7%) [54] is considered to account for possible non linearities in the energy scale of electrons reconstructed in the central (forward) region with $E_T < 55$ GeV and up to 1.5% (2.1%) for central (forward) electron with $E_T > 100$ GeV.

In the top two plots of Figure 3.36 the amplitude of the A_{FB} is shown at particle level for the CC, CF and FF classes separately as a function of $|y_{ee}|$ and m_{ee}. As expected the asymmetry for the CF class is found to be largest. The expected sensitivity to the particle level A_{FB} as a function of m_{ee} is shown in the bottom plot of Figure 3.36 for a chosen rapidity bin for the CF class.

The best fit value of $\sin^2\theta_{\text{eff}}$ is found by a χ^2 minimisation comparing the particle level A_{FB} to the prediction as a function of $\sin^2\theta_{\text{eff}}$ made at LO in QCD with the CT14 NNLO parton distribution function (PDF). The imperfect knowledge of the PDF results in general in sizeable uncertainties on A_{FB}, in particular in regions where the absolute value of the asymmetry is large, i.e. at high and low $m_{\ell\ell}$. Near the Z boson mass peak, the effect on $\sin^2\theta_{\text{eff}}$ dominates, while being significantly smaller at high and low masses. Thus, in this projection a global fit is performed where $\sin^2\theta_{\text{eff}}$ is extracted, while constraining at the same time the PDFs uncertainties [53]. With this analysis the expected sensitivities to $\sin^2\theta_{\text{eff}}$ are respectively 25×10^{-5}, 21×10^{-5} and 48×10^{-5} for the CC, CF and FF channel. These results are dominated by the PDF uncertainty. Combining the three channels together the expected sensitivity reaches a precision of 19×10^{-5} ($\pm 16 \times 10^{-5}$ (PDF) $\pm 10 \times 10^{-5}$ (exp.)) which exceeds previous single experiment precision.

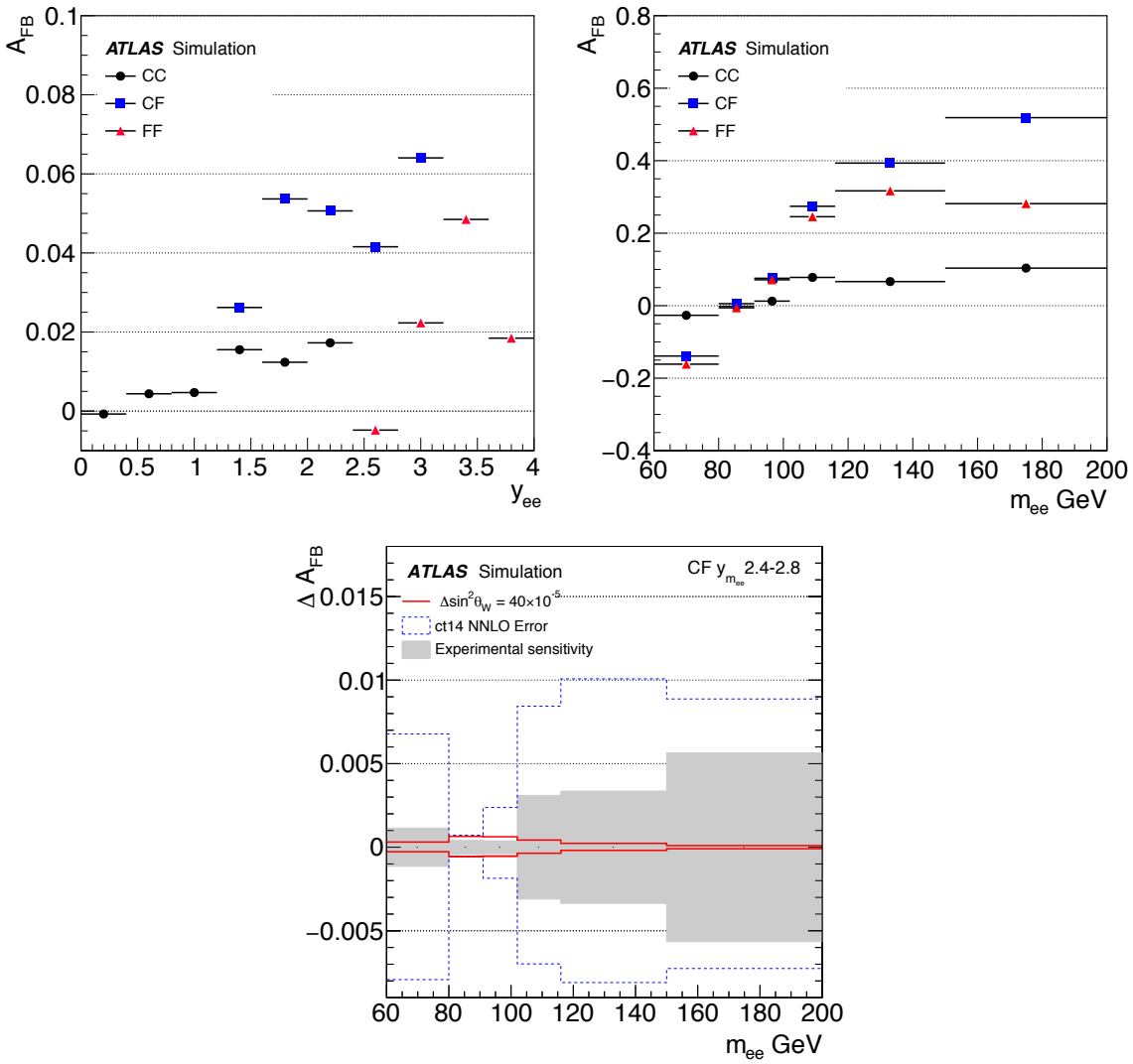


Figure 3.36: **Top**: A_{FB} distribution at particle level as a function of the di-electron rapidity (**left**) and the di-electron mass (**right**). The expected results are shown for 3000 fb^{-1} at $\sqrt{s} = 14$ TeV, in the fiducial volume for CC, CF and FF classes for $pp \to Z/\gamma^* \to e^+e^-$ decay. **Bottom**: Distribution of ΔA_{FB} as a function of mass for the CF class in a rapidity bin. The filled band corresponds to the experimental sensitivity. The solid red lines correspond to a variations of $\sin^2\theta_{\mathrm{eff}}$ corresponding to 40×10^{-5}. The dotted blue lines illustrate the total error from the CT14 NNLO parton distribution function.

3.3.5 Prospects for B-physics

The ATLAS B-physics programme exploits the large $b\bar{b}$ production cross-section in pp collisions to indirectly search for effects of new physics, through possible deviations from Standard Model predictions in precision measurements or by studying very rare processes. ATLAS focuses mostly on exclusive b-hadron decays that are fully reconstructable by the tracking system and that contain at least one muon in the final state selected with a high trigger efficiency. Many of these channels are statistically limited and thus the next phases of LHC offer opportunities for significant improvements. The achievable precision depends on the collected number of signal b-decay events, that for a given integrated luminosity is driven by the trigger performance; this aspect is discussed in the Muon and TDAQ TDRs [26, 44]. The other important aspect is the detector performance, which depends on the inner tracking and muon systems. The two key parameters for B-physics measurements are the invariant mass resolution and ability to resolve the position of the secondary b-hadron decay vertices. The former determines the ability to suppress combinatorial backgrounds and separate close states, while the latter is important to suppress prompt backgrounds and for analyses measuring the b-hadron proper decay times, like CP-violation studies involving B-meson mixing. Furthermore, pile-up robustness of the primary vertexing, isolation and flavour tagging performances are crucial to determine the b-hadron production and decay positions.

Results are presented for the two flagship analyses of $B_s^0 \to \mu^+\mu^-$ and $B_s^0 \to \mathrm{J}/\psi\phi$. Full simulation Monte Carlo samples were generated with PYTHIA 8.210 [11] for three run-periods: Run 1 in 2012, the beginning of Run 2 in 2015 (including the IBL) and the upgraded detector including the ITk for HL-LHC. The average number of pile-up events was set to $\langle\mu\rangle \sim 20$ for the Run 1 and the initial Run 2 periods, while for HL-LHC the average is set to $\langle\mu\rangle = 200$. The selection of the signal $B_s^0 \to \mu^+\mu^-$ and $B_s^0 \to J/\psi\phi$ events follows the Run 1 analyses [55, 56]. In addition a minimum threshold on the muon candidate tracks p_{T} is set to 5.5 GeV. The study is limited to $|\eta| < 2.5$ as this corresponds to the di-muon trigger acceptance.

For the analysis of rare $B_{s/d}^0 \to \mu^+\mu^-$ decays the invariant mass resolution drives the separation of the B_d^0 and B_s^0 states, as well as the separation of background contributions from partially reconstructed b-decays. At low momentum the inner tracking system dominates the momentum resolution and hence the invariant mass resolution is shown in Figure 3.37 using tracks only reconstructed using the ITk or the current ATLAS Inner Detector. The mass resolution depends strongly on the pseudorapidity of the reconstructed B_s^0 candidates. Improvements are seen over the whole η range for the ITk with respect to the Run 2 detector.

The proper decay time t of a B_s^0-meson candidate is calculated from the transverse decay length L_{xy} to the displacement of the reconstructed decay vertex from the primary vertex

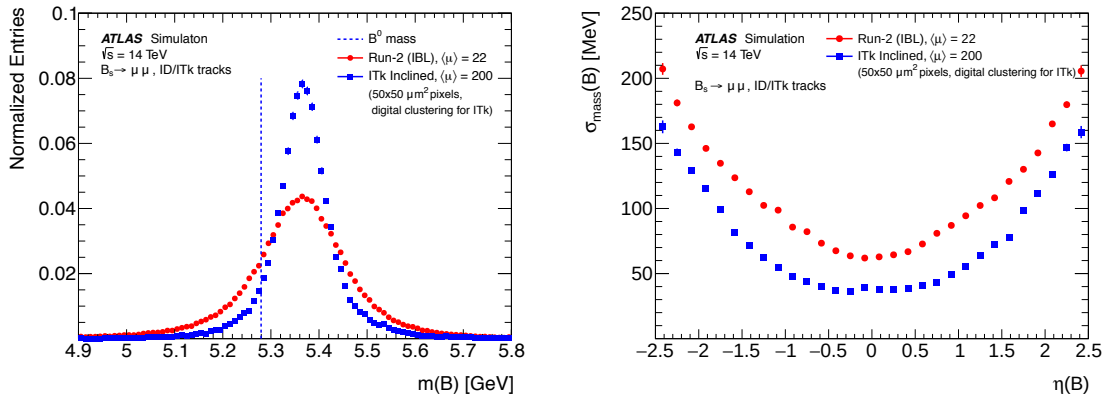


Figure 3.37: **Left**: Reconstructed $B_s^0 \to \mu^+\mu^-$ mass spectrum for muons with $|\eta| < 2.5$. For reference, the B_d^0 mass [57] is shown as a dotted line. **Right**: $B_s^0 \to \mu^+\mu^-$ mass resolution as a function of the B_s^0-meson pseudorapidity. For both cases the results for HL-LHC and Run 2 are compared. The resolution is defined as the RMS calculated from the difference between the reconstructed and generated invariant masses. The figure shows the mass resolution using only the ID/ITk track parameter measurement, evaluated at the fitted B-vertex.

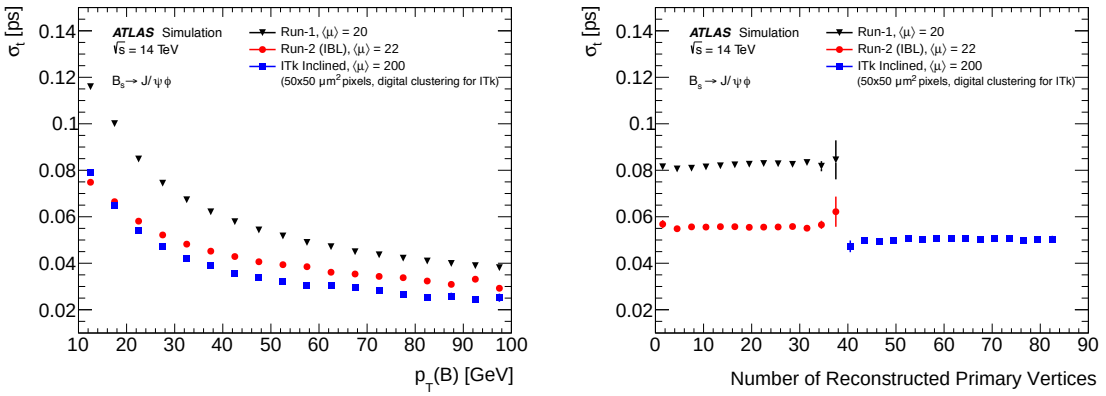


Figure 3.38: The average B_s^0 proper decay time resolution σ_t as a function of the transverse momentum p_{T} of the B_s^0-meson (**left**) and stability of the average B_s^0 proper decay time resolution against the number of reconstructed primary vertices (**right**), shown for ITk (blue), the Run 1 detector (black) and the Run 2 detector including the IBL (red), for their respective pile-up conditions.

in the transverse plane:

$$t = \frac{L_{xy} \cdot m_B}{c \cdot p_{\mathrm{T}}(B)}, \tag{3.6}$$

where $p_{\mathrm{T}}(B)$ is the reconstructed transverse momentum of the B_s^0-meson candidate and m_B denotes the mass value of the B_s^0-meson. To compute the decay length, the reconstructed

B_s^0-meson is extrapolated to the beam-line and the closest primary vertex[4] is selected. In order not to bias the measurement, the primary vertex position is refitted after removal of the signal B_s^0-meson candidate decay tracks. The proper decay time resolution as a function of the p_T of the B_s^0-meson for the Run 1 and Run 2 detectors, and for the ITk, is shown in the left plot of Figure 3.38. The resolution on the proper decay time is calculated per $B_s^0 \to J/\psi(\mu^+\mu^-)\phi(K^+K^-)$ decay candidate from the track measurement and primary vertex uncertainties. The improvement after installation of the IBL for Run 2 demonstrates the importance of the detector performance. For the ITk further improvements are observed. The stability of the resolution at high pile-up conditions is demonstrated in the right plot of Figure 3.38, showing no deterioration in events with the highest level of pile-up.

3.3.6 Prospects for SUSY Searches using the Disappearing Track Signature

Many supersymmetric models, for example anomaly-mediated SUSY breaking scenarios [58, 59], predict the supersymmetric partners of the Standard Model W bosons, the wino fermions, to be the lightest SUSY state. In such models, the lightest neutralino and chargino can be nearly mass-degenerate with a mass splitting around 160 MeV [60]. When produced in a high-energy collider, the chargino can acquire a relatively long lifetime [61], and leave multiple hits in the traversed tracking layers before decaying. A search for a disappearing track in the ITk can be exploited to search for these particles.

Monte Carlo simulated event samples are used to predict the background from SM processes and to model the SUSY signal. The simulated signal samples were generated assuming the minimal AMSB model [58, 59] with the ratio of the Higgs vacuum expectation values at the electroweak scale set to $\tan\beta = 5$, the sign of the higgsino mass term set to be positive, and the universal scalar mass set to $m_0 = 5$ TeV. Charginos were forced to decay into a pion and a neutralino. The detector response is taken into account using a set of parametrised response functions based on studies performed with Geant4 simulations of the upgraded detector in high luminosity pile-up conditions.

Events are required to contain at least one short track, called a tracklet. The tracklet reconstruction efficiency for signal charginos as a function of the decay radius inside the detector (shown in Figure 3.39) was estimated from a Geant4 detector simulation sample. A requirement of at least four pixel hits was used to maximise the sensitivity to shorter lifetimes.

The probabilities for an isolated electron or hadron to leave a disappearing track in the detector, because of interactions in the detector material, were calculated by correcting the Run 2 estimates for the material differences between ITk and the current ATLAS ID. The limited tracklet p_T resolution is taken into account by smearing the truth p_T distribution

[4] The ITk B-physics Monte Carlo sample was reconstructed with the Run 2 primary vertexing code and not with the AMVF algorithm described in Section 3.1.6. The Run 2 code yields fewer reconstructed vertices and a larger fraction of tracks from pile-up associated to the hard scattering vertex.

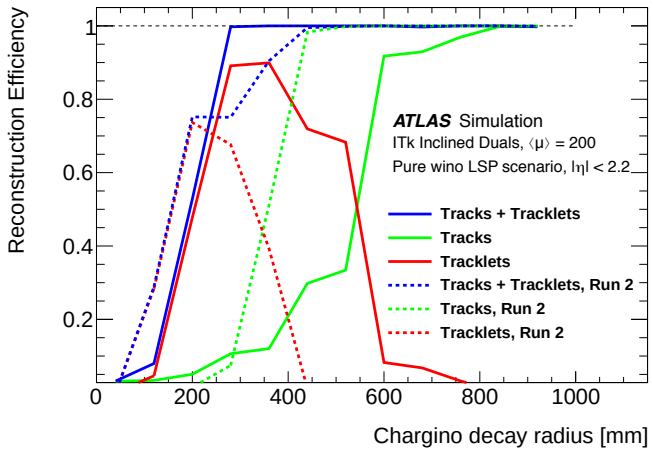


Figure 3.39: Disappearing track reconstruction efficiency as a function of decay radius. The reconstruction efficiency of pixel tracklets is shown in addition to the standard track reconstruction, for a minimum of 4 pixel hits. Shown as dotted lines are the corresponding reconstruction efficiencies for the current Run 2 detector.

Table 3.2: Expected yields in the signal region, together with their total uncertainty, for an integrated luminosity of 3000 fb^{-1}. The expected number of events for two signal samples is also reported.

	Events in Signal Region
Expected Background	4.6 ± 1.4
Fake Tracklets	4.6 ± 1.4
Hadron and Electron mis-Identification	0.02 ± 0.01
Wino-like $m(\tilde{\chi}_1^{\pm}) = 800$ GeV, $\tau_{\tilde{\chi}_1^{\pm}} = 0.2$ ns	11.9 ± 0.8
Higgsino-like $m(\tilde{\chi}_1^{\pm}) = 200$ GeV, $\tau_{\tilde{\chi}_1^{\pm}} = 0.04$ ns	18.8 ± 5.6

with the detector resolution taken from simulation. The probability of reconstructing a fake tracklet was estimated using Geant4 detector simulation.

Events with significant initial state radiation (ISR) are selected, by requiring at least one jet with a p_{T} larger than 300 GeV, to ensure that the $\tilde{\chi}_1^0$ are boosted. The minimum azimuthal angular distance, $min\{\Delta\phi(\mathrm{jet}_{\mathrm{ISR}}, E_{\mathrm{T}}^{\mathrm{miss}})\}$, between the leading four jets with $p_{\mathrm{T}} > 50$ GeV in the event and $E_{\mathrm{T}}^{\mathrm{miss}}$, is required to be greater than 1. Signal candidate events are required to have a missing transverse momentum $E_{\mathrm{T}}^{\mathrm{miss}} > 450$ GeV and a leading tracklet p_{T} >250 GeV. A 30% systematic uncertainty on the background yields was assumed, as observed for the Run 2 analysis [62]. The composition of the expected background, as reported in Table 3.2, is largely dominated by fake tracklets.

Expected limits at 95% CL are shown in Figure 3.40 as a function of the $\tilde{\chi}_1^{\pm}$ mass and lifetime for a pure wino and a pure higgsino LSP scenario. Simplified models including both $\tilde{\chi}_1^{\pm}$ pair production and associated production of a $\tilde{\chi}_1^{\pm}$ with a $\tilde{\chi}_1^0$ are considered. For com-

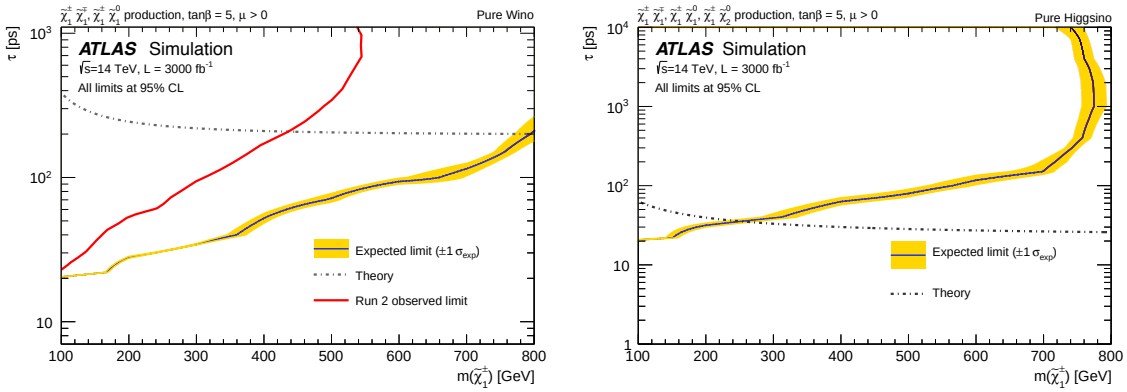


Figure 3.40: Expected exclusion limit at 95% CL from the analysis of 3000 fb^{-1} of 14 TeV proton-proton collision data as a function of the $\tilde{\chi}_1^{\pm}$ mass and lifetime. Simplified models are considered, including both $\tilde{\chi}_1^{\pm}$ pair production and associated production of a $\tilde{\chi}_1^{\pm}$ with a $\tilde{\chi}_1^0$. In the case of pure higgsino models, the associated production of a $\tilde{\chi}_1^{\pm}$ with a $\tilde{\chi}_2^0$ is also included. The yellow band shows the 1 σ region of the distribution of the expected limits. The median of the expected limits is shown by a blue line, with the excluded region above the contour line. **Left**: Expected limits for the pure wino LSP scenario. The red line shows the limits from the analysis of Run 2 data [62]. **Right**: Expected limits for the pure higgsino LSP scenario. The chargino lifetime as a function of the chargino mass are shown on both plots as a dotted line for an almost pure wino LSP scenario [60] and pure higgsino scenario [63], at two loop level.

parison the current Run 2 limit for 36.1 fb^{-1} in the wino LSP scenario [62] is shown as well. The HL-LHC dataset of 3000 fb^{-1} will allow the extension of the sensitivity for $\tilde{\chi}_1^{\pm}$ $\tilde{\chi}_1^0$, $\tilde{\chi}_1^{\pm}$ $\tilde{\chi}_2^0$ and $\tilde{\chi}_1^{\pm}$ pair production up to 250 GeV, assuming a pure higgsino scenario. Future improvements in the understanding of experimental systematic uncertainties on the SM backgrounds, mainly driven by the reconstruction of fake tracklets, would provide additional gains in sensitivity.

3.3.7 Prospects for SUSY Searches using the Displaced Vertex Signature

Massive and long-lived particles arise naturally in many models of beyond the Standard Model physics. Particles with lifetimes from $\mathcal{O}(10)$ ps to $\mathcal{O}(10)$ ns will frequently decay inside the inner tracker, and their electrically charged and stable decay products can be reconstructed as tracks with measurably distant impact parameters with respect to the primary vertex of the event. The reconstruction of displaced tracks poses separate challenges compared to reconstructing tracks from prompt particles, due to fewer hits along the track and a larger parameter phase space for track finding. Searches for such scenarios have been conducted by ATLAS during Run 1 and Run 2 [64, 65].

The efficiency with which ITk can reconstruct tracks originating from displaced vertices is tested in a benchmark SUSY model consisting of a gluino with a mass of 2 TeV and a

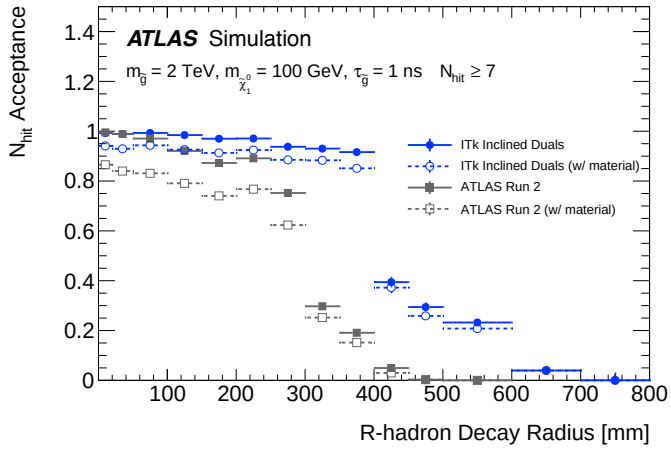


Figure 3.41: The probability that the charged decay products ($p_T > 1$ GeV) of a 2 TeV *R*-hadron with a lifetime of 1 ns pass through at least seven silicon layers, as a function of the radius of the *R*-hadron decay, for both the Run 2 and ITk Detector layouts.

lifetime of 1 ns. The long-lived gluino hadronises into an *R*-hadron, which decays into a 100 GeV neutralino and hadrons. A dedicated reconstruction algorithm is currently used in Run 2 to recover efficiency for reconstructing such displaced particles. As such algorithms have not yet been optimised for the ITk, this study assumes that the achievements of the Run 2 algorithm can be reproduced, given that the necessary hits are present. In Reference [66], it is shown that for particles which leave at least seven hits in silicon layers[5] of the Run 2 ID, the reconstruction efficiency is nearly 100%. For photon conversions, the reconstruction efficiency for secondary particles was studied for the ITk using a dedicated track reconstruction (see Section 3.2.1).

The probability of producing at least seven silicon hits in the ITk geometry is tested with a simplified simulation which has a description of the ITk active sensors and a modelling of the magnetic field. The kinematics and location of the decay products of the *R*-hadron are injected into the simulation and their trajectories are extrapolated through the detector model. Figure 3.41 shows the average probability for the decay products of a 2 TeV *R*-hadron with a lifetime of 1 ns to pass through at least seven layers of active silicon sensors in both the ITk and current (Run 2) Inner Detector geometries. The effect of taking into account the inefficiency due to hadronic interactions in the detector material is shown as well. Only charged decay products with $p_T > 1$ GeV are considered. The larger volume and increased number of active silicon layers of the ITk compared to the current Inner Detector shows a clear advantage for reconstructing displaced tracks, increasing the production radius at which decaying particles are efficiently reconstructable from around 300 mm to 400 mm, and extending some reach up to 550 mm. In addition, the larger number of silicon layers in the ITk leaves open the possibility of increasing the number of required hits-on-track in

[5] Each layer of silicon strips contributes two hits.

order to further suppress tracks from combinations of unassociated hits, if needed at higher pile-up.

4 Technical Overview

4.1 Introduction

In this chapter the reader is introduced to the most important aspects of the design of the ITk Pixel Detector. The design drivers are explained, the key components and proposed technical solutions are introduced. The measurements that demonstrate the required performance are presented at a relatively high level. More detailed descriptions of the design and a more complete report of the ongoing research and development as well as the preparation for production will be presented in the later Chapters.

4.2 Key requirements for the ITk design

The HL-LHC will operate in a regime of leveled instantaneous luminosity, with a maximum at the beginning of each fill of up to $\mathcal{L} = 7.5 \times 10^{34}$ cm^{-2}s^{-1} which corresponds to approximately 200 inelastic proton-proton collisions per beam crossing. Since the release of the Strip TDR in December 2016 the target Integrated Luminosity was increased from 3000 fb^{-1} to 4000 fb^{-1} which is now in accordance with what the HL-LHC machine will be able to deliver over the lifetime of Phase II [67]. This increase in integrated luminosity is still within the safety factors used in the design and prototyping of the Strip Tracker, and the design presented in [1] is compliant with this new requirement. For the new Pixel tracker, in order to meet the required total integrated luminosity and maintain good tracking performance over the lifetime of Phase II, it is foreseen that the inner two layers of the Pixel Detector will be replaced part way through the HL-LHC program.

The replacement detector is not described in this volume as it is entirely possible that it will be made using new technologies. The requirement to be able to replace the inner section of the ITk Pixel Detector during a long LHC shutdown (i.e. during a "large opening" of the ATLAS Detector) places severe constraints on the design of the pixel package. The mechanical design, and in particular its function in the support hierarchy, means that the outer section should not rely on the presence of the inner section. In addition, the pixel package must be able to support the beam pipe without requiring the inner section to be present. This is the same hierarchy already implemented in the current ID when the Insertable B-Layer was added in 2014 around a new, smaller radius beam-pipe [2, 3]. In this way it is possible to guarantee the integrity of the ATLAS Detector and some limited data

taking capabilities even in event of catastrophic failures of the inner section, such failures that could be repaired in a long shutdown. In terms of radiation tolerance, the replaceable part of the Pixel Detector is designed for a maximum dose of 2000 fb^{-1}. As illustrated in Table 2.9, when a safety factor of 1.5 is applied, this implies that the components installed in Layer 0 must be radiation tolerant up to a dose of 9.9 MGy.

As illustrated in Chapter 2, the acceptance of the Pixel Detector has been extended to ± 4 units of pseudo-rapidity, which requires an increase of the number of pixel layers and of the outer radius of the pixel volume. The new detector has been designed with less inactive material in the tracking volume (comprising less than one radiation length up to a pseudo-rapidity of 2.7) and will deliver a performance that is at least as good, and in many cases better, than the existing detector, but in a much more hostile tracking environment with an average of up to 200 proton-proton interactions per beam crossing. The ITk has been designed with efficient pattern recognition and track reconstruction in mind, to deliver high track reconstruction efficiency and a low rate of fake tracks. Up to a pseudo-rapidity of 2.7, this means efficiency greater than 99% for muons with transverse momentum above 3 GeV and greater than 85% for pions and electrons above 1 GeV, while keeping fake rates below 10^{-5}. In addition, the performance is robust against losses of up to 15% of individual channels or modules that could conceivably occur over the lifetime of Phase II.

At the start of HL-LHC operation, the ATLAS Detector will be read out with a single Level-0 trigger (L0) running at an average rate of 1 MHz with a maximum latency of 10 μs. The ITk Detector will be able to deliver data to a fast track reconstruction processor that will deliver track parameters as the input to High Level Trigger processing (HLT), in a trigger architecture that is similar to the one used in the present ATLAS FTK [68]. This trigger architecture is called "L0-only" and is considered to be the baseline for ATLAS. An alternative architecture is considered, that makes it possible to use ITk data in the first part of the trigger decision. This hierarchical scheme uses an additional level of trigger, called Level-1 (L1), and it is called "L0-L1". In the L0-L1 scheme the L0 trigger, generated, as in the L0-only scheme, using calorimeter and muon spectrometer data, is dispatched to all the detector elements that will provide data for the track trigger or in the refinement of the L0 muon or calorimetric decision. It is possible to send the L0 trigger only to a specific "region of interest" (RoI) identified as a part of the L0 decision. L0 will have a maximum rate of 4 MHz and a maximum latency of 10 μs. The Level-1 trigger, formed with calorimeters, muon spectrometer and tracker data, will have a maximum frequency of 800 kHz and a maximum latency of 35 μs. The "L0-only" and the "L0-L1" schemes are illustrated in Figure 4.1. More details concerning the triggering strategy can be found in the Phase II ATLAS Trigger and DAQ TDR [44].

The full ITk will be read out at L0 in the "L0-only" scheme. In the "L0-L1" scheme, different strategies will be employed in the different ITk sub-detectors. In particular, the Strip Detector will support L0 read-out at 4 MHz for 10% of the modules belonging to the Region of Interest (RoI) identified at L0, followed by full read-out at L1. An additional trigger signal (R3) will be used by the central trigger processor to specify the location of the RoI. The three

outer Pixel layers, barrel and end-caps, will support full read-out at 4 MHz. For the two inner Pixel layers full read-out at 4 MHz would require a prohibitive number of data cables; this part of the detector will only support full read-out at 1 MHz, and will be read out at L1. As a consequence, the data from the two inner layers will not be available at the track trigger processor to build the L1 decision, that will be based on Strips (inside the RoI) and outer Pixel layers. More details about the strategy adopted to read out the Pixel Detector in the two trigger schemes are given in Chapter 10. It must be noted that the L0-L1 scheme requires more output bandwidth, and, as a consequence, more data cables. The extra cables will have to be installed inside the detector from the beginning, even if the L0-L1 scheme will be adopted in a second phase of HL-LHC operations. The capability of handling the L1 trigger latency of 35 μs is a requirement for the pixel front-end chip, that will be explained in Chapter 6.

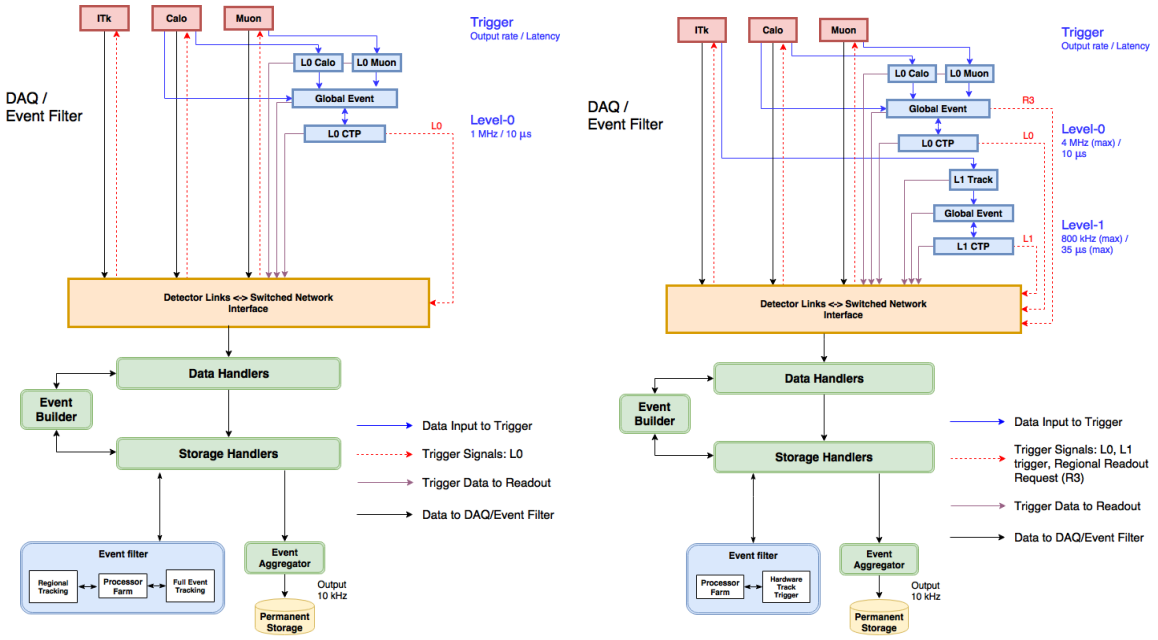


Figure 4.1: Schematics of the ATLAS Phase-II trigger scheme. **Left**: baseline with one hardware trigger level (Level-0, L0). **Right**: mode of operation with two hardware trigger levels (Level-0, L0, and Level-1, L1).

4.3 Pixel Module

The design of the hybrid pixel module is similar to the one adopted for the present ATLAS Pixel Detector and for the IBL.

"The hybrid pixel module" is made of two parts: a passive high resistivity silicon sensor and a front-end read-out chip fabricated in CMOS technology, called a bare module, and

a flexible PCB, called a module flex. The silicon sensor and front-end read-out chip are joined using a high density connection technique called "flip-chip bump-bonding". All connections to the bare modules are routed to the active elements via the module flex, which is glued to the backside of the sensor. A schematic of the elements of a bare pixel module is presented in Figure 4.2. Compared to the design used for the IBL, the ITk Pixel Module required several improvements:

- The pixel size has been reduced to 50×50 μm^2 or 25×100 μm^2 to improve intrinsic resolution and two track separation.
- The design of the read-out chip has been improved in several ways: the analogue front-end can operate at lower threshold compensating for the loss of collected charge due to radiation damage, the read-out architecture has been improved to comply with the higher hit density and event rate and the radiation tolerance has been increased to 1.4×10^{16} n_{eq}/cm^2. The power consumption was also reduced and this has a positive effect on the material budget (less massive cables and reduced cooling requirements).
- The output bandwidth has been increased to 5.12 Gb/s per front-end chip, to cope with the hit rates in the innermost section of the tracker.
- The size of the module has been increased; with the largest module the size of four front-end chips, which is about 16 cm^2, to reduce cost and fabrication time.
- A serial powering scheme will be adopted to reduce the number of cables and the amount of inactive material in the tracker.

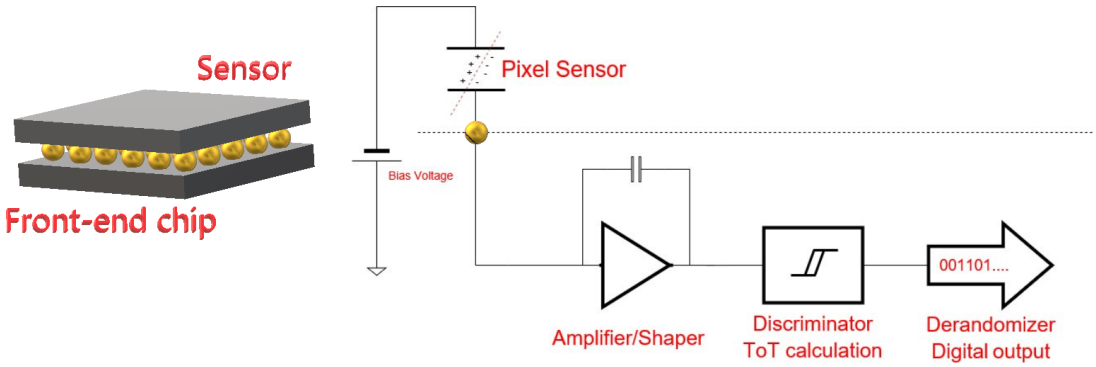


Figure 4.2: Schematic view of a bare pixel module.

There will be three types of hybrid pixel modules: Quad modules consisting of four chips bump-bonded to a single sensor, (around 4×4 cm^2 in area), which are used in the outer flat barrel layers and in the outer end-cap rings. Dual modules consisting of two front-end chips bump-bonded to a single sensor, (around 4×2 cm^2 in area), which will be used in the innermost barrel layer and the inclined part of the outer barrel, to optimizes the radial

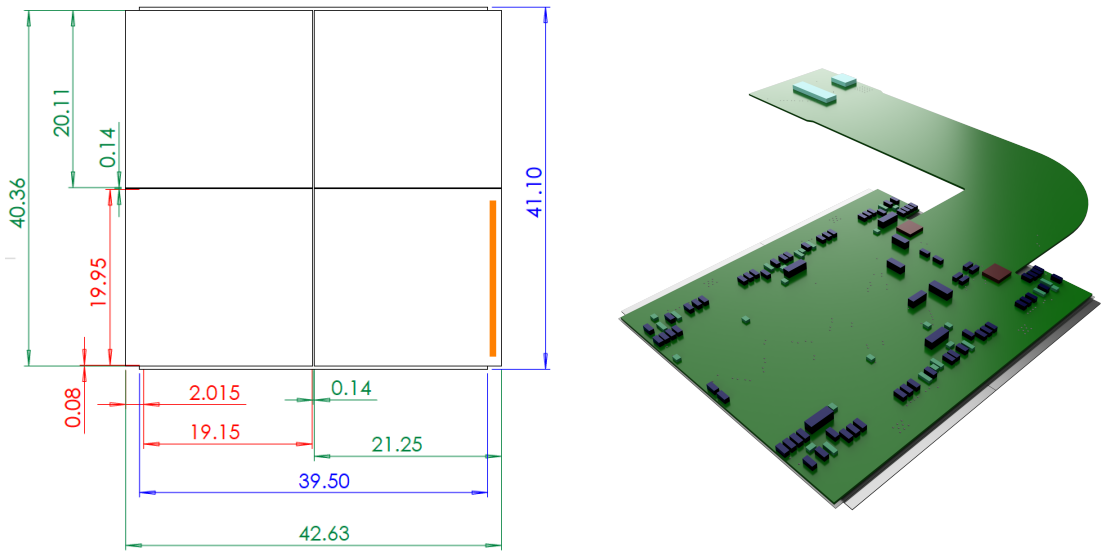


Figure 4.3: Left: Drawing of a quad module with four pixel front-end chips viewed from the front-end chip side, all dimension in mm. Front-end chip dimensions are green with the wire-bond pad area indicated in gold on the lower right chip. Sensor dimensions are in blue and in red the distances from and to the outermost bump-bond pads of the lower left chip are given. Right: 3D view of a quad module for the outer barrel flat section viewed from the module flex side.

tiling while introducing minimal material. In addition, the inclined part of the innermost barrel layer requires single-chip modules consisting of one front-end chip bump-bonded to a sensor, (around 2×2 cm^2 in area).

Figure 4.3 shows a drawing and a three dimensional rendering of a quad module based on the ATLAS pixel front-end chip with 50×50 μm^2 pixel size. As the dimensions of the new pixel front-end chip are not finally defined, an active size of 19.2×20 mm^2 (384×400 pixels) and a periphery region of 2×20 mm^2 are assumed as the current baseline. The area between read-out-chips is minimized and fully active being covered by ganged pixels on the sensor. All connections (clock and command input, data output, low voltage and sensor high voltage) to the modules are routed to the active elements via a flexible printed circuit (module flex) which is glued to the backside of the sensor. Internal to the module, the module flex connects the high voltage bias to the sensor's backside and the low voltage supply to the front-end chip. For multi-chip modules, the front-end chip chips are connected in parallel for powering from a common low voltage input on the module flex. A single downlink data line is connected to the module and the signal is routed in parallel to each chip in the module. The clock and command signals are extracted from this data by the front-end chip. The uplink data streams from the front-end chip are multiplexed together into a number of high speed electrical data cables, which are routed to the opto-converters. The data signals to and from the module are transmitted on differential pairs and are AC

coupled. For module temperature monitoring a temperature sensor (NTC) is connected to the Pixel DCS chip. The connections to the front-end chips and the sensor are made with wire bonds and passive components, such as decoupling capacitors and termination resistors, are mounted on the module flex.

The power consumption of a module is around 7 W and this must be removed to prevent thermal run-away and a per pixel leakage current above 10nA. The modules will be placed on the local support, with the backside of the front-end chips in contact with the support. This interface is part of the thermal path between the module and the cooling fluid.

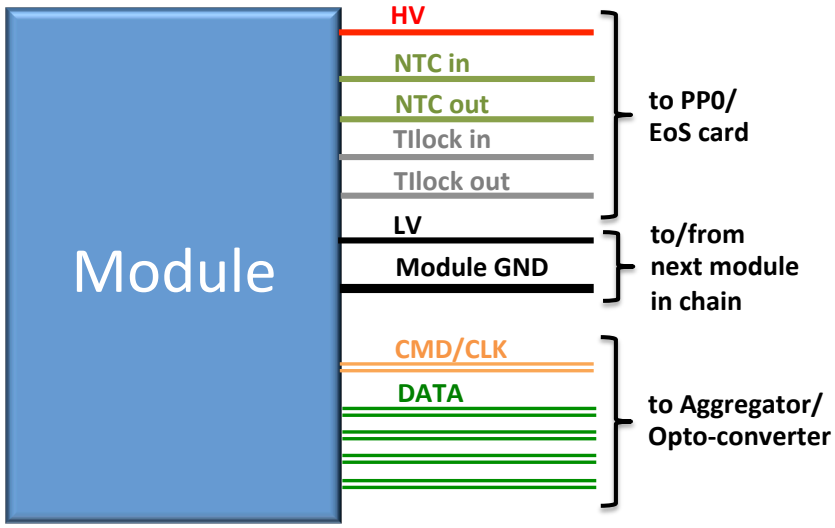


Figure 4.4: Schematic of the electrical connection of an ITk pixel module.

Apart from the three module types (quad modules, dual modules and single-chip modules) the modules vary slightly in the design of the connection between the module flex and the local support services especially between the flat barrel and the inclined barrel sections. For the outer barrel layers three different module flex types are required, one for the quad modules in the flat section and two for the dual modules in the inclined section. The inner barrel layers need five more flex types and one more quad module type is required for the outer end-caps. Therefore up to nine different module flex types are needed resulting in nine different module types

The details of the pixel module structure, the assembly and interconnection techniques and the quality control and quality assurance procedures are described in Chapter 8.

4.3.1 Front-end chip design in 65 nm technology

The IBL front-end chip (FE-I4) was designed in IBM 130 nm technology. To meet all of the complex requirements for the front-end chip within a significantly smaller unit cell size a new CMOS technology must be used.

Together with colleagues from CMS a decision has been taken to exploit the 65 nm technology, because it is dense enough to fit the digital architecture and there was indication that the analogue performance and radiation tolerance would fulfil the requirements for Pixel Detectors at HL-LHC. The same technology is being used in other projects for HL-LHC (e.g. for the data concentrator GBT [69] chip), and the ordering of wafers is covered by a CERN frame contract. This significantly simplifies the purchase of the parts for bulk production and guarantees a strong support in the HEP community.

Because of the radiation tolerance requirements, specifically for the innermost Pixel layer, an intense program of qualification of the different components of the standard cell library was carried out in 2015 and 2016. The goal of this campaign was to develop a chip with radiation tolerance beyond 5 MGy [70]. This radiation tolerance is sufficient for the ITk Pixel Detector over the entire Phase II program assuming that the two inner layers will be replaced at least once during the HL-LHC program.

The actual radiation hardness of the ATLAS FE chip is not yet known, and it must be noted that the radiation tolerance of a complex design like a pixel front-end chip is not easy to predict by extrapolating the performance of a collection of individual components. The actual tolerance will be measured on the first large prototype of the new chip. The only strict requirement in terms of radiation tolerance is the one imposed by the ITk layers that will not be replaced, and this limit is well below 5 MGy for 4000 fb^{-1} (see Table 2.9). The limit for the inner replaceable layers is close to 10 MGy for 2000 fb^{-1}, and the measured FE chip tolerance may be close to the acceptable limit. In this case it may be necessary to plan for a replacement before the 2000 fb^{-1}, considering at the same time the adoption of a more radiation tolerant solution for the replacement detector.

Besides the permanent damage induced by radiation, the chip will have to be robust with respect to local ionization effects, that could temporarily alter the functionality of the chip (SEU, single event upsets). This type of radiation induced effects is particularly dangerous for the digital parts, where memory cells contents or flip-flop status can be changed, causing a malfunction of the chip. The most critical flip-flops are implemented using a redundancy mechanism in which the output is determined by the majority output of three flip-flops connected to the same inputs. The same mechanism is difficult to use for the memories holding the configuration of the front end, as this would require too much space. It will therefore be necessary to periodically refresh the front-end chip configuration during data taking, to compensate for any upsets induced by the radiation. The refresh rate will depend on the sensitivity to single event upsets of the memory cells, on the distance from the interaction point and on the LHC background conditions. Taking into account the most

pessimistic scenario, the system will be designed to allow for a refresh rate of 10 Hz during data-taking.

The development of the new Pixel front-end chip is carried out within the framework of the RD53 collaboration [71], that will provide a common set of building blocks that can be used in the design of the ATLAS and the CMS chips. A large scale (2 cm^2) ATLAS-CMS prototype called RD53A has been fabricated in wafer form and just received at the time of this writing (Figure 4.5). Basic functionality has been already confirmed and a detailed characterization program including irradiations and construction of bump-bonded assemblies is now starting. The RD53A design already satisfies most of the requirements of the final ATLAS chip and will be used to demonstrate the performance of the new technology and test the Pixel module concept that will be developed around it. The design of the front-end chip and of the ancillary components of the Pixel module read-out is described in Chapter 6.

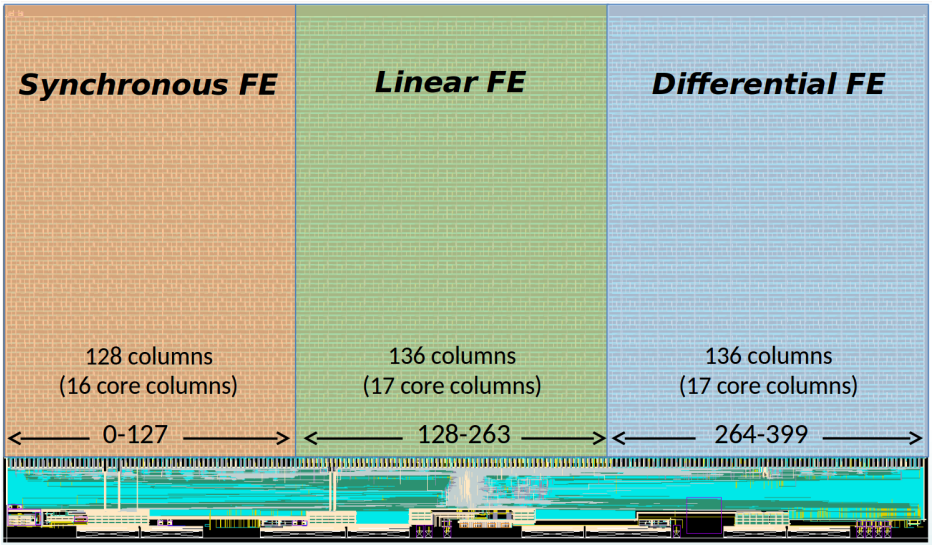


Figure 4.5: Photograph of the RD53A integrated circuit. The areas of the chip dedicated to the three different front-end amplifier designs are marked on the picture.

A lot has been learned from the experience with the FE-I4 design [72]. The new chip is optimized for the specific requirements of the inner layers of an HL-LHC detector. Particular attention is given to the capability of handling a large hit density, 100 or more hits/front-end chip per 25 ns bunch crossing (Figure 4.6). As illustrated in Section 6.3.1, the RD53A chip implements three different front-end amplifier designs and two different read-out architectures that will be compared to select the best solutions for the final design. To reduce the data volume at the digital output of the chip, hits coming from contiguous pixels (2×2 or 1×4 pixel arrays are tested) are grouped together and a single data word for the group is sent, indicating which are the pixels above threshold. This corresponds to sending a single data block per cluster (or part of a cluster) instead of a single block per hit. In the regions of the detector where the average cluster size is large, the average occupancy of a group of pixels can be larger than 1.6, and this data encoding strategy becomes advantageous.

The advantage in data compression becomes higher as the group occupancy increases, so, it is important to match the shape of the pixel group with the cluster shape to obtain good results.

The digital data output stage of RD53A uses four 1.28 Gb/s lines for a total output bandwidth of 5.12 Gb/s. In case less output bandwidth is required, the chip can be configured to use only one or two output lines. High speed transmission at 5.12 Gb/s will be managed by a custom active cable solution based on a commercial connector and twin-axial cable technology but using custom, radiation hard integrated circuits called "an Aggregator chip" and "an Equalizer chip". These chips are also described in Chapter 6. They are designed in the same process as the front end chip and share many elements such as digital libraries and I/O structures. The Aggregator chip has four 1.28 Gb/s inputs and one 5.12 Gb/s output. The same Aggregator chip will serve a single FE chip for the inner layer and up to four FE chips at higher radius, making for a modular system with a common data transmission for all the layers. The Aggregator chip shares some features with the CERN lpGBT chip, but is optimized for its single purpose and is sufficiently different that it must be a separate chip, nevertheless designed in collaboration with the lpGBT team. The Equalizer chip is a 5.12 Gb/s receiver including equalization matched to the twinax cable design for reliable transmission. The challenges of high speed electrical transmission are decoupled from the FE chip development (technically and schedule-wise) through the active cable system design.

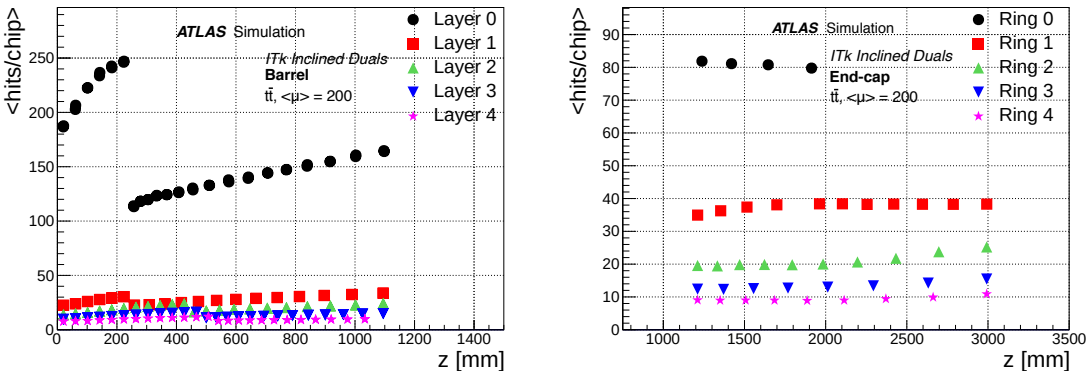


Figure 4.6: Average number of hit pixels per chip per event (hits/chip) in the barrel layers and end-cap rings (simulated $t\bar{t}$ events with 200 minimum bias events superimposed).

Another aspect that will be exploited in the new chip is the support for serial powering that will be adopted in the ITk Pixel Detector to reduce the volume of the cables needed to power the detector. For this reason, the chip is equipped with a regulator that is designed to maintain a constant current. This approach makes it possible to use the serial powering scheme that will be illustrated in Chapter 11, but has the other important advantage of maintaining a constant power consumption during physics operation, which prevents temperature fluctuations that would limit the mechanical stability of the detector. The average

power dissipation will be measured on the RD53A chip; the assumption used so far in the design of the cooling system is 0.7 W/cm^2. However, it will be possible to operate the FE chip in a reduced power mode by providing a limited current to the regulator. This feature will be useful during the construction of the Pixel Detector, when it may be necessary to verify the functionality of a module without a complete cooling system.

Several small prototypes of the new front-end chip have been submitted and tested before RD53A. Even if these chips are too small to provide conclusive results on performance, they all worked well, as reported in Section 6.5. In particular, noise and threshold figures are in accordance with the expectations from the pre-submission simulations. This is encouraging and gives confidence in the design and in the ability to control this complex technology. The RD53 team is already working on the design of the first version of the full size chip, that will be used for the Pixel Detector pre-production (ITkPix-V1). Considering that most of the functionalities needed for the ATLAS chip are already available in RD53A, there is considerable confidence that the design should be complete by the end of 2018 and the submission of ITkPix-V1 is scheduled for the beginning of 2019. A second iteration of the design is planned (ITkPix-V2), to give a chance to fix problems observed with the first version and to introduce small improvements. The submission of ITkPix-V2 is scheduled for Q1 2020.

4.3.2 R&D on pixel sensors

In going from the IBL to the ITk the main change in sensor technology is the increase in the required level of tolerance to radiation. For standard high resistivity silicon sensors, the effect of radiation damage is progressive and results in a reduction of collected charge. This can be mitigated by increasing the bias voltage. The increase of the bias also increase the current and this is critical for the performance of the analogue front-end that can compensate up to 10 nA/pixel. Another issue associated with the increase of the current is the "thermal run-away", a positive feedback loop related to the fact that the leakage current increases with the temperature. If the cooling system cannot compensate the self heating of the sensor, current and temperature will increase in an uncontrolled way. Therefore, it is important to make sensor design and technology choices for each region that can guarantee stable thermal operation and high intrinsic efficiency over the active lifetime of the sensor. For the innermost layer, the solution is provided by 3D sensors, while for the rest of the layers planar sensors will be used.

The 3D sensor design differs from the standard planar sensor in that the charge collecting electrodes (columns) are oriented perpendicular to the sensor surface and penetrate through the surface (entirely or almost entirely). See Figure 4.7 for a schematic view of the electrode position in a 3D sensor compared to a planar sensor. Provided the distance between the columns is properly designed, these detectors offer good charge collection efficiency even in the case of severe radiation induced bulk damage. The number of collecting electrodes per pixel can be tailored to the application, with one electrode per pixel known

as a 1E design and two electrodes known as a 2E design. Historically, one draw-back of 3D technology was a rather limited production yield, so the R&D effort in this area has been focused on the improvement of the fabrication procedures. Several process improvements have been implemented by three potential vendors, including more efficient techniques to etch the column electrodes, single sided wafer processing and larger (6″) wafers. Given the topology of the electrodes, reducing the pixel size is not a trivial process: the cell capacitance can increase and there could be isolation problems due to the limited space available to fit the bonding pads. This is particularly true for the 25×100 μm^2 geometry if two collecting electrodes are used per unit cell. The pixel capacitance of a 3D sensor is approximated by a coaxial capacitor unlike a planar device. As a consequence the detector capacitance increases with smaller pixel size and reduces with sensor thickness, converse to the planar sensor. From the sensor performance perspective, the optimal active thickness is a trade-off of collected charge after irradiation, demanding a larger active thickness and detector occupancy that can be reduced if the active thickness is reduced. The total thickness on the other hand is a trade-off of material budget and mechanical handling. For ITk the typical active thickness used is 150 μm; an extra 100 μm passive support wafer is added to facilitate handling and flip-chip bump-bonding.

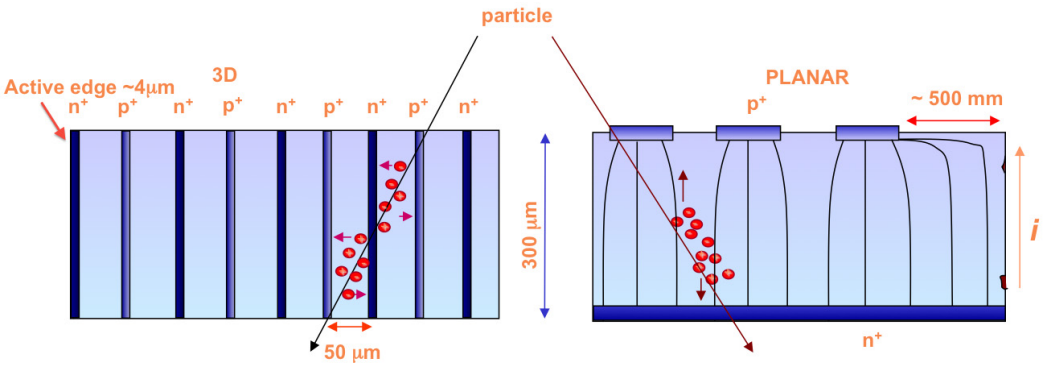


Figure 4.7: Schematic view of electrode arrangement and charge collection in planar and 3D pixel sensors.

The 3D technology has matured in the last 20 years and is now becoming a standard choice where extreme radiation hardness is critical. Within the ATLAS experiment both the ATLAS Forward Proton detector (AFP) [73] and part of the Insertable B-Layer (IBL) [3] rely on 3D pixel sensors. This first generation of 3D sensors with pixel sizes of 50×250 μm and a sensor thickness of 230 μm already demonstrated a radiation tolerance up to 9×10^{15} n_{eq}/cm^2 [74]. Beyond increased radiation hardness, the ITk Pixel Detector requires 3D sensors with smaller pixel sizes and thinner active areas to improve intrinsic position resolution and reduce detector occupancy in the innermost layer. To this end, the research and development effort is well underway. Productions of 3D devices with different thicknesses and pixel sizes of 25×100 μm^2 and 50×50 μm^2, but compatible with the existing (as of 2017) FE-I4 read-out ASIC, have been carried out and been characterized before and

after irradiation. In particular, hit reconstruction efficiencies greater than 97% with an associated power dissipation of about 10 mW/cm^2 have been demonstrated for 3D devices with 50 $\times$ 50 μm^2 pixel geometries irradiated with 24 GeV protons up to 1.4 $\times$ 10^{16} [75]. The key to the excellent thermal performance of 3D sensors is the lower bias voltage needed to achieve high hit reconstruction efficiency when the pixel size is reduced. This is shown in Figure 4.8.

The voltage $V_{97\%}$ required to achieve an efficiency of 97% is defined as the operation voltage. It is shown as a function of fluence and is compared for the new small-pitch and the IBL generation [76, 75]. The significant improvement due to the smaller 3D electrode distance and hence less trapping is visible. For example at 5 $\times$ 10^{15} n_{eq}/cm^2, the IBL-generation devices need 120 V at 0° tilt and 1.5 ke$^-$ threshold to reach 97%, compared to only 40 V for a 3D cell of 50 $\times$ 50 μm^2 under the same conditions.

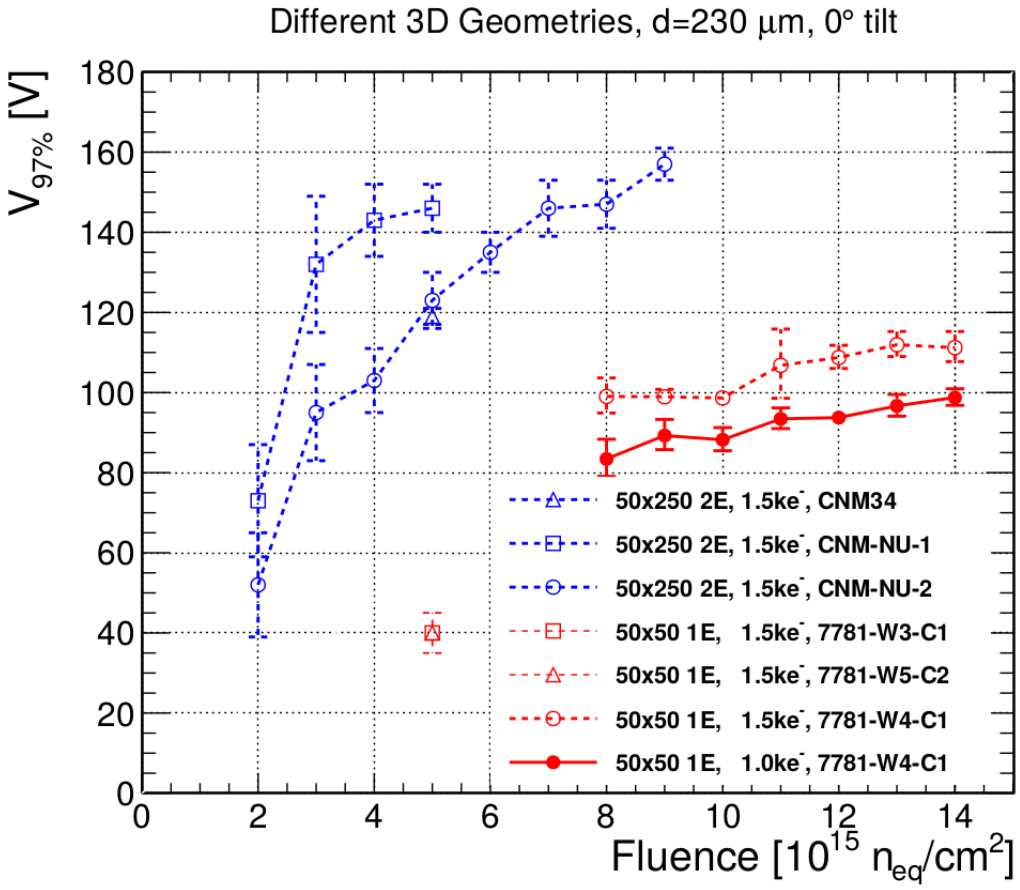


Figure 4.8: Voltage to reach 97% hit reconstruction efficiency as a function of fluence, comparing the IBL generation of 3D sensors (50 $\times$ 250 μm pixels with 2 collecting electrodes, 2E) and the ITk Pixel Detector baseline of 50 $\times$ 50 μm^2 with 1 collecting electrode, 1E, pixel sensors.

Furthermore, specific productions of 3D sensors compatible with the first ITk prototype front-end chip (RD53A) have been, or are being, completed at CNM (Barcelona), FBK (Italy) and Sintef (Norway). Details on the development of 3D sensors and recent test results are given in Section 5.4.

For the outer layers, planar n-in-p sensors are considered; n-in-n have also been studied (as used in the present ATLAS Pixel Detector), but n-in-p has the advantage that simpler (and hence cheaper) fabrication procedures can be used. Leakage currents after irradiation can be controlled by reducing the sensor thickness: 150 μm is adequate for most of the detector, but 100 μm is necessary in Layer 1 and possibly Layer 2 to meet the restrictions imposed on the power dissipation at the end of life. Another optimization that is needed for the ITk planar sensors is related to the so-called "bias grid", a mesh that is used to apply voltage to all the pixels in parallel and measure the I-V and C-V curves to test the sensor tile before coupling to the front-end chip. When the pixel size becomes comparable to the width of the traces used to build the grid, particular care must be taken to control field effects that may locally reduce the efficiency after irradiation. Several different geometries of the bias grid have been studied, to ensure full efficiency over the entire pixel cell.

Planar pixel sensors can also be further processed in order to extend the depleted region up to the edges without an increase of the leakage current. Implanted or diffused vertical sides have been used to control edge currents and to allow to reduce significantly the number of guard rings and the area allocated to them. In this way, significant hit efficiency can be maintained also in a region which would be normally inactive. Trenches are realised around the perimeter of each sensor with Deep Reactive Ion Etching (DRIE) using the mechanical support offered by an handling wafer. Trenches are then doped, extending the p+ implant of the backside. FE-I4 compatible sensors have been produced with this method at ADVACAM (Finland) and FBK.

In general, as will be discussed in Section 5.5, the design of the planar sensors for the ITk is rather mature, and several vendors have already demonstrated that they will be able to produce sensors that can survive up to 10^{16} n_{eq}/cm^2 maintaining high efficiency with a bias voltages between 400 V and 500 V. The hit efficiencies of FE-I4 compatible sensors produced by different vendors in a range of thickness from 100, 130 to 150 μm were compared after irradiation at different fluences. A summary of the performance of devices irradiated at 10^{16} n_{eq}/cm^2 is shown in Figure 4.9 [77]. It can be noted that sensors of 100 μm and 150 μm thicknees show the highest hit efficiency at moderate voltages of 400-600 V. More results are reported in Chapter 5.

The hit efficiency for 50×50 μm^2 pixel cells has been estimated by using FE-I4 compatible sensors with a modified geometry bonded to an FE-I4 FE chip. At a fluence of 5×10^{15} n_{eq}/cm^2 and a bias voltage of 600 V, the hit efficiency for a cell without biasing structures was calculated to be 97.5 % for a 100 μm thick sensor. The performance of 50×50 μm^2 and 25×100 μm^2 pixel cell sizes for 150 μm thin sensors have also been investigated with lower threshold thanks to the low noise of one of the RD53 small prototype chips (FE65-P2).

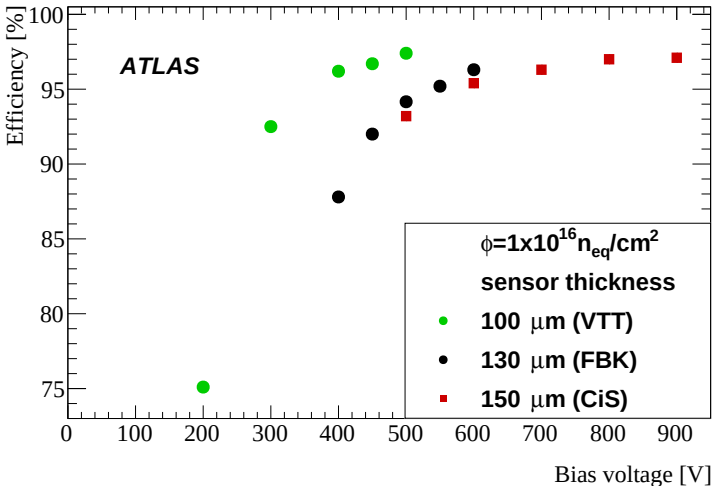


Figure 4.9: Hit efficiency measured at normal incidence in test beams at DESY and CERN SPS with FE-I4 modules assembled with 100, 130 and 150 μm thin planar sensors.

Even if, due to an issue with the prototype chip, the global efficiency drops as a function of the particle rate, the study of the two different geometries still allowed an evaluation of the relative effect of the biasing structures on the tracking efficiency. The measurements were carried out after tuning the chip to a threshold of 700 e. In the case of the 50×50 μm^2 geometry, after irradiation at a fluence of 3×10^{15} n_{eq}/cm^2 with 70 MeV protons, no significant efficiency loss within the available statistics is visible at the pixel cell boundaries in both cases of modules with or without biasing structures. The results indicate that due to the lower thresholds, the efficiency loss due to charge sharing or biasing structures are less than 1%.

The open options for the planar sensors regard mainly the design of the pixel cells and in particular the implementation of a biasing structure to allow for the characterization of the devices before interconnection to the read-out chip. A possible alternative to the bias grid, that is being explored, is the modification of the production process with the addition of temporary metal. This would allow for the measurements of the sensor leakage current by shorting all pixels. This additional layer is then removed after the device characterisation before further processing

One avenue of exploration is the possibility to produce passive pixel sensors using standard CMOS processes on high resistivity wafers. General purpose CMOS processes provide high production volumes at costs that are low compared to sensors produced in dedicated lines. Moreover, the availability of features like multiple metal layers or polysilicon layers offer the possibility to implement new design solutions. Small prototype sensors have been fabricated and show promising results. Further work is required to produce full size prototypes which are demonstrated to be radiation hard up to the level needed at least for Layer 4.

As explained in Chapter 3, there are indications that suggest a possible tracking performance advantage in using rectangular 25×100 μm^2 pixels rather than square 50×50 μm^2 ones. From the front-end chip point of view, the two solutions are equivalent because the connection pads are arranged in a way that is compatible with both geometries. From the sensor point of view, the effect induced by having one pixel dimension close to the size of the interconnection structures must be studied carefully, as efficiency or yield may decrease. Modules based on the RD53A chip will be used to compare the two solutions and study the performance before and after irradiation. For the planar sensor, the effect of changing pixel geometry is expected to be low, possibly limited to the effect of the bias grid. For the 3D sensors, the rectangular aspect ratio reduces the space available to place the bonding pads, and this could lead to a reduction of the sensor production yield, and, consequently, an increase of the cost.

A market survey process for the planar pixel sensors was launched in Q4 2017, to be sure that proper qualification of all the vendors will be completed in time to be able to place the sensor order for the pre-production in 2019. The specifications for the planar sensors allow the participation of interested CMOS manufacturers to the market survey. The 3D sensors are produced in smaller quantities, so there is no need for a formal market surveys. The qualification of the three available 3D vendors will however proceed in parallel with the qualification of the planar sensor vendors, using the RD53A front-end chip.

4.3.3 Hybridization

The high density interconnection technique used to connect the pixel sensor to the front-end chip, call hybridization, has been developed during the production of the present ATLAS Pixel Detector. This was done in close cooperation with two vendors who are currently working with members of the ITk to develop the particular techniques required for the bulk production of a large number of modules. Because of the large number of pixel modules additional potential vendors have been identified, and, at the time of writing, there are at least five companies who have expressed a willingness to be qualified as ITk bump deposition providers. The bump deposition is not a commonly used industrial process at the bump densities considered in the ITk, so having five providers can be seen as a prudent risk mitigation strategy. The hybridization process consists of two steps. First the bumps are deposited on the two dies to connect. This operation is performed at wafer level, and usually coupled with other wafer processes, in particular the deposition of a metal layer in the bump area (UBM, under bump metallization). Then the wafers are cut, and the individual dies are connected using a technique called “flip–chip”. This step is particularly labor intensive, as accurate alignment is needed and prone to errors. One clear lesson from previous production campaigns is that the hybridization can represent a severe chokepoint in the module production. For this reason, the possibility of being able to complete part of the flip-chip production in-house at the ITk pixel laboratories equipped with semi-automatic flip chip machines is being developed. This will increase the module production

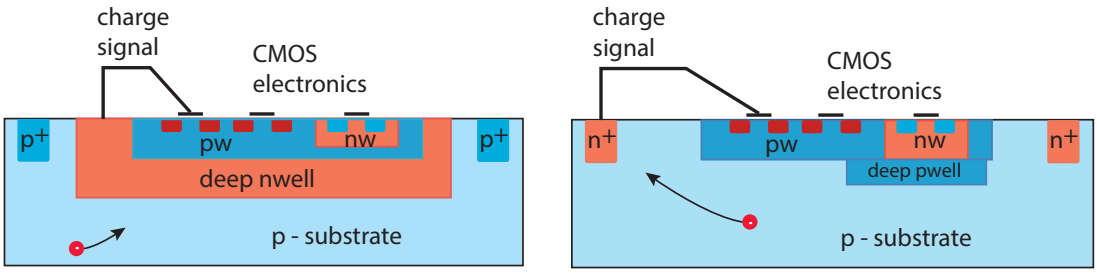
capacity and would allow the ITk to compensate for any temporary problems at a commercial vendor.

The technological challenge is more demanding than for the original ATLAS Pixel and IBL modules. The requirement to produce very thin pixel assemblies targeting a front-end chip thickness of 150 μm and a sensor thickness of 100 to 150 μm, is similar to the IBL module but more stringent than for the ATLAS Pixel module (190 μm and 250 μm thick front-end chip and sensor respectively). The required bump density represents a five-fold increase over the IBL FE-I4 chip due to the pixel pitch of 50 μm in both directions. However, the minimum bump pitch is unchanged. The ATLAS ITk Pixel chip will also be larger with 400 columns and 384 rows giving a total of 153 600 bump-bonds per chip, compared to 26 880 bonds for an FE-I4 chip. Another limitation the vendors need to consider is that the 65 nm process selected for the front-end chip uses 300 mm wafers, compared to 200 mm for the FE-I4 chip, so the wafer level treatments must be able to support this particular wafer size. Before processing RD53A wafers, the selected companies will be pre–qualified using dummy 300 mm wafers with resistive chains.

A potential problem is related to the flip-chip bonding of thin front-end chips, especially for processes requiring relatively high temperatures. For front-end chip thickness of 150 μm, special measures must be implement to compensate the thermal deformation during the bonding process. In general, these techniques have been demonstrated at several vendors using the FE-I4 chip, but clearly the complexity of the process, and consequently the fabrication time and the cost, increase with the reduction of the thickness. As shown in Section 7.6 and 7.7, preliminary hybridization results obtained using FE-I4 based modules or dummy structures are encouraging and do not indicate any potential showstopper. Nevertheless, flip-chip bump-bonding remains, for the intrinsic complexity and the limited number of reliable providers, a critical step in the pixel module production and one of the main drivers of cost and production schedule. To gain market understanding, a CERN based market survey was launched in the fourth quarter of 2017 and is expected to last up to one year. The market survey will aim to qualify at least 5 vendors using the RD53A wafer. The in-house flip-chip bonding process will also be qualified at the same time as the market survey.

4.3.4 CMOS monolithic Pixel Detectors

The fabrication of hybrid pixel modules relies on very specific technologies and construction techniques that do not have a large commercial market outside of particle physics. This poses particular constraints when considering the development and production of large area Pixel Detectors like the ITk. The total cost and required production rate are two areas that need particular attention in the design and development stage. For a long time, the ITk pixel community has been looking at the possibility of using high-volume, low-cost commercial processes to replace the bespoke technologies currently used in module production. Commercial CMOS processes used as a standard in industry are particularly



(a) Large fill-factor

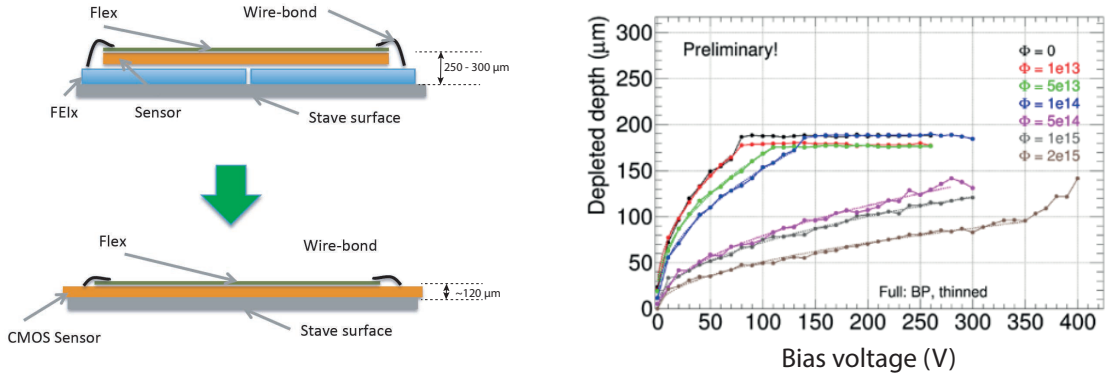
(b) Small fill-factor

Figure 4.10: The two principal variants of considered CMOS cell geometries: (a) Large fill-factor: the charge collecting deep nwell encloses the complete CMOS electronics. (b) Small fill-factor: the charge collection node is placed outside the CMOS electronics area (from [79]).

attractive. This is especially true if sensor and read–out electronics can be fabricated together in a single die, realizing a so–called monolithic Pixel Detector. Several monolithic pixel devices have been developed for experiments in high energy physics, including one for the ALICE ITS [78]. These devices, however, are designed for very low particle rates and fluences compared to HL-LHC. Collaborators at many ATLAS institutes interested in Pixel Detector development explored the possibility to design a monolithic pixel device capable of operating in the HL-LHC environment, and the results obtained so far have been particularly encouraging. In Chapter 9 an alternative module concept for the external barrel layer (Layer 4) based on monolithic Pixel Detectors is presented.

An R&D program started in 2007 demonstrating that it is indeed possible to produce pixel sensors in CMOS technology with radiation hardness of 10^{15} n_{eq}/cm^2 and above that will meet the radiation tolerance requirements for the outer layer of the Pixel Detector. This can be done with good charge collection efficiency within 25 ns, resulting in a hit efficiency above 95% even after irradiation. These promising results, achieved using several CMOS processes with different vendors, have encouraged the ITk pixel community to explore the possibility of using a monolithic CMOS device instead of a traditional hybrid Pixel Detector with planar sensors in Layer 4. The tracking performance compared to hybrid pixel modules is expected to be very similar or at most marginally different: using the same pixel size, a CMOS detector typically produces a smaller cluster because the depletion region typically is 50–100 μm, but the effect on track parameter reconstruction is not visible. There are, on the other hand, possible advantages related to the reduction in material (only one sensor is needed instead of sensor plus read-out chip) and to the output bandwidth (smaller cluster size). However, the important advantage of a monolithic CMOS solution is related to the simplification of the production process, the reduction in costs and savings in production time. In particular, the possibility to significantly reduce the number of chips to be bump-bonded could eliminate the principal choke-point in the detector production.

In order to be able to arrive at a decision on the use of CMOS that is consistent with the start of the production of hybrid pixel modules, it has been decided to only consider mono-

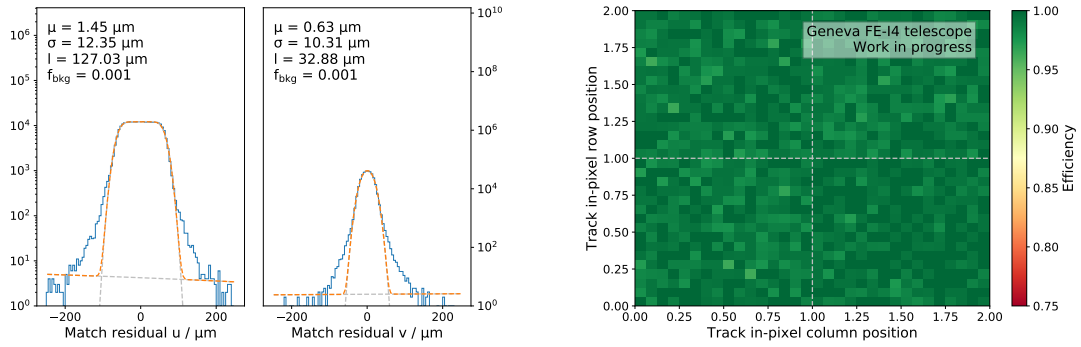


(a) (b)

Figure 4.11: Depletion depth as a function of bias voltage of CMOS pixel sensors (here: large fill-factor) for different radiation fluences (neutrons) up to 2×10^{15} n_{eq}/cm^2

lithic designs for pixel modules that would be used as a drop–in replacement of the existing hybrid modules. In particular, the CMOS module must have the same mechanical dimensions, physical interfaces, power consumption, voltage supplies, read-out and interface with the services as the hybrid pixel module. A comparison is shown in Figure 4.11(a). The activity on the CMOS option for Layer 4 started in 2014, first with small scale prototypes in various technologies, and then with submissions of full scale monolithic demonstrator chips (including the complex read-out architecture) in three different technologies in 2016 and 2017. The different submissions are exploring two different design options, called "small fill factor" and "large fill factor". As illustrated in Figure 4.10, in the "large fill factor" design the electronic circuits are completely surrounded by a charge collecting deep n-well, while in the "small fill factor" the charge collecting node is placed outside the CMOS circuitry. At the time of writing the three full scale chips are being characterised and evaluated, as illustrated in Section 9.3. Figure 4.11(b) demonstrates that CMOS sensors after 2×10^{15} n_{eq}/cm^2 still can have depletion depths of more than 100 μm. At the end of the current evaluation phase, a new design will be submitted, using the most promising solutions. This new design will be submitted for fabrication by the middle of 2018 and this design will have to implement all the functionality needed to ensure full compatibility with the hybrid quad module.

Figure 4.12(a) shows resolutions compatible with the pixel pitch obtained for 180 GeV pions for a pixel pitch of 40×130 μm^2. Figure 4.12(b) shows an in-pixel efficiency map. For unirradiated devices efficiencies in excess of 99.5% have been obtained. After irradiation with fluences (neutrons) of 10^{15} n_{eq}/cm^2 the efficiency is still close to 99%.



(a) (b)

Figure 4.12: (a) Space resolutions obtained with a full scale monolithic detector (un-irradiated), for a pixel size of 40 $\times$ 130 μm^2; (b) In-pixel MIP detection efficiency map. Average efficiencies are above 99.5% (unirradiated) and close to 99% (irradiated).

4.4 Data Transmission

When compared to the existing ATLAS Detector, the design of the data acquisition and extraction system for the ITk Pixel Detector is much more challenging. This is due to the larger trigger rate (x10 higher than current ATLAS), the larger number of hits associated with 200 proton-proton interactions per crossing and associated volume of data that goes with it. This is especially true in the inner layers that represent a particular challenge. The older generation of data links that operate at 160 Mb/s must be replaced with a new design that provide multi-Gb/s read-out without increasing the mass inside the tracking volume.

As much as possible ITk will take advantage of increased performance available in modern small feature size electronics. As discussed in Section 6.2.2, each front-end chip will have four serial output lines that can transmit data at 1.28 Gb/s. This serial outputs will be coupled to an electrical data transmission line, connecting the front-end chip with the optical conversion stage. Due to the adoption of serial powering, there is no common ground reference for all the modules, as the module reference voltage varies along the serial power line. As a consequence, the data transmission lines must be AC-coupled and an AC balanced protocol must be used. From this point of view, it would be simpler to move to optical data transmission as soon as possible, to get rid of potential grounding issues. It is indeed impossible to perform an optical conversion close to the Pixel module. It has not been possible to identify or develop laser diodes with a sufficient radiation tolerance to operate at a few centimetres from the interaction point. The preferred solution is to place the optical conversion stage sufficiently far from the interaction point where existing radiation tolerant solutions can be deployed. In addition, it is desirable to place the opto-conversion

stage in a region that can be accessed during a long LHC shutdown, which implies a 6–7 m long data transmission line. At the same time, in order to reduce material inside the tracker volume, it would be preferable to aggregate as soon as possible the front-end chip output lines into a single fast data line. As will be illustrated in detail in Chapter 10, several types of thin cables have been tested. A dedicated custom development with polyethylene dielectric for balanced performance between transmission quality and radiation hardness yielded prototype twinax with measured performance complying with the specifications of a loss of 20 dB over 5 m to still allow some connection loss. The lesson learnt is that 5.12 Gb/s over 6–7 m is feasible only if a combination of error correction and pre–emphasis techniques are used, and if the total attenuation along the line is kept below 20 dB. In practice, this means that the drivers at the transmitting (front-end chip) and receiving (optical converter) stages must be designed as part of a combined system taking into account the characteristics of the cable used, and that the number of interconnections along the line must be limited. A possible solution, initially explored, is to use a single piece of micro-coaxial cable with two inner conductors (twinax), with one connector on the module and one on the optical converter, but this could make the integration of the detector unnecessarily complicated. As already explained, the baseline solution is to combine the active components needed to aggregate the four FE chip serial outputs and to handle the high speed signals together with the twinax cable into a custom active cable (see Section 6.2.2). This approach has several advantages: first of all, it decouples the development of the 5.12 Gb/s serial output from the development of the ATLAS FE chip, that can use the same output stage as RD53A. A second advantage is that the active cable does not necessarily need to be connected to the module, but can be placed at some distance, for example at the end of the stave. In this way, data transmission along the staves can work at 1.28 Gb/s, widening the range of possible low mass cables that can be used. The price to pay will be an increase in number of lines (four serial lines and one power line for the Aggregator). As illustrated in Sect. 10.3.3, twisted pairs and flex lines are being considered for data transmission up to the end of the stave while the active cable will connect the end of the stave to the optical conversion stage, referred to, in the following, as opto-board.

Based on the occupancy estimates reported in Table 2.7, and taking into account the data format as implemented in the RD53A chip, it is possible to determine the average link occupancy in the various layers of the Pixel Detector. The detailed analysis is illustrated in Chapter 10, and the results are summarized here in Table 4.1. Here we present the data rate at 1 and 4 MHz L0 in the different parts of the detector. The same table shows the chosen design value of the data link. This value is somewhat larger than the maximum rate from simulation: the reason is that a sufficient headroom is needed to compensate the event-to-event fluctuations and to be able to guarantee a transmission latency suitable to feed the trigger processor.

As mentioned in Section 4.2, in the L0-L1 scheme, the two inner layers will not provide any input to the L1 Track Trigger, so the maximum read-out rate will be 1 MHz. Even at 1 MHz, Layer 0 and Ring 0 require a 5.12 Gb/s link per front-end chip, which is the maximum

Table 4.1: Data rates for Pixel barrel layers and for the forward rings for 1 MHz and 4 MHz L0-accept rate. The rates are averages per event; for each layer the value for the module with more data is indicated. The selected nominal data rate per front-end chip is also indicated.

Layer/Ring	Data rate (1 MHz L0) (Gb/s)	Data rate (4 MHz L0) (Gb/s)	Design data rate per FE chip (Gb/s)
Layer 0	3.97	-	5.12
Layer 1	0.89	-	2.56
Layer 2	0.52	2.08	5.12
Layer 3	0.32	1.28	2.56
Layer 4	0.22	0.88	1.28
Ring 0	2.15	-	5.12
Ring 1	1.07	-	2.56
Ring 2	0.65	2.60	5.12
Ring 3	0.39	1.56	2.56
Ring 4	0.27	1.04	1.28

number of data cables that can be used to extract the data. In the other layers, the front-end chip output links will produce an output of 5.12, 2.56 or 1.28 Gb/s. In order to make the best use of the available bandwidth and to reduce the amount of material in the data cables, it is necessary to aggregate several front-end chip to use the full 5.12 Gb/s bandwidth available in each data cable. This operation is performed by the data aggregator chip as illustrated in Figure 4.13.

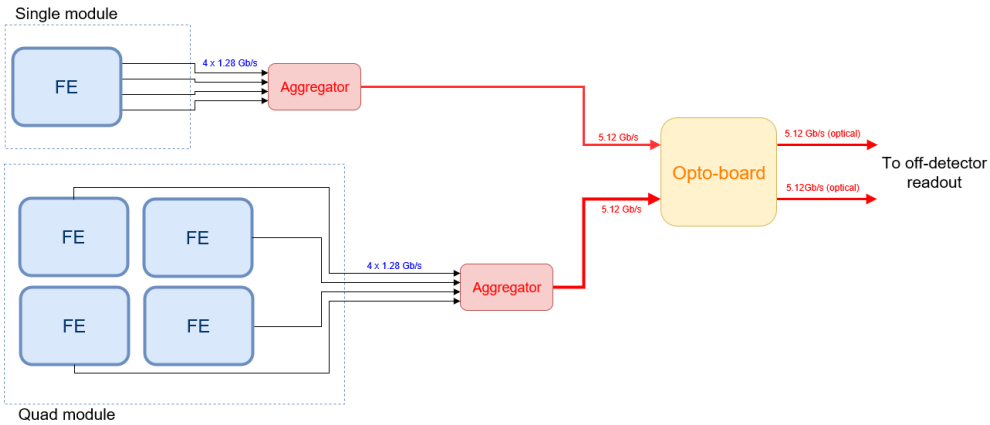


Figure 4.13: Examples of possible aggregation strategies for the high speed data transmission links.

The design of the so-called “down links”, used to distribute clock, trigger signals and configurations to the front-end chips is less challenging, but still requires a new implementation compared to the 40 Mb/s links used in the present detector. This concept is illustrated

in Figure 4.14, and uses a lpGBTx link [80], running at 2.56 Gb/s on fibre to connect the data acquisition system to the optical conversion stage. In this location there will be the optical to electrical conversion, and the lpGBTx chip will split the incoming 2.56 Gb/s link into individual 160 Mb/s lines for up to 16 modules. Each line has enough bandwidth to distribute clock and fast commands (like L0, L1) to the individual front-end chips, allowing for triggers in consecutive bunches (in the present system, two consecutive triggers must be separated by 4 bunches). In addition, it will be possible to refresh the front-end configuration every 60 ms while taking data, to compensate for the effects on the pixel memories of single event upsets. This continuous refresh for the front-end chip memory is referred to as "trickle configuration".

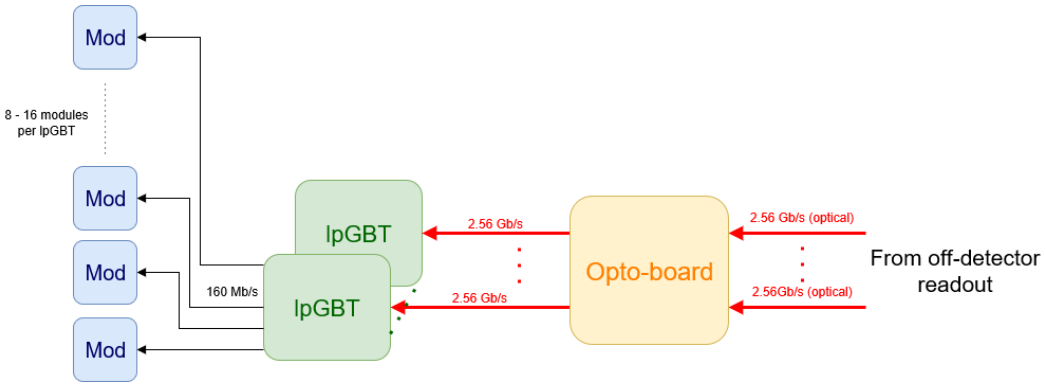


Figure 4.14: Interconnection schema for the data link providing clock and configuration data to the pixel modules.

The baseline opto-board technology is the Versatile Link+ module. The Versatile Link+ project is a joint ATLAS and CMS effort which aims to develop a radiation-hard optical link system. It is designed to withstand the radiation level of the trackers of both detectors during the High-Luminosity run. It has been qualified for 1 MGy Ionising Dose and for a total fluence of 10^{15} n_{eq}/cm^2. The project started its pre-production phase in 2017, while the production is expected to run in 2019 and 2020, when companies having successfully completed development (on time, in budget) will be invited to tender for the full production. The Versatile Link+ module can be interfaced with Serializer / Deserialize modules. Each module can host a single receiver (Rx) and multiple transmitters (Tx's). For the transmission part, the Laser Driver (LDD) can work in array mode driving multiple VCSEL's (Vertical-Cavity Surface-Emitting Laser), while for the receiving part the PIN diode is coupled with a trans-impedance amplifier (TIA). The LDD and TIA are custom designed modules, while the VCSEL array and PIN diodes are commercial, but qualified within the collaboration to prove their radiation hardness property. The LDD has been designed and prototyped in 65 nm CMOS technology. The Versatile Link+ works in a Multi-Mode Optical mode and it has a data rate of 5 or 10 Gb/s for the Tx and of 2.5 Gb/s for the Rx links. The development of the Versatile Link+ is proceeding according to schedule and the production phase is about to start. Preliminary tests have demonstrated the possibility to operate the Rx's and Tx's links up to 4.8 Gb/s and 10 Gb/s, meeting the ATLAS ITk requirements.

The off-detector electronics for the ITk will be common between Pixel and Strips. The DAQ chain consists of the FELIX system as front-end interface and the Local Trigger Interface (LTI), which interfaces the ITk systems to the ATLAS-global TTC system. The backend systems will consist of several PCs for DCS, ITk monitoring, data handling and control. These systems will be described in detail in Section 12.1.

The FELIX system is the main interface between the detector and all off-detector systems and it is maintained by ATLAS TDAQ [81]. The main task of the FELIX is to handle the communication between the off-detector backend systems and the detector. Therefore, triggers coming from the LTI (see below) and configuration data from the ITk control unit are merged into a single bit stream and then encoded with the ITk Pixel specific downlink protocol (see Section 6.2.1) on a lpGBTx e-link basis. During operation of the detector the configuration has to be re-sent regularly to mitigate loss of configuration from single event upsets in the FE chips. Therefore, all configuration data will be stored inside the FELIX system and will be sent by command of the LTI during gaps in the triggering using the trickle mechanism the FE chip provides as described in Section 6.2.1. In the uplink direction FELIX will decode the custom pixel FE data stream (see Section 6.2.2) and forward it to the backend data handlers. Besides that, also some monitoring information, like timeouts, received trigger tags, decoding errors and also a prescaled fraction of events with hit data, has to be forwarded to the ITk monitoring unit.

Data as processed by the FELIX system are distributed via commodity multi-gigabit networks. It is anticipated that at least 100 Gb/s network links will be used throughout the DAQ system. A "Data Handler" receives data from FELIX through such a network. During data taking, it will decode detector specific information prior to storing them in the Dataflow and also accommodate monitoring functionality. The latter requires trigger information to be sent in addition to the actual event data received from the FE electronics.

The Data Handler will operate a *ITk DAQ software* which is planned as the common software architecture to support various use-cases, including sensor and module testing during production and assembly in the local sites (starting from one front-end chip read-out $O(1)$), test beams, operation of the detector in the Point-1 (up to $O(10^5)$ front-end chips), and enabling well-organised calibration and data-taking. One of the key concepts for development of the ITk DAQ software is to establish a common high-level interface to different hardware platforms, such as FELIX and systems targeting module tests during production. This is achieved by providing a well-defined common interface for the different hardware platforms to communicate with the higher level software which steers communication to and from the front-end.

The core of the software framework can be divided in two parts:

- The scan engine which generates the bitstream of commands to communicate with the front-end. The calibration of tracking detectors is typically performed in terms of loops with many iterations of the same kind of command which scan over a parameter range, a subset of channels or perform calibration injections. The command sets are

organised as loop actions, which can be dynamically assembled into a nested loop structure to be executed by the loop engine.

- The data received from the front-end traverse a pipeline of processing steps. An important concept of this processor pipeline is its data driven manner, i.e. that all the information needed to perform the processing step is included in the data packets in the form of meta-data. The input and output data structures which are being exchanged by the processing blocks are well defined. This enables an easy exchange or integration of a processing algorithm into the chain or a hardware accelerator to perform a specific processing step; for instance histogramming is a step sometimes performed in hardware to reduce the required communication bandwidth. Furthermore this concept enables the data to be processed in a distributed manner. The concept of distributing the data processing is important for the scalability of the framework.

With common data formats and user interfaces, expertise on operating the system for a specific task is expected to be extensible to various use-cases, e.g. an expert of the module testing in the local laboratory site can handle the common user interface in the detector operation at Point-1 with little additional training.

4.5 Power Distribution

The power distribution system for the ITk Pixel Detector is designed to minimize the amount of material, especially inside the tracker volume, and to keep the power losses in the cables below 30% of the delivered power. A schematic diagram of the power distribution system, defining the nomenclature of the different sections of the cables and of the corresponding patch panels, is shown in Figure 4.15. Given the high number of modules, providing individual low voltage supplies to each functional element would result in a prohibitive number of cables. The adopted solution consists of connecting groups of modules in series on a single line.

The front-end chips, thanks to two shunt-low-dropout (shunt-LDO) regulators, can take a constant current from the serial input, use what is needed to supply the internal analog and digital circuitry and shunt surplus current to ground. In this way, the voltage drop generated by a module over the serial line is constant, and the voltage reference of each module (called local module ground) remains constant with time, even if different from module to module along the serial powering line. In order to prevent the loss of a full serial line in case of problems with a single module, a protection chip (PSPP) is used to monitor the current absorbed and to isolate the module from the serial line in case of problems (see Figure 4.16). The number of modules connected to a single serial line must be optimized taking into account the power dissipation along the cables (lower if more modules are connected to a single line) and the risk of propagating problems from one single module to the full chain (mitigated by the use of the PSPP chip). In the present PSPP design the number of modules in a serial line is limited to 16 by the addressing capabilities of the PSPP chip,

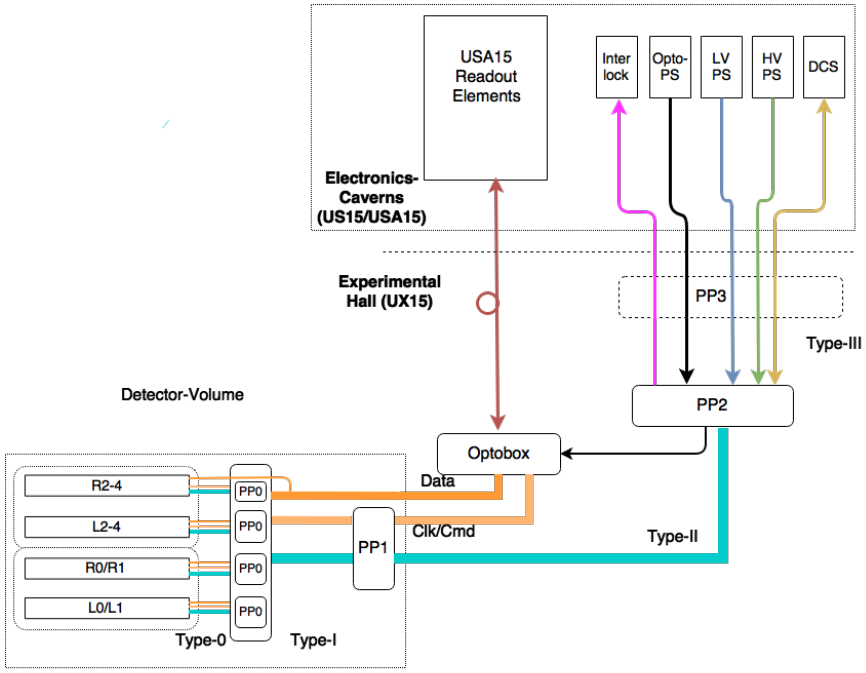


Figure 4.15: Schematic of services path between detector and US(A)15.

but, on average, the plan is to connect 8 modules per serial line. The supply of each LV serial line can be provided by a commercial power supply located in the service cavern. The necessity of adding an active regulation stage at PP2 is being considered.

The distribution of the sensor bias voltage will be parallel over each low voltage serial power line and will use a single line. The reference voltage will be the local module ground, so each module of the serial line will see a different bias voltage. In case of very long module chains or if the bias voltage requested by the module is not very high, as can happen in the case of 3D sensors, it may be necessary to use two HV lines per serial group. Again, to prevent collective failures, it must be possible to isolate each module from the HV line. This can be done using the same HV switch that will be used in ITk Strips.

The rest of the power distribution system is similar to the one implemented for the present ATLAS Pixel Detector. A detailed discussion of the design of the powering system, of the grounding schema and of the detector control system is given in Chapter 11.

4.6 Detector Control System

To provide monitoring, control, and safety to the operation of the ITk Pixel Detector a dedicated detector control system (DCS) is foreseen, which is integrated in the overall ATLAS

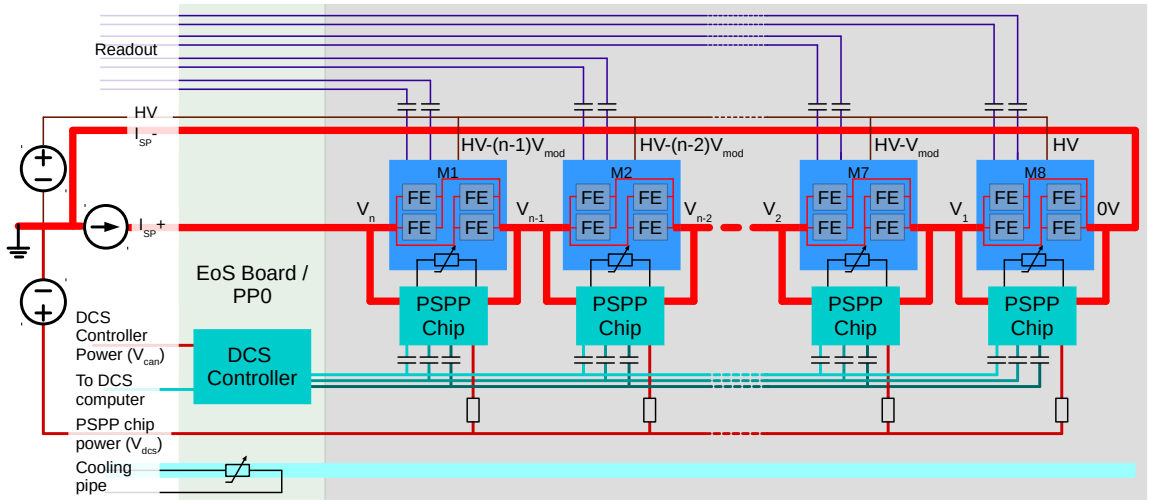


Figure 4.16: Schematic of the Serial Powering distribution on the local support.

DCS to allow common operation with all other ATLAS sub detectors. It is essential that detector conditions are monitored all the time and control to the different components of the detector is guaranteed over all the detector lifetime. To achieve a reliable control and monitoring the DCS consists of three independent paths: safety, control and diagnostics.These paths differ in granularity, availability, and reliability level. Figure 4.17 shows a diagrammatic overview of the DCS system.

To provide the fastest reaction to critical conditions of the detector the safety path is built on a hard-wired interlock system, which acts directly on power supplies or other equipment. The safety system acts on sections of the detector (coarse granularity) but has the highest reliability and is always in operation. The Interlock system itself, which is built in common for all ITk Detectors, is described in more detail in Section 12.3.

The control of the detector components is via the the control path. It provides an interface between operator and detector, enabling tasks such as calibration, commissioning, and data taking. All components of the detector can be steered and monitoring of all available parameters is provided. The design of the control path follows the serial powering requirements and consists of the DCS controller at the end of the serial powering line and the PSPP chips close to the modules (see Section 11.3.2). It requires a high reliability and therefore has its own powering and communication lines. The granularity is on module level to be able to provide control to these.

The third path is the diagnostics path, it provides the operator with additional monitoring values needed to debug the behaviour of the detector or tune its performance. The level of details delivered is the highest, providing feedback from each individual front end chip. The communication is via the data stream of the FE-chips and is extracted at the level of the data acquisition system.

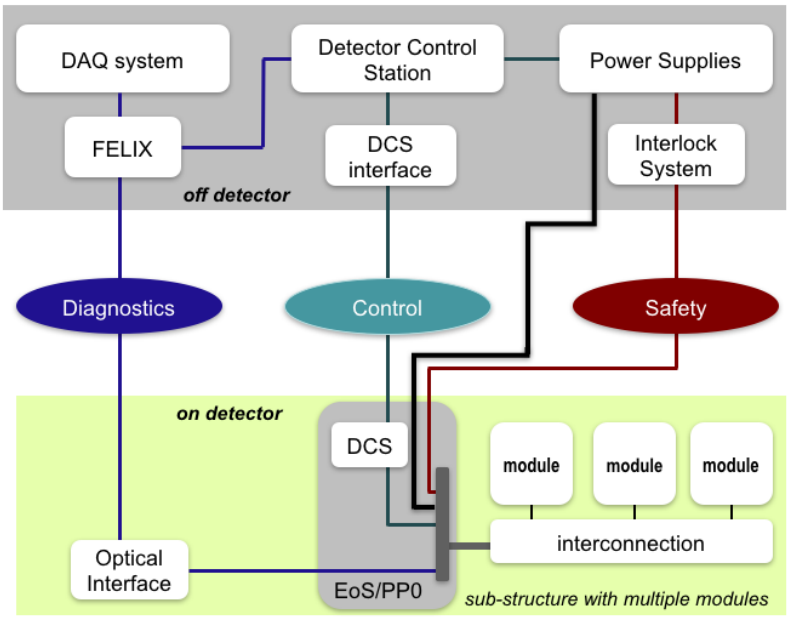


Figure 4.17: Overview on the ITk Pixel Detector Control System.

4.7 Local supports

The local supports provide mechanical support, alignment, routing of services and thermal management of the pixel modules. They are made of low mass, high rigidity and high thermal conductivity materials, including: carbon fibre laminates, pyrolytic graphite and other carbon based composites. A small diameter titanium pipe is embedded in the structure to allow heat extraction via a CO_2 cooling system (see Section 14.2). The outer barrel local supports are "staves" that are positioned along the beam direction at various radii. The outer end-caps local supports are "rings" which are positioned perpendicular to the beam direction at different z locations, chosen to guarantee hermeticity. The innermost system is equipped with both types of local supports. Local supports also carry all the electrical services from the modules to the end of the structures.

4.7.1 Constraints and Specifications

In general, the local supports must be designed to reproduce as closely as possible the positioning of the active element defined in the layout optimization phase and illustrated in Chapter 2. At the same time, the mechanical support structure must be as light as possible. Thermal performance and mechanical stability are the two key drivers of the design of the local supports and therefore set the most important specifications.

Most of the power dissipated by the modules comes from the front-end chip. However, the front-end power consumption is kept constant by the shunt-LDO regulators, and does not depend, to first order, on the dose accumulated by the detector. The most critical part is the power dissipated by the sensor's leakage current. As observed in Section 4.3.1, the leakage current increases with both temperature and radiation. If the sensor temperature is not properly stabilized by the cooling system, it will increase exponentially, making the detector unusable. This is the so-called "thermal runaway" process. It is therefore crucial to have a very efficient mechanism to extract the heat generated during detector operation minimizing the increase of temperature.

The local supports are composite structures with elements having different coefficients of thermal expansion (CTE). Temperature changes can produce non-uniform deformations in the mechanical structure which can lead to serious issues such as mechanical stress and misalignment of the modules.

Section 13.1 provides details on the mechanical and thermal performance requirements and specifications. A quantitative estimator of the local supports' thermal performance is particularly crucial to assessing the conformity of the mechanical design with the requirement of assuring stable and reliable operation over the entire life of the detector. The thermal performance parameter adopted for the local supports is the Thermal Figure of Merit, or TFM, defined as the ratio of the temperature difference between the evaporating cooling liquid and the hottest point on the sensor, to the module's power per unit of area. The required TFM value for a structure depends upon its expected total radiation dose, leading to layer-dependent TFM requirements, as illustrated in Table 4.2. The TFM is described in detail in Section 13.1.2. All the measurements performed so far on different samples and illustrated in Chapter 13 indicate that it is possible to satisfy performance requirements even in the most critical areas of the detector (the innermost sections or regions with inclined sensors, where the contact with the cooling pipe is reduced and the the heat extraction more difficult).

Table 4.2: Specifications for the Thermal Figure of Merit expressed in °C cm^2/W.

Layer	TFM
Layer 0 - 3D	18.7
Layer 0 - 100 μm Planar	14.2
Layer 1 - 3D	26.0
Layer 1 - 100 μm Planar	22.3
Layer 2 - 150 μm Planar	20.4
Layer 3 - 150 μm Planar	23.7
Layer 4 - 150 μm Planar	26.3

From the mechanical point of view, the Pixel Detector is divided into four parts. The Inner System is the replaceable part, and consists of the two inner layers, with coverage extended

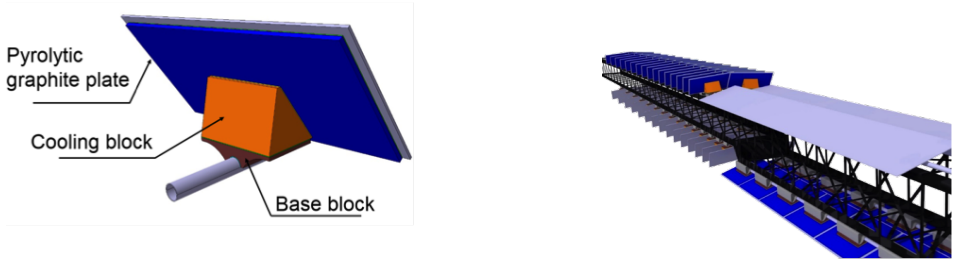


Figure 4.18: Left: Schematic representation of a tilted module cell. Right: A typical longeron (truss construction) supporting four cooling lines.

up to a pseudo-rapidity of 4. The Outer Barrel consists of the central part of the three outer layers, that are extended in rapidity by two End-caps. The four parts will be assembled separately, and then integrated in the ITk. In particular, the Outer Barrel will be first assembled with the two end-caps, then inserted into the Strip Detector. Finally, the Inner System will be positioned together with the beam pipe.

4.7.2 Outer Barrel Local Supports

The local supports for the Outer Barrel are made of staves oriented in the direction of the beam line. These 2 m long staves, called "longerons" are divided in two sections: the central part, covering a pseudo-rapidity range of $\pm$ 1, is made of quad modules oriented in a classical way parallel to the beam direction. At the periphery of the longeron, on both sides, there are dual modules with the sensor inclined with respect to the beam line. The inclination angle is 56° with respect to the beam direction.

The cooling pipe runs along the direction of the beam line, so in the inclined region the contact with the module surface is limited. To reach the required thermal performance, modules are first mounted on a pyrolytic graphite plate which is itself coupled to a highly conductive material glued to the cooling pipe by means of an intermediate base block (see Figure 4.18). The same strategy is used for the quad modules in the central flat region as well. In this way, the coupling of the module with the graphite plate, and of the pipe with the base block, which are critical for the overall thermal performance, are made separately, while the connection of the module to the base block can be engineered to reduce the assembly time, minimize the risk of collisions with other components and allow repairs in case of failure.

The inclined module concept requires two different types of longerons for layers 2 and 3 and for layer 4. The longerons for layers 2 and 3 are coupled, with the modules placed at the two radial ends of a trapezoidal shaped support structure. The longeron for layer 4

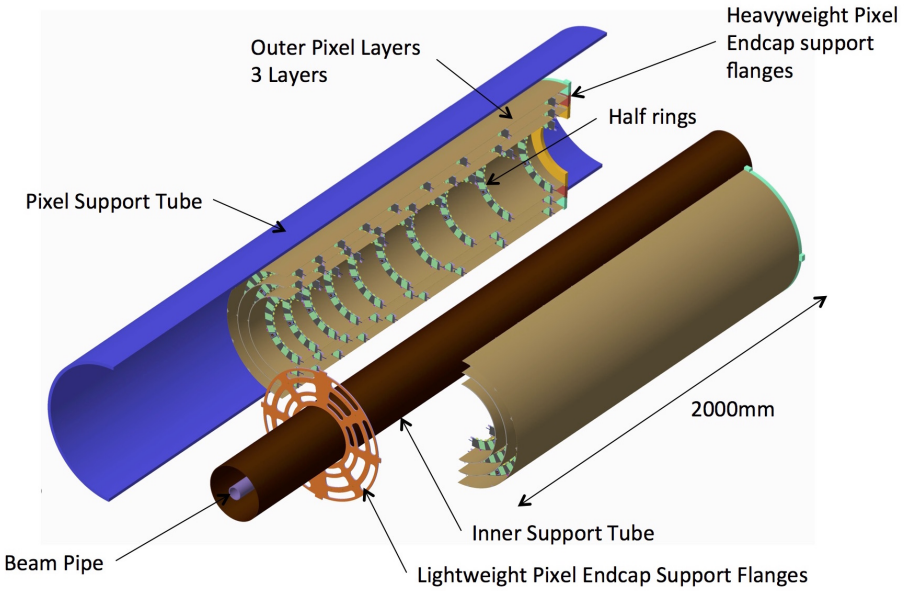


Figure 4.19: Exploded 3D drawing of one Outer End-cap.

has modules only on one side. The fabrication and assembly process of the Outer Barrel is detailed in Section 13.2.2.

4.7.3 Outer End-caps Local Supports

The design of the Outer End-caps local supports is somewhat more traditional and similar to the disk concept used in the Strips. However, instead of disks covering the entire radial range, the end-caps use three concentric sets of circular crown shaped "rings". This solution offers two big advantages: the gap between the concentric rings can be used to route the services, and the position along the beam direction of the rings at different radii can be adjusted independently, offering the possibility to maximize the coverage with a reduced number of sensors. Modules (all quads) are mounted on half-ring-shaped carbon structures which consist of carbon foam inserted between two carbon fibre plates, with an embedded titanium cooling pipe. Modules cannot be positioned side by side and are therefore mounted on alternating sides of the structure with overlap to provide full coverage in azimuthal angle. Power and DCS information is delivered to the modules via small patch ("EoS") cards which are mounted on the half-ring surfaces between modules, and which connect to the modules via bus tapes embedded in one edge of the half-ring.

Populated half-rings are inserted at the correct z positions into low-mass half-cylindrical shells that also support the Type-I services. When pairs of half-cylinders are complete, they are brought together and joined along the long edges to form full cylinders. Each pair of

Figure 4.20: Ring layouts in the "Inclined Inner" (left) and "Inner Alternative" (right) proposals. Modules are depicted as orange rectangles.

half-cylinders is brought together around the previous pair. The layers are fixed together into a complete end-cap by means of a low mass carbon fibre flange at the inner end and a heavier flange at the outer end (see Figure 4.19). Type-I services exit through the outer-end flange into the PP1 region.

Further details of the design of the Outer End-cap can be found in Section 13.2.3 and Section 16.2.2.

4.7.4 Inner System Local Supports

The Inner System comprises a barrel region with two layers (Layer 0 and Layer 1) and two end-caps with two layers of rings (Ring 0 and Ring 1). Layer 0 and Ring 0 are equipped with 3D sensors and single chip modules; Layer 1 and Ring 1 are equipped with thin planar sensors and quad modules.

The cell concept described for the outer barrel is carried over for the thermal management of the modules, but with small geometrical differences due to the different module sizes. For the particular case of the inclined and end-cap regions of Layer 1, flat cells featuring quads are arranged in a coupled-half-ring configuration in order to reduce the heat path to semi-annular cooling pipes and meet the TFM requirements (see Figure 4.20). The resulting rings are built around two hollow carbon fibre profiles, which support the various cells and provide the required mechanical stiffness to the assembly.

A system of carbon fibre semi-cylindrical shells linked at various intermediate positions is used to support the rows of modules in this part of the detector. The sensing elements are installed on the inner sides of these structures, while the detector services are routed towards the patch panels on the outside faces, which feature machined holes which permit the necessary electrical and fluidic connections to be made. Once integrated, the half-shells for Layer 0 and Layer 1 are connected together at six intermediate locations (taking advantage of the existing gaps in z between inclined modules) using lightweight interlinks. The resulting coupled structures are then placed around the beam pipe and inserted into the inner bore of the Inner Support Tube (IST).

Despite the similarity with the outer part of the Pixel Detector, the design of the Inner System is complicated by the fact that the space available to route the services is limited due to the small radius, while the number of cables is larger, because the required output bandwidth is larger. Moreover, in terms of tracking performance, it is important to minimize the amount of material between the first two points to maximize the impact parameter resolution. So, even if most of the technical solutions adopted in the outer part can be reused, a specific optimization of the design is necessary. For this reason, the design of the Inner System is less advanced than the design of the Outer Barrel. The situation is however evolving rapidly: alternative designs are being considered, in which the inclined region of the barrel is replaced with rings. In this case, the ring design employs a carbon sandwich construction which combines laminate facesheets and a high thermal-conductivity foam core featuring embedded titanium cooling pipes. This concept can be adapted to create the so-called coupled rings, which feature carbon spokes and are used to support modules from two adjacent layers (see Figure 4.20). Prototypes of these structures are being prepared to validate the design and optimize mechanical properties, thermal performance, service routing and module loading procedures. More details are given in Section 13.2.4.

4.8 Installation of the ITk into ATLAS

The different parts of the ITk (Strip and Pixel: Central and End-cap sections) are integrated into the ITk Outer Cylinder in the SR1 surface building (2175) at point-one. The integration is scheduled for completion in the middle of Q2 2024 and the ITk is scheduled for lowering into the ATLAS cavern in Q2 2025. The installation of the ITk is presented in detail in Chapter 17. The installation is the sum of all activities and procedures that start with departure of the ITk from the surface building, followed by the lowering and maneuvering of the ITk to the face of the Liquid Argon Cryostat (also called the Warm Vessel) and end with the beam pipe bake-out. Because of the size of the Outer Cylinder, the maneuvering of the ITk to the inner bore of the cryostat will require ATLAS to be in the "Large Opening" configuration, which is the only one that provides a gap between the end-cap and the barrel Toroid that is large enough for the Tracker to reach the point where the insertion starts. Temporarily access platforms will be installed to support the ITK in front of the calorimeter. This standard configuration has been used to install the Inner Detector in 2007 and more recently the IBL detector in 2014. When it is installed into the cryostat, the ITk is supported on rails fixed to the cryostat bore. These rails also serve to guide the ITk during its insertion into the calorimeter. This aluminum rail system is dimensioned such that it can take the load of the new tracker (about 5,000 Kg). The ITk rails are installed on both sides of the inner warm vessel on the same rail support that are used by the current Inner Detector, which is called the tracker support rail. The geometrical shape of the ITk rails will be defined with the interface support of the Outer Cylinder once its design is more advanced. The Tracker Support Rails contain M5 threaded holes distributed every 60 mm along their length, and provide the anchor points and the vertical and horizontal references for the rails. At the

time of writing it is not yet decided if the structure that will be designed to support the ITk during integration in SR1 will also be used to transport the ITk to the cavern. It would make sense to design a common support structure with both functionalities to minimize the manipulation during the transfer of the load between the structures. The functionality and feasibility details will be worked out when defining the tooling and this can only be done when the design of the Outer Cylinder is close to final. Several specific tools will be needed to perform the transport and positioning of the ITk into the barrel cryostat inner bore.

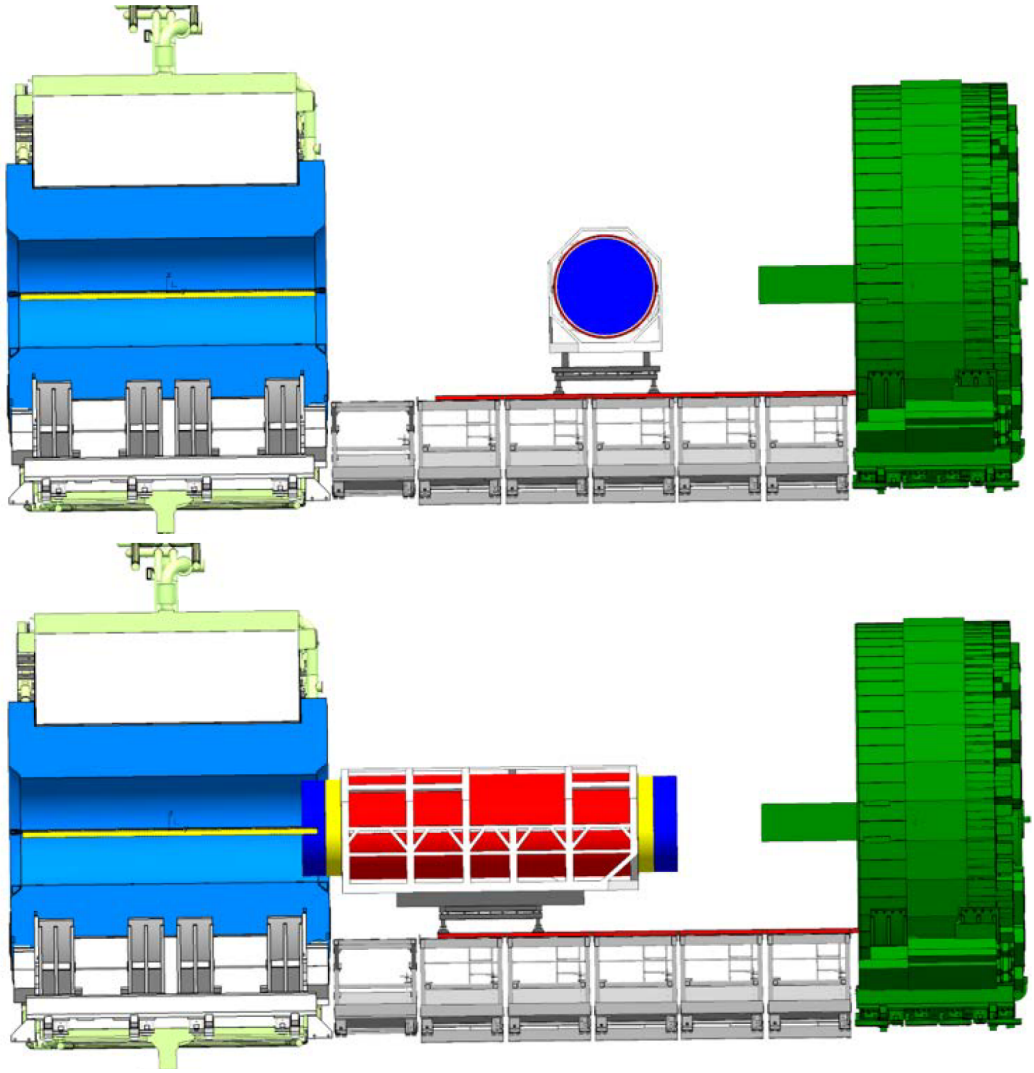


Figure 4.21: **Top**: ITk in rotation position at about 9.4 m from the IP. **Bottom**: ITk ready for insertion at about 7 m from the IP (after rotation).

It is not possible at this stage to give a detailed description of the different tooling items here, but the main functions are presented.

The transport Frame: The main function of the Transport Frame is to allow the lifting and the manipulation of the ITk with overhead and mobile cranes between the surface buildings and from the surface (Bldg. 3185, SX1) to the underground experimental cavern (UX15). The secondary function of this frame is to provide environmental protection for the ITk while it is transported out of clean and controlled environments.

The Support Cradle: The function of the Support Cradle is to support the weight of the ITk. The ITk Detector is similarly interfaced with the Support Cradle as it is with the calorimeter bore rail system. The adjustment of the Support Cradle allows the positioning of ITk prior to its insertion into the calorimeter bore.

The Rotatory Table: Whatever the lowering scenario will be, the ITk will be unloaded on to the support platforms with its axis perpendicular to the beam axis. There is a need to be able to rotate it by 90 degrees prior to installation. This is the primary function of the rotary table (see Figure 4.21). The table will also be used for the translation movement from the lowering point to the insertion point using wheels or rollers interfaced with the rails installed on the top of the minivans. The Rotary Table must be capable of supporting the weight of all the objects resting on it: The ITk, the Support Cradle and the Transport Frame. The preliminary estimate for the total weight of these objects is about 7,000 Kg.

The Transport Frame is interfaced with the Support Cradle; they can be combined such that they create a single tooling unit with both individual functionalities. Further study will define if a combined design makes sense with respect to the integration and transport constraints.

At the end of the translation and rotation steps described above and prior to the insertion of ITk into the calorimeter bore, a precise alignment and positioning procedure will be carried out to bring the ITk package co-axial with the inner warm vessel tracker support rails. This positioning is achieved with the help of the survey team and using adjustment mechanisms on the support structures. The Support Cradle will have a matching rail system that will be connected to the inner warm vessel tracker support rails for continuity. After the mechanical connection of both rail systems, the tracker will be moved on to the rails into the calorimeter bore. The insertion stroke is about 7 m. The rails act as a guide and support for the tracker during its insertion. The tracker translation is foreseen to be motorized, to control the insertion: force, position, speed and acceleration. The complete insertion mechanism and tooling will be designed to allow both, the insertion and the extraction of the tracker.

The insertion tooling will be motorized to control the insertion speed, the acceleration but also to control the power consumption of the stage. For all parameters, maximum acceptable values will be set and once reached the movement will be stopped. The threshold values will be adjusted during commissioning work with a mock-up. In particular the power consumption will be optimized to not to exceed any sticking points or conflict that might be encountered during the insertion or extraction operations.

The ITk final position is defined as follows:

- In Z (along beam axis) the translation movement is stopped when the tracker reaches its target operating position (provided by the survey team). To guarantee that the ITk does not move over time, the tracker is fixed to the calorimeter. The geometry of the fixations on Side A or C and their position on the Outer Cylinder will be decided in conjunction with the internal architecture and fixation points of the different ITk sub-systems.

- In Y (vertical) and X (horizontal) the positioning is achieved at the assembly stage by the vertical and horizontal positioning of the interfaces (V-shape rail and Flat-shape rail as well as the position of support wheels with respect to the tracker). Therefore no adjustment is foreseen during the insertion of the tracker into the calorimeter bore.

The services for the ITk will be installed at the same time Inner Detector is being removed. Where envelopes are shared or interfere with ID Services, their removal must complete before the start of ITk service installation. This is most critical in the case of the Type-II services. These run from the Type-I patch panels (PP1s) that are part of the ITk package, and run along the cryostat wall through gaps in Tile fingers, LAr power supplies, and Muon chambers to reach various Patch Panel 2 (PP2) locations. The envelopes along the cryostat wall and through the various gaps are very restrictive, and require accurate positioning of fibre, cable and pipe routing to assure envelopes are not violated.

From PP2, the services are routed radially outward either directly to the side caverns (US15 or USA15), or to patch panels (PP3) mounted on the walls of the UX15 cavern. There provide various access points to the detector volume, and are populated with equipment racks. All services leaving PP2 are called Type-III services, regardless of their destination. Cables running from PP3 to either US/USA15 are called Type-IV services. The ID Services will be removed by sector-by-sector, starting possibly at the top. This is preferred because the PP2 cooling boxes for the majority of ITk are in sector five which is on top. It is desirable to be able to install the CO_2 cooling lines near the beginning of service installation because they have the largest single cross-section (50 mm diameter flex-lines). Installation of ITk services-by-sector will allow a complete service chain to be installed and commissioned prior to connecting to the ITk. It is likely that this work will interact with many of the other activities happening at the same time in the cavern, most importantly refurbishment and upgrades to the Muon chambers, so advancing on multiple sectors in parallel will be required to fit around other complex activities.

While the work to complete service installation will be completed by sector, the installation environment is divided radially. The Type-II services will be installed by ITk personnel, up to the tile fingers, and ATLAS Technical Co-ordination personnel are responsible for routing beyond that. The termination of services at patch panel locations; connecting and testing are the responsibility of the sub-systems, e.g. Pixel and Strip communities.

The existing Inner Detector Patch Panel-II locations will be preserved, but on modified platforms. The modification will happen as soon as decommissioning starts and should be completed prior to routing Type-II services to the PP2. The PP2 are primarily for ITk electrical services, and are dominated by cables. The cooling services come from an independent PP2 in Sector five and are described in the cooling chapter. Other services, such as the optical fibres, are not routed via PP2, but directly to USA15. Some of the patch panels will require cooling, this service is routed to PP2 by ATLAS technical coordination and will be connected during patch panel installation.

The Pixel Detector will re-use most of the existing Type-III cables that service the current PP2. These cables were installed by plugging them into the current ID Pixel PP2, they were then pulled from there to US/USA15. There is no excess cable length on the Pixel Type-III cables at PP2 meaning that the ITk Pixel PP2 must either have the same connector layout, or a plan to re-terminate all of their Type-III cables prior to PP2 installation. New Type-III cables will use installed between PP2 and PP3 for the Strip Detector. This allows for the installation of the Strip PP2, then the cables will be pulled from it to PP3. In both cases not much space is available to store excess Type-III cable length. This means that the installation of the PP2 boxes, is independent of Type-II cable installation in schedule and can proceed in parallel. The installation order of Strip versus Pixel PP2 will depend on the work that may be required to re-terminate Pixel Type-III cables. It is also Sector dependent as each PP2 platform is configured differently so the installation order will be configuration dependent. There is space under each of the PP2 locations, with exception of the Sector thirteen location to store excess Type-II cables, which will be utilized once ATLAS Technical Coordination is able to route these services to the various PP2 locations. The primary schedule conflict for routing Type-II cables to PP2 is Muon Chamber installation.

ITk Type-II services can be installed at lower radius, but cannot be routed to PP2 until the work on the Muon chambers is complete. While this is a clear physical conflict, the additional work on Muon chambers may require other chambers to move into ITk service routing gaps to gain access. ITk Type-II service cross-sections are intended to be identical, but many of the cables will be larger in diameter. Bend radii of larger cables during installation may necessitate changes in routing or gap selection. This will be tested on the 1:1 mockup installed in Bat. 180 at CERN.

For the ITk Pixel Detector no significant work is planned to install cables beyond PP2. Some auxiliary cables may be required for Pixels, e.g. High Voltage, and some control cables, but these are few, (under 100). Some may be routed to PP2 or directly from PP1. The cables that are installed to PP2 can be installed along with the Strip cables which will be replacing the entire service chain from PP3 inward.

The Strip Type-III cables will be installed in the current ID SCT service envelope where space can be made available. This task will start at PP2 with pre-terminated cables which are pulled and dressed into the cable trays vacated by Inner Detector (SCT) cables, or in

newly installed cable trays. This work, both design and installation is controlled by Technical Coordination and is a work in progress. Investigation into currently installed services has begun during the last EYETS (Extended Year End Technical Stop) and will continue during Long Shutdown 2 where some more access will be available to verify currently installed services and to develop plans to remove those that are no longer required. The ITk Strip Detector plans to re-use the ID SCT Type-IV cables from PP3 to US/USA15. No significant work is planned to remove any of the type 4 cables in the service chicanes up to USA15, or the penetrations into the US15 cavern. Some few new cables may need to be installed in existing cable trays/penetrations to reach US/USA15, as mentioned above for HV, fibre optics, and some control cables.

4.9 Decommissioning of the current Inner Tracking Detector

Chapter 18 describes the decommissioning of the existing Inner Tracking Detector (ID) as part of the preparation for the installation of the ITk during Long Shutdown 3 (LS3). In particular, it describes the removal and storage of the beam pipe, the removal of the IBL, Pixel, SCT and TRT sub-detectors and the removal of all services from the cryostat volume and the ID endplates, up to the cable connections at Patch Panel 2 (PP2). Chapter 18 also includes general consideration of radiation protection, dose mitigation planning and radioactive waste management and presents updated radiation simulations. These calculations will form the basis on which the decommissioning procedure will be optimized. The work on different mockups to test and optimize the extraction procedure is presented including the different training campaigns that are currently foreseen as well as the planned dose optimization procedures. In addition, a first concept for possible shielding to lower the collective dose of personnel involved in the decommissioning process is proposed.

The proposed sequence for decommissioning is as follows:

1 Service Removal: Removal of non-radioactive services from the ID endplate up to PP2: This initial step involves disconnection at PP2, an initial cut of cables and pipes at a specific radius on the face of the ID endplate, and removal of cables running up to PP2, as permitted by other work in the region.

2 Removal of VI beam pipe on Side C: The beam pipe cavern table and transfer tool (designed, not yet manufactured) must be lowered and aligned, the services cut, and the beam pipe extracted from the IBL to its protective container. It is then delivered to the beam pipe group and will be reused.

3 Removal of IBL on Side C: After disconnection of the IBL services on both sides, the IBL can be extracted using the same tooling table and alignment as the beam pipe.

4 Removal of Pixel package on Side C: In order to access the Pixel package, service disconnection must be performed on both A and C sides. Heaters must be removed,

cables cut within the Pixel nose, and the Pixel package extracted to the dummy support tube for transfer to the surface.

5 Removal of ID End-plate Nose and related supports from ID Endplate, on sides A and C

6 Removal of ID services from cryostat face, Sides A and C. This step involves removing the remaining services from the face of the cryostat, thereby liberating access to the cryostat bore.

7 Removal of ID End-cap, Side C : The ID End-cap trolley must be lowered and aligned to the ID bore, allowing extraction and raising of the ID End-cap on Side C.

8 Removal of ID End-cap, Side A : The ID End-cap trolley must be lowered and aligned to the ID bore, allowing extraction and raising of the ID End-cap on Side A. This process requires a large opening on Side A.

9 Disconnection of ID Barrel services inside cryostat bore, Sides A and C : Now that the ID Bore has been cleared of all but the ID Barrel, work must commence inside the bore to cut and remove services holding the ID Barrel in place. In addition, the rails must be changed on the A side in order to allow the extraction of the ID Barrel.

10 Removal of ID Barrel, Side A : The ID Barrel trolley must be lowered and aligned to the cryostat bore for removal and extraction of the ID Barrel.

11 Removal of services from cryostat bore, Sides A and C : Now that the full detector has been removed, the cryostat bore must be cleared of all services and service trays.

12 Removal of all services from cryostat face, Sides A and C, and final cleaning

The decommissioning process begins approximately three months after the beginning of LS3, in March of 2024. The beam-pipe and beam-pipe services disconnected in preparation for beam-pipe removal. IBL removal begins approximately two weeks later, followed by the Pixel disconnection and removal over the following eight weeks. Removal of both End-caps takes place over the next six weeks, arriving at the four month point in the decommissioning process in mid-July. The final large item for removal, the ID barrel, is extracted in the next three weeks. The removal of all services and attachments from the Cryostat bore and faces leads to a final completion date approximately six weeks later (or just over six months into decommissioning), providing for clean access for ITk from that point onwards, currently October 2024.

In-situ radiation measurements were made during the 2016 EYETS at multiple points around the Inner Detector. These measurements are made at multiple radi at different points along the beamline. These measurements are then compared to the so-called Run 2 FLUKA model of the Inner Detector The final simulations are well within a factor of two for all measured values. It should be mentioned that the present simulations give reliable values at some distance from the source of the radiation. For the FLUKA model, materials are often smeared

into an average composition with an average density distributed with radial symmetry around the beam axis. In close proximity, the actual radiation can therefore be higher given specific local material composition. A dedicated measuring campaign, together with the CERN Radio Protection group (RP), is planned at the beginning of LS2 along the ID cover plate and, if possible, with the ID cover plate removed and the services accessible. Any hot spots found will be documented, marked and addressed in the dose optimization.

All new simulations concentrate on ID surroundings instead of the full detector, giving higher precision in the anticipated work environment. These simulations will be used to estimate the expected dose for each decommissioning step, and are the basis of all optimization and training efforts foreseen to take place on the mock-ups. The level of agreements between measurements and predictions give considerable confidence in the dose optimization procedures and that the work can be carried out in the allotted time.

5 Sensors for the ITk Pixel Detector

5.1 Introduction and requirements for the ITk pixel sensors

In this Chapter 5 sensor technologies designed for bump-bonding to read-out electronics are discussed. These are 3D and high resistivity planar sensors, with the possible extension to CMOS technologies for processing of passive sensing devices. The required radiation tolerance of the sensors is discussed in details in Table 2.9. The highest fluence in Layer 0 assuming a replacement scenario and a maximum integrated luminosity of 2000 fb^{-1} is 1.31×10^{16} n_{eq}/cm^2, with a corresponding dose of 7.2 MGy. For Layer 1 the highest fluence is 3.8×10^{15} n_{eq}/cm^2 and the dose 3.2 MGy. In the outer pixel layers, for an integrated luminosity of 4000 fb^{-1}, the highest fluence is 3.0×10^{15} n_{eq}/cm^2 in the barrel and 3.8×10^{15} n_{eq}/cm^2 in the end-caps with a dose of 3.2 MGy. Defining the required intrinsic efficiency at the end-of-life of the ITk Detector is a compromise between what can be realized with the presently available sensor technologies and what is required to maintain good tracking performance up to end of the data taking. A random single-pixel inefficiency of 3% is considered as part of end-of-lifetime ageing and failure effects on the tracking, the performance of which is discussed in Section 3.1.4. Therefore a minimum hit efficiency of 97% is required which can be realized with all of the technologies under consideration. Another critical performance parameter to consider for the sensor technology is power dissipation. While the total power dissipation of a module is dominated by the front-end chip, the sensor technologies typically require high operational voltages with moderate leakage currents to achieve high reconstruction efficiency after irradiation. The resulting values of power dissipation translate into constraints for the required TFM performance of the local support structures, as given in Table 13.2. 3D sensors have been chosen as baseline technology for the innermost layer, due to their radiation hardness and low power dissipation, whereas for the other layers planar sensors are the baseline option, given their high fabrication yield and lower costs.

5.2 Overview of 3D pixel sensor technologies for ITk

3D silicon detectors are intrinsically more radiation tolerant than other available sensor technologies. The distance between the columnar electrodes, which penetrate the sensor bulk perpendicular to the surface, is decoupled from the device thickness and can be chosen

to be significantly smaller than the thickness of the standard planar sensors where the electrodes are implanted in the surface of the device (see Figure 4.7). The reduced electrode distance leads to less charge trapping from radiation induced defects and lower operational voltages, which, in turn, translates into lower power dissipation after irradiation.

Over the last 20 years, 3D technology has matured from a basic research and development tool to a mature commercial product supplied by multiple vendors with bulk capacity and is becoming a standard technology of choice where extreme radiation tolerance is one of the key requirements. Within the ATLAS experiment both the Insertable B-Layer (IBL) [3] and the ATLAS Forward Proton detector (AFP) [73] exploit 3D developments. This first generation of 3D pixel sensors with inter-electrode distances of 67 μm and a sensor thickness of 230 μm demonstrated a radiation tolerance of at least up to 5×10^{15} n_{eq}/cm^2 [3], which was the required tolerance for both IBL and AFP. Follow-up studies have established good performance up to a fluence of 9×10^{15} n_{eq}/cm^2 [74]. The radiation tolerance and power dissipation make the 3D sensor technology the baseline option for the innermost layer of the ITk Pixel Detector (Layer 0 and Ring 0), and a possible alternative for Layer 1.

The ITk Pixel Detector requires very particular developments of the 3D sensor technology: smaller pixel sizes, thinner active areas and extreme radiation tolerance. For the ITk Detector the baseline active thickness foreseen is 150 μm; with an extra 100 μm passive support wafer added to facilitate handling and bump-bonding. Productions of 3D devices with different thicknesses and pixel sizes of 25×100 μm^2 and 50×50 μm^2, and compatible with the existing FE-I4 read-out ASIC have been carried out and been characterized before and after irradiation [75].

Hit reconstruction efficiencies greater than 97% with an associated power dissipation of about 10 mW/cm^2 have been demonstrated for 3D devices with 50×50 μm^2 pixel geometries irradiated with 24 GeV protons up to 1.4×10^{16} n_{eq}/cm^2 [75]. Furthermore, specific productions of 3D sensors compatible with the first ITk prototype front-end chip (RD53A) have been, or are being, completed at CNM (Barcelona), FBK (Italy) and Sintef (Norway).

In addition to the advances in performance of 3D sensors, the ITk Detector will benefit from reduced cost and production times with respect to the IBL productions, due to the optimization of the 4″ wafer production line and the establishing of new 6″ lines [82].

5.3 Overview of Planar pixel sensor technologies for the ITk Detector

Planar pixel sensors are the baseline for Layer 1 to Layer 4 for the ITk Pixel Detector. The n-in-p technology has been chosen because it is a single sided process, simplifying the product flow with respect to the n-in-n technology presently used in the Pixel Detectors of the experiments at the LHC. The sensors will be produced on 6″ and 8″ Float Zone (FZ) wafers with resistivity in the range 3-20 kΩ cm. The active sensor thickness is 100 μm in Layer 1

and Ring 1, and 150 μm elsewhere, with an option to deploy 100 μm sensors in Layer 2 and Ring 2, 200 μm sensors in the end-caps and 300 μm sensors as an option restricted to Layer 4 and Ring 4. The thickness final choice will be based on the requirements of radiation hardness and minimization of the material budget weighted against the cost implications of using thinner sensors. The sensors will be operated in the full depletion regime before irradiation and in the partial depletion regime towards the end of the detector lifetime. The planar pixel sensors will be n-type implants DC coupled to an Aluminum read-out pad. The inter-pixel isolation will be achieved by means of p-stop and/or p-spray doped to a level sufficient to reach the minimum specified inter-resistance value of 2 MΩ. The back-side of the sensors will be covered by a uniform metallization with a good ohmic contact to the bulk of the sensors using a p^+ implant. Different technologies are employed for the sensor manufacturing and for the substrate thinning: from the use of composite substrates such as Silicon on Insulator (SOI) or Silicon-Silicon wafers, where a handle wafer offers a mechanical support to the active layer, to local or homogeneous thinning after the front-side processing of thick wafers. The electrical characteristics of the sensors are measured before interconnection to the chip for acceptance qualification, employing punch-through structures or poly-silicon resistors. These elements allow to ground each single pixel implant and to measure the leakage current through a connection to the bias ring. Given the fact that these structures cause a reduction of the hit efficiency after irradiation to HL-LHC fluences (see Section 5.5.2), alternative methods have been explored to perform the measurements of the leakage current at sensor level, before interconnection to the read-out chip. In particular some planar pixel sensor runs implement a deposition of a temporary metal layer at wafer level shorting all the pixel implants. This step is performed after the completion of the sensor processing, and the temporary layer is removed before UBM deposition. Several prototype productions have been completed with FE-I4 compatible sensors and more recently with RD53A compatible sensors. Successful R&D productions for ATLAS ITK planar pixel sensors have been completed up to now at the following foundries: ADVACAM, CiS, FBK, HPK, MICRON, MPG-HLL, NOVATI.

Thin planar pixels can also be further processed to obtain activated vertical sides that allow for an extension of the depleted region up to the edges. This method achieves very narrow inactive regions, reducing them at the sensor edges down to 50 μm. This is particularly relevant for the innermost layers where it is important to reduce geometrical inefficiencies. SOI wafers are employed for the fabrication and trenches are realized around the perimeter of each sensor with Deep Reactive Ion Etching (DRIE) using the mechanical support offered by the handle wafer of the SOI stack. Trenches are then doped, extending the p+ implant of the backside. FE-I4 compatible sensors have been produced with this method at ADVACAM (Finland) and FBK.

5.3.1 Passive CMOS sensors

A different approach to planar sensor fabrication is the use of CMOS technologies for processing of passive sensing devices to be interconnected via bump bonding to a read-out chip [83]. Industrial CMOS processes on large, high-resistivity wafers enable sensor designs with high yield and high throughput at comparatively low cost. Furthermore, various parts of the CMOS processing technology like multiple metal layers, polysilicon layers, as well as metal-insulator-metal (MIM) capacitors can be employed for special sensor features that are otherwise not available. Examples are AC coupling of the sensor to the read-out electronics. Prototype small pixel matrices have been fabricated at LFoundry with both DC and AC pixels isolated by a 4 μm p-stop grid implemented below field plates made of a low resistive polysilicon layer. The sensors have been thinned to 100 and 300 μm, respectively, and then have been backside processed providing a p-implant and a metallization layer to allow bias voltage application from the backside. These prototypes have been produced within a reticule cell around 2×2 cm^2 and new productions are foreseen to explore the feasibility of "stitching" neighboring mask together to fabricate quad sensors.

5.4 3D sensor characterization before and after irradiation

3D sensors with small pixel sizes that can be interconnected to the FE-I4 chip have been produced by CNM and FBK. These prototypes have been extensively tested before and after irradiation. At CNM, the first "small pitch" 3D sensor run with cell sizes of 50×50 μm^2 or 25×100 μm^2 was carried out as a CERN RD50 project and finished in December 2015 [76, 84]. The production technology was similar to the IBL one, using double-sided processing on a 230 μm thick high-resistivity p-type substrate with non-fully passing through columns of 8 μm diameter. The small 3D sensor pixels are matched to the existing FE-I4 read-out chip (see Figure 5.1 top left and centre sketches): each 50×50 μm^2 FE-I4 chip pixel cell contains five sensor pixels, either 50×50 μm^2 pixels with one n-type electrode (1E) or 25×100 μm^2 pixels with two n-type electrodes (2E), so that only 20% of the sensor pixels can be connected to a front-end channel and be read-out. The remaining 80% insensitive sensor pixels are shorted to ground to be at the same potential as the ones being read-out. Also strips and pad diodes of various geometries are included in the run. The yield and the breakdown voltages of this first small-pixel prototype run are not ideal, but there have been significant process improvements at CNM, as already demonstrated by the second AFP run [85]. The wafers underwent electroplate copper or electro-less gold Under-Bump Metallization (UBM) at CNM. Ten devices were bump-bonded to the FE-I4 read-out chip, assembled on read-out boards. Although some of them showed areas of disconnected bumps due to a poor UBM, all were suitable for testing.

FBK sensors with different pixel geometries and bulk thicknesses are also being investigated. In February 2016, the first 6" single-sided production was delivered, with ten 100 μm

and 130 μm thick wafers. Again, the small 50×50 μm^2 (single electrode) and 25×100 μm^2 (single electrode) sensor pixels are matched to the existing FE-I4 read-out chip. As mentioned above, in this configuration only 20% of the pixel sensors are connected to the FE-I4 read-out chip.

Two complementary irradiation campaigns have been carried out at the Karlsruhe Institute of Technology (KIT) and CERN-PS IRRAD facilities. All devices were annealed for one week at room temperature. Two CNM 50×50 μm^2 pixel devices have been irradiated uniformly to 5×10^{15} n_{eq}/cm^2 at KIT with 23 MeV protons, while a third one was irradiated to 1×10^{16} n_{eq}/cm^2. The lower fluence is the same as used in the IBL qualification campaigns and hence allows a direct comparison to the IBL generation. The fluence uniformity also allows a simple determination of the power dissipation. Even though low-energy protons deliver a high ionising dose to the FE-I4 read-out chip, the three devices were functional after irradiation. However, higher fluences are likely to damage the chip. Note that no neutron irradiations of FE-I4 3D devices were performed due to tantalum in the FE-I4 chip that becomes activated. Irradiations have also been carried out at the CERN-PS IRRAD facility with 24 GeV protons, which provides a non-uniform fluence over the detector area. Hence, it was possible to study a broad range of fluences on one single pixel detector as already demonstrated in Ref. [84]. The Gaussian beam profile has been determined with beam position monitors to 20.4×18.3 mm^2 FWHM, and the overall normalisation has been obtained with gamma spectroscopy of a 20×20 mm^2 aluminium foil, which gave an average fluence of 1.1×10^{16} n_{eq}/cm^2 over this area. The fluence in the region studied ranged from 0.8 to 1.4×10^{16} n_{eq}/cm^2. Systematic fluence uncertainties have been estimated between 11% (high fluence) and 24% (low fluence) using beam centre, beam width and aluminium position variations by 1 mm. It should be noted that from the initially three irradiated devices (2 of 50×50 μm^2 and 1 of 25×100 μm^2), eventually only one device was operational (with pixel geometry 50×50 μm^2) with the other two being non-responsive due to either chip or read-out-board failure. FBK sensors with different ITk pixel geometries have also been irradiated, uniformly at KIT and non-uniformly at CERN-PS IRRAD, to IBL (as a benchmark) and ITk fluences, respectively. Test beam results of these 130 μm thick FBK devices provide critical information of the effect of the sensor thickness on performance.

5.4.1 Electrical tests in the lab

For the first CNM small pixel size sensor production, the current-voltage (IV) characteristics were measured and the breakdown voltage was found to be typically between 15 and 40 V before irradiation, while the depletion voltage was in the range of a few volts. The threshold and Time over Threshold (ToT) calibrations were carried out and charge collection studies with a ^{90}Sr source were performed. The capacitance was measured on 3D pad-diode test structures as 37 fF per 50×50 μm^2 1E pixel and 84 fF per 25×100 μm^2 2E pixel. The noise was found to be between 105 and 140 e^- for 50×50 μm^2 1E pixels and

160 e^- for 25 $\times$ 100 μm^2 2E pixels. More details of the run and initial laboratory and test beam characterisations are described in Refs. [76, 84].

As stated above, the first FBK single-sided 130 μm-thick 6" run included pixel sizes of 50 $\times$ 250 μm^2 (double electrodes), 50 $\times$ 50 μm^2 (single electrode) and 25 $\times$ 100 μm^2 (single electrode). Selected sensors from this run were bump-bonded and assembled for testing. The devices were calibrated to a threshold value of 3000 e^- and ToT target of 10 BC for 1×10^4 e^-. The noise of the devices, for which the inter-column distance plays a critical role, was found to be about 100 e^- for the 50 $\times$ 250 μm^2 and 25 $\times$ 100 μm^2 geometries, and 90 e^- for the 50 $\times$ 50 μm^2 device. This noise level is considerably lower than the approximately 150 e^- of the 230 μm thick sensors from the IBL generation and the first CNM small pixel production. Exposure of the samples to a ^{241}Am source indicated that the overall quality of the bump-bonding is good, since only a very small fraction ($<$ 0.1%) of disabled or disconnected pixels were observed.

5.4.2 Test beam analysis

Beam tests of small-pitch ITk 3D FE-I4 prototypes before and after irradiation up to 1.4×10^{16} n_{eq}/cm^2 were performed at the CERN SPS H6 beam line with 120 GeV pions. The EUDET-type beam telescopes or a custom-made 3D-FE-I4 telescope [84] were used.

Figure 5.1 shows the in-pixel hit-efficiency map of the CNM small-pitch devices before irradiation for reconstructed tracks restricted to the active small-pixel sensor area over 2 $\times$ 1 sensor pixels. For the determination of an average efficiency, due to the telescope resolution smearing, the region of interest (ROI) was even further reduced to the central 50 $\times$ 50 μm^2 in the 50 $\times$ 50 μm^2 geometry and a central 100 $\times$ 2.5 μm^2 area for the 25 $\times$ 100 μm^2 device. Figure 5.1 (right) shows the hit efficiency in this ROI as a function of bias voltage. Already at 1–2 V the small-pixel devices reach their plateau efficiencies of 96–97%. This value is similar to a standard reference IBL FE-I4 device, which however needs 4 V to reach the efficiency saturation due to larger inter-electrode distance, which results in a higher depletion voltage. It is shown that tilting by 14° greatly improves the efficiency to 99.9% due to minimising the influence of low-efficiency regions from the 3D columns or low-field areas.

The irradiated devices were cooled down in a controlled-temperature box with set temperatures between -40 and -50°C, corresponding to on-sensor temperatures between -25 to -35°C. No influence of temperature on the performance was found in this range. The FE-I4 devices were tuned to a threshold of 1.0 ke^- and 1.5 ke^-. Measurements were performed at 0 and 15° tilt with respect to the beam axis.

Figure 5.2(left) shows the hit efficiency as a function of bias voltage for different fluences, irradiation sites, thresholds and tilts for 3D sensors with 50 $\times$ 50 μm^2 pixels bump-bonded to FE-I4B ASICs irradiated to 5, 10 and 14 $\times$ 10^{15} n_{eq}/cm^2 [75]. As expected, the efficiency is higher for lower fluences, lower thresholds and a tilt. At 5 $\times$ 10^{15} n_{eq}/cm^2 and 0°, the benchmark efficiency of 97% is already surpassed at the minimally measured voltage of

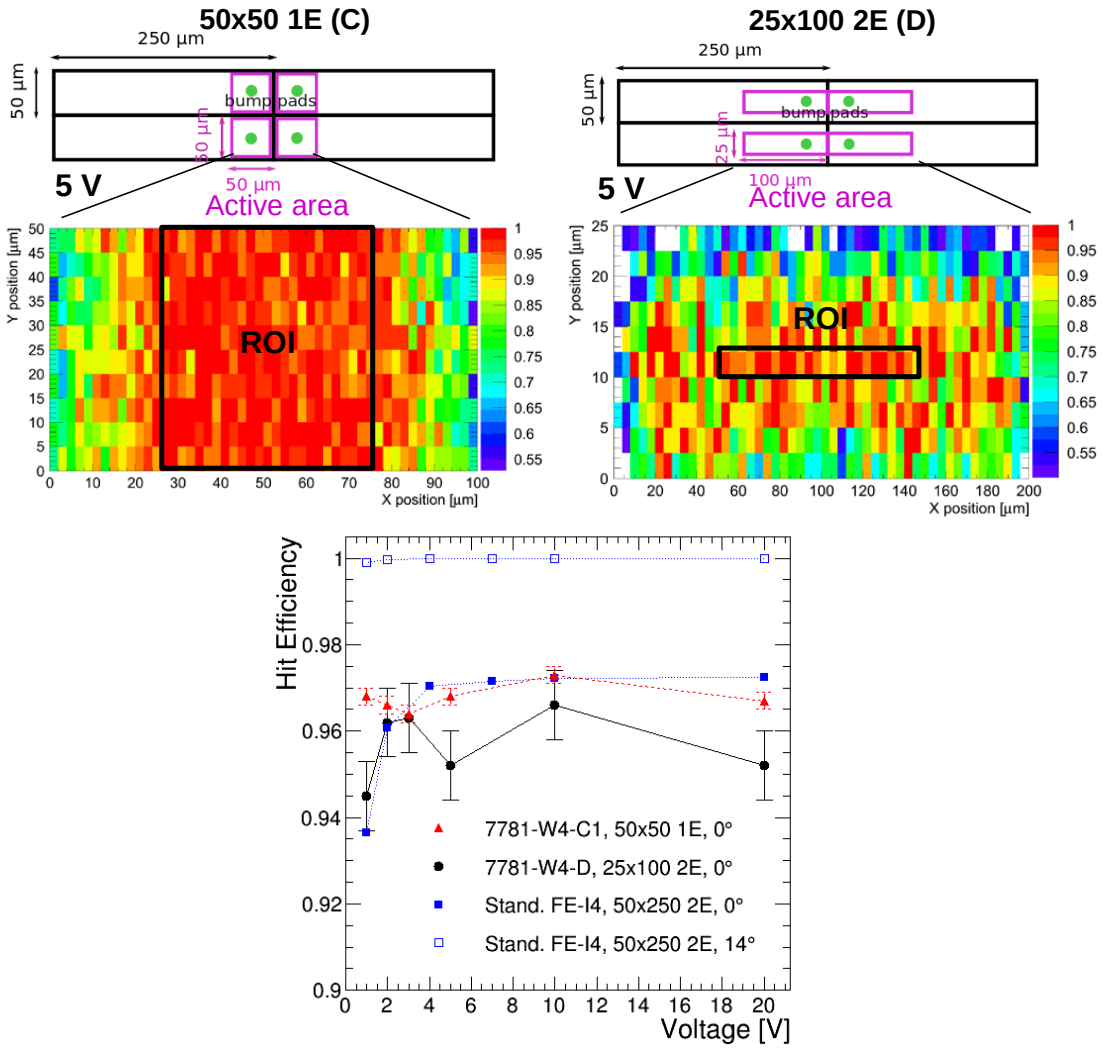


Figure 5.1: In the left and right part of the upper plots: on top, the sketch of 50×50 μm^2 (left) and 25×100 μm^2 (centre) 3D pixels matched to the larger 50×250 μm^2 FE-I4 chip pixels; at the bottom, the corresponding hit-efficiency maps for 2×1 sensor pixels at 5 V. In the bottom plot: average hit efficiencies in ROI vs. voltage for 50×50 μm^2 and 25×100 μm^2 pixel geometries at 0°, compared to a standard FE-I4 at 0 and 14° beam incidence. Figure taken from Ref. [84].

$V_{97\%} = 40$ V. Tilting the device by 15° increases the efficiency above 99%. At the highest fluence measured of 1.4×10^{16} n_{eq}/cm^2, the efficiency is above 97% at 100 V for 1.0 ke^- threshold and 0° tilt.

The voltage $V_{97\%}$ to reach an efficiency of 97% is taken as indication of a suitable operation voltage. It is shown in Figure 5.2 (right) (from linear interpolation) as a function of fluence and is compared for the new small-pitch and the IBL generation [84, 75]. The sig-

nificant improvement due to the smaller 3D electrode distance and hence less trapping is visible. For example at 5×10^{15} n_{eq}/cm^2, the IBL-generation devices need 120 V at 0° tilt and 1.5 ke^- threshold to reach 97%, compared to only 40 V for a 3D cell of 50×50 μm^2 1E under the same conditions. This results also in a significant reduction of power dissipation (product of $V_{97\%}$ and leakage current at -25°C) from 3.5 mW/cm^2 for IBL to 1.5 mW/cm^2 for 50×50 μm^2. For the non-uniformly irradiated device, the power dissipation cannot be directly obtained, but is estimated by combining $V_{97\%}$ with the leakage current measured on strip test structures [76] as 9 and 13 mW/cm^2 at 1.0 and 1.4×10^{16} n_{eq}/cm^2, respectively. Direct measurements from the uniformly irradiated 3D sensor at KIT up to 1×10^{16} n_{eq}/cm^2 confirm these results. Hence, the operational voltage and power dissipation are considerably lower than for planar pixels.

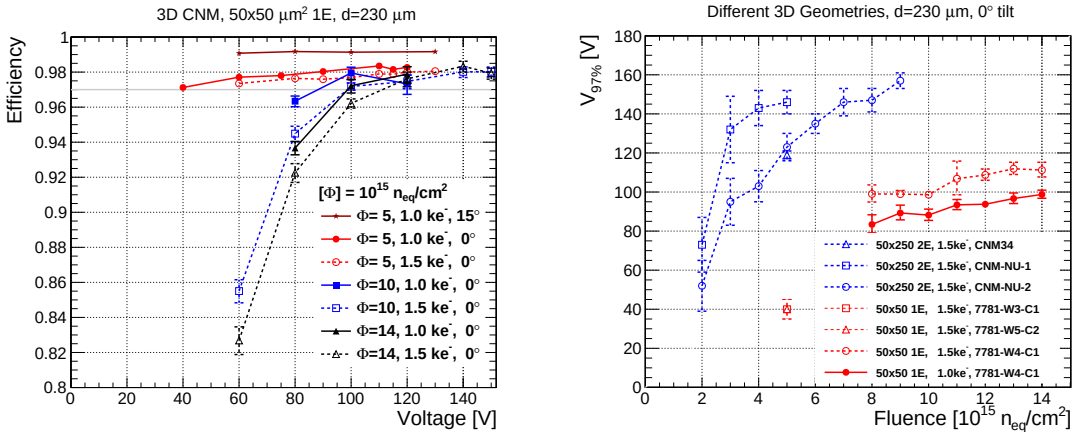


Figure 5.2: Left: Hit efficiency of 3D pixel sensors as a function of voltage for different fluences, thresholds and tilts. Right: $V_{97\%}$ as a function of fluence, compared for the IBL generation (50×250 μm^2 2E) and the new 50×50 μm^2 1E pixels. The uncertainties are statistical only. Figure taken from Ref. [75] and updated.

A test beam campaign for the non-irradiated small pitch prototype 3D modules of the first 6" FBK production took place in August 2016. Measurements were performed at the CERN SPS 120 GeV beam line (H6A), with the EUDET style telescope at CERN [84]. The sensors were placed inside a controlled-temperature box, which was set at room temperature. One planar sensor module was additionally inserted in the control box as the timing reference hit plane.

The average hit efficiency is calculated for the sensor pixels with the read-out electronics connected. For the 50×50 μm^2 (single electrode) and 25×100 μm^2 (single electrode) modules, due to the presence of the sensor pixels without read-out, the efficiency drops near the edges of the pixels that are next to grounded pixels. In order to avoid a bias in the estimation of the average hit efficiency due to this specific geometry, these edge regions are excluded from the average efficiency calculation.

The overall hit efficiency as a function of the sensor bias voltage for a fixed calibration target

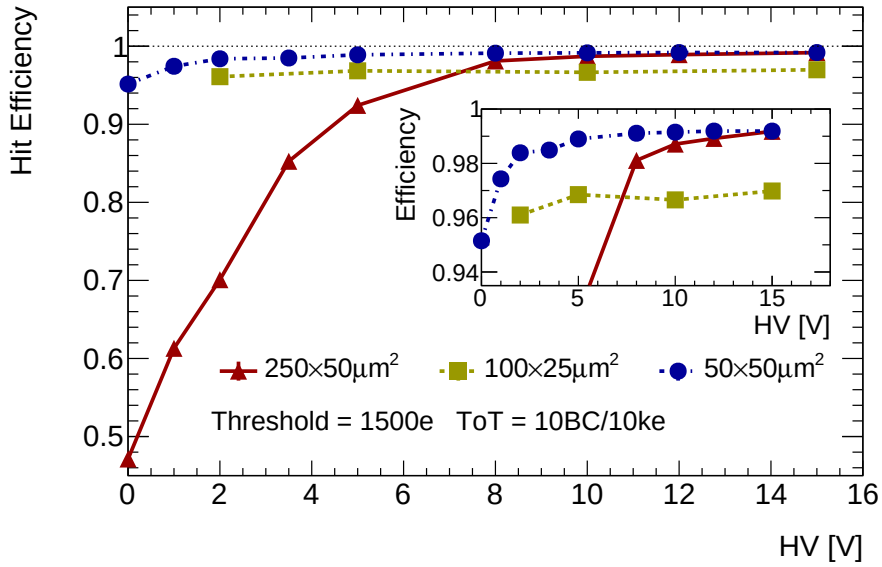


Figure 5.3: Hit efficiency of non-irradiated FBK 3D single modules at the region of interest as a function of the bias voltage and at 0° beam incidence. The inset displays the detail of the high-efficiency range. The calibration is made at the threshold of 1500 e^- and ToT of 10 BC for 1×10^4 e^-.

at the threshold of 1500 e^- and ToT of 10 BC for 1×10^4 e^- is presented in Figure 5.3. The hit efficiency of the 50×250 μm^2 module, which has the same pixel dimensions as the IBL 3D sensors, gradually increases from around 50% to over 98% with increasing bias voltage up to around 10 V, where it approximately saturates. The 50×50 μm^2 module achieves saturation at 2 V and achieves greater than 98% efficiency; this is a natural consequence of the smaller distances between the p- and n-columns.

In addition, the changes in hit efficiency when varying the calibration target with a fixed bias voltage at 10 V were studied. A 1% efficiency loss with increasing threshold (from 1500 e^- to 2500 e^-) was observed. This is due to the loss of small-charge hits below the threshold.

Beam tests of 130 μm thick FBK devices irradiated with protons at KIT to IBL fluences were carried out in July 2017 at the CERN SPS H6 beam line using an EUDET-type telescope for particle track reconstruction. Figure 5.4 shows the efficiency for the 50×250 μm^2 geometry of a 130 μm-thick device compared to the 230 μm IBL samples from FBK and CNM. The thinner active area presents a larger efficiency due to the smaller electrode column diameter, but at a larger bias voltage due to the reduced thickness.

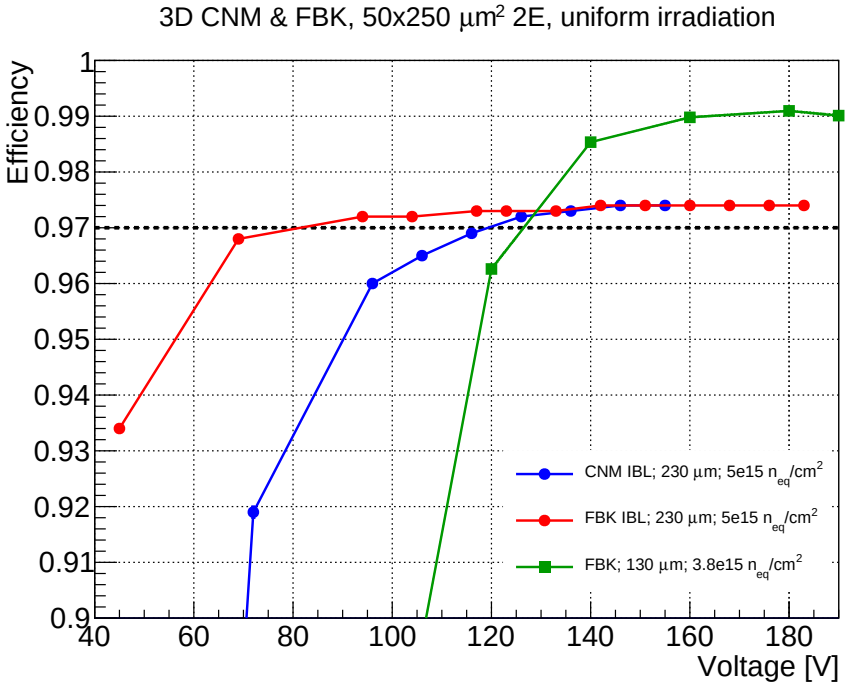


Figure 5.4: Hit efficiency as a function of bias voltage of an irradiated 130 μm-thick 3D FBK sample with the IBL geometry. Also included are the results of the irradiated CNM and FBK 230 μm IBL samples. The FBK fully passing-through columns explain the difference between these IBL results. A higher plateau is reached for the thinner sample due to the smaller diameter electrode columns, but it is reached at a higher bias voltage due to the reduced thickness.

5.5 Planar pixel sensor characterization before and after irradiation

5.5.1 Electrical tests in the lab

Several planar pixel productions in the thickness range of 100-200 μm have been completed and characterized including FE-I4 and RD53A compatible devices. In quad sensors, the area between neighbouring chips is instrumented with "ganged" pixels that are linked via an aluminum line to pixel cells connected to the chips. This arrangement constructs a full active area within the sensor bias ring. Yield, defined as the fraction of sensors with the breakdown voltage at least 50 V above V_{depl}, has been calculated after UBM processing and handle wafer removal for single and four-chip (quad) compatible sensors of a MPG-HLL production on SOI wafers. Three quad sensors over 32 were lost due to mechanical problems during the post-processing phase while one failed the electrical requirements. The total yield before chip interconnection for this production is therefore 87.5%. The IV curves for the quad modules, with a V_{depl} in the range 15-25 V, are shown in Figure 5.5. The

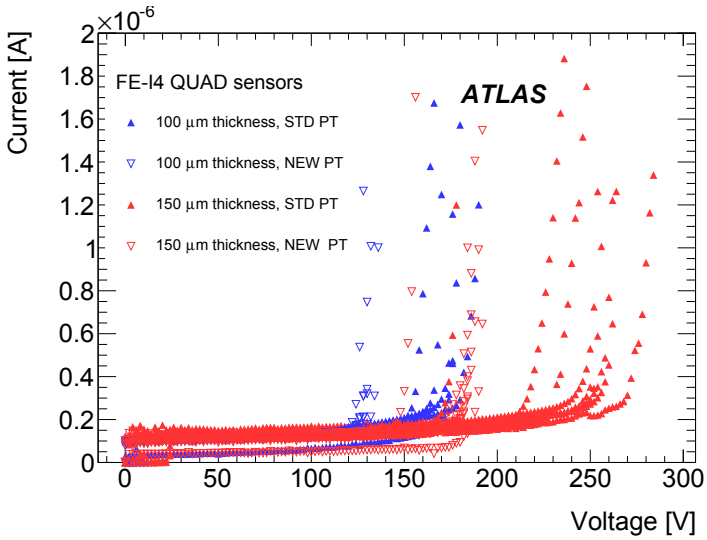


Figure 5.5: IV curves measured on FE-I4 planar quad sensors of the MPG-HLL SOI3 production of 100 and 150 μm thickness. The sensors have either a punch-through structure for every single pixel (STD) or a common structure for four pixel (NEW-PT).

power dissipation after irradiation for planar pixel sensors has been calculated for 100 μm thick FE-I4 compatible devices after irradiation with 25 MeV protons at a fluence of 2 and 5×10^{15} n_{eq}/cm^2 at a temperature of -25°C. The leakage current has been measured in a probe-station with the sensor in direct contact with the thermal chuck and evaluated after ten days of annealing at room temperature at a bias voltage of 300 and 400 V, for the lower and higher fluence point respectively. These V_{bias} values have been found to be high enough to ensure a hit efficiency above 97% with FE-I4 modules irradiated at these fluence levels. The resulting power dissipation is 4.5 mW/cm^2 at 2×10^{15} n_{eq}/cm^2 and 9 mW/cm^2 at 5×10^{15} n_{eq}/cm^2. These values of the sensor power dissipation are lower or comparable to those used to define the TFM specifications for the local support structures in Table 13.2, where for example 6.4 mW/cm^2 at 2×10^{15} n_{eq}/cm^2 was used.

5.5.2 Test beam analysis

The hit efficiencies of FE-I4 compatible sensors produced by different vendors of 100, 130 and 150 μm thickness, with a standard pixel cell design, were compared after irradiation at a fluence of 10^{16} n_{eq}/cm^2 [16] with neutrons and 24 GeV protons. The results are shown in Figure 5.6 and a better performance is observed for the 100 μm thin sensors, where they achieve the required hit efficiency at lower bias voltages compared to the thicker samples. The hit efficiency for 50×50 μm^2 pixels has been estimated by using FE-I4 compatible sensors with a modified geometry, shown in Figure 5.7. A higher charge sharing between neighbouring pixels has been observed with test beam studies in modules with these smaller implants with respect to standard FE-I4 pixel cells, especially at low voltages. After

irradiation a fluence of 3×10^{15} n_{eq}/cm^2 with 23 MeV protons, at a bias voltage of 300V, the hit efficiency is affected by the increased charge sharing. At a higher bias voltage of 500 V the hit efficiency is again more uniform across the unit cell, as shown in Figure 5.7(top). In these conditions, a hit efficiency of 98.2% was estimated for a 50×50 μm^2 cell of 150 μm thickness without any biasing structure whereas at a higher fluence of 5×10^{15} n_{eq}/cm^2 and a bias voltage of 600 V, the hit efficiency was calculated to be 97.5% for a 100 μm thick sensor (Figure 5.7(bottom)).

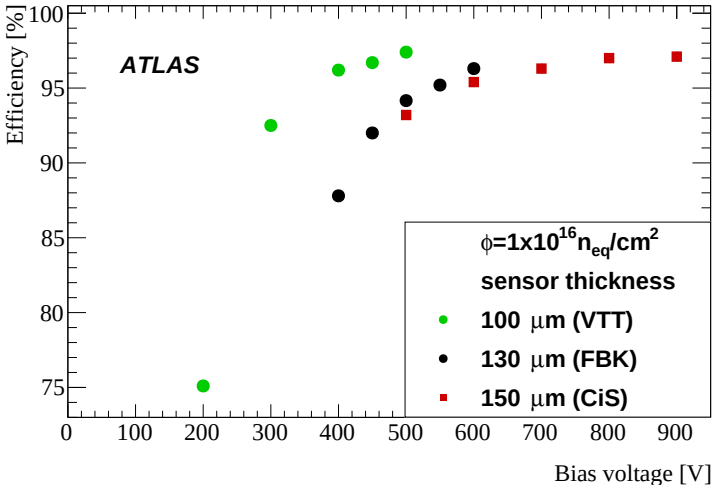


Figure 5.6: Hit efficiency measured at normal incidence in test beams at DESY and CERN SPS with FE-I4 modules assembled with 100, 130 and 150 μm thin planar sensors.

Similar studies were carried out with HPK FE-I4 sensors. In order to emulate 50×50 μm^2 pixel size, the area corresponding to two standard FE-I4 pixels, 50×500 μm^2, is divided into a 50×50 μm^2 pixel and a 50×450 μm^2 one. This is possible thanks to the particular pattern of the bumps in the FE-I4 chip, where the bump distances along the columns are alternating between 50 μm and 450 μm. In addition, pixels with 25×100 μm^2 n^+ implant shape have been implemented instead of the 50×50 μm^2 one. These two modified pixel cell geometries allow to evaluate the efficiency at the pixel boundary region for RD53A compatible devices. Three types of biasing structures for 50×50 μm^2 and one type for 25×100 μm^2 pixels are tested as shown in Figure 5.8, a) Bias rail is placed at the center of pixel boundary, b) Bias rail is shifted towards the pixel implant, c) No biasing structure implemented as reference and d) the same as type (b) but for 25×100 μm^2 pixel size.

The results of in-pixel efficiency, over the full pixel cell ($\epsilon_{overall}$) or restricted to the central region (ϵ_{center}) for various biasing structures are compared as shown in Table 5.1 after irradiation at a fluence of 3×10^{15} n_{eq}/cm^2 with 70 MeV protons. In general, the ϵ_{center} shows over 99% efficiency for all cases while $\epsilon_{overall}$ is lower than ϵ_{center} due to the charge sharing and bias rail effect at the pixel boundary region. For the sensor with no biasing structure, the efficiency loss is 2.2% due to the charge sharing effect mainly at the corners of the pixel

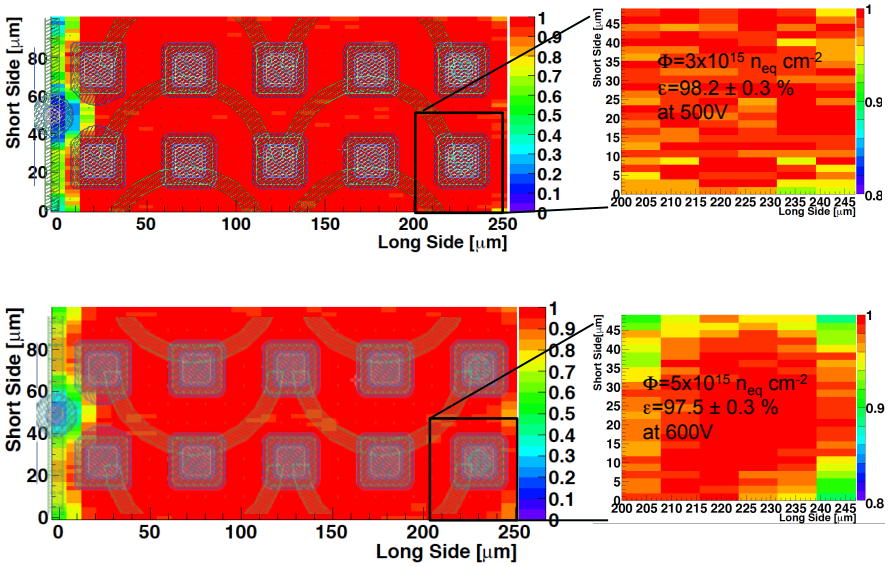
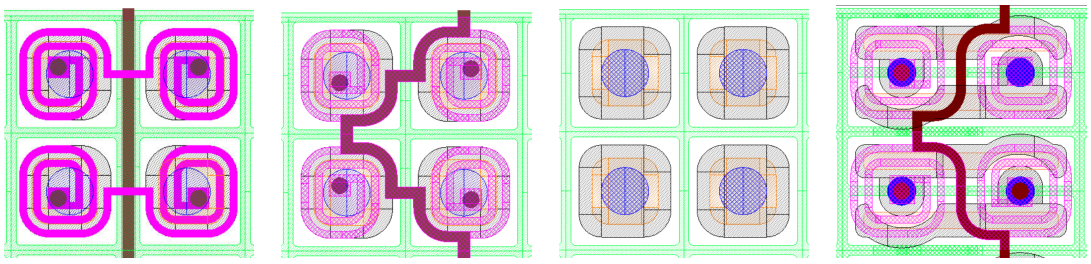


Figure 5.7: Hit efficiency measured at normal incidence for a module composed of a 150 μm thick planar sensor irradiated at a fluence of 3×10^{15} n_{eq}/cm^2 (top) and a 100 μm thin sensor irradiated at a fluence of 5×10^{15} n_{eq}/cm^2 (bottom). 50×50 μm^2 implants are read-out by neighbouring chip channels. The 50×50 μm^2 cells at the right edge are a close approximation of a RD53A compatible sensor without biasing structure and the hit efficiency is calculated for this geometry.



(a) 50×50 μm^2 with bias structure at the center of pixel boundary

(b) 50×50 μm^2 with shifted bias rail

(c) 50×50 μm^2 without biasing structure

(d) 25×100 μm^2 with shifted bias rail

Figure 5.8: Various sensor structure produced by HPK. Three types of biasing structures for 50×50 μm^2 and a type of 25×100 μm^2. a) Bias rail is placed at the center of pixel boundary, b) Bias rail is shifted towards pixel implant, c) No biasing structure implemented as reference and d) the same as type (b) but 25×100 μm^2 pixel size.

cell. An additional 3.2% efficiency loss is observed for the case of shifted biasing structure sensors due to electric field changes induced by the bias rail. A more detailed position dependence of the in-pixel efficiency for the shifted biasing structure is shown in Figure 5.9. In case the biasing structure placed at the center of the pixel boundary, the efficiency loss increases. For the 25×100 μm^2 pixel cell, the efficiency loss is 2.3%. This indicates that there is a smaller effect of the biasing structure than in the 50×50 μm^2 geometry, since the biasing structure is placed not at pixel boundary but rather overlapping to the n^+ implant as shown in Figure 5.8 (d).
In summary, with the threshold range achievable by the FE-I4 chip, a better performance is observed with sensors without any biasing structures, where the efficiency loss is only due to charge sharing effects at the pixel corners.

Table 5.1: Test beam efficiency of HPK sensors at normal incidence after 3×10^{15} n_{eq}/cm^2 irradiation with 70 MeV protons.

Type	(a)	(b)	(c)	(d)
Pixel Size	50×50 μm^2			25×100 μm^2
Biasing structure	Yes		No	Yes
Bias rail position	center of boundary	shifted	–	shifted
ϵ_{center}	99.04±0.08%	99.19±0.07%	99.33±0.07%	99.23±0.02%
$\epsilon_{overall}$	89.34±0.05%	93.87±0.04%	97.12±0.03%	96.93±0.02%

The hit efficiency has been measured in active edge sensors with a thickness range of 50-200 μm showing good performances in FBK and ADVACAM devices [86, 87]. An example of efficiency of FBK sensors along the 100 μm edge, with or without guard rings is shown in Figure 5.10. The largest difference between the two edge configurations investigated in this study is due to the data taking conditions. Due to the low energy momentum beam of DESY (electrons of 4 GeV) the pointing resolution of the telescope is poor (around 30 μm); this smears the curve describing the hit-efficiency vs track impact position. Anyhow it can be observed that both sensors are efficient well beyond the end of the last pixel implant ($x = 0$ in Figure 5.10).

The hit efficiency of passive CMOS sensors has been determined before and after irradiation with 24 MeV protons up to a fluence of 1.14×10^{15} n_{eq}/cm^2 with devices interconnected to the FE-I4 chip. A sensor breakdown at this fluence did not occur up to a maximum applied voltage of 700V. After irradiation the efficiency reaches values $>$ 99.9% for AC coupled sensors at bias voltages above 350 V, as shown in Figure 5.11. The DC coupled sensor efficiency is somewhat lower ($>$ 99% at 450 V) due to the 'blind' area taken by the punch-through biasing dot. This technology has therefore demonstrated to be radiation-hard at least up to the level expected for Layer 4.

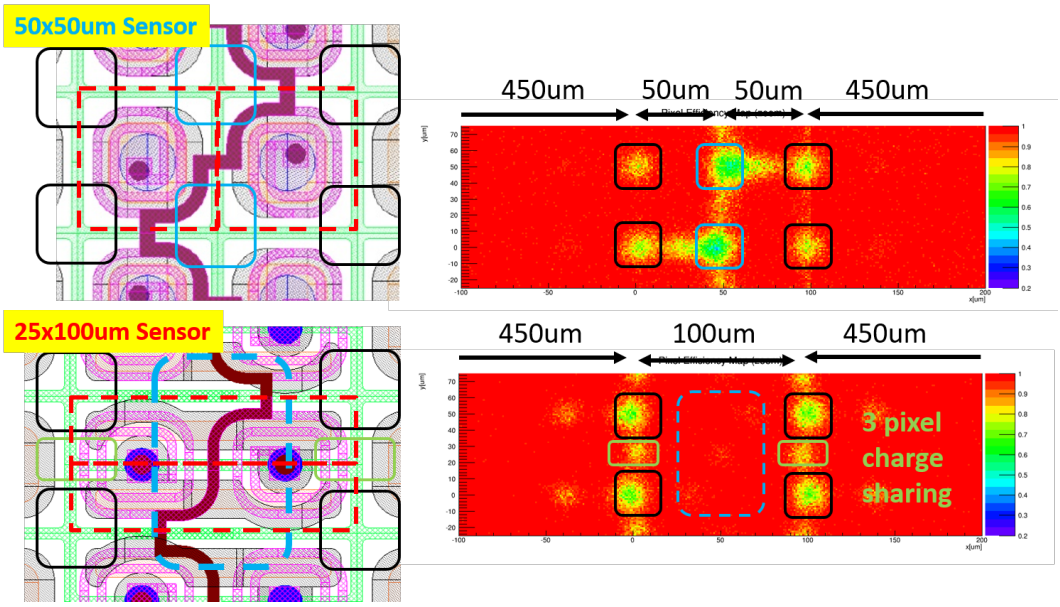


Figure 5.9: Measured in-pixel efficiency for 50×50 μm^2 (top) and 25×100 μm^2 (bottom) planar pixel cells at normal incidence after irradiation to a fluence of 3×10^{15} n_{eq}/cm^2. The left figures show the sensor structure and the right 2D-plots the in-pixel efficiency. The solid squares in the efficiency plots indicate the pixel corners as marked on the left figures.

5.6 Results with FE65-P2 and RD53A prototypes

5.6.1 Planar pixel sensors characterization before and after irradiation

Electrical tests in the lab

Planar sensors matched to the design of the RD53 chip, 100 or 150 μm thick, have been processed on SOI wafers at MPP-HLL and then electrically characterized. The pixel cells are 50×50 μm^2 or 25×100 μm^2 wide, isolated with p-spray. A fraction of the samples implement a bias rail with a punch through dot common to four pixels while in the remaining devices no biasing structures are present, as shown in Figure 5.12. The sensors with the biasing structure have been measured after UBM deposition, handle wafer etching and dicing, before interconnection to the chip. Good leakage current characteristics have been observed, as shown in Figure 5.13(a) with a yield above 95%, as calculated with about 60 structures from two different production runs.

Two devices with 50×50 μm^2 pixel cells have been irradiated with neutrons at fluences of 5×10^{15} and 10^{16} n_{eq}/cm^2. Leakage current levels compatible with those of 50×250 μm^2 pixel cells have been measured, and shown in Figure 5.13(b). The resulting power dissipation is also comparable with the one estimated for 50×250 μm^2 pixel sensors in Section 5.5,

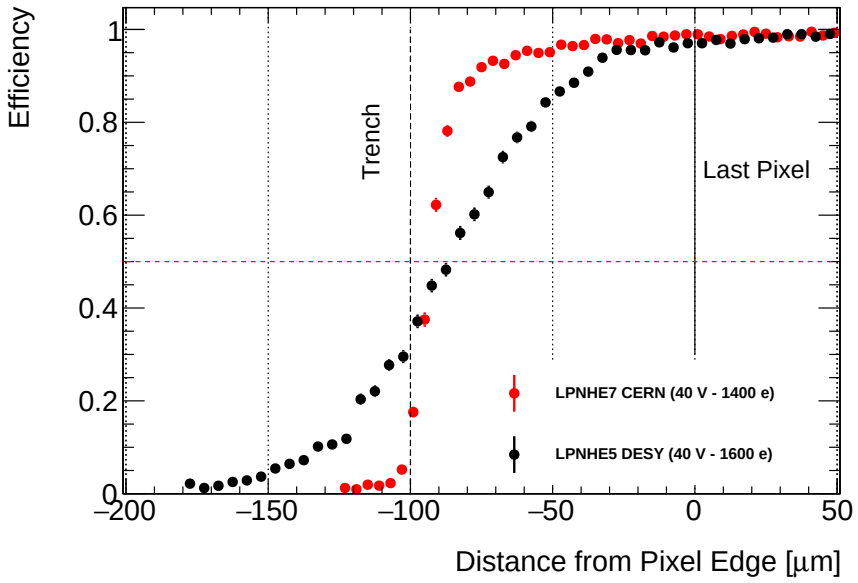


Figure 5.10: Edge efficiency profiles for two planar devices with a 100 μm active edge produced at FBK. The first one has no GRs (black markers) while the second one has 2 GRs implemented (red markers). The curves extend beyond the physical edge of the devices due to the effect of the track pointing resolution, different at DESY and CERN.

and so in agreement values used to define the TFM specifications for the local support structures.

5.6.2 Test beam analysis

Test beam analysis with modules composed of HPK planar sensors flip-chipped to the FE65-P2 chips (see Section 6.5) have been carried out at the Fermilab test beam facility and at CERN-SPS. The focus has been on studying the performance of 50×50 μm^2 and 25×100 μm^2 pixel cell sizes with lower threshold thanks to the low noise of the FE65-P2 chip. Different flavours of sensors, with and without biasing structures have been tested after irradiation with 70 MeV protons at a fluence of 3×10^{15} n_{eq}/cm^2. Due to an issue with the chip, the global efficiency drops as a function of the particle rate but the study of the different geometries still allows to evaluate the relative effect of the biasing structures on the tracking efficiency. The measurements were carried out after tuning the chip to a threshold of 700 e. Figure 5.14 shows the in-pixel efficiency projection along the column direction after having normalized to unity the average efficiency in the central part of the pixel. This shows the possible loss of efficiency caused by charge sharing and biasing structures at the cell edges. The effect of the poly-silicon resistors, implemented as illustrated in Figure 5.8(d) for a 25×100 μm^2 geometry, is visible at the pixel cell edges (x=0 and x=100 μm) in Figure 5.14(a). At 400V, when integrating over the full pixel area, the efficiency loss is

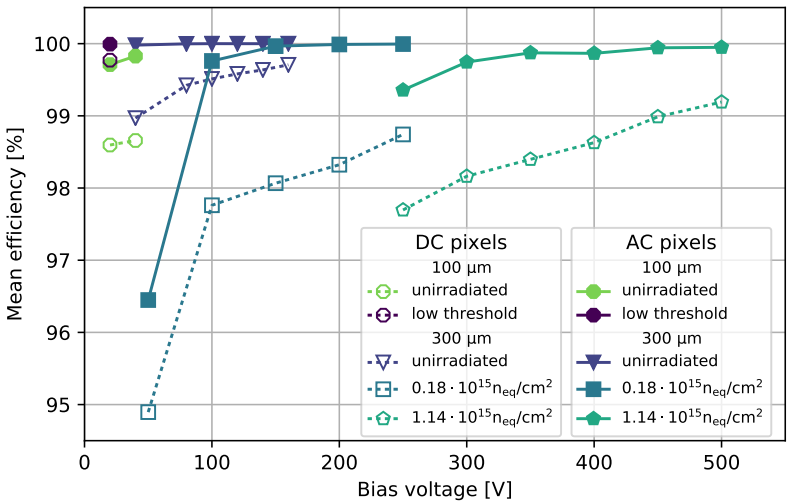


Figure 5.11: Hit detection efficiency of 100 and 300 μm thick passive CMOS pixel sensors produced by LFoundry. The hit efficiency has been extracted for different bias voltages and different levels of radiation damage. Each point represents the hit efficiency of at least 50 center pixels.

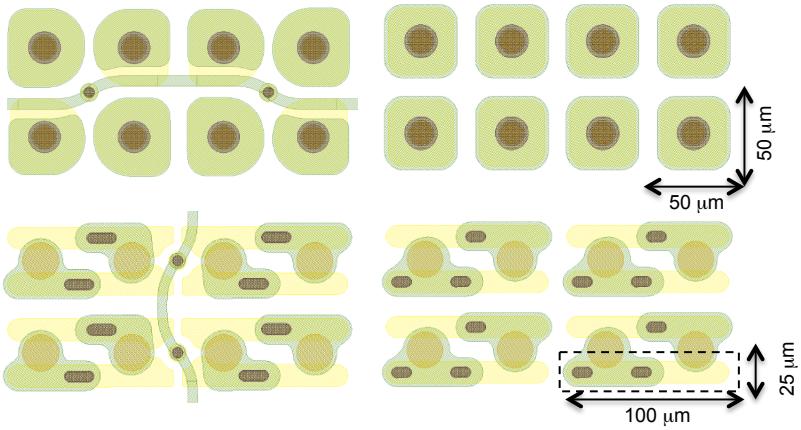


Figure 5.12: Design for 50×50 μm^2 (top) and 25×100 μm^2 (bottom) pixel cells, compatible with the RD53A chip. The designs on the left sides are relative to devices where a biasing structure has been implemented, with a punch-through dot common to four pixel cells. On the right side, pixel cells without a biasing structure are shown. The structures colored in yellow represent the n^+ implants, in green the Aluminum layer, while the brown circles show the position of the UBM pads.

(0.9$\pm$ 0.1)%, significantly lower than in the FE-I4 case, thanks to the reduced thresholds around 700 e achievable in the FE65-P2 chips. At 600V the modules without biasing structures are characterized by a flat efficiency profile along the pixel cells, with no appreciable effect either of charge sharing or biasing structures. In the case of the 50×50 μm^2 geometry, implemented as in Figure 5.8(b), no significant efficiency loss within the available statistics is visible at the pixel cell boundaries in both cases of modules with or without biasing

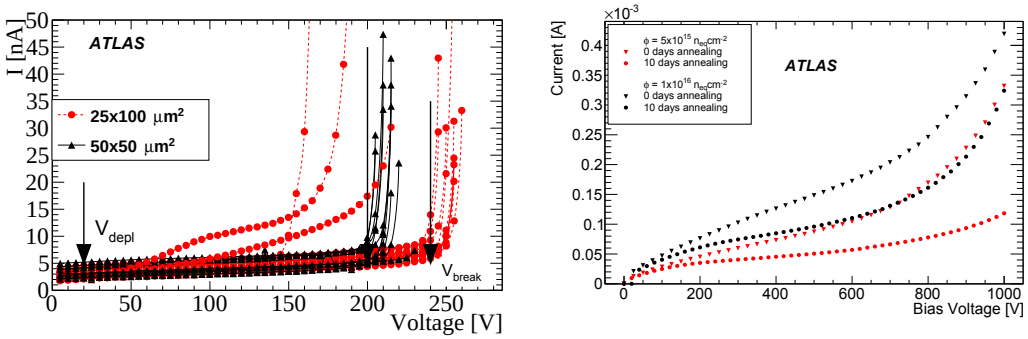
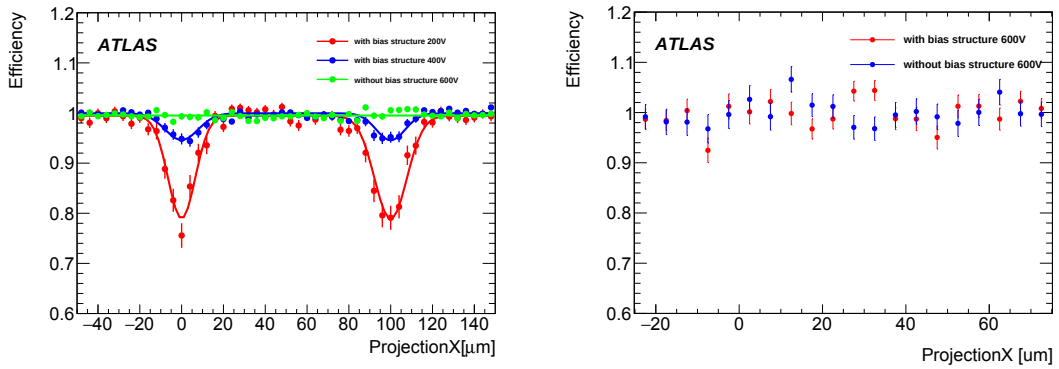


Figure 5.13: Left: IV characteristics for 50×50 μm^2 and 25×100 μm^2 planar pixel sensors, compatible with the RD53A chip, of 100 and 150 μm thin sensors, produced at MPG-HLL on SOI wafers. Right: IV characteristics after irradiation with neutrons at a fluence of 5×10^{15} and 10^{16} n_{eq}/cm^2 for 50×50 μm^2, 100 μm thick RD53A compatible sensors. The curves are shown at 0 and 10 days of annealing time at room temperature after irradiation. The current levels are compatible with those measured on FE-I4 compatible sensors.

structures. The results indicate that due to the lower thresholds, the efficiency loss due to the charge sharing or biasing structures are less than 1%.



(a) (b)

Figure 5.14: (a) Efficiency projection measured with FE65-P2 modules along the column direction for 25×100 μm^2 (a) and 50×50 μm^2 (b) geometries. The efficiencies have been normalized by fixing to unity the average efficiency in the central part of the pixel cell.

5.7 Discussion of open technological choices and production plans

5.7.1 3D sensors options

For the innermost ITk pixel layer, for which the 3D sensor technology is the only option given its power dissipation and radiation hardness results, the pixel geometry and active area thickness are still not fully decided. Both factors can have an impact on yield, which is a critical parameter for 3D productions. In particular, further studies are needed to select the optimal electrode configuration for the possible pixel geometry of 25×100 μm^2. While the single electrode design would be associated with a better yield, the double electrode approach would, in principle, offer more radiation tolerance.

These open choices can have an impact on yield. The IBL 3D sensor yield was about 50%. However, the fabrication facilities have indications that the yield of the future productions could be considerably increased after fabrication optimization. For example, the second AFP production (which finished in 2016) achieved a yield close to 85% [85]. The 6" production line of FBK and Sintef could also increase yield while reducing cost. However, when estimating the amount of time needed for the production sites to fabricate about 2 m^2 of 3D sensors to be 2 years, the fabrication facilities assumed a 50% yield.

The technical options of 3D sensors will be decided towards the end of 2018, after the performance of various prototypes from different fabrication sites is evaluated with test beams. The fabrication sites for 3D sensors will be selected shortly after that, early in 2019.

5.7.2 3D Quality control and assurance

The fabrication sites will perform electrical tests on the 3D sensor wafers to control the quality of the production. Before irradiation *good* 3D single chip sensors are required to have a leakage current below 2.5 μA/cm^2 at 20 V above the depletion voltage. Furthermore, the fabrication sites are requested to delivered wafers with at least 50% of good sensors. These requirements may be adjusted after the final decisions on the technology options are taken.

Test structures from the produced wafers will be provided to ATLAS institutions. These structures will be used to measure the leakage current as a function of the bias voltage before and after irradiation and thus monitor the quality of the sensors. Long term stability tests shall be performed on unirradiated and irradiated samples. Inter-pixel capacitance and resistance will be verified on specific test structures. Transient current technique measurements will be carried out on diodes or strip sensors to verify the depth of the 3D columns.

Sensors shall be bump-bonded to ATLAS ITk pixel front-end chips (either with SnAg/SnPb or Indium bumps). Selected modules prototypes will be irradiated to the target fluence for

the innermost layer. The performance of the sensors will be evaluated in laboratory and test beams. The hit efficiency is required to be larger than 97% (96%) before (after) irradiation at normal beam incidence (larger than 98% and 97% at 14° incidence). The power dissipation performance of the 3D sensors shall be better than 10 mW/cm^2 after irradiation at the target sensor temperature of -25 °C. The maximum operational bias voltage after irradiation should not exceed 250 V.

5.7.3 Planar sensors options

The open options for the planar sensors regard mainly the design of the pixel cells and in particular the implementation of a biasing structure to allow for the characterization of the devices before interconnection to the read-out chip. In case the associated loss of efficiency observed in the first studies with 50×50 μm^2 geometries will be confirmed in RD53A modules, a possible solution to maintain an efficiency above 97% during the entire lifetime of the detector is to omit the implementation of the biasing structure. The quality assurance before chip interconnection can be carried out depositing a temporary metal to short all the pixel cells allowing for the measurement of the IV characteristics. If a sensor production yield above 95% could be demonstrated in the pre-production phase, also this additional step could be avoided. CMOS passive sensors could represent a cost-effective alternative with respect to traditional planar sensors if full size prototypes can be demonstrated to be radiation hard up to the level needed at least for Layer 4 and if multi-chip sensors can be produced with small inactive areas in the inter-chip region. The decision on all these options concerning the planar sensor technologies will be taken within Q4 2018, before issuing the Call for Tender (see Section 5.7.4).

5.7.4 Planar Production plans

A market survey is currently in progress to identify the foundries for the planar pixel sensor production. The final step of the Market Survey process, foreseen in Q4 2018, requires the production of prototype sensors, according to the criteria that will be specified in an updated Technical Specification document and that will be as close as possible to the final ITk sensor specifications. A Call for Tender is planned for Q2 2019 and it will only be opened to those vendors that have successfully completed the Market Survey. The contract could be split among more vendors based on the quoted price, production capability (risk mitigation), and final sensor types (some types might be more suitable to certain vendors than others). Pre-production is foreseen to start in the second half of 2019.

5.7.5 Planar Quality control and assurance

Depending on the size of wafer used by interested vendors, the planar and passive CMOS pixel sensors may be delivered either as full 6″ or 8″ wafers without UBM or as diced single sensors with UBM or Indium bump deposition (mandatory for 4″ wafers), as will be described in great detail in Chapter 7. In the first case the sensor characterization and quality assurance will be performed by CERN and the ITk institutes both at wafer level and also on diced sensors after the UBM or Indium bump deposition, if permanent biasing structures are implemented in the pixel cells. In the second case the quality control will only be performed on the diced sensors with UBM. The electrical specifications will be finalized at the time of the Call for Tender. A preliminary set of criteria has been defined, requiring:

- A leakage current $< 0.75\ \mu\mathrm{A/cm^2}$ at V_{depl}+50V, where V_{depl} is the depletion voltage, measured at a temperature of 20°C and at a relative humidity <50%;
- The breakdown voltage in excess of V_{depl}+70V before irradiation, where the breakdown voltage is defined as the bias voltage where the leakage current increases by more than 20% in a 5 V step (with the exception of bias voltages between 0 and V_{depl});
- In case of full wafer delivery, a batch will be accepted if more than 80% of the sensors included therein satisfy the requirements in terms of the visual inspection and of the limits on the leakage current values.

A complete quality control program with measurements on test-structures inserted in the wafer is planned, to monitor parameters as the bulk resistivity, the inter-pixel capacitance and resistance together with sample measurements to assess the sensor properties after irradiation.

5.7.6 Path to the sensor decision in Layer 1

The decision on the sensor technology for Layer 1 will be taken within the year 2018 based on two different aspects. The first is the yield of RD53A compatible sensors that in 2018 can be estimated from several completed productions for planar and 3D sensors and the second is the performance of RD53A assemblies with the two sensor technology at the fluence expected for this layer.

6 Front-end Chips

6.1 Introduction and Requirements for the Front-end Chip

The FE chip integrates the charge generated in the sensor by crossing particles, amplifies and digitizes the signal, and sends the hit information to the DAQ system. There are two auxiliary chips for data transmission: the aggregator and the equalizer. In simplest terms, the FE chip must record the pixel charges and crossing times for 99% of incident charged particles, must hold this information until a trigger decision is received, and must read out the triggered information without loss, negligible fakes, and in a short enough time as needed for higher level triggering.

The detailed requirements of the read-out chip are derived from the detector performance as well as from interfaces with a large number of system components. It has electrical interfaces with sensor, module flex, DAQ system, DCS system, and test setups. It has mechanical interfaces with flip chip bump bonding, module assembly, mechanical supports, detector layout, and wafer processing and testing. The main requirements are covered in Sections 6.1.1-6.1.3, where the origin of each requirement is indicated.

The solution we have chosen to implement in order to meet these requirements is described in Section 6.2, followed by a review of development status and plans in the remainder of this chapter.

6.1.1 Physical, Power, and Environmental Requirements for the FE chip

A summary of physical, power, and environmental requirements is shown in Table 6.1. These FE chip properties have a large impact on the mechanical systems and layout. The power consumption is a compromise between cooling, mechanics and electronics. Higher power would necessitate significantly more massive mechanics, while too low power would make it impossible to meet the electrical performance goals. The size of the read-out chip determines the module geometry and in turn the layout modularity. The services modularity is also closely tied to the chip size as each module has an integer number of data links. At the same time the chip size is constrained by the chip fabrication process and by bump bonding planarity requirements and tooling. A chip size the same width, but slightly taller than the IBL FE-I4 chip has been selected. (See Figure 6.8 for definition of height and width.) The similarity to the FE-I4 size makes much of the module development carried out with

Table 6.1: Physical, power and environmental requirements for the Front-end chip.

Requirement	Value	Source
Matrix size columns × rows	400 × 384	Layout, IC design constraints
Input pitch	50 μm × 50 μm	Tracking performance, occupancy
d Last bump to edge on bottom	1.5 mm < d < 2.0 mm	Wire bonding, layout
d Last bump to edge elsewhere	$\leq$100 μm	Layout, sensor
Final thickness	150 μm	Material, bump bonding, local supports
Power dissipation	<0.7 W/cm^2	Cooling, local supports, sensor
Current consumption	<1.5 A/chip	Services
Temperature range	-40°C to +40°C	Cooling, operation, integration
Total ionizing dose tolerance	$\geq$500 Mrad	Inner layer lifetime before replacement
Full chip SEU upset probability	5%/hour	Inner layer operation
Pixel loss due to SEU	<1%/run	Hit efficiency, inner layer operation

FE-I4 applicable, while the slightly larger number of 50 μm rows (384 vs. 336) was shown by layout studies to simplify the local support construction, particularly in the end-caps. The radiation tolerance requirement is compatible with the inner layers being replaceable. (See Section 6.4 for details on radiation tolerance).

6.1.2 Performance and Trigger Requirements for the FE chip

The basic performance and trigger requirements are summarized in Table 6.2. As the same FE chip will be used throughout the whole ITk Pixel Detector, the innermost layer defines many critical performance requirements. Meeting these requirements in general does not hinder operation in the outer layers. As the internal settings of the chip are programmable, it will be possible to optimize differently for different layers– for example to reduce power in the outer layers. Support for more dramatic differences than optimizing bias settings has been studied and generally found not to be advantageous. For example, having the ability to mate to sensors with larger pixels in the outer layers was considered, but it was concluded that preserving fine granularity in the outer layers has performance advantages for tracking in high hit density environments such as boosted jets, while potential power reductions from larger pixels would have been modest and would not have led to significantly lower mass.

The baseline trigger requirement is uniform for the whole detector: single level 1 MHz. However, for the extended goal of 4 MHz Level-0, the outer layers would read out at the full 4 MHz without any changes to the trigger processing performed, while the inner layers would switch to a 2-level scheme with no read-out at L0 and read-out only at L1, up to 1 MHz. This is because inner layer read-out at 4 MHz would exceed the 5.12 GHz bandwidth per chip required for the chip output. The 2-level trigger processing needed by the inner layers is described in Section 6.2.1.

Table 6.2: Basic performance requirements for front end chip. (*) This is the maximum amount of time that hits may be required to be stored in the chip.

Requirement	Value	Source
Trigger Rate	1 MHz with option 4 MHz	Trigger and DAQ
Trigger latency	<35 μs	Trigger and DAQ (*)
Trigger protocol	Tagged trigger	DAQ, operation
Single pixel noise (ENC)	<100 e^-	Threshold, resolution
Min. stable threshold after irradiation	600 e^-	Hit efficiency for thin sensors
In-time threshold	< (thresh.+600 e^-)	Hit efficiency, out of time pileup
Threshold dispersion after tuning	40 e^-	Uniformity, efficiency
Threshold dispersion variation	<5%/K	Operation
Threshold variation	<10%/K	Operation
Noise occupancy per pixel	$<10^{-6}$	Tracking performance, operation
Hit loss at 75 kHz pixel hit rate	$\leq$1%	Hit efficiency for inner layer
Recovery from saturation	<1 μs	Efficiency, pileup
Charge measurement resolution	<600 e^-	Tracking performance, resolution
Charge dynamic range	$\geq$4 bits	Physics, high density tracking

Table 6.3: Basic electrical interface and Input/Output requirements for the FE chip.

Requirement	Value	Source
Analog front end current/pixel	<4 μA	Power requirements
Digital current/pixel, 75 kHz hit rate	4 μA	Power requirements
Periphery current	<200 mA	Power requirements
Power supply	single supply 2 V max.	Serial power distribution
Power supply mode	constant current	Serial power distribution
Command & control	serial DC-balanced	Mass, services (no separate clock)
Beam clock and phase	Recovered from serial in	Mass and services, operation
Beam clock phase adjustment	32 steps of 1.5 ns	Operation
Effective bandwidth for config. bits	>10 Mbps	Calibration
Data output	Differential serial port	Mass and services
Max. chip output bandwidth	5.12 Gbps	Inner layer at 1 MHz trigger
Output encoding	64b/66b standard	DAQ, bandwidth

6.1.3 Electrical and Input/Output Requirements for the FE chip

The basic electrical interface and I/O requirements are summarized in Table 6.3. There are two large differences compared to previous detectors: the use of serial power distribution (Section 6.2.3), and the much higher data output rate (Section 6.2.2): a factor of 39 higher than for the IBL detector (the frequency is 32 times higher but the use or 64b/66b encoding instead of 8b/10b adds another 22% of usable data bandwidth).

6.2 Front-end Chip Description

The FE chip to meet the above requirements will be produced in 65 nm feature size CMOS technology through a CERN frame contract and delivered on 300 mm diameter wafers. The completed and the remaining development to deliver the FE chip are described in Section 6.3. The FE chip will be a 20 mm wide by 21 mm tall die with 153,600 pixels (400 by 384). The chip will contain approximately 500 M transistors (to be compared to the IBL FE-I4 with 90 M). The pixel input bump pitch will be 50 μm by 50 μm, which was chosen to keep the same bump minimum spacing as in the original Pixel Detector and the IBL, to minimize bump bonding development and risk. This is compatible with sensors having square pixels 50 μm by 50 μm, but also with other pixel shapes, such as 25 μm by 100 μm, as long as the bump locations remain on a 50 μm by 50 μm grid. Wire bond pads will span the 20 mm width at the bottom of chip: no pads are allowed on the sides of the pixel matrix. These wire bond pads will be compatible with through-silicon via (TSV) processing to allow future development, even though TSV will not be used in the ITk.

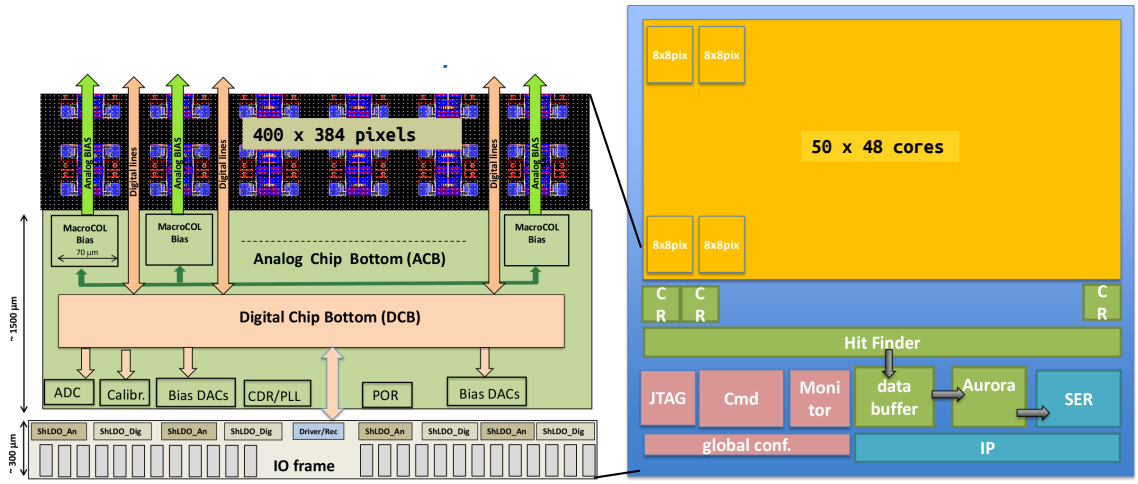


Figure 6.1: Diagram of the production read-out chip. The right side shows the digital hierarchy while the left side shows the top level organization including analog circuits.

Diagrams of the functional and the layout organization of the read-out chip are shown in Figure 6.1. The pixel matrix is built up of digital *cores* with 64 pixel channels each (8 by 8). The layout uses an "analog island in digital sea" approach, in which the 8 by 8 core is constructed as a unit using digital synthesis tools, which optimize placement for routing and logic area utilization, but do not have single pixel translational symmetry (Figure 6.2). The analog front ends are contained in 2 by 2 pixel units called "analog islands" as they are completely surrounded by synthesized logic.

The digital core handles all processing of the front end binary outputs, including masking, digital injection, charge digitization using Time over Threshold (ToT), storage of ToT val-

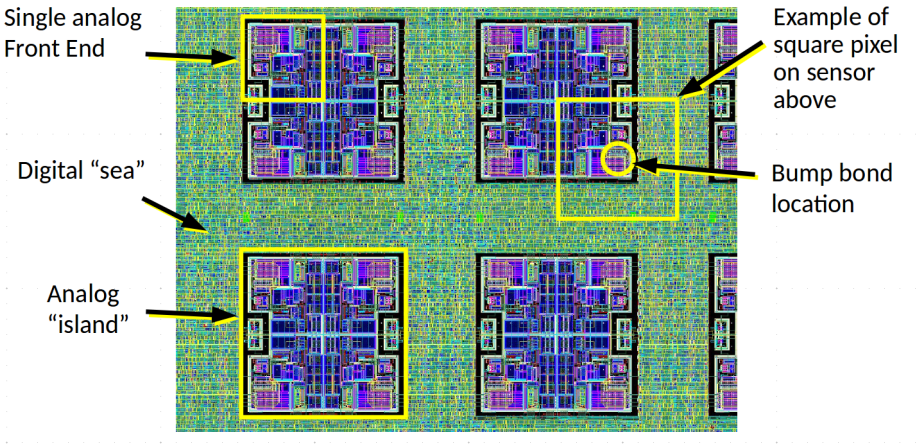


Figure 6.2: Layout detail from RD53A illustrating the concept of islands of analog circuitry (blue) embedded in a "digital sea" of synthesized logic (green).

ues, latency timing, triggering, and read-out. Each core is logically divided into 16 4-pixel regions, which have identical functionality, but differ in address and are not identical in terms of layout because they are all synthesized together in one flat layout (digital sea). Each region spans 4 columns and one row and therefore covers an effective area of 50 μm $\times$ 200 μm. In terms of a sensor this means 1 $\times$ 4 50x50 μm^2 pixels or 2 $\times$ 2 25x100 μm^2 pixels. Because the beam spot is extended in Z, clusters in the detector barrel have a rectangular rather than square shape and are more efficiently recorded with 50 μm $\times$ 200 μm regions than they would be with 100 μm $\times$ 100 μm regions. Note that there is no one-to-one correspondence between 4-pixel analog islands and 4-pixel digital regions.

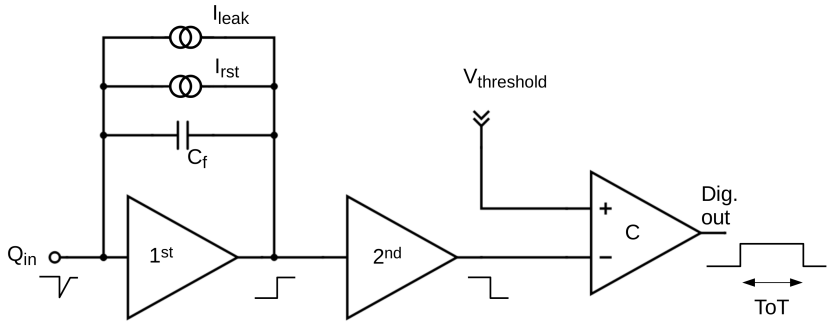


Figure 6.3: Simplified diagram of analog front end. This is conceptual only- refer to text for details on the different stages.

The analog front end is a pure analog circuit: it contains no memory latches, flip-flops or counters. A simplified schematic is shown in Figure 6.3. Static configuration values are

provided by the digital core, which receives only the comparator output signal from the analog part. The design is a small-area low-power free-running front-end, for negative input charge. The ADC function is implemented entirely in the digital core, by digitizing the time-over-threshold (ToT) of the comparator pulse. The pre-amplifier or 1st stage is a cascode circuit with NMOS input transistor in weak inversion. It has a continuous current reset that defines the trailing edge of recorded hits. This trailing edge must be fast enough to keep in-pixel pileup below the 1% hit loss spec, yet slow enough to allow time-over-threshold amplitude digitization using the effective counter clock rate of 80 MHz. The reset current is adjustable, but a typical value for HL-LHC will give a return to baseline for a 1 MIP pulse of 200 ns. It also contains a leakage current compensation feedback that is very low bandwidth and cancels DC leakage current in the sensor. A 2nd stage provides gain (with no additional shaping) in front of a comparator to discriminate the hit threshold. The threshold has a global adjustment plus local trimming (5 bits). The local trimming DAC is a resistor ladder. The trimming allows the chip to meet the tuned dispersion requirement.

The chip bottom contains analog bias generation and monitoring, global configuration and command processing (Section 6.2.1), event building and data output (Section 6.2.2), and power regulation (Section 6.2.3).

6.2.1 Command, Configuration, and Trigger

A custom communication protocol developed by RD53 will be used for all communication to the read-out chip. It consists of a single serial stream, differential and compatible with GBT e-links. The protocol uses a DC-balanced custom code at 160 Mbps, which allows for clock recovery by a Phase Locked Loop (PLL) in the chip. The reason a custom protocol was developed rather than using an existing standard, such as 8b/10b, was the requirement to have synchronous trigger commands. The RD53 protocol consists of a steady stream of 16-bit frames. Each frame has a specific meaning and known timing aligned to the bunch crossings (see [88] for details).

A trigger command occupies one single frame and specifies which of the 4 bunch crossings spanned by the 16-bit frame were triggered. Any combination of triggers is allowed, from any single one to all four of the bunch crossings. Additionally, the trigger command contains a *trigger tag*, which is a 5-bit code assigned by the DAQ system to that trigger. The FE chip simply remembers this code and returns it with the data belonging to the trigger, with an additional 2 bits to specify which one of the 4 bunch crossings is being read out. This new handshake protocol will solve loss of synchronization errors that occur frequently in operation of the current detector.

The communication protocols are more sophisticated than in previous chips, addressing several operational difficulties experienced in the present detector. Both control of the chip and data output implement two parallel, time multiplexed channels that are always active. It is no longer necessary to choose between configuring or triggering: both operations

can be concurrent. This permits a continuous reconfiguration of the pixels during operation (known as trickle configuration), which is an effective way to mitigate SEU upsets (Section 6.4.2). At 4 MHz trigger rate, which is the worst case, the rate at which trickle configuration can refresh pixel bits during triggered operation is approximately 20 Mbits/s, which means reconfiguring the 153,600-pixel chip would take 60 ms (as each pixel has 8 bits of configuration).

While the ATLAS baseline is a single level trigger up to 1 MHz, two level triggering is also supported to allow compatibility with the 4 MHz level-0 option (L0). The FE chip trigger protocol described above can run at 4 MHz, and the outer layers would do just that. However, the data output bandwidth in the inner layers is insufficient for 4 MHz read-out. Therefore, in 2-level trigger mode, the FE chip does not send any output on an L0 trigger, but retains the triggered data for an additional (L1) latency. The L1 signal simply initiates read-out of such stored data. It must still be decided whether the L1 command will identify data by its 7-bit trigger tag, or use a fixed latency. For a 25 μs L1 latency (following he L0), the 7-bit tag will not always be unique at 4 MHz average L0 rate, but this can be handled based on order or latency within a range.

6.2.2 Output Data Transmission and Compression

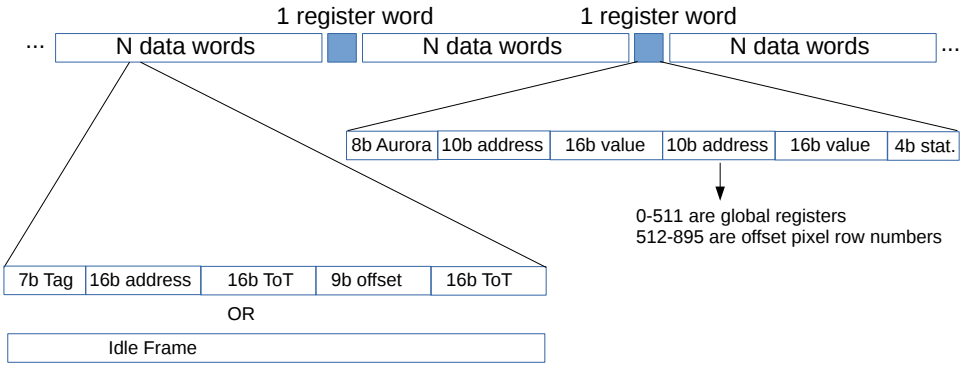


Figure 6.4: Diagram of the pixel read-out data output format. Each non-idle data frame contains a trigger tag and the address and ToT values for two 4-pixel regions.

The required output data bandwidth per chip is 5.12 Gbps for the inner layer, to be compared to 160 Mbps in the IBL. While simple scaling by the increase in pileup times trigger rate from 40 $\times$ 100 kHz in Run 2 to 200 $\times$ 1 MHz in Run 4 would suggest a factor of 50, there are mitigating factors such as reduced sensor thickness and use of a more efficient data encoding (64b/66b instead of 8b/10b). 64b/66b is an industry standard encoding protocol that provides DC-balance and is applied as the final step before transmission. The

data output format before the 64b/66b encoding is shown in Figure 6.4 (more details on data transmission can be found in [88]). A fixed fraction (about 2%) of output frames is devoted to non-hit information, such as register readback and error/warning/status messages (shown in blue). Hit information is sent out in just one frame type, with every frame containing a trigger tag. It packs the information from two 4-pixel regions into each 64-bit frame, including 4 bits ToT/pixel. Bandwidth calculations in this document assume this data format. Further lossless compression is possible, for example by using Huffman coding of ToT information. Such compression will be implemented as a switchable option, not as a baseline. In simulation, 20-40% reductions in data volume have been found with such compression. The compressed data volume approaches the expected information content limit [89]. However, compression makes the data more vulnerable because entire events must be compressed, not single hits, such that a single corrupted bit during transmission will corrupt an entire event. Compression will, therefore, be kept as a safety margin in case of higher rates than expected, but will be off as the baseline.

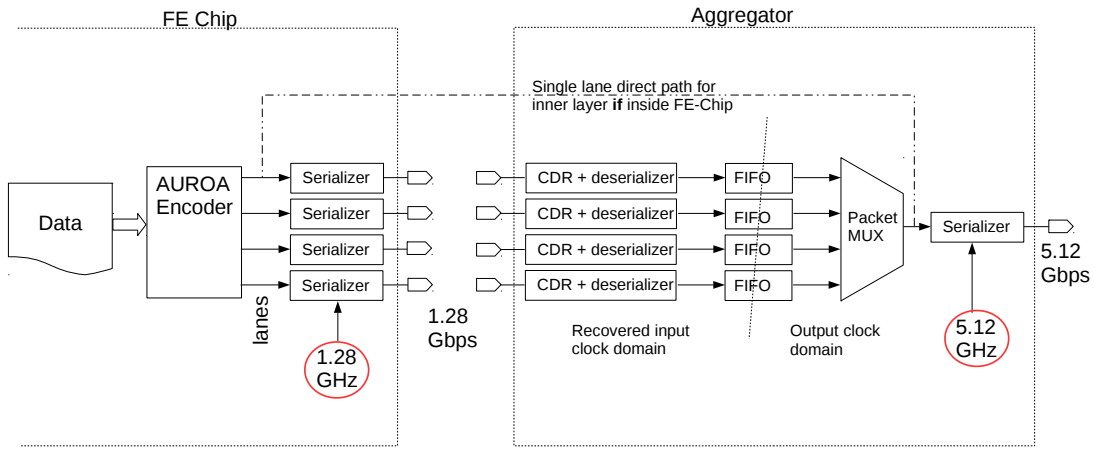


Figure 6.5: Diagram of the data aggregation between one or more FE chips and the 5.12 Gbps output. The vertical dotted line through the FIFO's indicates a clock domain crossing- data are written to the FIFO with one clock and read out with another without any frequency or phase synchronization.

The FE chip data output is implemented using four 1.28 Gbps differential lanes [1] using AURORA multilane 64b/66b commercial protocol. This protocol is supported by FPGA devices commonly used in ATLAS. The number of enabled lanes is programmable: inner layer FE chips will use all four lanes, while outer layer chips will use a single lane. In all cases, four lanes from the same module will connect to an aggregator chip that combines the 4 lanes into one 5.12 Gbps output. This is shown schematically in Figure 6.5. Because, for all but the inner layers, data from two or more chips must be aggregated, the baseline for the aggregator is a separate IC, rather than a circuit built into the FE chip. The baseline

[1] A data lane refers to a single serial link of a multiple link transmission bus. The term lane is colloquial and is analogous to traffic lanes on a highway.

placement of the aggregator IC is within the active cable link, as described below. Placing it on the module flex is an option. The high speed clock sources for both FE and aggregator have been circled in Figure 6.5 to indicate that decisions on their exact implementation still have to be made. These choices, along with the options for aggregator circuit placement, will be made following experience with the RD53A and lpGBTx chips, as well as clock prototype test chips, in September 2018.

Aggregator Chip

The aggregator chip is closely related to the lpGBTx and will be based on it, built in the same technology, and reusing critical high speed circuitry. However, there are some differences that require development. One such important difference is that lpGBTx is being designed for 200 Mrad total dose, whereas a 500 Mrad spec is needed for the aggregator. This involves selection of specific digital libraries and possible modification of analog blocks using RD53 simulation models. lpGBTx can accept four 1.28 Gbps inputs and produce one 5.12 Gbps output, but the lpGBTx is general purpose and implements other input and output modes as well as a down link. The lpGBTx uses an input high speed down link to define its clock reference, and expects the inputs to be derived from this clock reference (it can compensate for phase shifts, not frequency shifts). It does not assume anything about the encoding of the inputs and so cannot perform clock and data recovery on them. The ITk pixel aggregator baseline is to have an internal standalone clock reference, and to recover a clock from each input stream, as shown in Figure 6.5. The 5.12 Gbps driver of the ITk aggregator must match the impedance of the selected twinax, which is the planed output transmission medium inside the detector volume (see Chapter 10). The ITk aggregator will be significantly lower power by being single purpose rather than general purpose.

Active Cable High Speed Link

The active cable concept is modeled on commercial components in order to benefit from the high reliability of proven industrial solutions. Commercial products, however, are not intended for the Pixel Detector high radiation environment. Therefore, the pixel active cable will be fabricated by a commercial vendor on a commercial connector platform such as Firefly, but using two IC's supplied by ATLAS (aggregator at the transmitting end and equalizer at the receiving end). The active cable schematic is shown in Figure 6.6. The termination of twinax cable to connector substrate is done using specialized equipment and established methods to control impedance and achieve very low loss. The high speed transmission line is thus ideally coupled to both driver and receiver ends, and completely decoupled from the rest of the system. Thus it can be developed and qualified independently and, once plugged in, successful transmission is guaranteed.

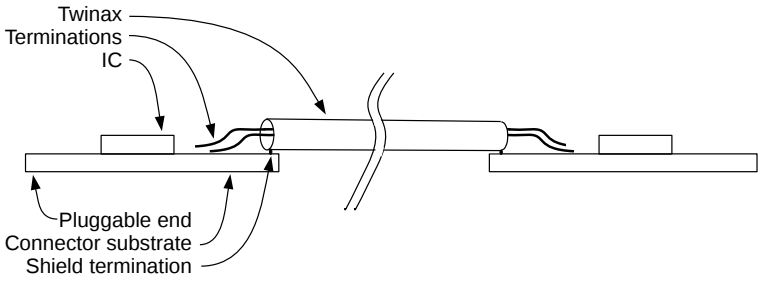


Figure 6.6: Diagram of an active cable. The transmission line is a twinax cable, the twinax conductors are terminated directly to the substrate of a commercial connector system, for example by laser welding.

In addition to decoupling the high speed data transmission development, the active cable approach affords significant system design flexibility. This is because the signals on module and module flex pigtails will be 1.28 Gbps which is much more tolerant of routing on lossy components and small impedance mismatches than 5.12 Gbps. Because the 5.12 Gbps transmission twinax cable is integrated between custom driver and receiver IC's without any intervening connectors, the cable impedance can be chosen as needed allowing for smaller diameter cables than would be the case for standard 100 Ω impedance.

As in commercial active cables, power for the chips within the connectors is supplied by the "clients" at either end the same way as the signals. The twinax cable is AC coupled so that both ends are DC isolated.

Equalizer Chip

At the other end of the active cable from the aggregator, the baseline is to have a receiver with equalization: the equalizer chip. Depending on the final twinax choice, the attenuation over a 5 m length will be between 10 and 15 dB at 3 GHz (the fundamental frequency of the 5.12 Gbps stream is 2.56 GHz). As in any cable, the attenuation is not constant with frequency and therefore distorts the signals. Without equalization, a clean eye diagram cannot be obtained. Driver pre-emphasis will be included in the aggregator chip, but this alone may not be enough and so we assume active equalization at the receiver as a baseline. Different types of equalizer are being studied (CTLE, DFE as available in modern FPGA's, and possibly others). The equalizer type will be decided in September 2018. The equalizer provides a regenerated, clean 5.12 Gbps signal that can be routed to the laser drivers in the opto board. The equalizer chip is at the opto box where power and cooling are available.

6.2.3 Serial powering

To support serial powered operation, the chip design assumes a constant current, rather than a constant voltage power supply. Special power regulators called ShuLDOs (a combination of the word shunt and the acronym for Low Drop Out regulator) are used to generate internal constant voltage rails while drawing a constant current from an external power source (Figure 6.7). The ShuLDO topology was developed and already included in the FE-I4 chip as a standalone element [90]. FE-I4 ShuLDOs are used in the IBL detector to suppress voltage transients and so comply with power distribution over resistive cables, but constant current powering is not used in IBL.

The ITk chip ShuLDO architecture will be implemented as a distributed network in the FE chip, with design improvements over FE-I4 in order to lower the overhead power needed for regulation and to address potential startup issues. The distributed design avoids the concentration of all chip current at a single point, as is the case for the FE-I4 stand-alone regulators. Other improvements prevent transient ringing that can happen in FE-I4 ShuLDOs under certain startup conditions. The read-out chip will contain two separate ShuLDO circuits to generate separate analog and digital internal rails from a common input current source. Although the maximum transistor gate voltage is 1.32 V, the circuit is designed to function safely up to 2 V input, providing a large operating margin for serial power chain implementation.

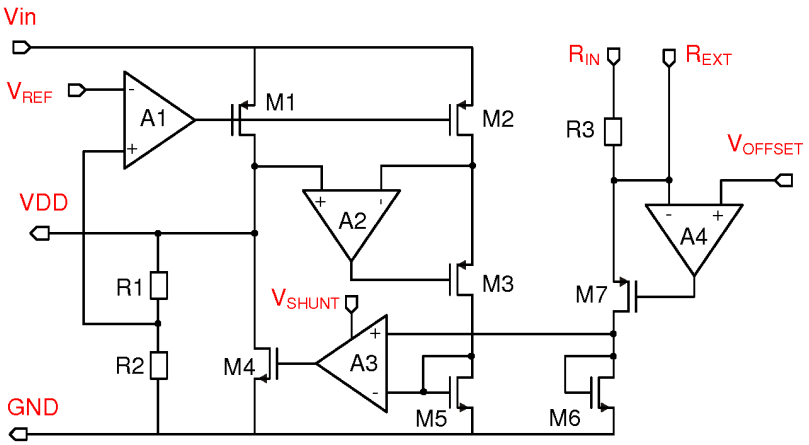


Figure 6.7: Circuit schematic for LDO regulator with shunt capability (Shunt-LDO or ShuLDO). Two such regulators will be used, one generating analog and the other digital internal rails, from a common input current source. For each, the transistors M1 and M4 will be composed of multiple replicas along the chip bottom to evenly distribute the current.

6.3 Development Status and Plan

The pixel read-out chip requirements represent a very large step compared to Run 1 and the present status is the result of many years of evolutionary development. This development is now entering its last phase: the definition of final specifications and their implementation into the physical final design chip. A half-size prototype called RD53A, containing all elements and using the same process (65 nm CMOS) and design flow as the ITk chip has been fabricated (Nov. 2017), but not yet characterized. In particular, radiation testing and characterization of modules produced with RD53A will happen after this TDR. These steps are essential before the ITk pixel chip design can be finalized. Nevertheless, even before these steps, the design process, technology, and performance are well understood, making the overall technical risk low, and moderate in the case of data transmission (Section 6.2.2). Results on performance of hybrid pixel modules with 50×50 μm^2 pixels were obtained using small scale demonstrator chips discussed in Section 6.5.

When assessing the technical risk and schedule of the read-out chip it is important to keep in mind the technology development time-line, which is much longer than for any other detector component and even precedes the definition of the ITk project. This is currently year 10 of a 12 year development cycle. Already in 2006 an upgrade requirements document [91] stated: "we assume that the electronics for the B-layer replacement will be developed in a 130 nm CMOS process. For SLHC developments, assume that we will look at 90 nm and 65 nm processes", while in 2008 ref. [92] said: "Development of this chip [FE-I4] is considered as an intermediate step towards super-LHC upgrade, and also allows having a smaller radius insertable pixel layer." The final development step following the use of the FE-I4 chip [72] in the IBL detector [3] has been carried out by the RD53 Collaboration (Section 6.3.1), established in 2013 to "develop the next generation of pixel read-out chips, needed for the High Luminosity LHC detector upgrades" [93]. While RD53 started from the experience of the FE-I4 chip, it was a ground-up development on a larger scale, with a more advanced technology, and with an expanded scope to serve the needs of both ATLAS and CMS upgrades. The production design will also be carried out by the RD53 Collaboration for both experiments.

6.3.1 The RD53 Collaboration and the RD53A Prototype

The RD53 Collaboration[2] was established with the goal of developing the technology and design platform specifically for the pixel chips needed by ATLAS and CMS at the HL-LHC. The collaboration has 18 member institutes and approximately 30 IC design engineers plus 20 students, postdocs and physicists. The deliverable of the RD53 Collaboration as originally planned is embodied by the RD53A integrated circuit. RD53A validates the design environment and basic circuit blocks, which are to be reused in the production chips, thus

[2] www.cern.ch/RD53

retiring most of the technical risk from the production design. The original scope of RD53 ended at this point, but it has now been extended to execute the production chip designs, as it has been recognized that there is a strong design team that works very well together, and splitting into separate ATLAS and CMS efforts would diminish both.

The RD53 Collaboration and the CERN IC design group investigated the chosen 65 nm CMOS process in great detail, as well as other processes for comparison. Effects of radiation up to 1 Grad dose have been characterized and understood at the level needed, as discussed in Section 6.4. Models of radiation damage have been created and using these models the RD53A has been designed to meet all requirements after 500 Mrad dose. Testing of the actual circuit will determine the ultimate radiation tolerance beyond 500 Mrad and expose any weak points to be addressed in the production chip design.

The 65 nm feature size process is needed for its high logic density. Radiation tolerance and smaller pixel size were not the reasons for choosing 65 nm over the 130 nm feature size process used for FE-I4. Logic density is critical to operating efficiently in a very high hit rate environment with relatively long trigger latency because logic density determines how many hits can be stored per unit area during the latency period. While radiation tolerance considerations exclude the use of the absolute smallest size devices in the 65 nm technology, the logic density achieved is still about 3 times higher than in 130 nm technology for similar radiation tolerance.

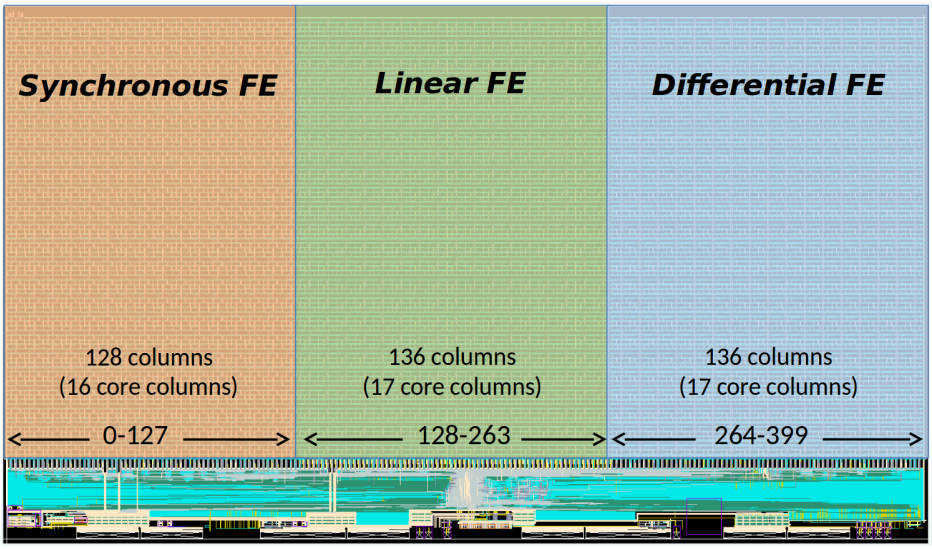


Figure 6.8: Photograph of the RD53A integrated circuit. References to bottom, top, left, and right throughout the text assume the orientation in this picture.

The RD53A chip (Figure 6.8) was designed to meet prototype (not production) specifications [94] developed ahead of time and approved by ATLAS and CMS. The physical size is half of that desired for production in order to fit in a shared wafer run to lower prototyping cost. Nevertheless, this is large enough to validate "large chip" effects in both design and

Table 6.4: Basic properties of RD53A chip compared to the production specifications. Differences are highlighted in bold.

Feature	RD53A	Prod. spec.	Comment
Input pitch	50 μm × 50 μm	50 μm × 50 μm	aspect ratio defined by sensor
Bump columns × rows	400 × 192	400 × **384**	
Input polarity	Negative	Negative	
Min. stable threshold	600 e^-	600 e^-	with 50 fF load, 4μA/pixel analog.
In-time threshold	< (thresh.+600 e^-)	< (thresh.+600 e^-)	varies w/ front end
Hit loss to in-pixel pileup	$\leq$1%	$\leq$1%	at 75 kHz avg. hit rate
Single pixel noise (ENC)	<100 e^-	<100 e^-	with 50 fF load; varies w/front end
Trigger latency	<12.8 μs	**<35 μs**	
Trigger mode	single level	**t**wo level	
Current/pixel, analog	3-4 μA	<4 μA	varies w/ front end
Current/pixel, digital	4 μA	4 μA	at 75 kHz/pixel and 1 MHz trigger
Current, periphery	<150 mA	**<200 mA**	4 enabled output drivers
Command & control	serial 160 Mbps	serial 160 Mbps	DC-balanced, no separate clock
Output	4 × 1.28 Gbps	4 × 1.28 Gbps	
Output protocol	Aurora 64b/66b	Aurora 64b/66b	can use 1 to 4 lanes
Data aggregator output	none	bf 5.12 Gbps	

performance. RD53A is 20 mm wide by 12 mm tall, containing 76 800 pixels and 240 M transistors. It contains three different analog front end designs and two different pixel matrix read-out architecture implementations, to allow for detailed performance comparisons.

Table 6.4 summarizes some basic properties of RD53A side-by-side with the specified values for the production chip. There are very few differences in the specifications, mainly having to do with size and trigger. The features that carry over from RD53A to production will need minor or no revisions. They include powering (Section 6.2.3), command and configuration protocol (Section 6.2.1), and output data format.

RD53A has been produced on an engineering wafer run shared with the CMS MPA and SSA chips. The wafer diameter for this process is 300 mm, which presents some challenges for processing (probing, thinning, bump deposition, dicing) as all prior experience is with 200 mm or smaller wafers and much of the available equipment cannot handle the larger size. Single chip tests are starting and 2 wafers are being sent untested to processing for initial bump bonding at the time of writing (Nov. 2017). The TDR schedule is not compatible with including RD53A test results.

6.3.2 Novel Features in RD53A

RD53A contains most of the features described in Section 6.2, which represent important advances relative to prior state of the art. These features were aggressive and high risk at the time they were introduced, but are now proven and available for the ITk read-out

chip with essentially no risk. Waiting for full characterization of RD53A is not necessary to understand these items.

The pixel size is 5 times smaller than FE-I4, yet it can cope with higher hit rate per pixel (75 kHz vs. 50 kHz for FE-I4). The RD53A layout uses the "analog island in digital sea" approach described in Section 6.2. Both the pixel size and layout approach have been validated in silicon with small prototypes leading up to RD53A (Section 6.5).

The pixels within a core are further grouped into logical units called regions for efficient memory utilization. Two region variants have been implemented in RD53A: a 4-pixel region with distributed memory, similar to the FE-I4 architecture, and a 4-by-4 centralized memory region. The latter stores only the ToT values of up to 6 hit pixels per event in a shared memory bank, whereas the former stores the ToT value of every pixel in every event, even if the value is zero. Both hold up to 8 events with at least one hit pixel per event during the trigger latency. The 4-pixel region turns out to occupy less silicon circuit real estate, even though it contains more memory per unit area, because it needs less logic and has simpler connectivity. It additionally consumes slightly less power, and so we have assumed it will be used in the ITk chip, barring surprises in RD53A test results.

The input and output communication protocols described in Section 6.2 have already been implemented in RD53A. While testing of RD53A will confirm that there are no problems with the implementation, the functioning of the protocols has already been validated with extensive simulations.

The RD53A chip has been designed from the start to operate in a serial power chain, and the power circuits have been sized for a full production chip (twice as many pixels as RD53A). The power circuits will, therefore, be preserved unchanged (unless problems are revealed by RD53A and system testing).

There are improved calibration functions, such as the ability to inject consecutive pulses into the same pixel, improved system level functions, such as internal adjustment of the clock phase to time-in each chip to the bunch crossings, and many test functions, such as dedicated ring oscillators to monitor radiation damage to different types of logic cells.

6.3.3 Changes from RD53A to Production

The following list gives the basic changes to the RD53A chip that are needed to arrive at the ITk chip design. While technical design details are beyond the scope of this TDR, this list should give an idea of the work scope. Most of the changes are evolutionary and straightforward, even if they involve a significant amount of work. The new feature that needs development and carries moderate technical risk is the 5.12 Gbps serial output of the aggregator chip. This development is decoupled from the FE chip following the active cable approach as already explained.

- Choose one front end flavor (there are 3 flavors in RD53A).

- Double the matrix number of rows from 192 to 384 (number of columns remains the same at 400).
- Adjust bias ranges to comply with specified maximum allowed current consumption.
- Add different bias settings for edge (left, right, and top) pixels for inter-chip gap spanning.
- Choose a pixel region architecture (there are 2 architectures in RD53A).
- Modify the command protocol to include a L0 fast clear as needed for two trigger level operation.
- Add the level 0 fast clear function to the pixel region logic.
- Increase the latency range from 9 bits to 11 bits to span the full L1 latency in the two-level trigger case.
- Add capability to count ToT at 80 MHz.
- Add capability to switch to more than 4 ToT bits in outer layers, as well as the ability to switch to binary read-out.
- Add boundary scans to all bottom of chip logic for structural testing. Additional design for test features should be investigated.
- Add additional SEU hardening to bottom of chip logic if tests show it is needed (experience shows this is never perfect the first time).
- Change the standard cell library used for high speed elements to increase radiation tolerance if needed (12 track library was not available for RD53A development, but is available now).
- Reduce digital power through optimization if needed.
- Add event truncation functionality to clear rare extremely high occupancy events.
- Add data compression functionality to optionally reduce output data volume.
- Address sub-optimal aspects of RD53A, such as higher than desired timing variation of charge injection pulses from column to column.
- Potential functionality enhancements such as real-time self-tuning of pixel threshold [95].

This design work will be carried out by the RD53 collaboration following initial testing of RD53A. Some work can start even sooner, as it arises from new specifications and requires no input from RD53A testing.

6.4 Radiation Tolerance

Radiation effects on 65 nm technology have been extensively studied by the CERN IC group, the RD53 Collaboration, and others. The radiation damage mechanisms and how they impact transistor performance have been understood and predictions validated. (See eg. [96, 70].) This knowledge and the associated data have been used by RD53 to make transistor and logic cell models for irradiated devices.

RD53A was designed to meet specifications after 500 Mrad total dose in HL-LHC conditions. This is because accurate modeling beyond 500 Mrad has not been developed. Oper-

ation should still be possible beyond 500 Mrad, but the amount of degradation will have to be measured, and will depend on operating conditions such as temperature and annealing. There is thus high confidence in operation up to 500 Mrad, while operation after higher dose is uncertain pending detailed tests with RD53A.

Mitigation of Single Event Upsets (SEU) uses a two pronged approach of conventional hardening plus continuous external refreshing known as *trickle configuration*, allowing both schemes to be evaluated.

6.4.1 Total Dose Tolerance and Modeling

Not all effects from charge generation in the dielectrics are equally important. As radiation dose increases, understanding and managing previously negligible effects become necessary. The importance of each effect also depends on transistor geometry and size. In this respect, the 130 nm CMOS technology node represented a "sweet spot" for which commercial logic libraries could be used out-of-the-box up to doses well in excess of the 250 Mrad requirement (double or perhaps triple that dose). In contrast, in the 65 nm node it is necessary to select or customize logic cell designs depending on the desired radiation tolerance, effectively trading off radiation tolerance for logic density. If the expected radiation dose is low, the out-of-the-box commercial logic can be used, while for higher expected doses, lower density logic cells must be substituted.

RD53 digital design relies on accurate modeling of radiation damaged transistors. Conventional (rad soft) digital design already offers several different models for the same transistor: a *typical* model plus so called *corner* models, which simulate operation with different temperatures, voltages, and/or variation of fabrication process parameters within an allowed range. The same transistor will be faster or slower depending on temperature, and so on. The synthesis tools produce circuits to function in all the selected corners. The new design approach is to use additional corner models that represent the radiation damaged transistors. Such models can be custom made by parameterizing measurement data. In this way, logic can be synthesized to work both before and after radiation damage, even though logic gate propagation delays, setup and hold times, etc. can change very significantly: a factor of 2 or more. This is to be compared to changes of just tens of percent between the operating temperature extremes. Such large changes will limit the achievable clock speed, but most pixel read-out applications require clocks of order 100 MHz, rather than the typical GHz speeds of microprocessors in the same technology. Radiation damaged transistor models are also used to simulate analog and mixed signal circuits in order to confirm the design prior to fabrication and radiation testing, which still provides the ultimate validation.

A transistor simulation model has been developed that captures the behavior after 500 Mrad dose based on fits to single transistor data. The model uses worst cases bias conditions, but not high temperature annealing.

Analog circuits have been designed following the guidelines shown in Table 6.5 and then simulated with the 500 Mrad model. In addition, all analog circuits used in RD53A have already been prototyped and radiation tested in silicon to doses above 500 Mrad.

Table 6.5: Gate-dimension recommendations (width and length) for transistors in 65 nm technology to ensure 500 Mrad radiation tolerance.

Device	W	L
NMOS	any	$\geq$ 120 nm
PMOS	$\geq$ 300 nm	$\geq$ 120 nm

A number of digital libraries have been simulated with the 500 Mrad model and a radiation corner model has been developed that is used in synthesis. In addition, sample cells from these libraries have been tested in silicon and the irradiation results were compared to the model predictions. Figure 6.9 shows gate delay results from a digital library test chip compared to transistor level simulations. The measured degradation is less than the models predict because the models are based on worst case bias of single transistors, whereas transistors in logic cells spend only about half of their life under worst case bias. This shows that our damage modeling is conservative for logic circuits, which provides a safety margin for the digital design.

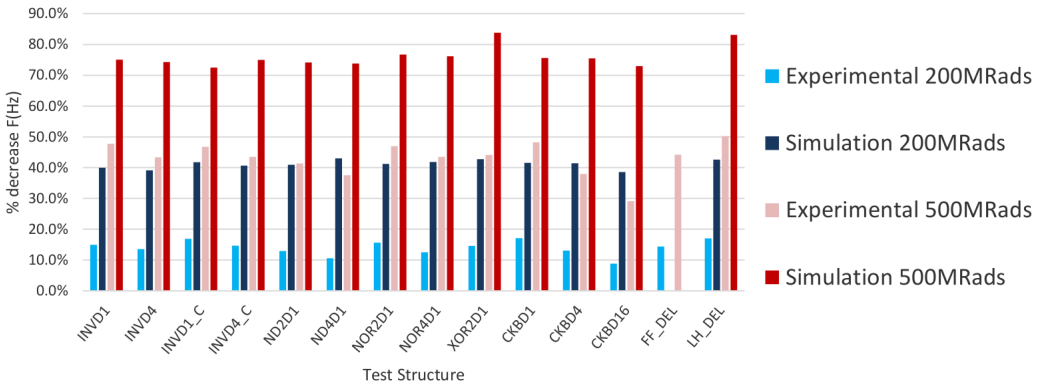


Figure 6.9: Gate delay increase measured in the DRAD digital library test chip compared to transistor level simulation using 200 Mrad and 500 Mrad damage models.

6.4.2 Single Event Upsets

Mitigation of SEU involves protection of memory, control signals and state machines. Memory in the data path is not protected, because the amount of corruption expected during the time that hit data spends in chip memory (of order 20 μs) is much less than the specified 1% hit loss limit. With a single bit upset cross section of 5×10^{-14} cm^2 and an estimated rate of particles above upset threshold of 500 MHz/cm^2, even taking the extreme case that

every single upset corrupts an entire 64-bit Aurora frame, the calculated fraction of lost hits in 20 μs is 3×10^{-8}. Global configuration memory is protected with triple redundant (TR) DICE latches with TR error correction. Pixel configuration can be protected at most with simple DICE latches. However, the DICE latches provide only an order of magnitude smaller upset cross section than standard latches, which leads to a single bit upset rate of 2×10^{-4} Hz. This means that even using DICE latches, 1% of channels would be corrupted after just 100 s, which is not an acceptable loss. (Already in present IBL operation a few percent of pixels are lost due to configuration SEU upsets by the end of each run). The solution for long-term protection of pixel configuration is, therefore, trickle configuration (Section 6.2.1), where the chip is no longer required to hold configuration for more than a fraction of a second at a time. The same method can be applied to global configuration if needed. For IBL operation starting in 2017, the global configuration is being automatically reloaded every few seconds, and this leads to improved data taking efficiency. (This is not trickle configuration because it cannot be performed while triggers are being sent, so in the IBL case it requires a dead time, which is much smaller than the data corruption losses that were experienced before this scheme was introduced). Control paths are protected with triple redundancy of circuits such as counters, and/ or deglitching of controls signals.

6.5 Prototype Test Chips

A number of test chips have been produced and tested by the RD53 collaboration as part of the development leading up to RD53A. Thus, the technical risk on the individual circuit blocks of RD53A was low, and will be even lower in the production chip after RD53A has been fully characterized. The front ends, ShuLDOs, clock multiplier and 1.28 Gbps output serializer, differential I/O pads, DACs and ADCs, current and voltage references, and power on reset have all been prototyped and radiation tested prior to RD53A. Additionally, single transistor and digital library cell test chips have been used to generate and validate the radiation damage models used.

The front end designs and performance have been validated with the FE65-P2 (differential front end) and Chipix (synchronous and linear front ends) test chips. FE65-P2 also validated the substrate isolation approach used in RD53A and the validity of the synthesized logic core approach discussed in Section 6.3.2.

6.5.1 FE65-P2 and Chipix Test Chips

The FE65-P2 and Chipix each contain a matrix of 64 by 64 pixels on 50 μm by 50 μm pitch. They were implemented in 65 nm bulk CMOS and were fabricated in a multi-project run delivered in December 2015, and September 2016, respectively. The goals were to demonstrate excellent analog performance while isolated well enough from digital activity to achieve

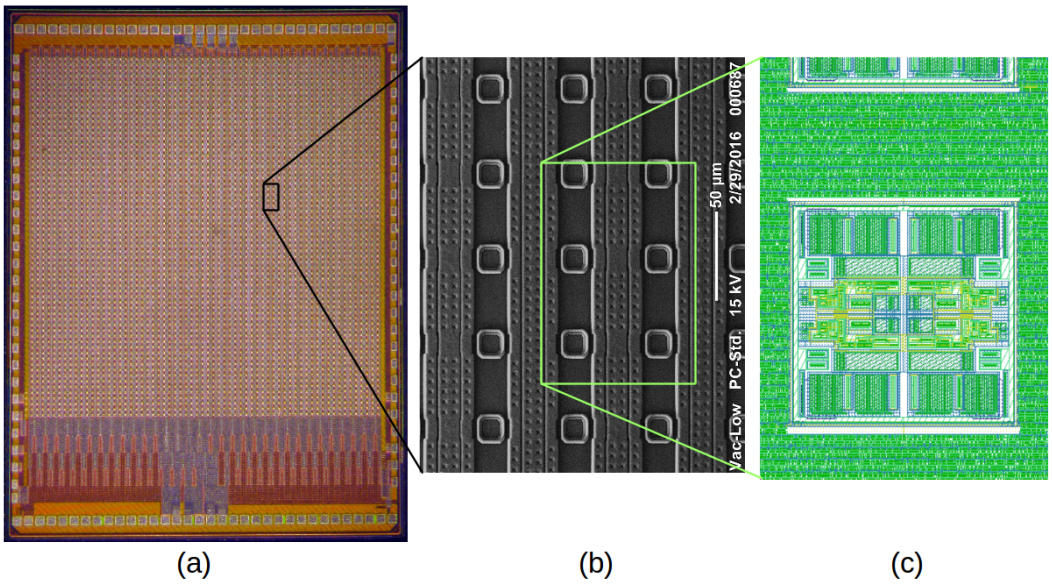


Figure 6.10: (a) Photograph of FE65-P2. (b) SEM micrograph showing detail with several bump pads on 50 μm pitch visible. The column power bus structure can also be seen. (c) Layout detail showing an analog quad island surrounded by synthesized logic.

600 electron stable threshold, radiation hard to at least 500 Mrad, and to prove the "analog islands in a digital sea" layout concept. Figure 6.10 shows a photo, layout detail, and an SEM image of the bump pad structure for the FE65-P2 chip, approximately 3.5 mm by 4.4 mm.

These test chips provided an early vehicle to read out 50 μm by 50 μm or 100 μm by 25 μm pixel sensors ahead of RD53A. Because it was produced earlier, results from bump-bonded modules produced with FE65-P2 are available. Bare chip measurements of FE65-P2 and Chipix are summarized here, while module results are described in Chapters 5 and 8.

Both test chips were primarily exploring analog design questions and not demonstrating high speed digital read-out. Nevertheless, FE65-P2 implemented the region architecture borrowed from FE-I4 while Chipix used a central buffer design. Both read-outs remained operational after irradiation to 500 Mrad at room temperature and without high temperature annealing, which is a good outcome because the digital circuitry in these chips was not synthesized with radiation corner models, as these were being developed in parallel, nor did it undergo the same level of simulation and verification scrutiny demanded for RD53A.

There were many variants of analog front end circuits prototyped in FE65-P2 and Chipix. This large variety was used to make design choices for which simulation tools may not be able to give conclusive answers. Consequently, in RD53A there are 3 different front end

designs, but no variants of those designs, and all three designs share some features like the injection circuit and the bias generation and distribution. This section shows selected results from FE65-P2 and Chipix that are most relevant to the RD53A specifications or illustrate important behaviors. Threshold and noise values are converted to equivalent input charge in electrons (e^-). A note of caution is that there is always an uncertainty of 10% to 20% in this conversion as a precision absolute calibration can only be done with modules and sources giving known energy deposits.

No surprises were observed in noise measurements, which generally matched simulations before irradiation (ranging from 35 e^- for the lowest FE65-P2 variant to 80 e^- for the Chipix synchronous variant at 4 μA analog current) increasing between 10% and 25% after 500 Mrad. This refers to the bare chip noise (no sensor). The simulated noise with 50 fF sensor capacitance and 10 nA leakage current is between 60 and 100 e^- depending on variant.

Minimum stable threshold is a critical figure of merit for pixel read-out chips. While FE65-P2 and Chipix do not probe large chip effects, they include all other aspects and there would be no hope for a large chip if they could not be tuned to low threshold. FE65-P2 was therefore designed with 500 e^- minimum threshold in mind instead of the required 600 e^-. Figure 6.11 shows the average threshold achieved by "noise occupancy tuning" for all the front end variants in FE65-P2 at 4 μA per pixel analog current. In this kind of tuning, each pixel's threshold is reduced until it sees a small rate of noise hits (of order 1 Hz), allowing to mask off a few percent of pixels as hot channels. The best performing variant (lowest threshold) formed the basis for the RD53A differential front end design. Figure 6.12 shows traditionally tuned (scan the DAC settings and choose the ones closest to a target threshold value) threshold distributions for the synchronous front end variant in Chipix at 5 μA per pixel analog current. This design formed the basis for the synchronous front end of RD53A.

An important question is how stable is the threshold tuning during irradiation, since the single run dose at the ITk inner layer will approach 1 Mrad. In present detector operation, the pixel thresholds are re-tuned only every few weeks, but this will not be adequate at the HL-LHC. Figure 6.13 shows the increase of threshold dispersion (RMS of pixel thresholds) in FE65-P2 front end variants as the chip was operated at $-10°$C and exposed to 50 MeV protons at a dose rate about 8 times that expected at the ITk inner layer. In the right side of the plot, the dose rate was reduced to 4 times nominal. This chip was previously unirradiated and the detuning is larger than for previously irradiated chips. For the best (lowest slope) variant, the de-tuning is 80 e^-/Mrad in Figure 6.13, while for 150 Mrad and 350 Mrad irradiated chips the slope was 10 e^-/Mrad and 20 e^-/Mrad, respectively.

In-time threshold and timing dispersion are critical parameters for chip operation. Thanks to the low input capacitance of smaller pixels, front ends have higher gain and faster rise times than for existing detectors. This translates into significantly smaller time walk than specified. Figure 6.14 shows an analog measurement of comparator firing delay vs. injected

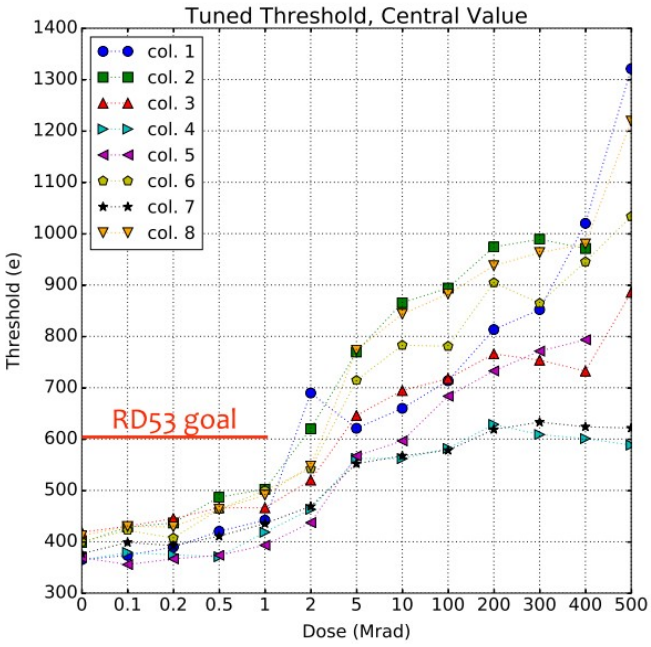


Figure 6.11: FE65-P2 tuned minimum stable threshold vs. dose from x-ray irradiation at room temperature. Taken from [97].

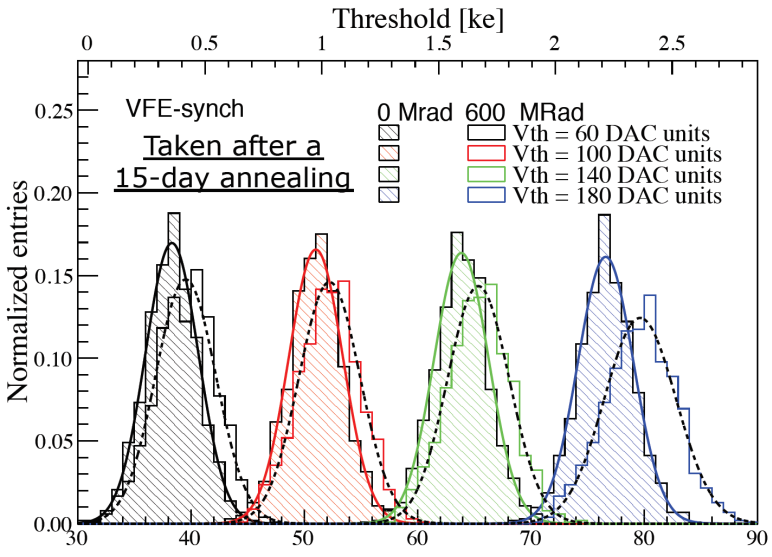


Figure 6.12: Chipix synchronous front end tuned threshold distributions before and after irradiation with low energy protons. The indicated annealing time is at room temperature. Taken from [98].

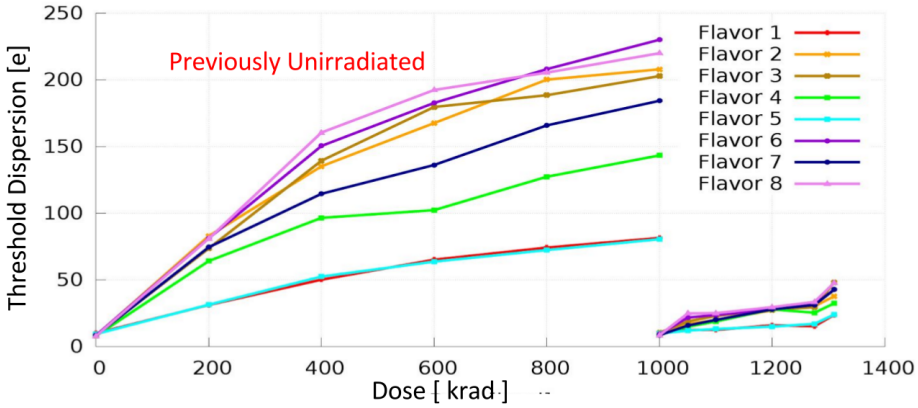


Figure 6.13: FE65-P2 added threshold dispersion due to radiation dose for an initially unirradiated chip. The initial dispersion of 40 e^- has been subtracted in quadrature. At 1 Mrad the chip was re-tuned and dose rate decreased. At 1.3 Mrad the temperature increased to 20°C. Taken from [99].

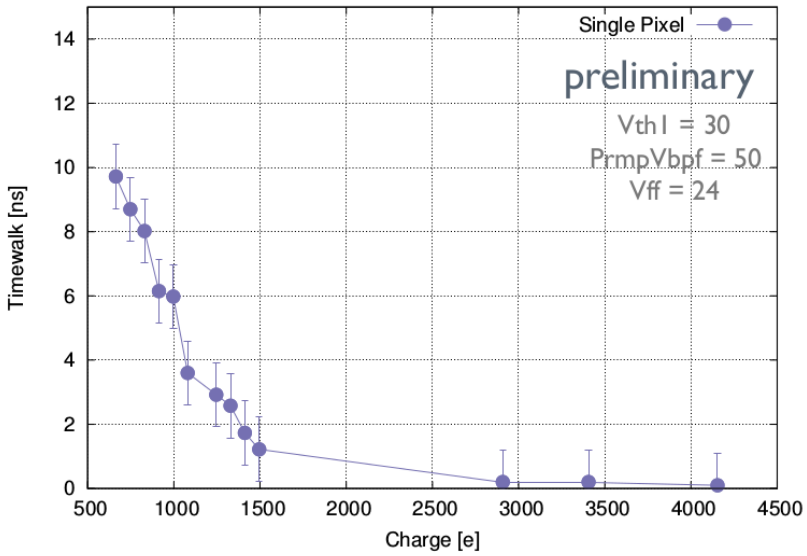


Figure 6.14: Time walk measurement for a typical pixel in FE65-P2, without sensor capacitance.

charge for a typical pixel in FE65-P2. Even for an injected charge value of 100 e^- greater than the set threshold of 500 e^-, the time walk delay is only 10 ns. Sensor capacitance will slow down the front end, but simulation shows in-time threshold of 300 e^- above threshold for 50 fF sensor capacitance, to be compared with the specification of $< 600\,e^-$.

Figure 6.15 shows the timing dispersion in FE65-P2, which is the RMS variation in the time that comparators fire across the matrix for a fixed time input pulse. This is shown as a function of the comparator bias current, which is adjustable, but must be kept low to fit into the 4 μA per pixel analog current budget.

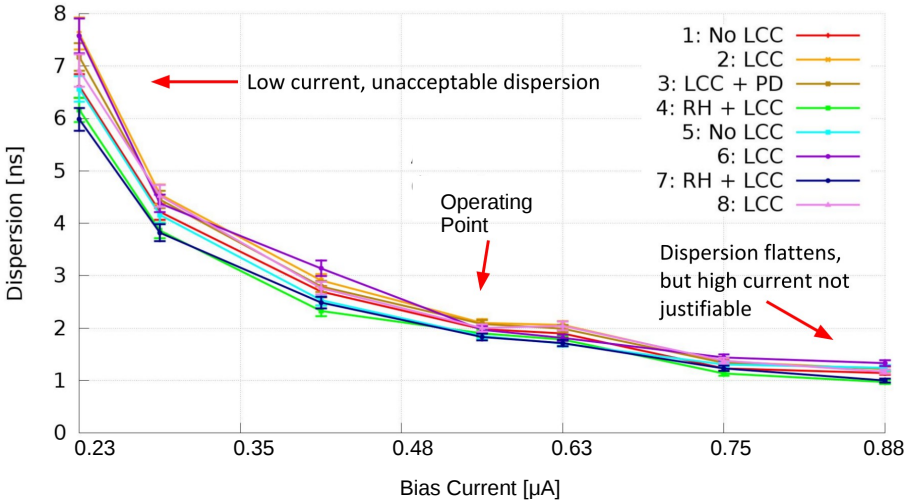


Figure 6.15: FE65-P2 timing dispersion vs. comparator bias current.

6.5.2 RD53A Chip

A note added in March 2018. The design for the RD53A was submitted at the start of September 17 and returned in November of the same year. In December a limited number of wafers were sent to IZM for dicing and the fist chips were wire-bonded and rudimentary tests were started in the institutes. The first results of basic functionality have been very encouraging and a campaign of irradiations is expected to start soon. A complete set of characterisations will be delivered by the middle of 2018.

7 Pixel module Hybridization

7.1 Introduction

The hybridization of the sensor and front-end chips to make the bare ITk pixel module is a time consuming post-processing procedure and represents the most expensive portion of the pixel module construction. Fine pitch (50 μm pitch) bump deposition and flip-chip technologies have been chosen as the method to electrically and mechanically bond the sensor to the front-end chip. The hybridization process can be split into four main stages, which are:

1. Deposition of solder or indium bumps on the front-end chip wafer, known as bump deposition.
2. Sensor wafer processing, which includes the deposition of a solderable metal layer on the sensor pixel pads, known as the under-bump metallization (UBM), and for some technologies bump deposition.
3. Wafer thinning and dicing.
4. Face-to-face joining of the parts, known as flip-chip bonding.

The hybridization process may be performed at a single vendor or a combination of vendors specializing in a given process.

Wafer-level bump deposition has been chosen due to its high yield and low per bump cost. Two classes of bump material are considered: solder based bumps (PbSn or SnAg) and indium bumps, both of which were used in the present ATLAS Pixel modules [4]. The choice of the bump material determines the details of the process which are described in Section 7.2 for the different technologies. The option of applying a high voltage insulation layer during the bump deposition process to prevent sparking between the sensor and the front-end chip is also covered in this section.

The flip-chip process is the process by which the front-end chip is joined face-to-face with the sensor chip. The process requires precise alignment of the two parts followed by the application of pressure and heat to form an electrical and mechanical bond. A fluxless bonding process is used and to improve the bond performance the parts undergo a deoxidation stage before flip-clip bonding. Details of the flip-chip process applied to the bump technologies are given in Section 7.2.

The technological challenge is more demanding than for the original ATLAS Pixel and IBL modules. The requirement to produce very thin pixel assemblies targeting a front-end chip thickness of 150 μm and a sensor thickness of 100 to 150 μm (see Chapter 5), is similar to the IBL module but more stringent than for the ATLAS Pixel module (190 μm and 250 μm thick front-end chip and sensor respectively). The required bump density represents a five-fold increase over the IBL FE-I4 chip due to the pixel pitch of 50 μm in both directions. The ATLAS ITk Pixel chip will also be larger with 400 columns and 384 rows giving a total of 153 600 bump-bonds per chip, compared to 26 880 bonds for an FE-I4 chip. An additional requirement on the process is introduced due to the increased front-end chip wafer size from 200 mm to 300 mm in diameter.

These additional requirements will impact both the bump formation and the flip-chip bonding. The full hybridization specification is described in Section 7.3. The specifications do not place a detailed requirement on the technology to be used, but will assess the quality of the product via a qualification process. The ITk Quality Control and Quality Assurance approach is described in Section 19.1: the planned procedures during production are covered in Section 7.4. The qualification process is based on that used for the IBL.

The second significant challenge is the production rate and volume required for the substantially enlarged pixel system with 10276 modules with a total surface area of approximately 14 m^2 compared to the original ATLAS pixel sub-detector of 1.73 m^2. To gain confidence in the ability to meet the production challenge, as well as the technical one, the ATLAS ITk pixel community is actively working with suppliers of the hybridization technology which are listed in Section 7.5. The vendor may supply the full hybridization process or a sub-section of it and the production model is deliberately left open to allow production flexibility to gain price and schedule advantage. The choice of the vendors for production will be performed via a two-part process consisting of a market survey, to pre-select a number of competent vendors, followed by a tender exercise. The present development status for each vendor is summarized in Section 7.6.

To progress towards processing the RD53A and ATLAS ITk Pixel chips a 300 mm diameter bump-bond test wafer is being produced. This test wafer will enable the vendors to demonstrate their process with the final wafer diameter, bump density and die size. While they will not behave the same mechanically as the final chip they will nevertheless allow the wafer thinning to 150 μm, bump deposition and flip-chip bonding to be demonstrated. Details of the test wafer and hybridization results are given in Section 7.7.

The final section (Section 7.8) details future hybridization development plans and progress towards the ATLAS ITk Pixel chip and pre-production.

7.2 Bare module assembly process

7.2.1 Front-end chip and sensor wafers

The front-end chips are produced on 300 mm diameter wafers. The wafers will be supplied to the bump deposition vendor at full thickness (approximately 750 μm) after probing to determine the known good dies. The wafers will be thinned to 150 μm during the hybridization process to reduce dead material in the pixel sub-detector.

Compared to the FE-I4 chip, the new chip will not impose an additional constraint for bump formation due to the passivation thickness and per pixel passivation opening for bump growth. The pixel pitch is uniform at 50 μm in both directions over the matrix with a matching bump pitch. For the FE-I4 chip the minimum bump pitch is the same but arranged in columns of two bumps with a 450 μm spacing between them. The bump size demonstrated in the present ATLAS Pixel and IBL systems is therefore applicable to the new ATLAS ITk Pixel chip with some fabrication details optimised to realise bumps at the increased overall density. The flip-chip process needs to be studied in detail due to the increased total number of bonds and reduced die thickness.

The sensors will typically arrive at the hybridization vendor as probed wafers with known good dies. To be used with solder bumps, the sensor requires post-processing to realise UBM, but the option is open to process the UBM at the sensor vendor and ship diced sensors directly to the flip-chip vendor. The planar sensors will be fabricated on 150 or 200 mm diameter wafers. The baseline active thickness of the planar sensors is between 100 and 150 μm, with an option to employ thicker sensors up to 300 μm in the outermost layers. Different fabrication technologies are employed some of which use a support wafer that is thinned after UBM deposition and before flip-chip at the hybridization vendor. The 3D sensor wafers will be either 100 or 150 mm in diameter, with an active thickness of 150 μm and a physical thickness as high as 250 μm. Processing UBM on thin sensor wafers and post-processing thinning has been demonstrated during the development phase.

7.2.2 Assembly process outline

The hybridization process is outlined by the following stages, broken down into the four main activities, with technology dependent variations noted:

Front-end chip bump deposition

- Vendor reception of wafers, including visual inspection and cleaning.
- Depending on technology, wafer level deposition of an additional passivation layer (Benzocyclobutene, BCB, or similar). The BCB may also provide high voltage discharge protection, see Section 7.2.6.

- Under-bump metallization deposition.
- Bump formation on the wafers. For solder bumps, the bumps are electroplated, while for indium, the bumps are evaporated.
- Vendor QC.

Sensor processing

- Vendor reception of wafers, including visual inspection and cleaning.
- Depending on the final technical solution deposition of an additional BCB passivation layer for high voltage discharge protection.
- Solder bumps: Under-bump metallization deposition.
- Indium bumps: Under-bump metallization and bump deposition.
- Vendor QC.

Wafer thinning and dicing
Front-end chip wafer thinning may be performed before or after bump formation depending on the technology.

- Front-end chip wafer thinning to 150 μm.
- Front-end chip wafer backside stress relief process, for example chemical-mechanical polishing (CMP)
- Depending on the interconnection process, a glass substrate wafer is bonded to the back of the front-end chip wafer to allow flip-chip processing.
- Depending on the interconnection process, a stress compensation layer is deposited on the back of the front-end chip wafer to allow flip-chip processing.
- Sensor wafer thinning to remove the support wafer if required.
- Dicing of the front-end chip and sensor wafers.
- Die sort. Only known good dies are used for flip-chip.
- Vendor QC.

Flip-chip bonding

- Deoxidation of the bumps to improve the bond performance.
- Flip-chip assembly of a module by connecting 1 to 4 front-end die to a silicon sensor using flip-chip technology. In a multi-chip assembly the front-end chips are placed at an edge-to-edge distance of 150 μm.
- For solder bumps, after the flip-chip process there may be an optional solder reduction to remove oxides and reflow of the flip-chip bonded device to decrease electrical resistance and perform die self-alignment.
- Depending on the interconnection technology, removal of the temporary support wafer after flip chip takes place.
- Quality control of every module at the vendor and finally at the ATLAS ITk institutes.

7.2.3 Bump growth and flip-chip bonding

For solder bumps the front-end wafer is processed with a uniform seed layer via sputtering to form an electroplating base. The wafer is masked using photo-lithographic techniques to create a via pattern, aligned to the pixels, for bump growth with electroplating [100]. Depending on the vendor, the bumps are either a copper pillar with a eutectic SnAg solder cap [100, 101] or a pure eutectic SnAg solder bump [100, 102]. The resist is stripped and the un-plated seed layer etched to realise isolated bumps. Finally, the solder is melted into spheres by a reflow step. Flip-chip bonding is performed with thermo-compression at the solder reflow temperature of approximately 250°C. After flip-chip bonding the solder is typically reflowed at approximately 250°C in a reducing atmosphere to improve the electrical conductivity of the bond. The distance between a chip and the sensor is about 20 μm, a value which is safe in terms of cross-talk and the bump connection resistance is smaller than 1 Ω.

Indium bumps are grown by evaporating indium on both mating parts though a pattern photo-resist [103, 104]. The UBM process is very simple, consisting of about 10 nm of chromium deposited just before indium evaporation in the same vacuum cycle. The resist is removed with a lift-off process to realise isolated bumps, which limits the bump height to 10 μm. Flip-chip bonding is performed with thermo-compression at 90 °C with a force of 6 mN per bump. As no reflow process is included no self-alignment takes place. With these parameters, the bump electrical resistance is 10 Ω for FE-I4 test devices, compatible with that obtained for the ATLAS pixel production [105] and the chip to sensor separation is approximately 10 μm. For further details on bump formation for hybrid pixel modules see [106].

7.2.4 Sensor UBM

The sensor UBM recipe is important for the flip-chip yield. The ability of the bump to adhere to the UBM is a critical requirement as it gives the bump joint its shear strength.

For the solder bump process the sensor UBM is often complex and costly and is typically applied at the bump vendor. A significant cost reduction for the UBM process, (up to 90%, based on information price estimates from the sensor vendors), is expected if the UBM is deposited as the final step in the sensor fabrication process. A number of sensor vendors are developing UBM processes which have been successfully flip-chip bonded to FE-I4 front-end chips.

For the indium deposition, the UBM is a simple layer of chromium deposited just before the indium bump in a single process step and will therefore always be deposited at the bump vendor. While the UBM is simple, the requirement to deposit indium on the sensor wafer as well as on the front-end chip wafer increases the process steps and is thus more complex.

7.2.5 Front-end chip bow

The top side of the front-end chip has metal and dielectric layers, for example the FE-I4 chip has 8 metal layers with a total back-end-of-line (BEOL) metal/dielectric stack thickness of 16 μm. The ATLAS ITk Pixel chip will have a similar BEOL stack. Additionally, large discontinuous metal bumps are distributed over the die surface at the pixel pitch.

The difference in the coefficient of thermal expansion (CTE) between the silicon substrate and the BEOL materials causes stress in the chip, resulting in chip bow which increases with reducing substrate thickness. At room temperature a 100 μm thick FE-I4 die is concave, with the BEOL layers in compression, and is bowed by about +50 μm measured on the chip backside from centre to corner. As the temperature increases the sign of the bow changes and the layers go into tension to bow by -175 μm at 250°C, corresponding to the solder reflow temperature [102, 107]. Such large bows are not tolerable for the standard flip-chip process and results in disconnected bumps. A die bow of 15 μm is considered maximum for high bump bond yield in the standard hybridization process with reflow.

Various techniques have been developed by industry to overcome this issue, including; the use of a temporary support wafer bonded to the backside of the chip wafer to hold the chip flat during flip-chip bonding, or the use of solder reduction in the flip-chip bonder to allow reflow of the solder while the device is held flat using the vacuum tools of the bonder. In the absence of a large area pixel chip from TSMC, thin chip hybridization techniques using FE-I4 wafers have been demonstrated at different vendors and are described in Section 7.6.

7.2.6 High Voltage protection

The change from the n-in-n to the n-in-p technology for planar sensors implies that the guard ring structures are on the pixellated face of the sensor. This leads to a significant portion of the sensor bias present at the perimeter of the pixellated surface of the sensor, which faces the front-end chips with a separation of between 5 μm and 25 μm. The front-end chip's surface potential is at local ground. A sensor bias voltage of up to 800 V will be used and therefore high voltage insulation is required in the overlap area of the sensor perimeter and the front-end chip. One method to achieve the required isolation is the application of a 3 μm layer of BCB on the sensor or front-end chip as an additional passivation material on the wafer. To reduce cost the preferred method is to apply the BCB on the front-end wafer, rather than sensor wafer, before bump deposition in the areas that overlap the edge of the sensor. The BCB passivation is a standard part of the bump formation process for some vendors but is also available at most of the other vendors. The application of BCB on the sensor has been demonstrated and shown to allow over 800 V to be applied to the pixel assembly [77, 108]. Visual inspection to identify defects and optical measurement of the coating thickness will be used to control the coating quality. An alternative HV protection methods has been demonstrated with the use of a 3 μm layer of Parylene coating applied after the module is assembled, including wire bonding [108]. Again, operation of modules without HV discharge issues has been demonstrated for a sensor biased of 1000 V. Modules have been made with both methods (in quantities of a few tens for each method) and irradiated and thermally cycled to demonstrated compliance to the required environment. During production, test items will be made using both methods and tested to 1000 V.

7.3 Hybridization specifications

The hybridization specifications define the various process stages required to obtain a hybrid pixel module and are based on the ATLAS and IBL specifications. The specifications will be kept under review until the end of pre-production. During this period, the module yield will be better understood and the effect of higher pixel defect rates, especially at higher radius, will be studied. The final module bad pixel count is a function of the electrically dead pixels, missing or merged bumps as deposited on the wafer and additional merged or disconnected bumps from the flip-chip process. The final specification on the maximum number of bond failures for a given chip is 600 with the maximum size of continuous group of failed bonds equal to 30. This is a bump failure rate of 4×10^{-3} bumps per chip. This is the same failure rate for the IBL and is designed to keep the final dead pixel rate below 1%. To reduce the risk of merged bumps the maximum bump size after the flip-chip process must not exceed 45 μm, while to minimize cross-talk between the electronics and the sensor the minimum bump height, after the flip-chip process, is 5 μm. To guarantee the long-term connectivity of the sensor and front-end chip the tensile and shear

strengths of the bumps must be greater than 0.1 g/bump, which is 15.4 kg for an ATLAS ITk Pixel front-end chip.

In addition to the requirement on the number of good pixels, the hybrid pixel module must also maintain the electrical characteristics of the sensor. After flip-chip, the sensor leakage current must not increase by more than a factor of 2 from that measured at sensor reception. The absolute sensor leakage current, measured at 20°C, must be, for planar sensors less than 1.5 μA/cm^2, (measured at $V_{\text{depl}} + 50$ V), and for 3D sensors less than 5.0 μA/cm^2, (measured at $V_{\text{depl}} + 20$ V). The breakdown voltage must also remain high and must not change by more than 10 V and 5 V for planar and 3D sensors respectively, compared to that measured during the reception tests. The absolute breakdown voltage must be, for planar sensors greater than $V_{\text{depl}} + 80$ V, and for 3D sensors greater than $V_{\text{depl}} + 40$ V.

In addition, the size of the flip-chip assembly will be specified for the different module designs.

7.4 Planned quality control and quality assurance during production

To maintain production quality there are many quality control (QC) and quality assurance (QA) tests performed at the hybridization vendors and at the institutes on bare modules. The tests are performed at each vendor in the production chain and at each process stage to ensure the above specifications are met and to identify any issues as soon as possible to enable the vendors to rapidly react to them and maintain quality.

7.4.1 At the vendors

For bump deposition, the incoming wafers undergo initial visual inspection and post-clean visual inspection to guarantee the quality of the incoming parts. These are followed by photoresist adhesion and lithography quality inspections at a stage where resist stripping is still possible to avoid subsequent metal deposition issues. After the solder or indium deposition the wafer's surface profile is measured to confirm the deposition parameters. After seed layer removal or indium lift-off, visual inspection confirms isolated bumps. Inspection of bump quality follows where automated wafer level inspection of the diameter and height of the bumps takes place, missing bumps and shorted bumps are recorded. Similar quality control tests will exist for the sensor processing. The vendor controls will be reviewed during the pre-production and production phase to maintain the quality of the product.

For the wafer thinning and dicing processes the wafers are inspected before dicing to confirm thickness tolerances and wafer backside surface finish. After dicing, single chip inspection takes place to confirm dicing quality. Electrical probing of the FE chips at this stage of production is possible but not foreseen.

Flip-chip bonding follows, after which the assembly undergoes visual inspection and X-ray inspection to identify merged bumps, missing bumps and misplaced chips. The X-ray inspection may take place at the flip-chip vendor or at a second party and is optional if bump yield is demonstrably high during the R&D phase. Electrically open bumps cannot be determined without an electrical functionality test which takes place at the institutes. The assemblies are measured to confirm they are within geometric specification. The shear and tensile testing of an assembly to confirm the bond strength is a destructive test measured with dedicated test stands on full single chip assemblies and on special test structures for single bumps and will be performed at least once per bump deposition batch. A shear test of an FE-I4 pixel assembly with a 150 μm thick sensor and a 150 μm thick front-end chip has been demonstrated with a shear strength for the whole assembly in excess of 80 kg, equal to 3.0 g per bump before the silicon die broke.

7.4.2 At the ITk institutes

After delivery of the bare modules to the ATLAS ITk institutes acceptance tests will be performed to confirm the hybridization specifications have been met. All tests will be performed with standardized test equipment and procedures. The test results will be stored centrally in the production database. The acceptance test are:

- Visual inspection and metrology of the assemblies.
  - Confirm the dimensions of the bare module are within tolerance.
  - Confirm that no gross mechanical defects are present.
- Sensor current-voltage measurement, measured on the bare module with a probe-station at a temperature close to 20°C.
  - Confirm that the change in leakage current of the sensor is within specification.
  - Confirm that the change in the breakdown voltage of the sensor is within specification.
- Verification of front-end chip electrical functionality using the pixel module DAQ system and probe-station.
  - Simple functional chip scans to show each chip is functioning.
  - More detailed chip tests to confirm functionality is within specification.

- Determination of the bump bonding connectivity using the pixel module DAQ system and a probe-station.
  - Chip scans to determine the position and number of non-connected bumps.
  - Chip scans to determine the position and number of merged bumps.

The two final front-end chip based acceptance tests can either be performed with a bare module on a probe station or after the addition of the module flex and wire bonding. Using a probe station to test each chip one at a time is slow and adds risk to the module, but has the advantage that it allows for the replacement of front-end chips on the module at the flip-chip vendor and is therefore an acceptance test. Chip rework was demonstrated on the FE-I3 chip set during the ATLAS Pixel production [109, 110], but to date has not been demonstrated with the thin larger FE-I4 ATLAS Pixel chip. Chip re-work will be investigated for the ITk over the next year with the RD53A chip set. Testing of a module with the module flex attached removes the possibility of chip re-work at the vendor and implies that the yield will be accepted by the ITk. For the original pixel production 10.5% of the 16-chip pixel modules with PbSn bumps required a chip to be reworked. As there are maximally four front-end chips in an ATLAS ITk Pixel module and if a failure rate twice the original build is assumed, due to the increased technical demand imposed by the new chip, the bare module failure rate due to bad bonding would be approximately 5%. It is reasonable to produce modules without flip-chip rework with this level of failure. The probing of bare modules is being performed during the R&D phase and its utility for production will be assessed before pre-production commences when the flip-chip yields are better understood. If bare module probing is not part of the final production model then rapid turn-around of the module dressing and initial testing is required to catch hybridization issues as early as possible.

More in-depth testing of the complete module will be performed, described in Chapter 8, which includes thermal cycles performed on each module and thermal shock tests performed on a sample of devices.

7.5 Vendor engagement

The ITk Pixel system described in this document will have 10 276 installed pixel assemblies mainly consisting of 4-chip modules, which requires about 15 000 bare modules to be built with the present assumptions on yield in the module build, (estimated at 77% based on previous ATLAS & IBL module builds), and in all the other procedures to up system integration (estimated at 90% based on past experience). Compared to the present ATLAS Pixel system this is an increase of over five times the number of installed modules but only approximately 1.25 times the number of front-end chips and flip-chip bonds. The volumes and timescales are discussed in Chapter 19.

The front-end chips will be produced on 300 mm diameter wafers, this reduces the number of wafers to be processed by the bump deposition facility by approximately 2.5 times compared with using 200 mm wafers, however, there are a reduced number of 300 mm wafers processing facilities. To overcome lack of vendor capability the wafer can be cored to 200 mm for bump deposition with an associated increase in cost per unit area. Therefore, bump deposition vendors with wafer capability of 200 mm diameter will be considered for the production as long as the overall module price is competitive, and as such the ITk community is actively working with these vendors during the development phase.

The ATLAS ITk community is actively working with six suppliers for bump deposition who also typically supply the flip-chip process, described in Table 7.1. As flip-chip is recognised as a potential bottleneck in the production, the ITk community is working with several additional suppliers of flip-chip to guarantee supply; these include both commercial suppliers and laboratories that are part of the ITk Pixel project that possess fully automated flip-chip machines, described in Table 7.2. The tables list bump technology and proven experience with the FE-I4 chip-set of the different vendors.[1] The large number of suppliers during the development phase have been chosen to solve the challenges imposed for volume production of thin chip assemblies as well as allowing a meaningful choice of supplier at tender. Additional third parties maybe subcontracted to supply wafer thinning and dicing services.

Table 7.1: Vendors of bump deposition and flip-chip presently actively working with ITk Pixel institutes.

Vendor	**Technology**	**FE-I4 thickness demonstrated**	**Wafer diameter (mm)**
IZM	SnAg solder	90 μm	300
HPK	SnAg solder	150 μm	200
CEA LETI	SnAg solder on copper pillar	100 μm	300
Micross	SnAg solder	250 μm	200
Leonardo	In thermal compression	100 μm	300
RAL	In RT compression	750 μm	200

[1] Leonardo was formally known as Selex Sistemi Integrati, Rome, and Micross Advanced Interconnect Technology was formally known as RTI. Advacam is the commercial company formed from the flip-chip activities of VTT, Finland. Advacam has presently been investigated by ITk Pixel institutes for sensor UBM, dicing and flip-chip bonding but has the capability to perform the full hybridization process with 200 mm front-end chip wafers.

Table 7.2: Flip-chip only vendors presently actively working with ITk Pixel institutes.

Vendor	**Technology**	**FE-I4 thickness Demonstrated**
Advacam	SnAg solder	200 μm
IFAE	SnAg solder	400 μm
MIET	Indium SnAg Solder	640 μm thick daisy chains

7.6 Test results of thin FE-I4 prototype modules

Four different hybridization processes with the FE-I4 chip have been investigated, including both solder and indium bumps, to enable thin chip flip-chip and are described below.

IZM has developed a thin-chip hybridization process that was successfully used for the IBL module production [102]. First the front-end chip wafer is thinned and polished for stress relief. The wafer is bonded to a carrier substrate for further processing using a polyimide high temperature bonding technology that performs beyond 250°C. The substrate is an UV transparent glass to enable laser induced de-bonding at the end of the process. The front-side solder bumps are deposited in the traditional fashion. To reinforce the read-out chip also during flip chip assembly and the solder bump reflow the read-out chip wafer is diced into individual die with the carrier wafer still attached. The support wafer is able to hold the die flat throughout the solder reflow process, with a 150 μm FE-I4 die bonded to the support wafer bowing only by 1.5 μm at 250°C. The technique has been demonstrated with chip thicknesses as thin as 90 μm as reported in [102] and sketched in Figure 7.1. With this technology IZM produced all the modules for the IBL (423 2-chip planar and 286 single chip 3D) using FE-I4 chips thinned to 150 μm [2]. The IBL had a module requirement of less than 1% failed pixels per front-end chip, including bump bond failures. Excluding the initial batches which suffered a very high defect rate [111], the bump defect rate was dominated by mis-handling during the laser de-bonding which resulted in large numbers of bond failures in a given module. On average the module failure rate was less than 10% for planar and CNM modules, and 25% for FBK modules, where the difference in the yield is due to statistical fluctuations rather than on sensor type. Of the modules that fulfilled the specification, the mean number of failing pixels was 0.33% for the planar sensor modules with a comparable fraction for modules built with 3D sensors [112]. Significant process optimisation has taken place since the IBL build and a higher module yield is expected. To date, during the ITk R&D phase 30 quad assemblies with 150 μm thick FE-I4 chips bonded to 150 μm thick sensors have been produced with the same technology and all show acceptable performance. Exact bump yield data is presently being measured.

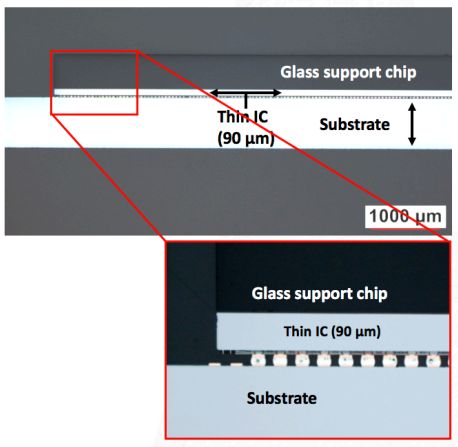


Figure 7.1: The cross-section of a 90 μm thick FE-I4 die with carrier substrate connected to a sensor, with a zoom of the edge pixels. Perfect interconnection is demonstrated.

Two other solder based processes have been developed for the ATLAS ITk module production with the aim to produce solder based flip-chip assemblies without the use of a carrier wafer to increase throughput and reduce price.

The method developed at HPK is based on flux-less SnAg bump bonding [113]. The process is based on the use of a hydrogen plasma to reduce the solder bumps just before bonding. The front-end chip is held flat during reflow on the flip-chip machine to prevent bow and allowed to cool before removing from the machine. HPK have successfully produced over 30 quad assemblies with 150 μm thick FE-I4 chips bonded to 150 μm thick planar sensors which demonstrate high bond yield. A response map of a quad-sensor based module to a uniform ^{90}Sr β ray illumination is shown in Figure 7.2(a), which shows a lack of any low count regions illustrating the high bond yield. These have been subjected to thermal cycling reliability tests from -40°C to +85°C and 70 MeV proton irradiation (CYRIC at Tohoku University, Japan), to a fluence of 3×10^{15} n_{eq}/cm^2 at -15°C without any observed change in the bump quality. The process has been demonstrated with the FE-I4 chip set with bumps deposited by HPK, CEA LETI and IZM and can be considered agnostic to solder bump vendor.

The method developed by CEA LETI [107] uses a dielectric and aluminium layer deposited on the backside of the read-out chip wafer, known as the stress compensation layer (SCL) to balance the bow induced from the front-side BEOL stack. This layer is not removed after flip-chip. The bumps are fabricated on the frontside of the wafer, followed by the bonding of the frontside of the wafer to a temporary support wafer, which is removed before dicing. The backside is thinned and polished for stress relief, followed by the SCL deposition. The die bow has been shown to be significantly reduced due to the SCL: for a 100 μm thick die, the bow reduced from -275 μm to about +30 μm at 260°C. The die bow is very sensitive to the SCL recipe and it has not been possible to eliminate it completely. A limited number

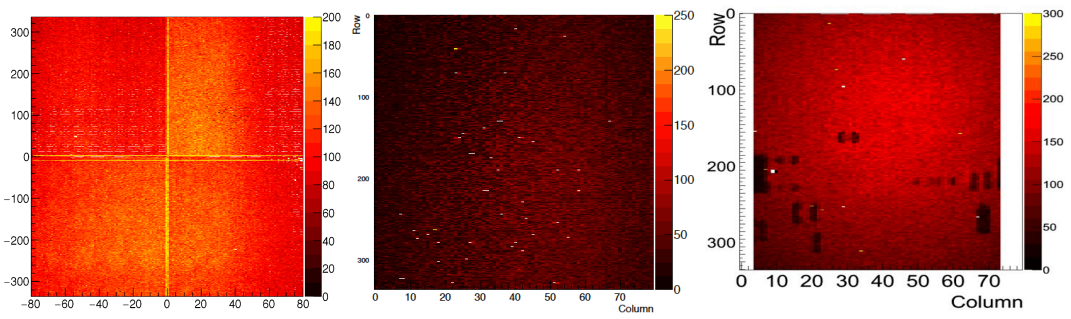
of FE-I4 assemblies fabricated with a solder reduction step just before flip-chip have been made with very few open bumps. A response map of a single chip module to a uniform ^{241}Am γ-ray illumination is shown in Figure 7.2(b), which shows a lack of any low count regions illustrating the high bump-bond yield. The module consists of a 100 μm thick FE-I4 chip with a backside SCL processed at CEA LETI and a 200 μm thick planar sensor and flip-chipped by Advacam. The assemblies have been shown to be robust to thermal cycles from +60°C to -40°C.

A low temperature flip-chip process using indium bumps has been developed at Leonardo for thin chip processing. Leonardo has successful demonstrated flip-chip bonding with indium bumps on 100 μm thick FE-I4 die bonded to both 200 μm thick 3D and planar sensors [105]. The Leonardo process starts with indium bump deposition, followed by frontside polyimide layer deposition to protect the bumps and backside wafer thinning. After which the front-side protection is removed and the wafer is diced before flip-chip. The standard Leonardo bump deposition process was modified to include a post-thinning wafer backside stress relief process. Furthermore, a modification was applied to the flip-chip bonding process. Wafer bow is overcome by holding the die flat on the vacuum tool of the flip-chip machine while the bond is performed at 90°C. The die is released only after the chip has cooled to below 50°C, the temperature at which the bow of the die is negligible. This process has been shown to work well. An example of a high yield bump-bonded thin-chip FE-I4 based single chip module is shown in Figure 7.2(c). The module is made with 100 μm thick FE-I4 read-out chips connected to a 200 μm thick planar sensor with a flexible PCB glued to the sensor backside to attach the FE-I4 chip to the DAQ system. The response to a uniform ^{241}Am γ-ray illumination is shown. The module shows a lack of any low count regions, which illustrates the high bump-bond yield. The dark areas are due to signal attenuation by the surface mount components on the flexible PCB mounted on the sensor.

To mitigate the low flip-chip through-put of the indium process, flip-chip bonding using bumps deposited by Leonardo is being investigated at two ATLAS institutes, namely; National Research University of Electronic Technology (MIET) Moscow, Zelenograd, and the Rutherford Appleton Laboratories (RAL), Oxfordshire.

Indium based hybridization has also been demonstrated at RAL with FE-I4 wafers with full thickness wafers [114]. RAL have deposited the indium on both the front-end and sensor wafer in house with many of the other process stages outsourced. The in-house flip-chip takes place at a temperature of only 30°C. Single chip modules have been fabricated with very few bump defects. Due to bump deposition being limited to 200 mm diameter wafers, future work at RAL will concentrate on the flip-chip bonding of devices with indium bumps provided by Leonardo.

The ability to bond thin FE-I4 chips to make pixel modules has been demonstrated at several vendors, with the number of assemblies made varying between the vendors. To give some evidence of a robust bump deposition process and fast flip-chip production several



(a) (b) (c)

Figure 7.2: Hit map of FE-I4 based modules. (a) A HPK quad-sensor module, consisting of 150 μm thick FE-I4 chips and a 150 μm thick quad planar sensor exposed to ^{90}Sr β rays [113]. (b) A CEA LETI/Advacam single chip sensor module, consisting of a 100 μm thick FE-I4 chip and a 200 μm thick planar sensor exposed to ^{241}Am γ-rays [107]. (c) A Leonardo single-chip sensor module, consisting of a 100 μm thick FE-I4 chip and a 200 μm thick planar sensor exposed to ^{241}Am γ rays [105].

hybridization batches have been processed. The batch size for bump deposition, wafer thinning and dicing consisted of order 10 FE-I4 wafers, with the FE-I4 wafers thinned to a final thickness of 400 μm. The results show a good bump deposition yield and give a degree of assurance that the dump deposition process is well controlled. However, to date the vendors have not demonstrated the full hybridization process with the final pixel chip with the high through-put required for the build process and moreover significant volumes of wafers will not be processed until the pre-production phase of the project due to the limited number of wafers and cost.

7.7 Test results of ATLAS daisy chain prototype modules

Three sets of daisy chain test structures have been produced within the ITk community to demonstrate the hybridization process on devices closer to the proposed ATLAS ITk Pixel chip before the real chip is available. The test structures, fabricated on oxidised silicon wafers, consist of a single aluminium layer of bump-bond pads arrange in a matrix with a pitch of 50 μm $\times$ 50 μm. In each row the pads are connected together in pairs by an aluminium trace with a 50 μm gap between connected pairs. The aluminium traces are passivated with an opening above the bond pad representative of the RD53 chip design. Exposed probe pads at the end of each row allow electrical connectivity to the structure. Two designs are fabricated with the connectivity path displaced by one row such that when they are flip-chip bonded a continuous conductive path exists along a row, as illustrated in Figure 7.3. The test wafers are processed with bumps and UBM, thinned, diced and flip-chip bonded at a number of the hybridization vendors mentioned above. The probe pads allow connectivity testing of each row to obtain a bump yield.

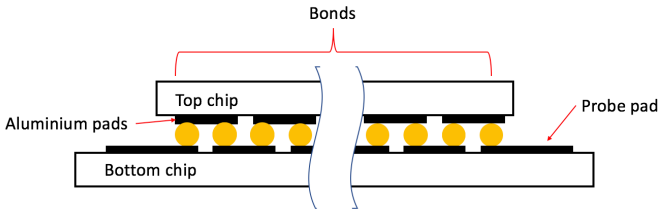


Figure 7.3: An illustration of the side view of the daisy-chain structure after dies are bonded.

The first set of test structures were produced by FBK on 150 mm diameter 640 μm thick wafers. The die were the same size as an FE-I4 chip but with a uniform bump pitch of 50×50 μm^2 producing in 120 000 bumps per die. The resistive chain geometry allowed 21 000 bumps to be tested per die. Indium bumps of diameter 12 μm and 16 μm both with an average height of 10 μm were deposited by Leonardo. Flip chip bonding was performed by Leonardo and MIET producing assemblies with an average die separation of 10 μm. Leonardo and MIET both measured a bump resistance of 10 Ω. Probe measurements demonstrate bonded assemblies with zero defects. The ability to bond the high density chips with an FE-I4 sized die was demonstrated, albeit with thick chips.

Two sets of daisy chain test wafers are being produced on 300 mm diameter wafers to allow the full hybridization chain to be exercised, with the significant exception that the daisy chain structures will not exhibit the same bow as the final chip. CEA LETI are fabricating a test wafer which contains a daisy chain matrix with 400×192 bond pads, equal to the RD53A chip design, as part of a CEA LETI internal multi-project run, with a planned delivery date of November 2017. The bond connectivity will be tested in areas over the array rather than for each row, for example the edge regions and the corner regions. The wafers are being processed with bumps consisting of a copper pillar with a solder cap and with UBM, thinned to 100 μm and then will be inspected for defects, and diced. Flip-chip assemblies will be fabricated at Advacam and CEA LETI to demonstrate that they satisfy the bump bond yield specification as part of the hybridization process.

IZM will produce a daisy chain test structure on 300 mm diameter wafers with an array of 400×384 bond pads, equal to the proposed ATLAS ITk Pixel chip. They will produce 13 wafers, which will be thinned to 400 μm. The design allows testing of individual rows to obtain a measurement of the bond yield. Bumps will be deposited by IZM on six wafers (pure solder) and on three wafers by Leonardo (indium). As required for solder bumps, IZM will also process UBM on the remaining four wafers to allow flip-chip bonding. Matching daisy chain structures have been fabricated by HPK on 150 mm wafers, which have been processed by HPK and Advacam with their solder compatible UBM. The wafers will be thinned, diced and flip-chip bonded. Flip-chip will be performed with the solder bumps by IZM, Advacam, HPK and IFAE, while the indium bumps will be flip-chip bonded by Leonardo, RAL and MIET.

7.8 Future hybridization development plans and production risks

In the last quarter of 2017 the first RD53A wafers will be available for processing. The first three wafers will be processed at IZM as thick wafers to allow module development. In parallel, TSMC will produce top metal and dielectric only wafers to allow bump deposition vendors to gain process experience with the chipset. This will only take place at a limited number of vendors dictated by available funding. At the start of 2018 a significant number of RD53A wafers will be produced, (in batches of 24), and processed into modules by the vendors that have been taken forward to the final stage of the market survey. The RD53A wafers are required to fully demonstrate the hybridization process as they are the closest the ITk has to the final ATLAS ITk Pixel chip.

The hybridization process is an expensive specialised process and the ITk project expects a limited number of interested vendors. To gain market understanding, a CERN based market survey was launched in the fourth quarter of 2017 and is expected to last up to one year. The market survey consists of two stages; a technical questionnaire, to be completed by Q1 2018, and the purchase of prototypes based on the RD53A wafer, to be completed by the end of 2018. Only the firms that fulfil the market survey qualification process will be invited to tender. The tender for the hybridization process will follow the market survey and start in Q1 2019.

The market survey will be divided into three parts, following three distinct phases of the hybridization process, to which each vendor can respond. The first part is the processing and dicing of the sensor wafer; which includes the UBM deposition on the sensor wafer for the solder bump based process, and the deposition of indium bumps on the sensor wafer for an indium bump based process. The second part is the deposition of bumps on the front-end chip wafer and all the necessary processing of the wafers to allow flip-chip assembly, including wafer thinning and dicing and the addition of a temporary glass handling wafer, as required by some of the processes. The third is the flip-chip assembly of the sensor and front-end chips. The market survey will state that the volume of the flip-chip process is subject to change to accommodate the possibility of performing the flip-chip in-house at ATLAS ITk Pixel institutes. Each of the three processes will be qualified separately. The final number of vendors for the bump deposition contract will depend on the capacity of the vendors and their matching to the schedule and their fulfilment of the technical requirements. It is assumed that around 3 bump deposition vendors will be chosen. It is expected that there will be more flip-chip vendors than bump deposition vendors to guarantee the required module production rate as the flip-chip step is a lower volume process. The hybridization PDR will take place in 06/2018, during the market survey followed by the Final Design Review which will take place in 01/2019 after the end of the market survey. The tender exercise will take place in Q1 2019 based on the market survey outcome. Pre-production will be performed between 10/2019 and 09/2020 where 10% of the number of final parts will be started using the ITkPix-V1 front-end chip. This is followed by a PRR in 09/2020, which will take place at the same time as the module

PRR. The final quality of the hybridization process can only be truly assessed via tests on a module and as such the hybridization and module PRR are coupled. Production will be performed from 12/2020 to 11/2022.

The major technical risk associated with the hybridization process is the yield of the flip-chip process using 150 μm thick front-end electronics. The deposition of bumps on the wafers should not be a significant technical risk. A larger wafer format (300 mm) compared to the present ATLAS Pixel system (200 mm) will be used which limits the vendor supply but does not significantly increase the technical risk. The same minimum bump separation as the present ATLAS Pixel chips (50 μm) is being used, but in the ITk it is equal in both directions over the matrix, and as such bump pitch should not be a significant risk increase over past ATLAS hybrid pixel module productions. The flip-chip of the larger ATLAS ITk chip, with a pixel array of 20 mm $\times$ 19.2 mm in size, and thickness of only 150 μm is however a significant risk. The yield of the module has been extrapolated from the ATLAS and IBL hybrid module productions, but significant uncertainty exists until more modules can be fabricated during the market survey process. The development of thin module production has been demonstrated at several possible vendors using the FE-I4 chip to mitigate the risk as far as possible until the final chip set arrives. If the risk of low bump yield is realised during pre-production then several mitigation options are available, which include: purchasing more modules with associated cost increase; increasing the allowed bump defect rate, especially for modules in the outer layers, which has a negative physics impact; and increasing the front-end chip thickness for modules in the outer layers, again with a negative physics impact. The impact on the physics performance of these options will be studied in 2018 before the risk is realised.

8 Pixel Modules

8.1 Introduction and requirements for the ITk Pixel modules

The basic mechanical and electrical unit of the ITk Pixel Detector is a module which also serves as the main electrical interface to the read-out and services and thermal interface to the local supports. The baseline module concept for the ITk Pixel Detector is the well-proven hybrid Pixel Detector in which modules are composed of a sensor and the front-end chip bump-bonded to each other to form a bare module and a PCB module flex glued to the back face of the silicon sensor to connect the front-end chip and the sensor to the outside world. Alternate module concepts such as drop-in CMOS are discussed in Chapter 9.

There will be two main types of hybrid pixel modules: Dual modules (two front-end chips bump-bonded to a single sensor, around 4×2 cm^2) will be used in the innermost layer and the inclined part of the barrel, which optimizes the radial tiling while introducing minimal material. Quad modules (four chips bump-bonded to a single sensor, around 4×4 cm^2) will be used in the outer flat barrel layers and in the outer-end-cap rings. In addition, the inclined part of the innermost barrel layer requires single-chip modules (one front-end chip bump-bonded to a sensor, around 2×2 cm^2). As discussed in Chapter 5, 3D and planar sensors are being considered for the innermost layers. For quad modules in the outer barrel layers and outer end-cap rings, the standard planar sensor technology is foreseen. The front-end chip is presently under development within the RD53 collaboration, which produced the RD53A prototype chip. Following this chip an ATLAS ITk pixel chip will be developed using the basic blocks designed by RD53 while integrating additional functionality to meet ATLAS specifications, see Chapter 6.

Figure 8.1 shows a drawing and a three dimensional rendering of a quad module based on the ATLAS pixel front-end chip with 50×50 μm^2 pixel size. The dimensions of the new pixel front-end chip are not yet defined. An active size of 19.2×20 mm^2 (384×400 pixels) and a periphery region of 2×20 mm^2 are assumed as discussed in Chapter 6. The area between read-out-chips is minimized and covered by ganged pixels on the sensor, see Chapter 5 for more details. All connections (clock and command input, data output, low voltage and high voltage power) to the modules are routed to the active elements via a flexible printed circuit (module flex) which is glued to the backside of the sensor. The connections to the front-end chips and the sensor are made with wire bonds and passive components such as decoupling capacitors and termination resistors are mounted on this

printed circuit. An aggregator chip and a DCS (Detector Control System) chip may also be mounted on the module flex, see Section 8.2.

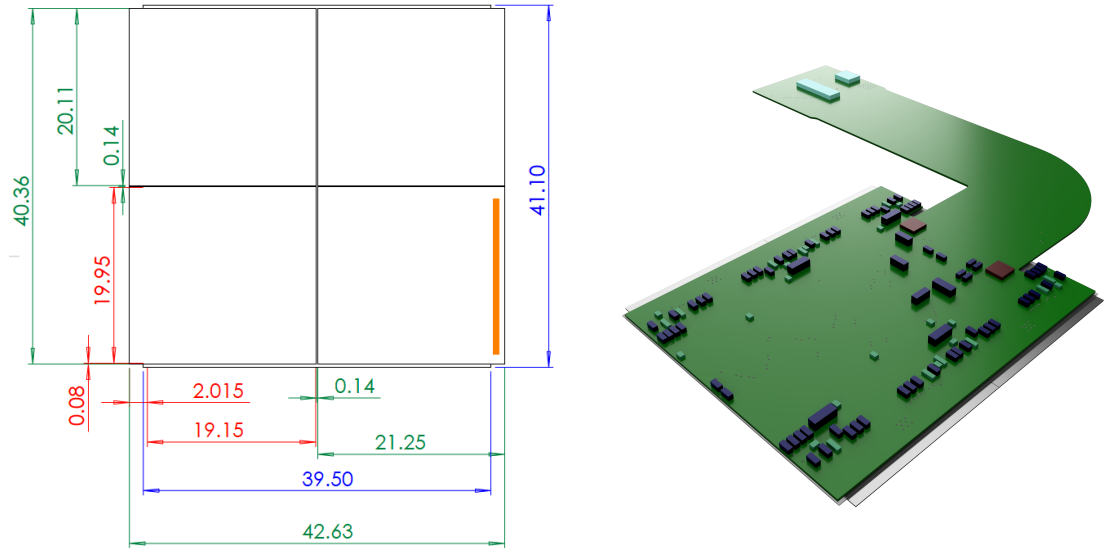


Figure 8.1: Left: Drawing of a quad module with four pixel front-end chips viewed from the front-end chip side, all dimension in mm. Front-end chip dimension are green with the wire-bond pad area indicated in gold on the lower right chip. Sensor dimension are in blue and in red the distances from and to the outermost bump-bond pads of the lower left chip are given. Right: 3D view of a quad module for the outer barrel flat section viewed from the module flex side.

Table 8.1 summarizes the number of required modules for the three different assembly types. It is based on the Inclined Duals Layout of the ITk Pixel Detector as described in detail in Section 2.1.2 The total number of modules is about 10,000 with about 33,000 FE-chips used. The exact number of modules and chips will depend on the final chip size. Apart from the three main module types (quad modules, dual modules and single-chip modules) the modules vary slightly in the design of the connection between the module flex and the local support services especially between the flat barrel and the inclined barrel sections. For the outer barrel layers three different module flex types are required, one for the quad modules in the flat section and two for the dual modules in the inclined section. The inner barrel layers need five more flex types and one more quad module type is required for the end-caps. Therefore up to nine different module flex types are needed resulting in nine different module types. To cope with this number of modules and module types during the production of the ITk Pixel Detector, a highly parallel assembly structure with up to 10 assembly sites is required.

The module flex provides the electrical connection to the module. The pixel module requires the electrical services shown in Figure 8.2. These are provided from the external system by their connections to the electrical services on the local supports, which them-

Table 8.1: Summary of the module count per assembly type and per layer in the Inclined Duals Layout of the ITk Pixel Detector. For the rings the module number is multiplied by two reflecting the existence of two end-caps.

Layer	# of quad modules	# of dual modules	# of single modules	Sum
Barrel 0		192	512	704
Barrel 1	760			760
Barrel 2	660	660		1320
Barrel 3	960	1040		2000
Barrel 4	1300	1300		2600
Ring 0	128			128
Ring 1	484			484
Ring 2	640			640
Ring 3	704			704
Ring 4	936			936
Sum	6,572	3,192	512	10,276

selves connect to the module flex. Internal to the module, the module flex connects the high voltage bias (HV) to the sensor's backside and the low voltage supply (LV and Module GND) to the front-end chip. If the Pixel DCS chip is mounted on the module flex hybrid three additional electric connections are required, see Chapter 11 and Section 8.2.3 for more details.

A single downlink data line pair (CMD/CLK in Figure 8.2) is connected to the module and the signal is routed in parallel to each chip in the module. The clock and command signals are extracted from this data by the front-end chip. The uplink data streams from the front-end chip are multiplexed together into a number of high speed electrical data cables, which run all the way to the opto-converters. The data signals to and from the module are transmitted on differential pairs and are AC coupled. For module temperature monitoring a temperature sensor (NTC) is connected to the Pixel DCS chip (NTC in and NTC out). In addition a second NTC per module can be connected directly to the independent DCS interlock system (TIlock in and TIlock out), which allows for a fast interlock of the power supply system in case of cooling system failures. For multi-chip modules, the front-end chips are connected in parallel for powering from a common low voltage input on the module flex.

The electrical connection of the module to the flex cables carrying services on the local supports must be done in such a way as to not constrain the module. So it must be avoided that the difference in thermal expansion of the service cable and the local support causes stress on the module. Additionally, the connection must be compatible with the module-to-stave loading procedure. The electrical connection is be done via a connector, solder or wire-bonds. Whichever method is chosen the connection must fulfill the electrical specific-

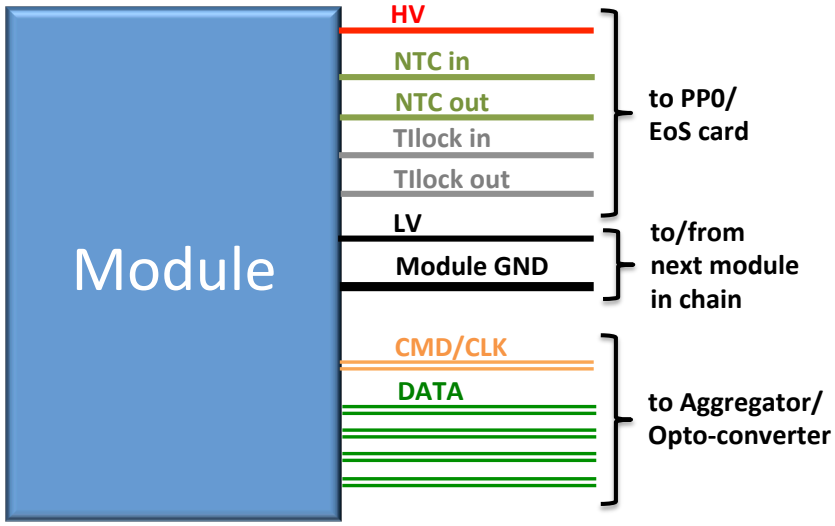


Figure 8.2: Schematic of the electrical connection of an ITk pixel module.

ations for the given interface. The power consumption of a module is around 7 W and this must be removed to maintain the sensor temperature at about -25°C. The modules will be placed on the local support, with the backside of the front-end chips making contact with the support. This interface is part of the thermal path between the module and the cooling fluid. The attachment method and thermal performance studies are discussed further in Chapter 13 whereas the details of the powering are covered in Chapter 11.

In the following the individual components of the pixel module are described in more details before the module assembly procedure and the quality control and assurance procedures are addressed.

8.2 Components of ITk Pixel Modules

8.2.1 Bare Modules

The bare pixel module consisting of a sensor bump-bonded to a number of front-end chips is the main part of the pixel module. Flip-chip bump bonding is an industrial process and is described in Chapter 7. The bare modules are delivered to the module assembly sites, and after some acceptance tests as in detail discussed in Section 7.4.2, will be assembled into ITk pixel modules.

8.2.2 Module Flex

The module flex is glued to the backside of the sensors and forms the connection between the front-end chips and the local support electrical services. The connections to the front-end chip will be established via wire-bonds, the connection to the type-0 services can be done via connectors or wire-bonds as well. In addition to the necessary low voltage, high voltage, DCS, data and command lines, the module flex will contain several passive and possibly active components that are needed to operate and read-out the front-end chips. The details of the geometrical layout, the number of lines, passive and active components on the module flex depend on the detector layout and the front-end chip design, and also on the number of front-end chips per module and the position of the module in the detector.

The module flex will consist of two metal layers, where one of the layers serves as the line for the supply current, while the second layer will represent the local module ground. Differential pairs for the module uplink and downlink are placed within these layers, as well as the supply line for the sensor bias voltage and necessary lines for the DCS system. The sensor bias voltage will be routed to one or more holes on the module flex, from where it will be supplied to the sensor backside via wire bonds.

Termination resistors and coupling capacitors for the downlink, and bias resistors and filter capacitors for LV and HV supply lines will be mounted on the flex. The resistors that define the reference current for the Shunt-LDO regulator, together with additional filter capacitors if required, will also be placed on the flex.

As a part of the Detector Control System (DCS), two NTCs will be placed on each module flex. One of these will be connected directly to the Pixel DCS chip, which monitors the temperature and voltage drop across a module and has the capability to bypass a module in the serial powering chain. The second NTC will be routed directly to the interlock system, however most likely only for the first and last module connected to one cooling pipe.

A possible active component on the module flex is an aggregator chip (Chapter 6) for the uplink, which combines the data sent by the front-end chips into a single differential pair that is connected to the electrical services. Any passive components, and supply and command lines for such a chip would have to be placed on the module flex as well. In some detector designs, the module flex could also contain the DCS chip, see Section 8.2.3.

Fiducial marks are present on the module flex to aid with the assembly process. At least two fiducial marks must be present near to each front-end chip wire bond pad array.

For the connection between the module flex and the electrical services, the module flex have a pigtail which needs to be bent in order to make the connection. The minimum bending radius is around 2 mm, depending on the final thickness of the flex. The details of the connection will depend on the final layout of the system and the geometry of the local supports, see Chapter 13 for more details. Currently up to nine different module flex

designs are required but a further design optimization process is in progress to potentially reduce the number.

The pigtail in the barrel section would contain the necessary connectors for all lines that have to go from the module to the power supplies, the opto-converters, the interlock system and the DCS chip. In Figure 8.3, an example of a module flex for a quad chip module in the flat barrel section is shown. In the rings, the layout of the flexes is slightly different, as power and data connections lie on opposite sides of the module flex.

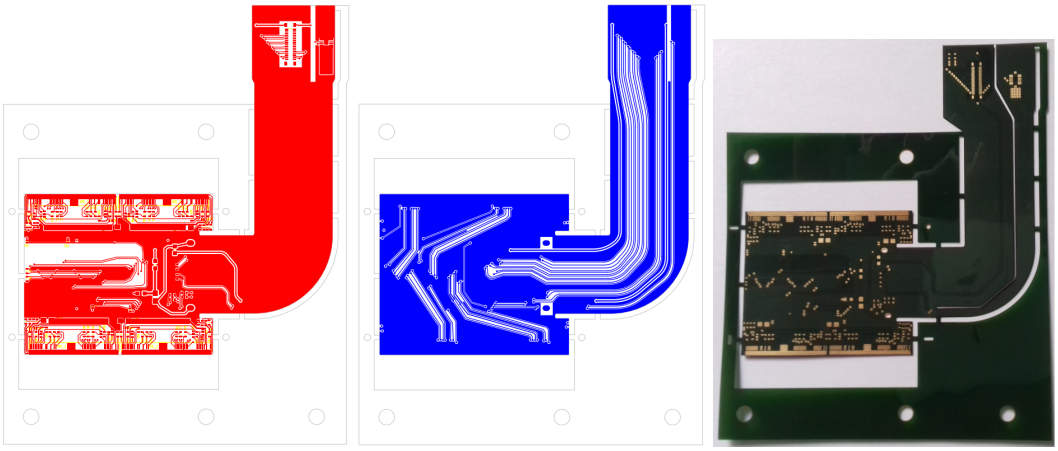


Figure 8.3: An example of a design for a quad module flex for the ITk Pixel Barrel Section. The flex has two layers, the top layer (red, left side) serves mainly as input for the low voltage current supply, while the bottom layer (blue, middle picture) serves as local module ground and return line. The two holes for the sensor bias voltage can be seen close to the pigtail, while the view of the top layer shows the positions for possible passive components on the module flex. On the right side a photo of a manufactured module flex can be seen.

8.2.3 DCS chip

To ensure reliability of the entire serial powering chain, monitoring and control must act on the module level. Removing a module from a serial powering chain in case of detected over-voltage or other problems must be possible. The main component of the control path is a Pixel DCS chip (also known as Pixel Serial Powering and Protection chip or PSPP chip) which provides monitoring and control capabilities in close proximity to the module. Details of this chip can be found in Chapter 11. The Pixel DCS chip will be mounted either on the module flex or on the local support service close to the connection to the module. The latter position is the preferred option in order to mitigate the risk of a power connector failure in a serial powering chain. The DCS chip will dissipate much less but still a considerable amount of power of about 1 W in addition when bypassing a module. If the DCS chip is located on the local support service chain this adds to its power dissipation budget. If the DCS is not in operation the power dissipation is small.

As baseline, connection between the DCS chip and the module flex using industrial standard C4 flip chip processes is foreseen. Such processes promise a robust electrical connection with better heat transfer between chip and module flex. The alternative mounting method of the Pixel DCS is gluing on the module flex or local support service chain followed by wire-bonding for the electrical connection. For this method the number of wire-bonds is large and would perhaps take up too much area on the module flex or local support. In both cases the DCS chip is attached to the module flex before the module flex is attached to the bare module or the local support.

8.2.4 Aggregator Chip

Depending on the position in the ITk Pixel Detector, the uplink data streams from the front-end chips of a multi-chip module are multiplexed together into a number of high speed electrical data cables. This is done in a dedicated aggregator chip which is mounted on the module flex or at the connector to the data cable. The functionality of this aggregator chip is described in Chapter 6. If located at the module flex the baseline mounting method is gluing to the module flex and wire-bonding before assembling the module flex to the bare module. An industrial C4 bump bonding process is considered as an alternative.

8.2.5 Material budget of the ITk pixel module

The radiation length of the ITk pixel module is estimated based on experience with IBL and ATLAS pixel modules. Table 8.2 summarizes the material budget (in units of radiation length for normal particle incidence) of the ITk pixel modules; the contribution of the different components is averaged over the whole module area. The result for the module is estimated to be 0.67% of a radiation length which is comparable to other hybrid pixel modules built in the past such as the IBL pixel module which achieved between 0.58% and 0.61% of a radiation length [2]. The module material is dominated by the module flex, which is in turn dominated by the copper layers and the SMD components, connectors and the solder to attach them. The contribution of the two copper layers is inevitable because they control the voltage drop for the LV and serve as ground planes for the high speed data lanes. However, it is investigated to reduce the coverage of the copper layers by meshing them. The module DCS and aggregator chips are not considered because it is not clear whether they are needed as individual module parts. But even if these chips will be on the module flex their contribution would be small because both chips are small in size and thickness when compared to the full module. It is assumed that the front-end chip thickness and sensor thickness is 150 μm which may differ among different module types. The effect on the material due to variations in the physical thickness of these items could be severe. An increase in material by 52% over the baseline design is observed with a FE-chip thickness of 400 μm and a sensor thickness of 200 μm.

Table 8.2: Breakdown of material budget for the ITk pixel modules in units of the radiation length.

	% X_0
Front-end chip, 150 μm thick	0.19
Sensor, 150 μm thick	0.17
Bumps	0.03
Module flex incl. SMD components	0.27
Flex adhesive	0.01
Total	0.67

8.3 Pixel Module Assembly and Quality Control

8.3.1 Module Assembly Steps

The module assembly process consists of following steps in the indicated order:

- Acceptance tests

  Visual inspection of all components

  HV tests of flex if this is not performed in industry

- Preparation of components

  Module flex cleaning if not performed by the vendor

  Bare module cleaning

- Adhesive attachment of module flex to bare module
- Wire bonding and wire bond protection

All assembly procedures shall guarantee a uniform module quality which is defined by the module specification and will be checked by the module quality control and assurance plan described in the Section 8.3.2. Promising candidate technologies and procedures based on experience with modules of the current ATLAS Pixel Detector and IBL are in development. Detailed assembly procedures are being prototyped with modules based on the FE-I4 front-end chip. Although the methods are similar in general, they differ on details like usage of automated tooling or the glue application for the module flex adhesion. So a range of assembly methods are developed while technologies and procedures will be standardized as much as possible. But all assembly methods will be qualified to produce modules to the same specifications. The quality across the different assembly sites will be ensured through a site qualification stage as discussed in Chapter 19. In the following the assembly procedure based on different current developments is described in more detail.

Bare modules, and flex circuits are mechanically joined using dedicated adhesives which are currently in qualification. In the case of a more automatized process bare modules and flex circuits can be assembled using a custom semi-automated "pick-and-place" machine integrated with optics, pattern recognition software, vacuum and glue dispensing tools, electro-valves and pressure sensors. The module assembly sequence begins by manually placing pre-tested, known good bare quad modules and flex circuits onto custom vacuum chucks on the baseplate of the pick-and-place machine. The control program successively moves the camera to view fiducials on the bare quad modules and flex circuits and acquires the part locations using pattern recognition, picks up a stamping tool from a tool rack, dips the stamp in a glue reservoir, stamps the epoxy onto the sensors of the bare quad modules, returns the stamping tool to the tool rack, picks up vacuum tools from the tool rack and pick-and-places an individual flex onto the bare quad module sensors (making adjustments based on the actual part locations to accurately align and join the components). The vacuum tools remain vacuum clamped to the baseplate until the epoxy is cured at room temperature. Curing time can be reduced by curing at higher temperatures but curing time is not expected to limit assembly rate limiting step. After the epoxy is cured, the machine returns the vacuum tools to the tool rack, leaving the assembled modules ready for removal from the pick-and-place machine.

Alternatively, a more manual custom-made tooling consisting of a module pick-up tool and a flex positioning and module gluing jig is used. In detail, a bare module placement jig is used to position the module with Perspex pins. The jig has two bolts to position a module pick-up jig which holds the bare module with vacuum. An example of a jig with a silicon quad piece attached, can be seen on the photo in Figure 8.4 (right). The module flex is positioned upside down on a flex positioning jig and held by vacuum. It is shown on the left part of Figure 8.4. The adhesives are applied on the back-side of the flex. In the picture the yellow dots represent dots of an epoxy and in green, at the wire-bond area, the area covered with tape is shown. The flex positioning jig features the same bolts and the module is placed on top of the flex by lowering the pick-up tool with an accuracy of less than 100 μm. For curing it rests in this position and weights (20 g/per chip) are placed on top. First shear tests of this gluing concept with lap joints show stable adhesion even after thermal cycling.

Following mechanical assembly and metrology, the front-end chips and sensor HV are electrically connected to the flex circuit using wire bonds made with an automated ultrasonic wedge bonder as shown in Figure 8.5. Aluminum wires with a diameter of 25 μm are used. Routine pull tests of sample wire bonds are performed for quality control using a tensile pull tester. Routine visual inspection of the wire bonds is performed. After passing inspection, all wire bonds will be encapsulated with an elastomeric compound dispensed by a semi-automated encapsulation station. In addition to mechanical protection, wire-bond encapsulation helps preventing corrosion of Al wedge wire bonds and suppresses the sensitivity to resonant wire-bond oscillation breakage and is therefore considered as a necessary precaution for the pixel modules. A "connector saver" pigtail cable will be used to connect

each assembled module to DAQ instruments for testing. These pigtails are needed to protect the connectors of the module flexes and will be removed before the module is loaded to the local support.

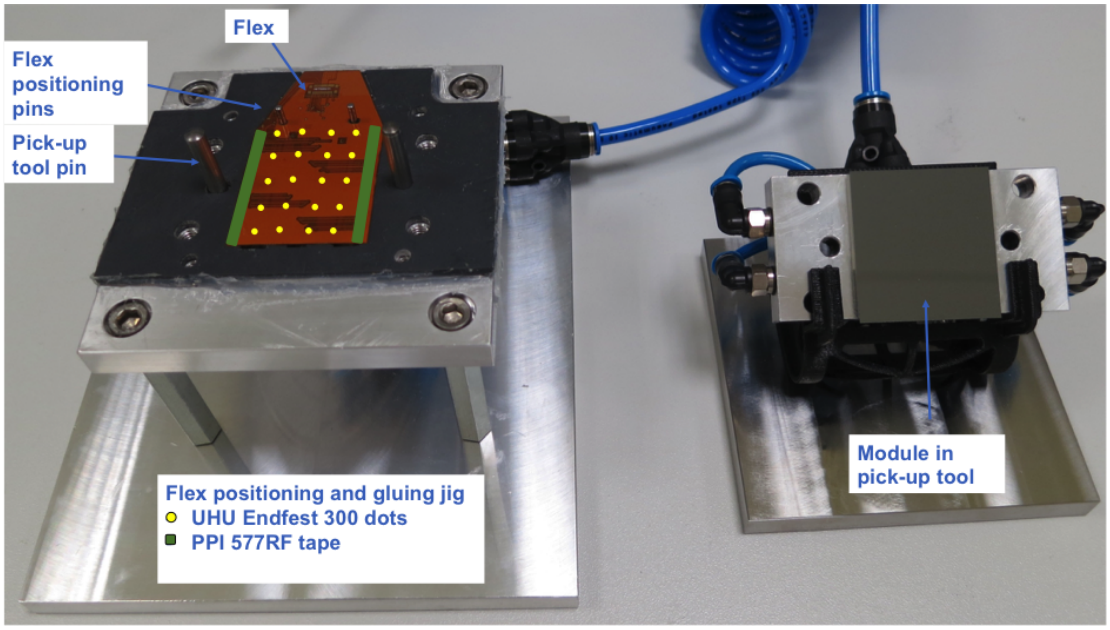


Figure 8.4: Photo of a module flex in flex positioning and module gluing jig (left). Areas of glue application are indicated. Module in pick-up tool for assembly on flex (right).

All module assembly and testing must take place in a clean environment equipped with temperature and humidity control and ESD protection for personnel at all work-stations and on work surfaces and floors. Specification for this environment will be developed and all critical steps shall take place in a clean room of Class 10000 or better. A database will be used to record the status of each module at every step of assembly including the electrical test results. A nominal assembly rate of at least two modules per day at each module assembly site is foreseen. Details of the module production organization including total numbers and work sharing will be discussed in Chapter 19. Assembled, tested and fully qualified modules will be shipped weekly to the loading site, where they will be mounted on the local supports.

The assembled pixel modules will be loaded into a combined storage, transport, and testing case. This unit is based on a rigid machined aluminium plate, the spine, and a secure plastic enclosure. After the module has been completed it will be attached to the spine and all other processes and tests can be carried out while the module is protected by the case. Figure 8.6 shows a design of the complete module transport system. The test PCBs allow the modules' functionality to be checked after transportation to the module mounting site without removing it from the case. It is also possible to use the combination of the vacuum holes and locating holes to carry out other tests on the module while it is protected in the

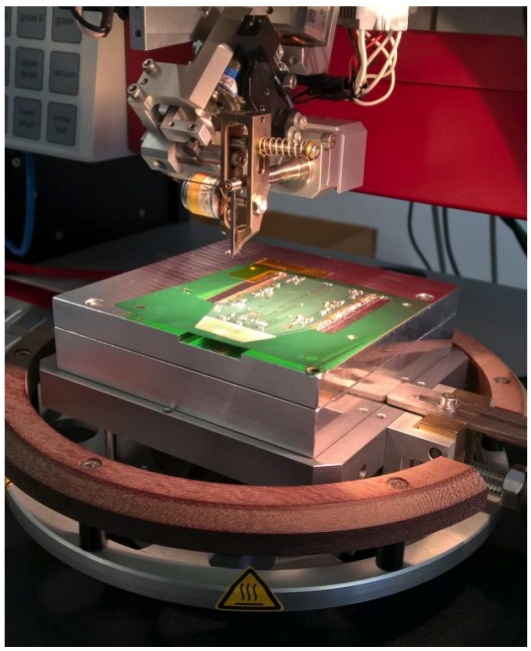


Figure 8.5: Photo of a module on an assembly- and wire-bonding jig, installed in a semi-automated bond machine.

transport case i.e. thermal cycling. This transport system will allow safe, secure transport and testing of completed pixel modules and storage until they are ready to be mounted. The transport boxes can be re-used once the module is loaded so the number of boxes is only 25% of the number of required modules, i.e. about 4,000.

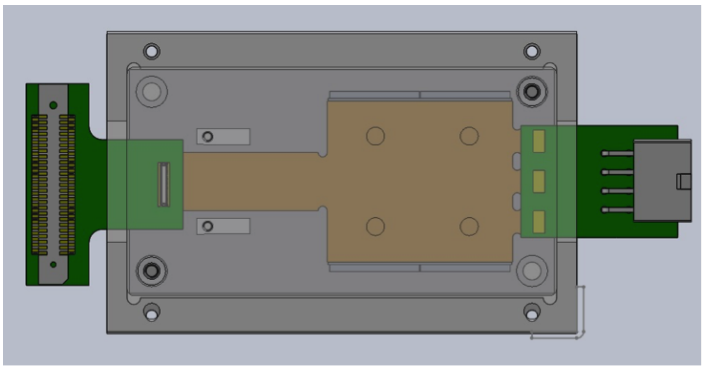


Figure 8.6: Drawing showing the completed module mounted on a spine loaded in to the transport case. This figure also shows the connector saver PCBs that provide safety for connecting the data and power to the module when in the case.

Up to 50 dual and quad modules based on the FE-I4 front-end chip have been assembled with the described procedures at different sites and with good yield. As an example the

2D histogram in Figure 8.7 shows the result of a source scan performed with such an FE-I4 based quad module. For the source scan, electrons from a ^{90}Sr source are used. A scintillator underneath the quad module is used as an external trigger source. The colour coding indicates the number of hits per read-out channel. The quad module is built from a 150 μm thin n-in-p planar sensor equipped with 4 front-end chips which are thinned to 150 μm using a glass handling wafer and a prototype module flex. Apart from some dead pixels almost no dead area is observed in the illuminated module center and the inter-chip area covered by larger pixels is working nearly completely.

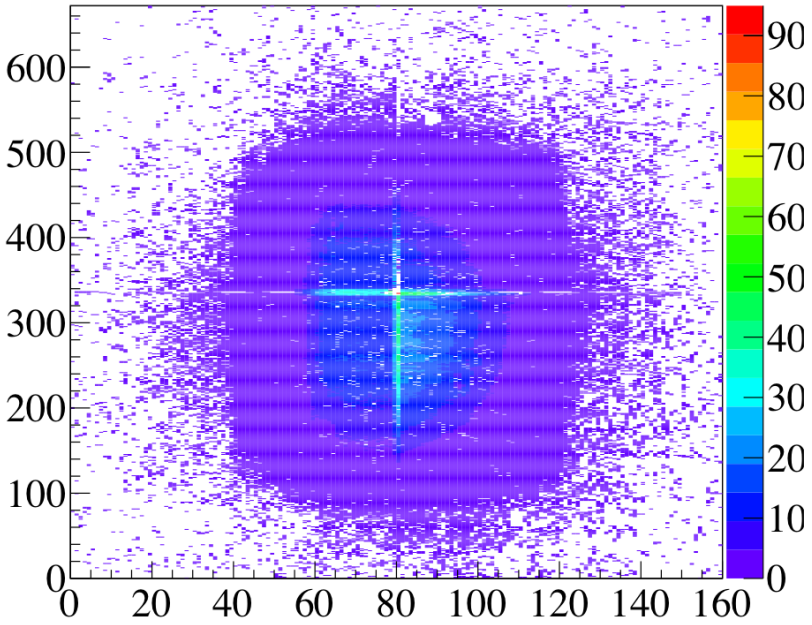


Figure 8.7: ^{90}Sr source scan of a FE-I4 based quad module.

8.3.2 Planned Quality Control during Production

The entire module assembly process will follow a Quality Control plan which is designed to ensure uniformly high quality of all modules produced at the required rate throughout the production period. The ITk general approach is described in Section 19.1. Tests are divided into Quality Control (QC) tests which are applied to all modules or their components and Quality Assurance (QA) tests, i.e. tests which are done on a subset of modules or their components. In the following all planned quality control and quality assurance test stages are discussed. The entire procedure follows this sequence:

- Bare module reception tests (QC)
- Module flex reception tests (QC)

- Quality assurance tests to module flex and dedicated test tokens (QA)
- Mass measurements and inspection of the fully assembled modules (QC)
- Wire bond pull testing (QC)
- Initial module tests (QC)
- Long term module tests (QC)
- Module tests beyond its operating range and destructive tests (QA)

Each of these test stages consists of a number of individual test steps. Quality control tests include long term module tests such as sensor IV test, electrical tests of chip functionality, source test for bump bond quality as well as thermal cycles and long-term tests at the expected operational temperature of about -25°C, as measured on the NTC on the module flex. The results of all tests are uploaded to a production database at the end of each phase. Table 8.3 and 8.4 list all quality control tests at the different stages during and after the module assembly process. Some of the tests maybe omitted after the pre-production. In particular, the bare module reception tests about electrical properties (front-end chip and sensor IV tests) require dedicated and specialized equipment. It is only justified in case of relatively low bare module yield to allow a rework of the bare module at the bump bonding vendor.

Table 8.3: Overview of the quality control tests during the module assembly.

Bare module reception tests	Module Flex reception tests	Assembled modules: Mechanical tests
Visual inspection	Visual inspection	Weighing of assembled module
Weighing of bare module	Metrology	Visual inspection
Sensor IV curve	HV test	Metrology
FE chip electrical tests	Wire-bond pull test	Envelope check
	Weighing	Wire-bond pull tests

The most important module tests are the electrical tuning and performance tests during the initial and long term module tests. These consist of the necessary fine tuning of the pixel threshold and charge response followed by noise, cross-talk and minimum threshold measurements. The results of these tests will be compared to the specifications and performance figures of merit will be derived which will be used for the evaluation and ranking of modules. In addition, these measurements will be used to monitor the performance of the module after it is mounted on local supports and installed in the global supports.

Table 8.4: Overview of the quality control tests of the assembled modules.

Assembled module: Initial module tests	Long term module tests
Sensor IV curve	Thermal cycling
Electrical tuning at 20°C	Burn-in test
Detailed performance tests at 20°C	Final Sensor IV curve at -25°C
Source testing at 20°C	Electrical tuning at -25°C
	Electrical performance tests at -25°C
	Source testing at -25°C

Quality assurance tests such as thermal shock tests, HALT[1] and HASS[2] tests as well as radiation tests are performed only on a sample of items to control the quality between batches or different assembly sites. Number and size of samples will be adjusted in order to capture any changes in the production process while minimizing the work load. Table 8.5 summarizes the planned reliability tests for quality assurance to module flexes and the fully assembled pixel modules.

Table 8.5: Overview of the quality assurance tests during module production.

QA tests to module flexes	QA tests to pixel modules
Via and trace resistance tests	Thermal shock tests
Thermal aging tests	Accelerated aging tests
S-parameter tests	Stress tests
Peel tests	Radiation tests
Thermal shock tests	
Radiation tests	

All tests are done with standardized test equipment and procedures. Test results are stored centrally in a production database. The most important test stages are the initial module and long term module tests which will be the key ingredient for the module selection and ranking procedure. A fast turnaround in bare or initial module electrical tests is needed to provide rapid feedback on the quality of the bump-bonding.

Modules are ranked according to their performance and quality based on all test results. This ranking will be done in terms of the number of non-working pixels per module. Each test step will reveal a number of pixels failing this test. Such pixels are regarded as non-working pixels. After all tests for each module the total number of non-working pixels

[1] Highly Accelerated Life Test
[2] Highly Accelerated Stress Screening

will be determined without double counting and for non-conformities during mechanical and sensor testing a penalty in terms of additional non-working pixels can be added. All tested modules of each type are ranked according to this number of non-working pixels and a cut can be applied for the rejection of modules. Modules with a certain percentage of non-working pixels (e.g. 3%) are rejected. The best modules, i.e. the modules with the lowest number of non-working pixels can be selected for the use in the innermost layers. If necessary, selection cuts for other detector areas can be defined to ensure that the best pixel modules will be used in the most sensitive detector areas. The entire testing and ranking procedure will be developed during the prototyping phase and applied during the pre-production phase of the first 10% of the module production. Afterwards the procedures will be evaluated, improvements applied and rejection and selection cuts will be adjusted according to the results obtained.

The requirements of the ITk pixel modules are summarized in a module specification document which has been reviewed internally. Once the first complete design of the module for the final components is finished, a preliminary design review (PDR) is foreseen for April 2018 to allow for further adjustments and improvements after the experience with modules based on the RD53A front-end chip. A final design review (FDR) with external referees is planned for the second half of 2019 after careful evaluation of prototype modules including results after irradiation. Before the pre-production phase of the module construction starts, an extensive site qualification process is planned in 2019 to ensure an equally good quality of assembled modules on all sites. The review process of the module design is concluded with a production readiness review (PRR) in the fourth quarter of 2020 after the pre-production phase of assembling 10% of the total module production.

9 CMOS pixel

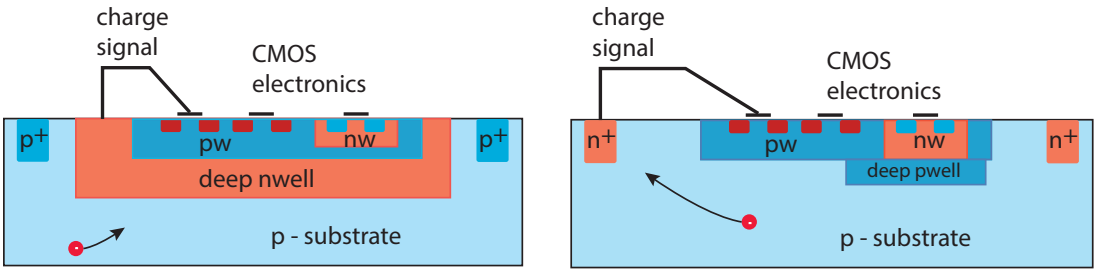
9.1 Motivation and R&D Overview

A new approach towards a pixel module is a "monolithic" module with pixel sensor and read-out chip being one entity, in contrast to the traditional hybrid pixel module described in the preceding chapters. This approach exploits recent advancements in CMOS technologies, in particular regarding multi-well processes and suitable substrates [79]. It offers a number of advantages, but it still needs to address a few technical features to demonstrate its integrability in the ITk. The route towards a possible implementation of CMOS pixel modules in ATLAS is described in this chapter and summarized in Section 9.5.

The CMOS imaging technology is highly mature and used in chip industry for a long time. CMOS sensors for optical and X-ray imaging are found in our personal cameras and in medical clinics. These detectors usually operate by collecting the charge from energy deposits in a thin epitaxial layer underneath the CMOS electronics layer. The HEP community has experimented with CMOS pixels and successful implementations (so-called Monolithic Active Pixel Sensors, MAPS) can be found in several experiments [115, 116, 117, 118]. However, these implementations largely collect deposited charge by diffusion rather than by (fast) drift in an electric field. The read-out is usually implemented using a rather slow rolling-shutter scheme that limits the timing resolution that the sensor can achieve. As a consequence they are not suitable for the high hit rates and radiation levels at the HL-LHC.

In recent years, CMOS technology add-ons became available to the HEP community, in particular the possibility to apply high-voltage and use high-resistivity wafers and as multiple wells that can be used for embedding and shielding of transistors and charge collection nodes. Employing a sufficient number of wells (≥ 4), full CMOS logic implemented on a depleted bulk becomes possible with sufficient shielding allowing for complex in-pixel circuitry plus depletion of a large volume underneath the pixel implantation. These developments open the possibility of implementing radiation-hard pixels with sufficiently complex circuitry in small pixels to meet the rate and timing requirements of the ITk pixel volume [79]. Such *depleted CMOS pixel sensors* (DMAPS) constitute monolithic pixel modules as they combine sensor and read-out functionality.

CMOS foundries capable of implementing the design offer many advantages compared to the traditional process for hybrid pixel modules. The foundries' production capabilities



(a) Large fill-factor (b) Small fill-factor

Figure 9.1: The two principal variants of considered CMOS cell geometries: (a) Large fill-factor: the charge collecting deep nwell encloses the complete CMOS electronics. (b) Small fill-factor: the charge collection node is placed outside the CMOS electronics area (from [79]).

exceed 30 000 wafers per month with an average processing time of three months. This allows for a quick supply of sensors with a quick reaction time in case of problems with the production. For large area production, the cost per wafer also goes down as the main initial cost is the price for mask production. As CMOS pixel modules contain sensor and read-out logic, hybridization, which is a very labor-, time-, cost-, and yield-loss-intensive production step, is not needed.

After the first proof of principle in 2007 [119], depleted active CMOS pixel sensors for the ITk Pixel Detector have been investigated in a systematic way. A series of demonstrator detectors investigating various pixel configurations in different CMOS technologies and comparing different front-end and diode designs were submitted and evaluated by measuring charge collection, radiation tolerance and rate capability. These early demonstrators were no yet full DMAPS realisations as no matrix read-out architecture was implemented yet. From a large number of CMOS technology prototype designs,[1] the technology of three vendors was found to be most suitable for ITk pixels: ams (180 nm), LFoundry (150 nm) and TowerJazz (180 nm). In order to characterise these prototypes the FE-I4 pixel chip was exploited to decouple read-out electronics effects from sensor while providing fast matrix read-out functionality. The CMOS sensors were bonded to the FE-I4 chip, either via bump bonds or by capacitively coupling (gluing) the sensor to the FE-chip (so-called CCPD detectors [120]).

As a next step large pixel matrices ($\sim 1\,\mathrm{cm}^2$) were addressed following two development lines[2]:

- large fill-factor designs (large-FF)
- small fill-factor designs (small-FF)

[1] ams aH35, ams H18, ESPROS-130, GF-130, IBM-130, LFoundry-150, STM-160, Toshiba-150, TowerJazz-180, XFAB-180, where the attached numbers indicate the feature size.

[2] The word *fill-factor* is used here despite the fact that large or small *electrode* design would be more correct.

The difference is explained in Figure 9.1. In large-FF designs (Figure 9.1(a)) the logic is embedded in a large deep n-well, which also acts as the charge collection node. In small-FF designs (Figure 9.1(b)) the collection node is placed outside of the electronics circuitry. In both cases full CMOS electronics can be implemented in the active area of the pixel. Since in large-FF designs the average drift distance is small, they are less prone to radiation induced charge trapping. However, the total input capacitance to the amplifier, represented by the n-well capacitance to all boundaries plus the capacitance between the deep p-well and the deep n-well, is large (up to several 100 fF, depending on layout), influencing the noise, power, and timing performance. In addition, potential capacitive coupling of digital transient signals into the sensor must be prevented by dedicated design. Small-FF designs offer small ($\mathcal{O}(10)$ fF) capacitances and little cross coupling. However, additional technology effort is needed to increase the radiation tolerance to HL-LHC levels by improved charge collection by drift over a larger depleted volume (see Section 9.3.2). The difference in capacitance also drives the difference in expected noise performance: for small fill-factor designs we expect an approximate in-time-threshold of 400 e^-, while for large fill-factor designs we expect an in-time threshold of approximately 1200 e^-.

For large CMOS pixel matrices, first *large-FF designs* were pursued in two technologies, because the radiation tolerance was regarded the most important issue to address. Pixel matrices with FE-I4 aided read-out as well as fully monolithic CMOS detectors including complex read-out architecture were fabricated and tested (Section 9.3.1). All radiation tests so far obtained with large-FF CMOS designs have shown that these sensors perform well to the radiation levels (TID and NIEL) expected for 4000 fb^{-1} in Layer 4 and even in Layer 3 and possibly Layer 2 (see Table 2.9). Initial small-FF prototype designs indeed showed radiation damage effects after a few times 10^{14} $\text{n}_{\text{eq}}/\text{cm}^2$ (see for example [121]), not sufficient for ITk application. Based on the ALICE ITS development [122], however, a small-FF design effort with appropriate radiation tolerance including a process modification to strengthen the lateral drift motion was started in 2014/2015 based on the TowerJazz 180 nm process (Section 9.3.2). A full-size matrix has been submitted in September 2017; preliminary characterising measurements have been obtained in November 2017. At the time of writing the CMOS Pixel Collaboration expects that the small-FF approach will yield the required radiation tolerance while maintaining the multiple benefits regarding power, timing, noise, and read-out architecture, offered from a small input capacitance and spatial separation of charge collection area and CMOS electronics.

In summary the benefits of depleted CMOS Pixels in the ITk are:

- Usage of a commercially mature process technology
- Much less elaborate assembly process (e.g. no hybridization)
- Much lower cost (factor 2.5-3 compared to hybrid pixel modules)
- Fast turn-around production at large volume producers
- Pixel size 50×50 μm^2 and smaller (25×25 μm^2 achievable)
- Thin modules (100 μm)

Section 9.2 describes motivations and schedule of a possible realisation of CMOS pixels in the ITk. The status of the current developments is described in Sections 9.3.1 and 9.3.2; the integration in the ITk is described in Section 9.4.

9.2 CMOS sensors in the ITk

For the ITk a most natural implementation of CMOS pixel would be at the innermost pixel volume (Layer 0 and Layer 1) as b- and τ-tagging would directly benefit from thin, small size pixel modules. However, at present the logic density needed for the data rates expected at the innermost layers cannot yet be achieved given the feature sizes offered by current CMOS technologies suitable for DMAPS. In addition radiation hardness has not yet been systematically checked at the level required for these layers.

The low cost and ease of production has most benefit for the large area outer layers, where also the radiation levels and data rates are reduced by roughly an order of magnitude compared to the inner layers. Therefore, we believe that an attractive scenario for CMOS pixels on the time scale of the construction of the ITk are DMAPS modules for the outermost barrel layer (Layer 4).

The particular attraction of CMOS modules is the fact that there is only a single die integrating the functionality of sensor and read-out offering a huge production ease and cost benefit in terms or sensor production and required processing which is particularly relevant for the largest surface layers of the ATLAS Detector. Rate and radiation levels in the outer barrel region are similar to those faced for the current ATLAS Pixel Detector ($\sim 10^{15}$ n_{eq}/cm^2 and 60 Mrad) and thus do not require the high level of integration of the front-end electronics needed in the innermost layers (see Chapter 6). A feature size in the 130-180 nm range, as provided by most high-voltage and high-resistivity commercial processes, is adequate to provide the necessary level of local hit-buffering and read-out speed.

With 9400 FE-chip equivalents, including pre-production and spares, the ITk Layer 4 requires a total of 235 CMOS-wafers, which suggests a production volume of 300 wafers at 80% yield and 500 wafers at 50% yield. Based on demonstrated prices in the three different CMOS technologies used (ams, LFoundry, TowerJazz), we have estimated the resulting production cost. The cost reduction of the ITk CMOS module over the comparable ITk hybrid planar module is the sum of sensor cost, FE-chip cost, and bump bonding cost, amounting to approximately a factor of 3 compared to hybrid pixel modules. Taking into account the non-recurrent costs, it will change the module production cost of Layer 4 from 4.1 MCHF to 1.3–1.7 MCHF (for a 50%–70% yield).

The fast turnaround time of CMOS foundries will also be beneficial in terms of production schedule. The reduction in production load on the bump vendors and the possibility to perform the CMOS module production in parallel may provide a reduction of up to six

months of the module production time (including testing time) by eliminating the need for UBM and flip-chip processing associated to the sensors in a hybrid pixel module.

CMOS sensors can efficiently be operated with depletion layer thicknesses between 20 μm and 100 μm. Sensor thinning to thicknesses between 50 μm and 100 μm will reduce the material budget of the module silicon by a factor 3 compared to hybrid pixel modules (150 μm each for sensor and front-end chip, see Sections 5.3 and 7.1). The thinner depletion layer results in a smaller cluster size, reducing data size and bandwidth requirements correspondingly. In the small-FF approach, there is the additional potential of reduced pixel size, improving the granularity with respect to the default 50×50 μm^2 size. Designs with 36×36 μm^2 have already been realised. These aspects are quantified in Section 9.2.1.

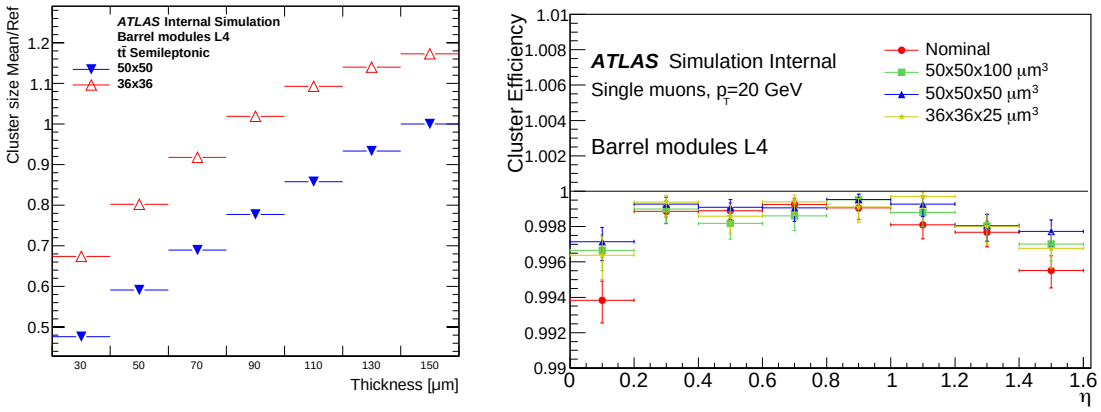
We only mention here in passing that thin CMOS pixel sensors at the inner layers Layer 0 and Layer 1 would more directly benefit the physics performance of ATLAS in terms of flavour tagging once the logic density can be achieved in processes with smaller feature size rendering 25×25 μm^2 pixel pitches with ultra-thin (<100 μm) modules possible. Radiation hardness at the level expected for inner layers needs also to be verified, but they should not be show stoppers since already used in the hybrid front-end electronics in Chapter 6.

9.2.1 Tracking performance studies

The impact of deploying CMOS sensors in the outermost barrel layer on the overall ITk performance has been investigated. Simulation studies assume an average signal height for normal incidence particles of 100 e^-/μm (with a most probable value of 80 e^-/μm), and a threshold of 500 e^- and 150 e^- respectively for large and small fill-factor designs. These thresholds are significantly larger than the expected noise and threshold dispersion (respectively 50 e^- and 20 e^- for large and small fill-factor designs) to guarantee stable operation of the detector.

With the technologies considered a range of depletion region thicknesses can be realized determining the signal height. Also the noise level depends of the pixel layout, being strictly correlated with the different capacitances obtained for small and large fill-factor designs as described in Sections 9.3.2 and 9.3.1. Therefore a fast digitization algorithm is used to perform scans for several detector parameters. Figure 9.2(a) illustrates the effect of the depletion depth on the cluster size for the standard 50×50 μm^2 pixel size and for the smaller 36×36 μm^2 pitch used by the small fill-factor prototypes described in Section 9.3.2. It is obtained from a simulated sample of $t\bar{t}$ events and it shows relative variations, up to 50% level, with respect to fully depleted 150 μm thick sensors of a hybrid pixel module.

Tracking performance has been studied with a full detector simulation for the benchmark points 50×50 μm^2 and 36×36 μm^2 and compared to the layout described in Section 2.1.2. Comparisons to hybrid pixel modules with 150 μm depletion have been done in terms of cluster efficiency, total number of clusters per track, track parameters d_0, z_0 and q/p_T, and track reconstruction performance have been made. No significant differences have



(a) (b)

Figure 9.2: Performance studies for CMOS detectors (small-FF) in Layer 4: (a) relative cluster size variation as a function of the depleted region size for the reference pixel size 50×50 μm^2 (blue) and the 36×36 μm^2 (red) already realised in small fill-factor designs, reference point is a fully depleted 150 μm thick sensor foreseen for the baseline layout; (b) efficiency for association of cluster to tracks in Layer 4 for different CMOS pitches and depletion depths: fully depleted hybrid modules (red) fully depleted large-FF (green), partly depleted large-FF (blue) and small-FF (yellow).

been seen. As an example we show in Figure 9.2(b) the cluster efficiency in a single-muon sample.

In conclusion, the ITk performance is robust against variations of the pixel granularity of Layer 4, while the overall bandwidth usage benefits from the smaller cluster size obtained with reduced depletion depth.

9.3 CMOS pixel sensor developments: Designs and Performance

To meet the requirements for the ATLAS outer layer ITk pixel system, several technologies have been studied, employing different strategies to achieve the required performance mainly in terms of charge collection, radiation hardness, timing, and power. In order to obtain sufficient signal charge over the entire lifetime of the detector, sufficient depletion depth with a substantial electric field in the depleted zone must be achieved and maintained during operation. In Section 9.3.1 the more mature large-FF approach is described, for which R&D has already been ongoing for more than five years, and in Section 9.3.2 small-FF R&D and development is described, a very promising approach that started in 2014/2015, relying on the experience of the ALICE experiment [122]. A summary of the devices that are part of these R&D and mentioned in this chapter is shown in Table 9.1.

Table 9.1: CMOS sensors involved in the latest ATLAS demonstrator R&D

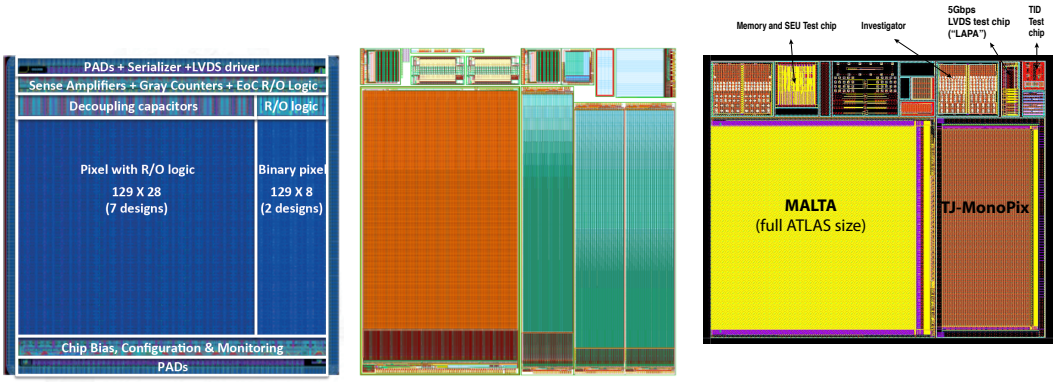
Device	Process	Design	Pixel size	Matrix size	Availability date
LF-CPIX	LFoundry 150 nm	Large-FF	50×250 μm^2	106×36	July 2016
LF-Monopix	LFoundry 150 nm	Large-FF	50×250 μm^2	129×36	July 2017
MuPix8	ams aH18	Large-FF	80×81 μm^2	200×128	October 2017
ATLASPIX_M2	ams aH18	Large-FF	50×60 μm^2	320×56	October 2017
ATLASPIX_Simple	ams aH18	Large-FF	40×130 μm^2	400×25	October 2017
Investigator	TowerJazz 180 nm	Small-FF	various		
MALTA	TowerJazz 180 nm	Small-FF	36.4×36.4 μm^2	512×512	January 2018
TJ-Monopix	TowerJazz 180 nm	Small-FF	36×40 μm^2	224×448	January 2018

9.3.1 Large Fill-Factor CMOS sensors

large-FF pixels have been implemented in HV/HR-CMOS technologies using a deep N-well acting as a collection diode in which further wells are embedded (triple or quadruple well technologies). The extra wells are used to shield PMOS and NMOS transistor nodes and their wells from the collection diode and the depleted bulk as illustrated in Figure 9.1(a). Taking advantage of further technology features, high resistivity wafers are used in the processing line and a high bias voltage (typically 100–300 V) can be applied to the substrate through top, edge or back biasing to generate a substantial depletion volume in the whole area covered by the pixel with a high electric field.

Different digital read-out architectures are being investigated using large-FF designs: a column-drain architecture, similar to the current ATLAS FE-I3 front-end chip, and a parallel pixel-to-buffer (PPtB) architecture. They have been implemented in LFoundry 150 nm and ams aH18 (180 nm) and aH35 (350 nm) technologies in order to evaluate their performance. Figure 9.3 is an overview of the submitted fully monolithic Pixel Detector chips including read-out architecture. During the prototyping phase to develop these chips pixel sizes of 50×250 μm^2 have been chosen in order to match the pitch of the FE-I4 chip [72] to allow it to be used as auxiliary read-out and to compare with the standard pixel size.

The LFoundry **LF-Monopix** [123] (Figure 9.3(a)) chip is 9.5×10 mm^2 large and contains 50×250 μm^2 sized pixels. The design inherits from an analog cell implemented in the LF-CPIX chip (9.5×10 mm^2) which was intensively characterized [124, 125] and optimized for rate capability. It contains a charge sensitive amplifier (CSA) with current feedback and an output stage with 4-bit threshold trimming and 7-bit configuration register. Analog information is obtained using 8-bit gray coded Time-over-Threshold (ToT). The digital read-out architecture is of column-drain type, where hits are buffered in the pixel cell and a "token" clock signal is passed from top of the column to the bottom through each pixel. If a pixel is hit, the pixel address is transferred to the column bus when the token passes by. The bunch crossing identifier (BCID) time-stamp is added for each hit and time-over-threshold is encoded using the 40 MHz bunch-crossing (BX) clock. Upon a trigger the hits are transmitted from the End-Of-Column (EoC) logic buffers off the sensor. The sensor guard ring



(a) (b) (c)

Figure 9.3: Large-FF prototypes: (a) LF-Monopix01 in LFoundry 150 nm containing a column drain and a PPtB read-out architecture; (b) ams aH18 180 nm containing the MUPIX8 chip for the Mu3e experiment and several variants of the ATLASPix chip including PPtB read-out. (c) Small-FF prototypes in TowerJazz technology: MALTA chip with asynchronous read-out, TJ-Monopix chip with column-drain read-out

structure has been especially optimized and special attention has been given to mitigate possible cross coupling of digital signals into the sensor, e.g. by using current steering logic, differential logic, and ground potential decoupling at critical nodes. The electronics is embedded in a deep n-well (see Figure 9.1(a)) manufactured on a high-resistivity substrate $> 2\,\mathrm{k\Omega\,cm}$ (usually p-type) 8" wafer. The unirradiated device can be biased up to 280 V. The sensor capacitance is about 400 fF.

The **ATLASPix** CMOS sensors (ams aH18, Figure 9.3(b)) are fabricated in combination with the Mu3e development [126, 127] using four different resistivities between $20\,\Omega\,\mathrm{cm}$ and $1\,\mathrm{k\Omega\,cm}$. In addition to the standard aH18 features, a deep p-well implant has been added that allows isolation of PMOS transistors from the deep n-well (see also Figure 9.1(a)). This has been used here for the first time in one of the matrix variants. The reticle contains three large chips: MuPix8 (pixel pitch $81 \times 80\ \mu\mathrm{m}^2$, 128×200 pixels, 10.24 mm $\times$ 16.2 mm), ATLASPIX_M2 ($60 \times 50\ \mu\mathrm{m}^2$, 56×320 pixels, 2.8 mm $\times$ 19.2 mm), and ATLASPIX_Simple ($130 \times 40\ \mu\mathrm{m}^2$, two times 25×400 pixels, 3.25 mm $\times$ 16 mm). Two types of read-out architecture are realized: column drain as described above (ATLASPIX_Simple) with physical separation of digital part and sensor, and parallel pixel to buffer read-out (PPtB, ATLASPIX_M2). Pixels contain amplifier and comparator. A trigger buffer receives the comparator outputs, generates hit information (address and time stamp) and keeps the information for the duration of the trigger delay.

In what follows we first show results obtained with prototype designs which do not yet including a full pixel read-out architecture but are nevertheless representative regarding the sensor technology. Then first preliminary results obtained from large ($> \mathrm{cm}^2$), fully

monolithic CMOS chips including complex read-out architecture(s) are given.

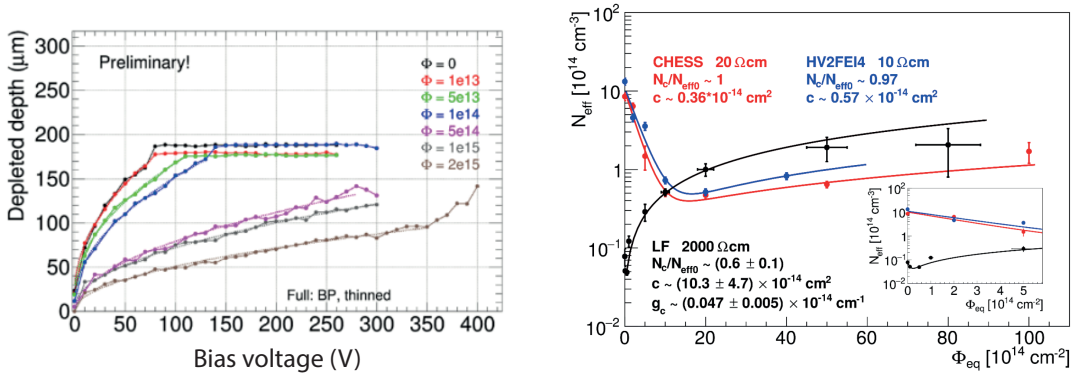
Prototype results for large fill factor designs

Before arriving at the monolithic designs introduced above a large series of prototype chips in ams and LFoundry technologies (but also in other technologies, see Section 9.1) have been fabricated in order to evaluate radiation hardness and other properties of large-FF designs and used technologies. These prototypes were made with 50×250 μm^2 as well as with 33×125 μm^2 pitches. The CMOS prototypes generally contained a one or two-stage preamplifier, a discriminator, threshold tuning and a large pad for coupling to the FE-I4 read-out chip, either capacitively (using a $< 1\,\mu$m glue layer) or by means of bump connections.

Prototype CMOS detectors as well as fully monolithic CMOS Pixel Detectors were characterized in test beams: at the CERN H8 SPS beamline with 180 GeV pions, at DESY with typically 4.5 GeV electrons, and at ELSA (Bonn) with typically 2.5 GeV electrons. For the measurements dedicated beam telescopes were used to define the incoming particle trajectories: FE-I4 telescope [128] at CERN (pixel granularity 50×250 μm^2, data rate up to 50 kHz and the MIMOSA telescope [129] (pixel granularity 18.4×18.4 μm^2, data rate up to 5 kHz) at Bonn and DESY.

Charge collection Signal responses of prototype devices have been measured in various test beams for different bias voltages. The measured charges in unirradiated devices correspond to depletion depths of up to 170 μm. The extracted substrate resistivities are in accordance with those specified by the vendors and can be as high as 3 kΩcm (LFoundry devices) demonstrating that an optimum resistivity can be chosen. With irradiation the change in effective doping concentration develops as shown in Figure 9.4(b), i.e. depending on initial resistivity. While the depleted volume shapes after irradiation are more complex in detail, grosso modo the signal charge changes inversely proportional to $\sqrt{N_{eff}}$, coming to about the same value around 10^{15} n_{eq}/cm^2. Below this fluence the signal for low resistivity starting material is small but increasing, whereas for high resistivity material is starts large but decreases. After 10^{15} n_{eq}/cm^2 N_{eff} roughly remains constant at $10^{14}/cm^3$ within error bars.

TID tolerance An evaluation of the performance of the CMOS electronics implemented in ams and LFoundry prototypes when exposed to ionizing radiation has been performed using X-ray irradiations to doses of 100 Mrad and above. Gain and noise of the front-ends were measured during irradiation in order to characterize the performance during the lifetime of a CMOS detector. All measurements show a degradation of less than 30% in gain up to 100 Mrad, and about 10-20% increase in noise, well tolerable in an environment as for ITk Layer 4.



(a) (b)

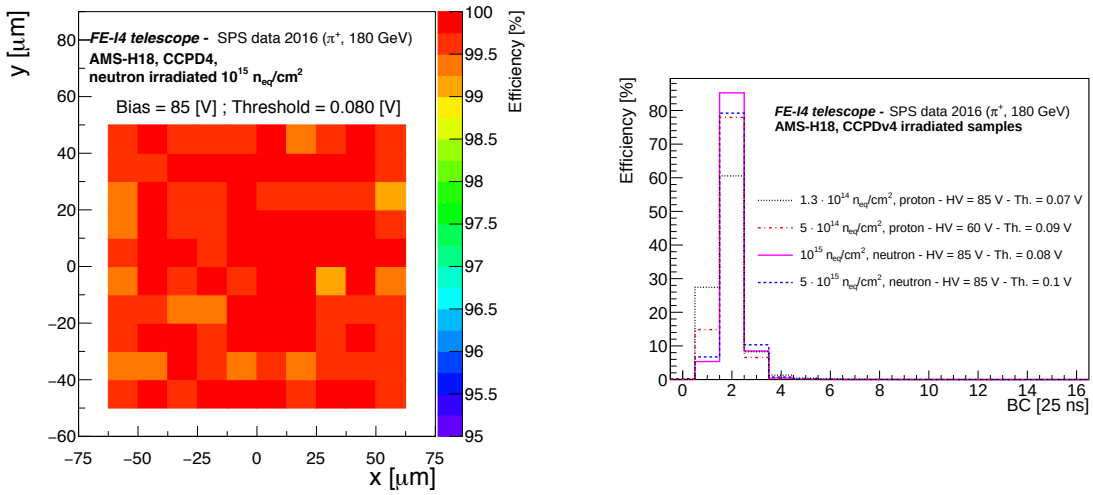
Figure 9.4: Edge TCT measurements on large-FF devices [132]: (a) Depletion depth as a function of bias voltage for different radiation fluences (neutrons) up to 2×10^{15} n_{eq}/cm^2 (LFoundry diodes with about 3-5 kΩ cm resistivity, thinned to about 200 μm, backside biasing (BP), leading to the plateauing of the curves at lower fluence); (b) effective doping concentration as a function of fluence for different substrate start resistivities, measured on bulk resistivities chosen for ams devices (red and blue) and for LFoundry devices (black).

Tolerance with respect to non-ionizing radiation Prototype active pixel sensors with FE-I4 read-out and some full monolithic CMOS sensors have been irradiated to ITk fluences using neutrons and/or protons. They have been characterized [130, 131] with MIP-like ^{90}Sr electrons and with 60 keV X-rays from ^{241}Am and ^{55}Fe (5.9 keV) X-rays before and after neutron (nuclear reactor) or proton (in the 18 MeV–24 GeV energy range) irradiation to about 10^{15} n_{eq}/cm^2.

In order to evaluate the evolution of the depletion region with fluence, edge-TCT measurements were performed on dedicated test structures placed on the prototypes. The structures were irradiated with neutrons and/or 24-GeV protons and characterized by edge-TCT with increasing radiation fluence.

Figure 9.4 summarises the results obtained for large-FF sensors having 10 Ω cm (ams), 20 Ω cm (ams), and 2 kΩ cm (LFoundry) substrate resistivity, respectively. Figure 9.4(a) shows that large depletion depths of more than 50 μm are maintained up to the fluences of 1×10^{15} n_{eq}/cm^2. In high-resistivity p-type substrates (here LFoundry) as in Figure 9.4(a), the depletion region steadily decreases with increasing fluence as is known from standard planar pixel sensors.

In low resistivity substrates (shown in Figure 9.4(b)), initial acceptor removal dominates the behavior at fluences below 10^{15} n_{eq}/cm^2, i.e. the depletion depth first increases and then decreases with fluence. A detailed study of this effect is ongoing comparing several intermediate substrate resistivities on ams prototypes. Furthermore, irradiation effects after same fluence using (a) neutrons and (b) protons (24 GeV) were not identical. Irradiation



(a) (b)

Figure 9.5: (a) In-pixel MIP detection efficiency measured for an ams aH18 prototype after 1×10^{15} n_{eq}/cm^2 and 100 Mrad (18 MeV protons, Bern). (b) efficiency distribution in time bins of 25 ns for different radiation levels.

with protons (and likely also pions) further enhance the acceptor removal mechanism compared to neutron irradiation [133].

The evolution of the effective doping concentration N_{eff}, starting from an initial value (initial substrate resistivity), as a function of fluence is shown in Figure 9.4(b). The plot shows that after fluences of 10^{15} n_{eq}/cm^2 N_{eff} becomes of order $10^{14}/cm^3$ independent of the initial substrate resistivity. The evolution of the depletion volume can be estimated from this. In all cases, however, the depletion region is sufficiently large to maintain good detection efficiency during the lifetime of the detector provided that the implemented electronics operates at sufficiently low thresholds.

Detection Efficiency Matrix as well as in-pixel MIP-efficiencies have been measured for prototypes (ams aH18 CCPD-V4) irradiated with neutrons to 1×10^{15} n_{eq}/cm^2 and 5×10^{15} n_{eq}/cm^2, with protons to 1.3×10^{14} n_{eq}/cm^2 and 5×10^{14} n_{eq}/cm^2, respectively. Good uniformity is observed across the matrix (not shown) and within the pixel cell (Figure 9.5(a)). The average efficiency is 99.7%. The sensors can be operated at high efficiency up to doses of 5×10^{15} n_{eq}/cm^2 at moderate voltages. Evidence of charge multiplication is observed at the highest damage level and highest bias. LFoundry prototype efficiencies were measured at 99.5±0.1% (unirradiated) with excellent homogeneity over a large matrix with only about 0.3% spread.

Time response The time response of CMOS CCPD pixel sensors has been measured for assemblies bonded to the FE-I4 read-out chip. Figure 9.5(b) shows the measured time stamp distributions for irradiation fluences of up to 5×10^{15} n_{eq}/cm^2. The spread of the distribution is caused mainly by the jitter of the clock distribution system of the read-out, as explained in [134]. The time stamps hence largely accumulate in one 25 ns bin as required for operation at HL-LHC (see also [135]). There is no evidence so far that the in-time requirements at the ITk cannot be met with proper tuning of input capacitance and power (i.e. transconductance g_m).

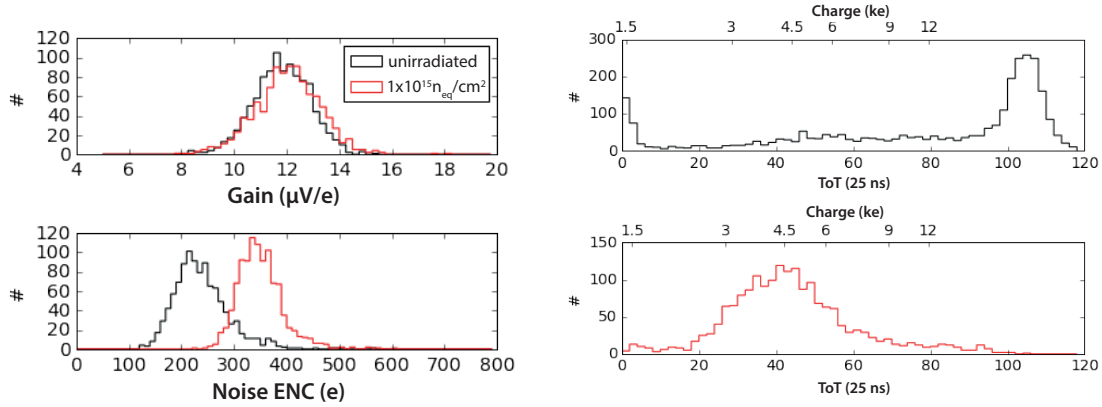
Thermal performance While no detailed temperature studies have been performed yet, one can qualitatively say that radiation damage in CMOS sensors is not any different than in standard pixel sensors. The leakage current is proportional to the volume under the electrode and thermal runaway depends on how much power ($I_{leak} \times V_{bias}$) is dissipated. For high resistivity CMOS ($>$ kΩ cm) order of 100 μm depletion depth is obtained with not too high voltage (around 100–200 V). Therefore CMOS sensors should not perform any worse thermally than standard sensors, if not better. Operation experience in terms of cooling (e.g. using dry ice) have qualitatively confirmed that similar thermal behavior can be assumed.

Results from large fill-factor monolithic pixel matrices

The fully monolithic, large pixel chips shown in Figure 9.3 that include a complete read-out architecture as explained on page 217 were designed and fabricated to demonstrate that depleted monolithic CMOS pixels can integrate architectures that meet the ITk demands in terms of rate (and radiation) at the outer layers. The expected rates roughly correspond to those rates seen by the B-layer in current ATLAS today.

Compromises in the designs have been made, for example by still holding to larger pixel sizes than the 50×50 μm^2 baseline for the ITk. This was done to be able to benefit from preceding prototype designs that had 50×250 μm^2 or 33×125 μm^2 pitches in order to map to the FE-I4 footprint. Correspondingly and with the addition of the relatively large pwell/nwell capacitance in large-FF designs the total input capacitances are substantially larger than in an optimized 50×50 μm^2 design.

LF-Monopix The fully monolithic chip LF-Monopix in LFoundry 150 nm technology has been described on page 217. The chip with area of about 1 cm^2 has been tested before and after irradiation to 1×10^{15} n_{eq}/cm^2 fluence in test beams at CERN (H8, 180 GeV pions) and at ELSA (Bonn, 2.5 GeV electrons) using a 6-plane Mimosa telescope with better than 5 μm spatial resolution per plane and data taking rate of 10 kHz. The breakdown voltage is larger than 260 V before and larger than 300 V after irradiation (it was not tested up to



(a) (b)

Figure 9.6: Performance of the fully monolithic LF-Monopix before and after irradiation (a) gain and noise distributions (measured by charge injection), (b) charge collection measured in test beam on unirradiated (top) and irradiated (bottom) sensors. The signal calibrated in units of e^- is given on the top of the x-axis. Note that the ToT calibration is not linear.

breakdown). TID up to 100 Mrad did not show any significant degradation of the electronics. Note that the tested devices were still 750 μm thick and the bias is applied from the top side. Thinning and backside biasing improves charge collection substantially as demonstrated with prototypes. The main results on LF-Monopix can be summarized as follows.

- The chip was tested and works well at clock frequencies of 40 MHz also after irradiation. The output is designed for 160 MHz. Read-out and threshold tuning works to below 2000 e^-. Noise averages are around 200 e^- before and 350 e^- after irradiation which are excellent values for an estimated capacitance of about 400 fF. Figure 9.6(a) shows the gain and noise distributions before and after irradiation.

- The depletion depth (at V_{bias} = 200 V) is large resulting in a large signal of about 18000 e^-. After a fluence of 1×10^{15} n_{eq}/cm^2 it still is as large as 4500 e^-, even though (for technical reasons) only 130 V could be applied. Figure 9.6(b) shows the signal measured for 2.5 GeV electrons before irradiation and after 1×10^{15} n_{eq}/cm^2.

- The mitigation measures implemented to suppress cross coupling of transient digital signals into the sensor via the pwell/nwell capacitance have been shown to do their job such that the chip can be operated properly during data taking.

- The efficiency is above 99.5% before (at 200 V bias, shown in Fig. 9.7(a)) and about 99% after 1×10^{15} n_{eq}/cm^2 at (only) 130 V bias (Fig. 9.7(b)) and should be even better with thinned devices and backside biasing.

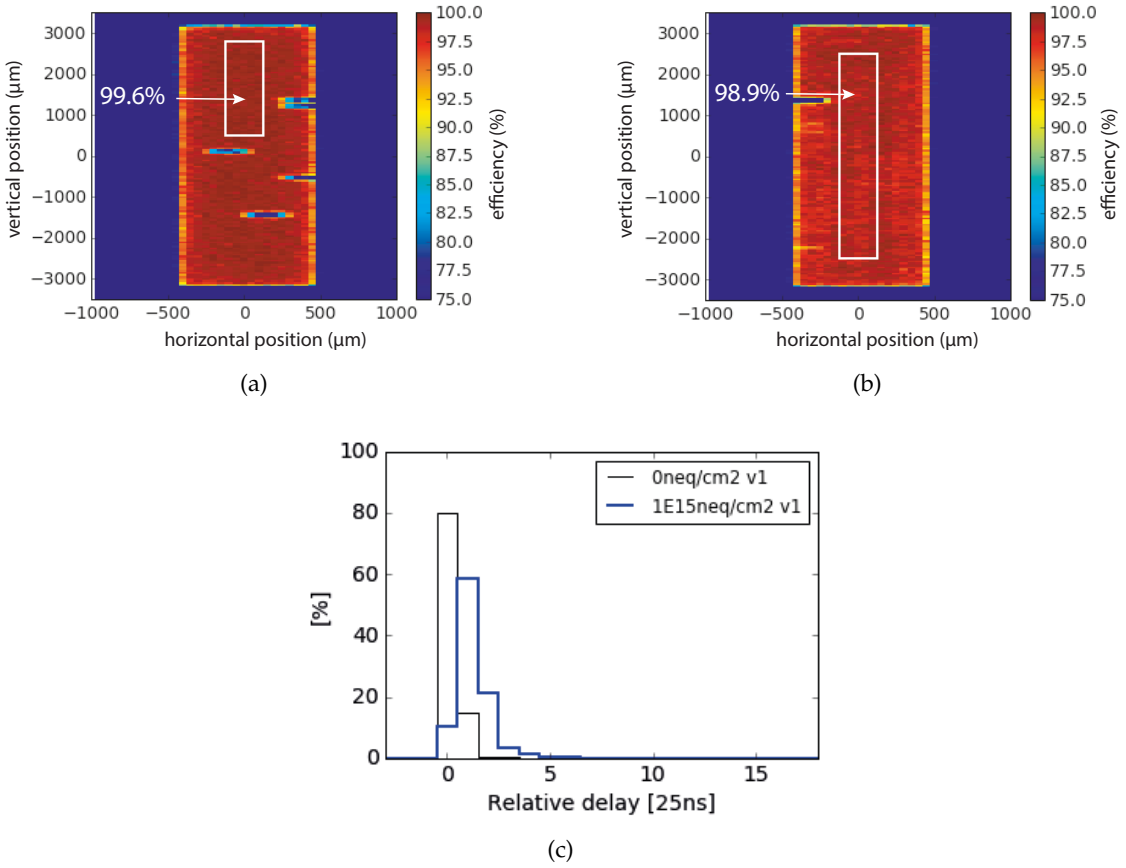


Figure 9.7: Detection efficiency comparison of LF-Monopix (a) before (bias -200 V) and (b) after (bias -130 V) neutron irradiation to 1×10^{15} n_{eq}/cm^2. (c) Distribution of the time difference of pixel signals and the signal of the reference trigger scintillator before and after irradiation. Distribution of the time difference of pixel signals and the signal of the reference trigger scintillator before irradiation (black histogram) and after 1×10^{15} n_{eq}/cm^2 (blue histogram). The signals are "in time" if they appear within two bins.
Note that for technical reasons not related to the sensor the bias voltage after irradiation was limited to 130 V and no thinning and backside biasing has as yet been applied.

- The timing performance has been characterized by plotting the time difference between a scintillator reference signal and the time mark of the pixel pulses (Fig. 9.7(c)). Since the absolute position of the scintillator signal relative to the 40 MHz clock edge is random a pixel signal is "in time" within the 25 ns time difference between two bunch crossings if it appears within two 25 ns bins. This is the case to 98% before irradiation and to 80% after irradiation. This is a remarkable result given the large capacitance and non yet optimized tuning. For a pitch of 50×50 μm^2 the capacitances are expected to be below 100 fF such that the in-time efficiency meets the requirements also after irradiation.

ATLASPix The fully monolithic chip ATLASPix in ams aH18 technology was tested in the CERN SPS test beam with 180 GeV pions in October 2017 using the FE-I4 telescope [128] and the CLIC Timepix3 telescope [136] and at DESY with 5 GeV electrons in November 2017 using the MuPix telescope [137] equipped with MuPix8 reference planes. In all campaigns an un-irradiated ATLASPix with standard thickness (600 μm) and substrate resistivity of 80 Ωcm was tested. With an early-prototype read-out system and at a bias voltage of 65 V a global efficiency of 99.5%, defined as the ratio of tracks detected versus reconstructed in the acceptance of the detector in a 100 ns time window from trigger, was measured at CERN SPS. This setup hat a limited read-out speed of 200 Mb/s, corresponding to a timing clock frequency of 10 MHz. The operation clock frequency in the DESY testbeam was 125 MHz. The global efficiency at 60 V bias was measured to be 98.6%. Only little charge sharing with an average cluster multiplicity $<$ 1.04 was observed. The efficiency as a function of the operational threshold is shown in demonstrating that a large range of operation thresholds with high efficiency are possible.

The spatial resolution of ATLASpix was mapped with the high energy CERN testbeam and found to be compatible with the pixel pitch as illustrated in Fig. 9.8(a). Good in-pixel uniformity of the efficiency is shown in Figure 9.8(b). The efficiency as a function of the operational threshold is shown in Fig. 9.8(c), demonstrating that a large range of operation thresholds with high efficiency are possible. The timing resolution measured at CERN with the slow read-out system is presented in Fig. 9.8(d) and found to be consistent with the used 100 ns sampling.

The radiation tolerance of the ATLASpix has not yet been studied. However, a detailed characterization study of p- and n-irradiated Mupix7 sensors, a small scale predecessor of ATLASpix, was performed [138] with the aim to investigate the radiation hardness of the design including data serialisation, data transmission at 1.25 Gbit/s and the on-chip PLL. All irradiated MuPix7 were fully operational after irradiation with neutrons up to $5.0 \cdot 10^{15} \mathrm{n}_{eq}/\mathrm{cm}^2$ and protons up to $7.8 \cdot 10^{15}$protons/cm^2, i.e. to multiples of the expected fluences at L4. Despite the small depletion depth provided by the low-ohmic substrate (10-20 Ω cm), the hit efficiency degraded only somewhat to values around 93% [138] for fluences up to $1.5 \cdot 10^{15}$protons/cm^2 measured at a noise occupancy of 5×10^{-6} at a temperature of 10°C.

9.3.2 Small Fill-Factor CMOS sensors

As outlined in Section 9.1 a small-FF design approach (see Figure 9.1) offers many benefits inherent from a small ($\mathcal{O}$(10 fF)) input capacitance, in particular in terms of power, timing, and noise, and also spatially separates the charge collecting node from the electronics area, hence reducing transient coupling from digital to sensor compared to large-FF designs. At first, it was believed that the radiation demands at HL-LHC would render fast drift of electrons over comparatively large distances impossible. Building on the developments within ALICE-ITS [122] and introducing improvements in design and technology features,

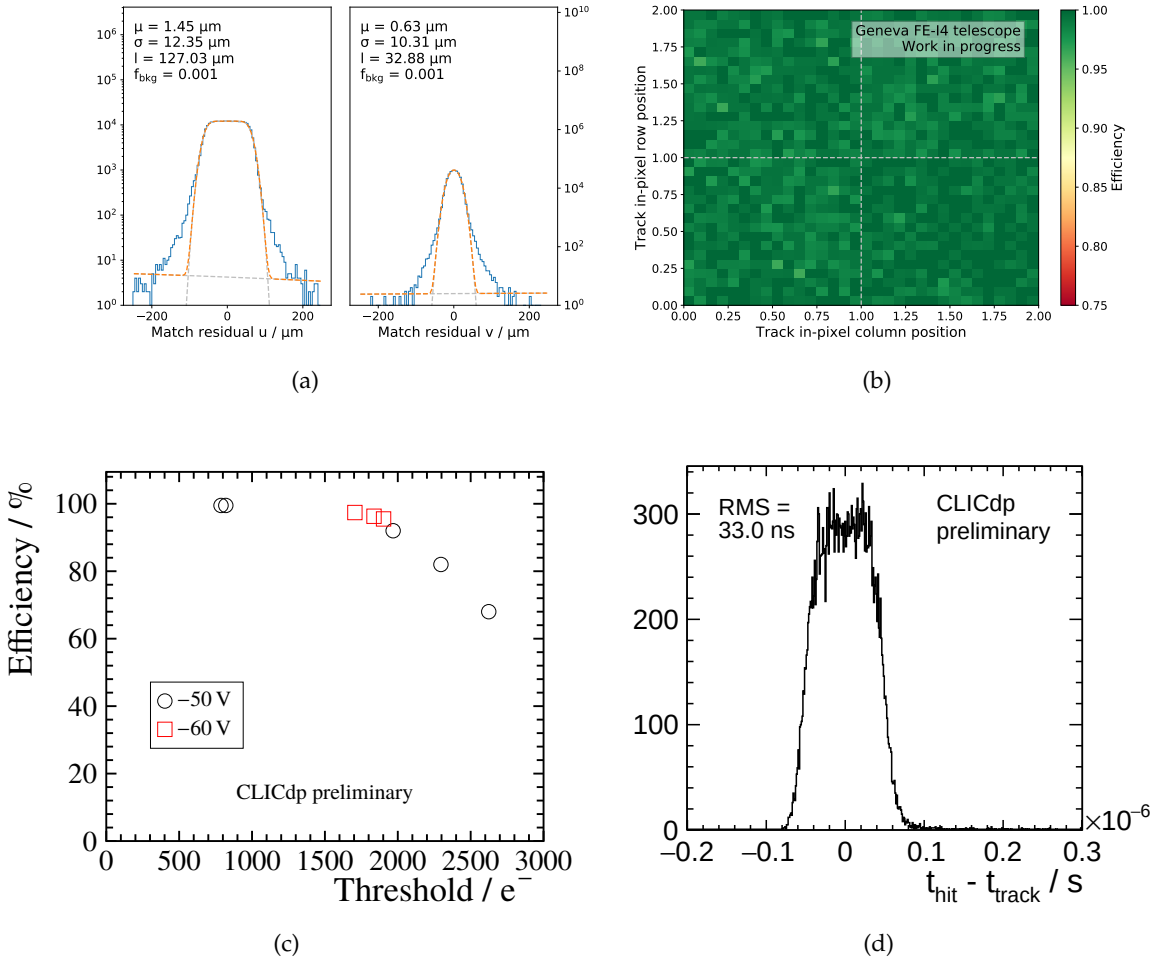
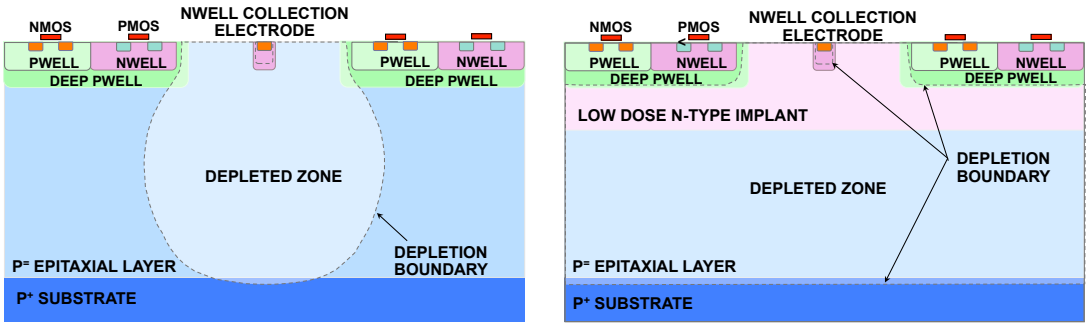


Figure 9.8: (a) Unbiased residuals for the ATLASPix monolithic detector (un-irradiated), for a pixel size of 40×130 μm^2; (b) In-pixel MIP detection efficiency map with average values of $\epsilon = 99.5\%$ for V_{bias} = 65 V, V_{thresh} = 0.845 V, 10 MHz clock and $\epsilon = 98.6\%$ for V_{bias} = 60 V, V_{thresh} = 0.845 V, 125 MHz clock (see text); (c) Efficiency versus operational threshold; (d) timing distribution of hits as measured in ATLASPix versus time measured in the telescope. The granularity of the ATLASPix is limited to 100 ns due to the read-out, while the telescope provides timestamps with 1.6 ns accuracy.



(a) (b)

Figure 9.9: Small-FF cell in TJ180 technology (p-type epi-silicon and p-substrate): (a) ALICE ITS cell cross section with n-well charge collection node; (b) new TJ180 cell with process modification to provide better depletion and improve charge collection from all regions.

rendered a dedicated effort worthwhile. It started in 2014/15 resting on the TowerJazz 180 nm CMOS technology featuring a 25 μm thick Si epitaxial layer (as in ALICE ITS), but with a technology add-on to enhance fast charge collection by drift. The technology modification was first tested using an "investigator" chip [139].

The TJ180 cell as used in ALICE-ITS is shown in Figure 9.9(a). A small collection diode is placed outside of the deep p-well hosting the CMOS electronics. The geometrical size of the diode limits the depletion that can be achieved laterally for a given bias voltage. Especially at the pixel edges undepleted regions result in significant charge loss after irradiation. Vertically, the depletion zone is constrained by the thickness of the epi-layer (25 μm). Hence - cell-size dependent - the deposited charge is only in part collected by drift, a non-negligible fraction being collected by (slow) diffusion. Therefore, apart from radiation softness, the ALICE-ITS cell design is not suitable for ATLAS also for reasons of rate capability.

With a technology modification [140, 139] (planar deep n^--p junction to increase depletion over the full epi-layer, Figure 9.9(b)) and cell geometry optimization (cell size and collection node geometry) the small-FF approach has been looked at again in a TJ 180 submission in September 2017 including two large designs (see Figure 9.3(c)):

- Asynchronous read-out scheme (Monolithic ALice to ATLAS, or "MALTA")
- Synchronous read-out scheme ("TJMonopix")

The process modification does not require layout changes with respect to the standard process, yet it has significant influence on the charge collection as will be presented in the following sections. The two TJ180 designs include the full analog front-end and all pixel digital logic for asynchronous and synchronous read-out in pixel pitches of approximately 36 μm to 40 μm.

A new asynchronous read-out architecture is used in MALTA. It avoids excessive clock activity and hence further reduces transient coupling into the active matrix region. In addition its power consumption is low compared to clocked read-out. Address, time stamp and charge information of every hit is encoded in the asynchronous signals propagated through a column bus to the periphery where decoding is performed. The decoded information is buffered and then transmitted off the matrix. The synchronous design in TJ-MonoPix is based on the column drain architecture similar to the present ATLAS Pixel Detector (FE-I3) as described for LF-Monopix in Section 9.3.1 on page 9.3.1. In both architectures the End-Of-Column (EoC) logic buffers all hits on the sensor and transmits the hits off the sensor.

MALTA and TJ-MonoPix share the same analog front-end designs which target low noise and low power consumption. The analog front-end (FE) includes a charge sensitive amplifier followed by a discriminator and hit buffer. The n-well collection electrode is kept geometrically small with capacitances between 3 fF and 10 fF. A total current consumption of significantly less than 50 mA/cm^2 is expected for both designs, noise is predicted to be approximately 8 e^- (at 500 nA), time-walk of less than 20 ns, and a threshold dispersion $< 12\ e^-$ at a targeted in-time threshold of approximately 300 e^-. Amplitude measurement is provided by either 6-bit ToT (MonoPix) or "bunch-crossing time to hit-signal leading-edge" encoding (MALTA).

Prototype sensor results for small fill factor designs

The process modification for small-FF monolithic CMOS matrices has been tested by means of a prototype chip[3] ("Investigator"), featuring different 8×8 submatrix variants (different geometries of cell and collection node), which were included as test structures for an ALICE ITS submission [141, 78, 142]. The wafers have been thinned to 100 μm. The prototype sensor's amplitude spectrum and rise-time distributions are measured in test beams and source tests by recording single pulse waveforms with typical thresholds of approximately 100 e^-. The size of the depletion zone depends on the collection n-well size and the spacing between collection n-well and deep p-well, as well as the epitaxial layer thickness. The pixel pitch for MALTA and TJ-Monopix is 36.4 μm, which is simulated as the optimal choice as a compromise between radiation hardness and small capacitance, spatial resolution and logic area.

Charge collection (small-FF) Signal response measurements to ^{55}Fe and to ^{90}Sr using unirradiated samples show nearly identical distributions for the modified process as before modification. The gain is lower than before modification due to a larger input capacitance (by 30%). The response to ^{90}Sr after irradiation is shown in Figure 9.10 (a) demonstrating an excellent signal response even after 1×10^{15} n_{eq}/cm^2, much in contrast to a sensor in the

[3] The Investigator chip is a chip without read-out architecture, submitted to address particularly the process modification.

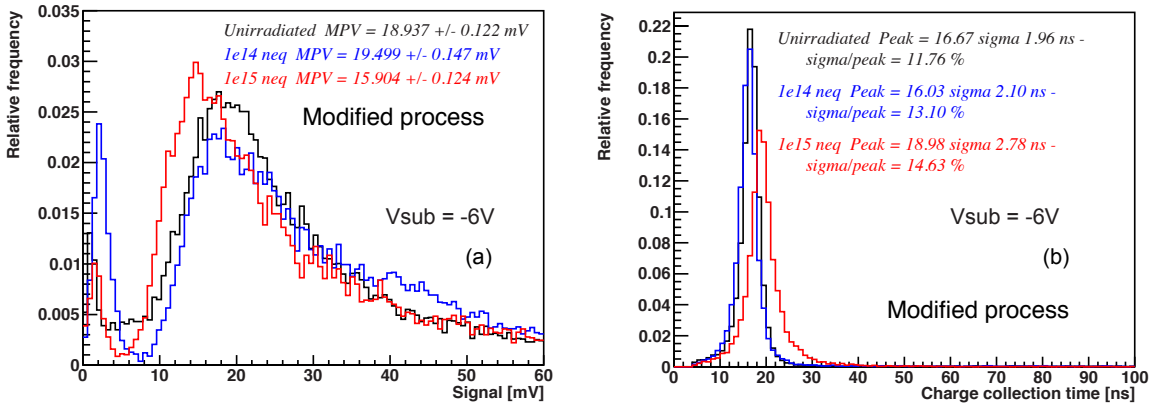


Figure 9.10: Signal response of 50×50 μm^2 pixel pitch produced in the modified process before irradiation (black curves), after 10^{14} n_{eq}/cm^2 (blue curve) and after 10^{15} n_{eq}/cm^2 (red curve). Figure (a) shows the amplitude distribution for ^{90}Sr source tests and plot (b) the signal collection time.

standard process after this irradiation fluence. The slight amplitude decrease vanishes after re-calibration.

Timing Already in unirradiated devices, the collection rise-time distributions a substantially different behaviour in comparison to the standard process is observed. While the mean collection times are similar for standard and modified process, the width of the distribution decreases substantially from 4.6 ns in the standard to 1.9 ns in the modified process. The undepleted volumes are significantly reduced and so are the contributions from slow diffusion signals. A more uniform charge collection is achieved, in particular in the volume under the p-well, by suppressing slower diffusion signals for the benefit of faster drift signals.

Figure 9.10(b) shows the rise-time of the output voltage signal. The comparison before and after irradiation shows that the fast signal response is maintained after a fluence of 10^{15} n_{eq}/cm^2. Only a small increase in the mean collection time and in the spread is observed. The time spread after 10^{15} n_{eq}/cm^2 is still significantly smaller than for the unirradiated sensor of the standard process (4.6 ns).

NIEL characterizations by eTCT measurements Edge-TCT measurements are used to map out the charge collection uniformity across the pixel depth. The depth of the charge collection was found to reach 25 μm to 30 μm which matches well to the thickness of the epitaxial layer. For both pitches the charge collection is uniform to within 10% .

Test beam results Test beam measurements were employed to study the cluster size for several pitches and irradiation levels: unirradiated 50×50 μm^2, as well as 25×25 μm^2 and 30×30 μm^2 after 10^{15} n_{eq}/cm^2. While single-pixel clusters dominate the response of the 50×50 μm^2 CMOS sensors (mean 1.06), we find approximately 30% of double-pixel clusters for the 25×25 μm^2 and 30×30 μm^2 sensors (mean values are 1.35 and 1.37, respectively). In addition to the pixel pitch, the cluster width is influenced by the spacing between n-well and p-well. The 50×50 μm^2 CMOS sensors has a very large spacing between DPW and DNW of 18 μm, whereas the 25×25 μm^2 and 30×30 μm^2 sensors have only a spacing of 3 μm. In our measurements there are no significant difference in cluster width distribution for 25×25 μm^2 and 30×30 μm^2.

The acceptance corrected hit efficiency is shown in Figure 9.11 for the unirradiated 50×50 μm^2 pixel sensor across a 4-pixel area (a) and as projection onto the y-axis (b). The efficiency is uniform across the pixel area with 98.5% $\pm$ 0.5% (stat) $\pm$ 0.5% (syst) average value. It is slightly below 100% due to higher than usual threshold (approximately 600 e^-) which was necessary to suppress common mode noise (pick-up) in the test beam setup during the measurements. The same measurements are shown in Figure 9.11(c),(d) for the 25×25 μm^2 "Investigator", irradiated to 10^{15} n_{eq}/cm^2. The efficiency measured is uniform across the detector to 98.5% $\pm$1.5% (stat) $\pm$ 1.2% (syst) for 25×25 μm^2 pixels, and 97.4% $\pm$1.5% (stat) $\pm$ 0.6% (syst) for the sensor with 30×30 μm^2 pixels. These results demonstrate the substantial improvement of radiation hardness achieved through the process modification with a planar n-doping layer.

9.4 Towards a CMOS Pixel Module and Stave

The CMOS "Drop-in" module concept aims to replace the baseline hybrid pixel modules with CMOS pixel modules while remaining compatible with the electrical, mechanical, and cooling environment of the ITk Pixel Detector. The dimension of the reticle for the foreseen CMOS technologies can reach 20×26 mm^2. The CMOS module will be composed of individually diced chips. However, we aim keeping the dimensions compatible with hybrid quad modules where the chip active area is defined as 19.2×20 mm^2. We specify the inactive gap to 200 μm excluding the physical gap (150 μm). This defines the width of the module to 40.95 mm. For the height, we need to include the periphery of the CMOS sensor which will occupy as much as 10% of the area. Therefore, we can estimate the height to 42.79 mm. It is still to be determined how close together the chips can be placed. 50 μm might be achievable with the proper assembly mechanics. The periphery is located on one side along the beam axis. The inactive chip edge circuitry shall not exceed 200 μm on buttable sides to minimise dead area. The final choice on the in-active gap size is contingent on acceptance simulations. At higher eta, for instance, significantly larger inactive gaps can be tolerated.

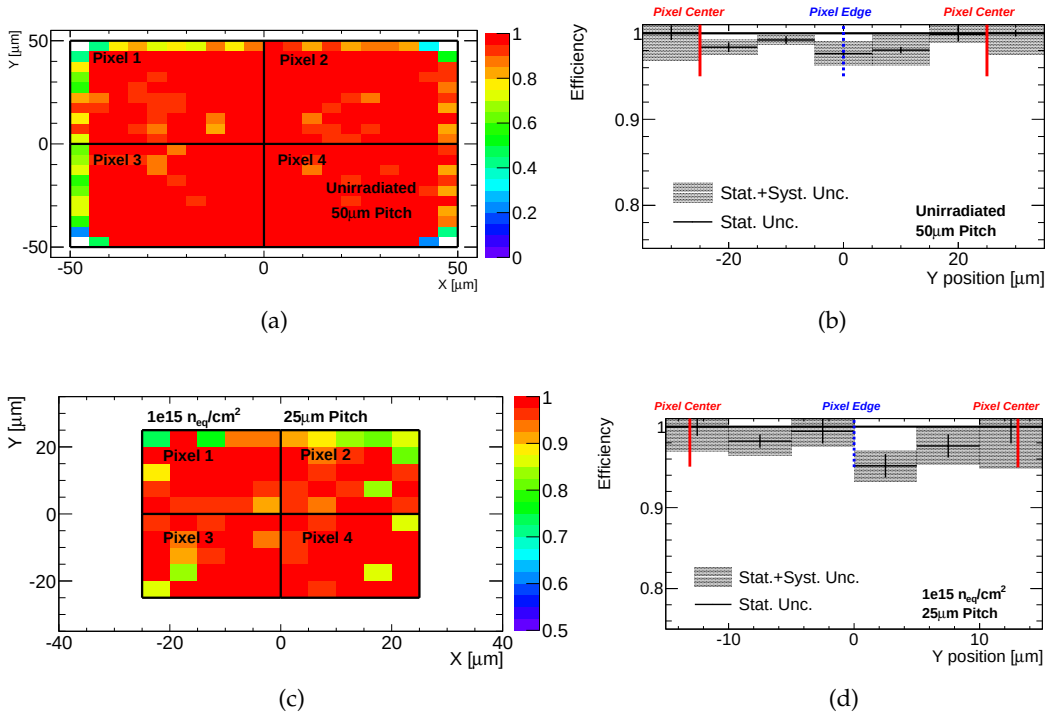


Figure 9.11: (a) Detection efficiency as function of hit position for an unirradiated modified process 50×50 μm^2 pixel sensor with 3 μm electrode and 18.5 μm spacing. (b) Efficiency projection between the pixel centers in Y direction as shown in graph. (c), (d) same measurements for an irradiated investigator matrix (10^{15} n_{eq}/cm^2) with pixel pitch 25×25 μm^2.

The data of four sensors are interfaced to the ITk read-out and TTC chain using a "Multi-Chip-Controller" (MCC) which serves as data aggregator and control interface. This data aggregation will happen in the "active-cable" design on the PP0 board at the end of the Layer 4 stave, approximately 1 m away from the module. Signals from each CMOS sensor are transmitted as LVDS signals at 1.28 GHz from CMOS sensor to the aggregator ion PP0.

The data provided by the CMOS sensor include pixel hit addresses and any required TTC info (e.g. BCID). Current designs of CMOS sensors also include analog information in the hit data. The ITk read-out and control is passed from MCC to CMOS sensors. The detailed sharing of functionality between MCC and CMOS sensors is currently under study. The small-FF and large-FF designs will implement the necessary periphery blocks required to interface to the data concentrator / MCC chip planned for the outer layers of ITk pixels. The specifications used for the design of the CMOS interface are based on preliminary considerations using lpGBTx specifications.

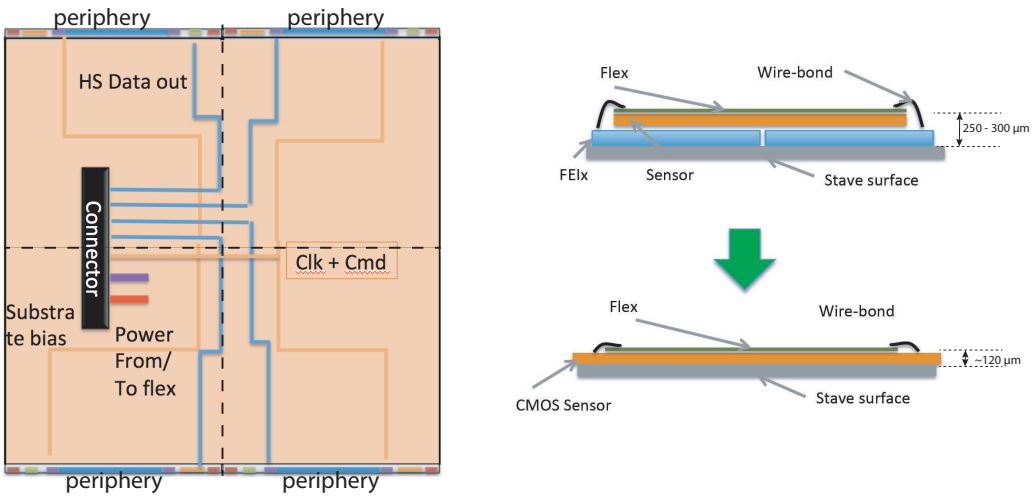


Figure 9.12: Schematic view of the ATLAS CMOS-1 sensor layout (a). The CMOS sensor includes the 19.2×20 mm^2 active pixel matrix as well as a dedicated periphery which interfaces to the MCC. Implementation of the CMOS module is shown in sketch (b) in comparison to the hybrid pixel module.

9.4.1 ATLAS CMOS-1 sensor design and periphery

Based on the established requirements and specifications for the CMOS sensors [143] we have established the design parameters and interfaces to be used for the integration of the CMOS sensors/modules to the ITk read-out and powering architecture. The CMOS sensor will include a 19.2×20 mm^2 active pixel matrix as well as a dedicated periphery which interfaces to the MCC. The MCC in turn will interface to the ITk read-out and powering on staves. A sketch of the CMOS-1 module is shown in Figure 9.12 as top view and from the side. Note that the thickness of the module itself will be less than half of that of a hybrid module due to the obsolete read-out chip for the CMOS module and the somewhat thicker sensor required for bump bonding of a hybrid pixel module (Figure 9.12(b)).

In the active matrix each pixel will contain the charge-sensitive amplifier, hit discriminator and buffer using either a small-FF or a large-FF design for the pixel layout geometry. The matrix read-out will be organised in double columns which transmit the data from a pixel to the End-of-Column logic (EoC). The EoC block will encode pixel address and hit timing information together with additional ATLAS information on trigger and BC-timing. Hit information will be stored in periphery memories large enough to store the information until the read-out-trigger is received. Upon a trigger signal the requested hit information will be transmitted via a serialiser and LVDS driver to the data aggregator chip, where it will be merged with the information of the other CMOS sensors. While the previous section described the active matrix, this section will introduce the required periphery block

in order to interface to the ITk read-out and powering and the steps towards the realisation of a drop-in CMOS module.

The hit memory will be dimensioned to accommodate all hit information for a latency up to 10 μs [4] for Layer 4. The needed space on chip estimated for the hit memory is in the order of 2-3 mm^2 at hits rates expected for the outer layers. This area can be accommodated on-chip within the present 150-180 nm technologies. The memory, formatter and serialiser, which drives the data from memory to LVDS output will be driven through the 640 MHz/1.28GHz clock generated by a PLL on the CMOS sensor or received from the lpGBTx chip if found to be electrically advisable.

The CMOS sensor will be powered by a serial powering chain. Dedicated Shunt-LDO regulators are hence needed in the CMOS sensor or on an external "power chip".

The configuration required to operate the CMOS sensor will be loaded through a serial link to the aggregator chip where clock and data are forwarded from PP0 to CMOS sensors. Present CMOS sensor designs already include slow-control logic in the periphery which takes care of storing and loading the configuration. The configuration values are stored "permanently". Hence the registers to be used to store the values are SEU hardened through triplicated logic. The configuration line also transmits trigger and timing information as well as reset signals.

9.4.2 Demonstration of CMOS technology for module design

As described in Section 9.4.1, modules based on the monolithic CMOS-1 sensor need to demonstrate to be able to cope with the ATLAS trigger and DAQ scheme, integrating all required functionality in their periphery. They must also be integrated into the ITk services, in particular serial powering and loading into the local support. This translated in the previously mentioned drop-in module concept, i.e. that the monolithic CMOS module should be completely compatible with the baseline services and mechanics. A plan to achieve this compatibility has been developed. The steps towards drop-in CMOS modules for ITk outer layers can be divided into several milestones:

- Design and characterisation of periphery blocks for radiation hardness and SEU tolerance.
- Mechanical prototypes with four dies and flex circuit within specifications.
- Electrical prototypes with flex and dies for read-out and operation of the sensors.
- Prototypes with flex and dies containing regulators for serial powering tests.

[4] see ITk pixel trigger and read-out baseline system

- Full drop-in ready prototypes including serial powering using CMOS-1 sensors. Full drop-in modules may also be implemented in a demonstrator/systemtest setup using the prototypes of the PP0 boards with data aggregation.

Periphery and utility blocks, such as DAC, RAM cells for pixel configuration, sLDO, command decoder and trigger buffer interface are currently in production or in the design phase. These blocks will be tested for radiation hardness and for general functionalities for later integration in the CMOS-1 sensors. These circuits will constitute the building blocks for a drop-in solution using CMOS sensors.

The first electrical and mechanical prototypes will be assembled using manual alignment jigs or pick-and-place machines available in the collaborating institutes. The goal of this exercise will be to demonstrate that the mechanical and electrical requirements detailed in the specification document [143] are met, in terms of placement accuracy, mechanical stability and electromagnetic compatibility of the flex circuit with the CMOS sensors. The following prototypes will closely follow the development of the modules for outer layers using ITk baseline sensors. These later prototypes will demonstrate the drop-in capabilities of the CMOS modules by demonstrating the compatibility with the baseline serial powering chain and the communication protocols foreseen for ITk, in terms of data and trigger rate, operability, power consumption and reliability.

The main differences between the drop-in CMOS module and baseline hybrid pixel modules, are that the module flex has also a structural mechanical function, connecting the four sensors, that the local regulation need to provide a 1.8 V supply, instead of 1.5 V used by the 65 nm technology and that for large-FF approaches high-voltage insulation is required between the sensor backside and the local support. On the other side, the smaller foreseen power consumption of the CMOS sensors will make them readily interchangeable with planar modules in terms of cooling and power distribution when integrated into staves.

The CMOS-1 module prototype will also allow evaluating the production process for the CMOS sensor and establishing a standardised procedure for large-scale production. The assembly of CMOS modules will not require the use of bump-bonding, which is a bottleneck in the production of standard hybrid pixel modules. In addition, the production yield will be increased because it suffers only the chip yield and not the corresponding bare module yields for read-out chip, sensor and hybridization steps. The production capabilities of CMOS foundries allow for quick sensor delivery in comparison to the production of standard planar and 3D sensors, for a fraction of the cost. The combination of these factors makes CMOS module an attractive option in terms of gain in production time and cost.

9.5 CMOS-pixel deployment plan for ATLAS ITk

During recent years, many ATLAS and non-ATLAS institutes have been collaborating in the realisation of CMOS sensor prototypes, both with an hybrid approach, focused on ca-

pacitive coupling [120] as well as on monolithic designs [144, 145, 123, 146, 147]. They have shown that these detectors can be designed to be radiation hard to fluences well above 10^{15} n_{eq}/cm^2. Table 9.2 shows the path aimed for finalizing the R&D activity by addressing few remaining open issues and building a realistic drop-in module prototype by the end of 2019, on which a final decision on the deployment of this technology in Layer 4 could be based. A decision on the possibility to used CMOS technology requires both the evaluation of sensor performance, that will be performed in parallel with the qualification of the sensor technologies described in Chapter 5, and of the integrated electronics performance, including the chip integration in the powering read-out chains, that will be performed in parallel with the qualification of the production chip (Section 6.3), with similar milestones.

In 2017, a set of prototypes were submitted in order to investigate different read-out architectures for a monolithic detector implemented in CMOS technology. These prototypes are being used to verify the radiation hardness and the tolerance to transient cross coupling into sensor. In addition simulation studies will be used to define the read-out architecture and chip periphery. In parallel the mechanical features of module assembly, will be addressed. That will allow a Preliminary Design Review of the CMOS sensor in mid 2018, defining the read-out architecture and allowing to complete the R&D with the full size pre-production sensor CMOS-1.

A requirement on the pre-production sensor is the inclusion of interfaces for integration in the ITk services: in particular serial powering and data communication with the aggregator. Therefore its layout requires a definition of the ATLAS solution for data aggregation, in order to complete the design of CMOS pixel modules. Due to this dependence a submission in late 2018 will be performed. In order to minimize the risk that one of the two technologies fails the system integration aspects, the institutes collaboration in CMOS pixel design will continue to support both large and small-FF designs. The qualification will require also the assembly of electrical functional modules. It will be completed in late 2019, at the same time as the qualification of the production FE chips for hybrid modules.

At the end of the qualification stage, in November 2019, a choice for Layer 4 pixel modules, i.e. between hybrid, large-FF, and small-FF monolithic modules, can be made. It will be based on tracker performance parameters (primarily the in-time detection efficiency and noise rate after irradiation) and compliance with engineering constraints (service, powering, cooling, data transmission requirement). If CMOS pixels are selected, a final design review (FDR) is scheduled at about this time. If necessary minor modifications will optionally be implemented to obtain a PRR together with the production FE for the hybrid modules in 2020.

Table 9.2: Critical technical decision and milestones for the deployment of CMOS sensors in the ITk Layer 4.

Time	Technical achievement or milestone	Comments
2017 - 02/2018	Radiation hardness	Radiation hardness has already been verified for large-FF technology; small-FF (especially radiation hardness) will be tested on the TowerJazz prototypes MALTA and Monopix
	Tolerance to transient cross coupling into sensor	Already verified in LF-Monopix01. Verification on ams aH18 ATLASPix and MuPix will be carried out in fall 2017
	Definition of the read-out architecture	Based on results of simulation studies of the architectures implemented in the fully monolithic prototypes and scaled to a full size chip.
2017-06/2018	Complete evaluation of monolithic prototypes	
	Demonstration of mechanical module assembly	
06/2018	**Preliminary Design Review**	Full size detector, active area of 1.9 $\times$ 2 cm^2, large- and small-FF implementation with the same read-out architecture and periphery.
11/2018	**Submission of CMOS-1 prototypes**	
07/2019	Qualification of CMOS-1 prototypes	Main figure of merit will be in-time efficiency after irradiation. Verification of read-out architecture and power consumption.
11/2019	**Fully operational Drop-in Module prototype using CMOS-1 prototypes**	Drop-in module integrating full size prototypes, serial powering and interfaced with data aggregator.
11/2019	**Monolithic CMOS sensor and modules FDR**	Decision about using CMOS modules in Layer 4 and technology choice based on CMOS-1 prototypes.
12/2020	**Monolithic CMOS sensor and modules PRR**	

10 Pixel Data Acquisition and Front End Control System

10.1 Introduction

The read-out and control of the ITk Pixel Detector is embedded in the general TDAQ common read-out and control architecture [44]. An overview of the TDAQ architecture is shown in Figure 10.1. The upper figure shows the baseline read-out scheme with a single hardware trigger (Level-0, L0). In this scheme, the ITk Pixel Detector is fully read out on every L0 accept trigger signal with data received by the data handlers for further processing. A trigger rate of 1 MHz at a latency of 10 μs is foreseen at L0. The mode of operation with two hardware trigger levels (Level-0, L0, and Level-1, L1) is shown in the bottom, which allows to go to a higher L0 trigger rate of up to 4 MHz at a latency of 10 μs, while the L1 latency is 35 μs. In this mode, the outer pixel layers are still fully read out on every L0 trigger, providing input to the L1 Track trigger system [148]. The innermost layers store data on detector upon L0 trigger while only events passing L1 trigger are read out. This mode allows more control of the inner layer data rate, which is expected to be a delicate balance between data transmission capacity and detector material. In both the single and hierarchical trigger modes the data from the entire Pixel Detector are always passed to the data handlers for further processing.

Communication between on- and off-detector electronics is realised via dedicated links, separated into command and data links. Data as well as command links are split into an electrical and an outer optical part to allow the optical components to be located in an area which is less challenging in terms of radiation levels. Read-out simulation studies discussed below show that data transfer from on- to off-detector electronics in the innermost barrel layer requires a rate close to the maximum of 5.12 Gb/s provided by the read-out chip. The link architecture is designed to make optimal use of the available link bandwidth in all layers while keeping the number of links as small as possible to minimise the material in the detector volume. This is realised by a dedicated chip on the module which allows the aggregation of individual FE links into fewer data links. The data rate per FE from simulation combined with such an aggregation scheme define the data rate criteria for electrical and optical links. Command links operate at a significantly lower speed of 160 Mb/s such that technical solutions fulfilling requirements for data transfer are expected to qualify also as command links.

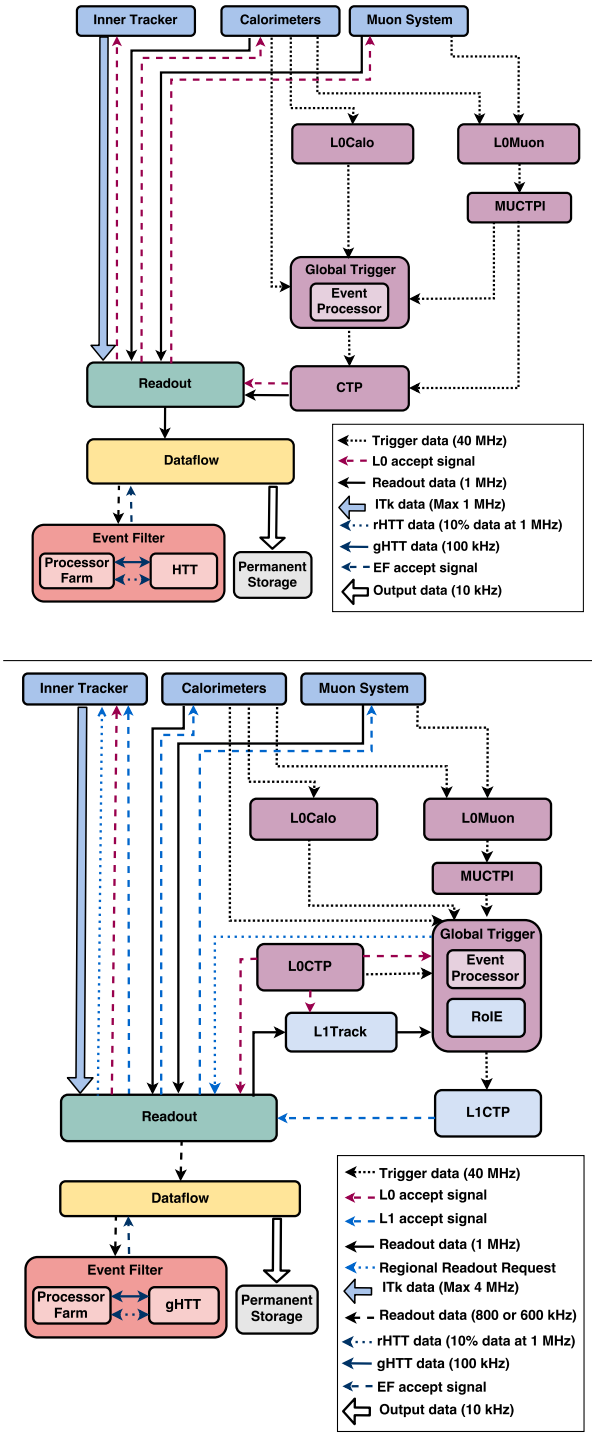


Figure 10.1: Schematics of the ATLAS Phase-II trigger scheme. **Top**: baseline with one hardware trigger level (Level-0, L0). **Bottom**: mode of operation with two hardware trigger levels (Level-0, L0, and Level-1, L1).

10.2 Read-out Simulation Studies

The data rates are derived from hit rates calculated from simulations of physics events in the ITk geometry as described in Chapter 2. Samples of $t\bar{t}$ events with 200 minimum bias events superimposed have been simulated, including secondaries, and passed through the ATLAS reconstruction, see Sections 2.2.3 and 2.2.4. From the simulations, the average hit rate per front-end chip per event can be determined.

To determine the average data rate from the average hit rates, the FE chip data format described in Section 6.2.2 is used. The pixel matrix is divided into fixed 1×4 regions in ϕ and η. Most of the 64 bit words of that data format correspond to hits in two such regions. Therefore, a 32 bit word ($= b$) is assumed to be read out for each region with a hit. A factor $c = 1.05$ is applied to correct for the overhead of non-hit information (see Figure 6.4). The trigger rate is $f = 1$ MHz for the baseline TDAQ architecture shown in Figure 10.1.

Reading out 1×4 regions rather than each pixel provides an effective compression by only reading out an address for each 1×4 region, reducing the data rate. The average regional occupancy is the average number of hit pixels per chip and event in a 1×4 region.

The average data rate r per chip is calculated from the average number h of hit pixels per chip and event and the average regional occupancy o as follows:

$$r = c \cdot b \cdot f \frac{h}{o}.$$

The average number of hit pixels per chip per event and the average regional occupancies per chip as a function of z-position are shown in Figure 2.16 in Section 2.2.4. The regional occupancy is highest in the central regions where the tracks are inclined and pass though more pixels as η increases. In the inclined region, the regional occupancy is less as the particle trajectories are typically closer to normal to the sensor and therefore do not pass through as many pixels as in the central barrel region.

The average data rates per chip as a function of chip z-position are shown for the barrel layers in Figure 10.2(left) and for the end-cap rings in Figure 10.2(right). The highest value of the average data rate for each barrel layer and end-cap ring are given in Table 10.1.

Furthermore the bandwidth required can be estimated from Figure 10.3. For the average number of regions hit per chip and event expected for the innermost Barrel layer (see Figure 2.16) the latency is determined as $T99$, the time for which 99% of events are stored without loss in the FE chip buffer (10,000 bits). Based on a simple queuing simulation, $T99$ is determined versus the trigger rate for various read-out bandwidths. A data compression on the FE chip as discussed above is already assumed in these simulations. The bandwidth required for a reasonable latency is therefore estimated to be 5.12 Gb/s for the innermost Barrel layer at a trigger rate of 1 MHz, while significantly higher trigger rates would require an even higher bandwidth.

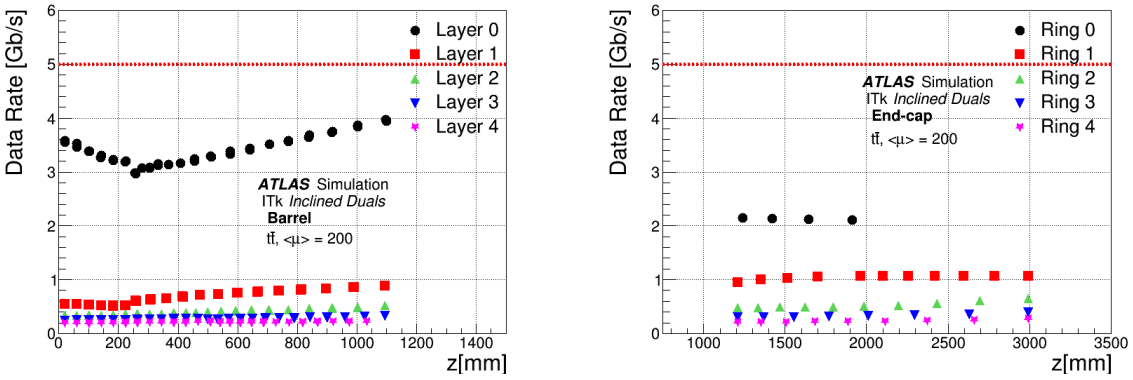


Figure 10.2: Average data rates per chip (Gb/s) in the barrel layers (left) and end-cap rings (right).

Table 10.1: Data rate per FE chip for barrel and ring layers. The highest value in Z of the average rate for each barrel layer, split into flat and inclined, and the end-cap ring is given.

Layer	Maximum data rate/chip (Gb/s)		
	Flat Barrel	Inclined Barrel	End-cap
0	3.58	3.97	2.15
1	0.55	0.89	1.07
2	0.38	0.52	0.65
3	0.28	0.32	0.39
4	0.22	0.22	0.27

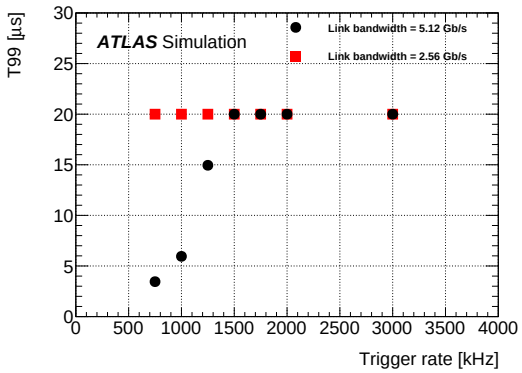


Figure 10.3: Simulated latency $T99$ to read out 99% of L0 triggers, in which values at $T99 = 20$ μs represent also values of $T99 > 20$ μs. The latency is simulated vs. the trigger rate for different read-out bandwidths. The average number of regions hit per chip and event expected for the innermost Barrel layer as shown in Section 2.2.4 is used. The simulations are done with different read-out bandwidths indicated in the legend.

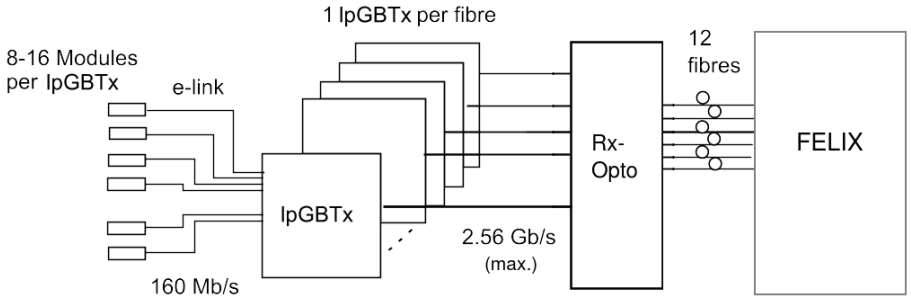


Figure 10.4: Drawing of the downlink layout. The bandwidth required between optical receiver (Rx-Opto) and lpGBTx as well as on the optical fibres depends on the multiplexing into electrical links and will be 1.28 Gb/s for 8 modules per lpGBTx and 2.56 Gb/s for 16 modules per lpGBTx.

10.3 Link Architecture

Communication between on- and off-detector electronics is handled via two separate links. Downlinks (also TTC-links) carry clock and command signals from off-detector electronics to on-detector modules while uplinks (also data-links) carry data from the on-detector modules to the off-detector electronics. Due to radiation levels, both links are split into an electrical and an optical part. This allows the opto-converter interface (opto-box) to be located in a region of relatively low radiation.

10.3.1 Downlinks

The downlink signals carry clock, trigger and slow commands encoded into one bit stream as described in Section 6.2.1. Bit streams for several modules are combined into a single optical data link between the off-detector electronics and the opto-converters to reduce material in the active ATLAS Detector volume. The combined bit stream is fanned out into one stream per module by the lpGBTx chip (see Section 12.1.1 in Ref. [1]) after optical-to-electrical conversion. The individual bit streams are sent to the modules via dedicated electrical links. The resulting layout of the downlinks is shown in Figure 10.4.

10.3.2 Uplinks

As discussed in Section 10.2, the average number of hits per front-end chip per event changes with layer resulting in a corresponding variation in output rate. To allow for event-to-event fluctuations in the data rate and to allow some overhead it is required that the data

rate does not exceed 70% of the bandwidth available on the link. Applying this to the maximum speed of the FE chip differential drivers[1] of 5.12 Gb/s gives a maximum allowed data rate of 3.6 Gb/s. The innermost layer therefore requires the FE chip to send data at its maximum rate and electrical links have to be designed accordingly. It has to be noted, that the data rate per FE chip in the inclined part of the innermost layer is slightly higher than this value, which holds a potential risk to operate the electrical links with less overhead for event-to-event fluctuations. This risk can be mitigated by exploring further compression of for example ToT information, see Section 6.2.2. Using the same high-speed data cables also in outer layers allows to aggregate the data link of several FE chips into fewer links per module, optimising the use of available bandwidth, which in turn minimises the number of electrical and optical links needed and thus reduces the material in the detector volume. Aggregation is realised per module with a dedicated chip to be attached to the electrical link as described in Section 6.2.2. Aggregation allows links from up to four FE chips to be combined in case of a quad chip module. The multiplexing scheme for the baseline trigger scenario with a maximum Level-0 trigger rate of 1 MHz is listed in Table 10.2(left), with the listed data rates derived from Table 10.1 by multiplying with the number of FE per (module) data link. The resulting data rates per link thus corresponds to the maximum in Z, i.e. the worst-case module in each (sub-)layer.

Operation with the trigger mode with a Level-0 trigger rate of up to 4 MHz is expected to increase the data rate by a factor of four. This exceeds the maximum data rate of the FE chip in the innermost layers. Thus the FE chip will be operated in fast clear mode as described in Section 6.2.1, sending data on reception of a Level-1 trigger operating at a maximum rate of 800 kHz. Affected layers are indicated in Table 10.2(right). Since the Level-1 trigger rate in that scenario is below the Level-0 trigger rate of the baseline scenario, in which these layers are read out fully, the rate on the data links is expected to be lower and thus not considered further. The rate of the other layers fully read out at a Level-0 trigger rate of 4 MHz is listed in Table 10.2(right), indicating the need to alter the multiplexing scheme for some layers to not exceed the available FE chip and link bandwidth[2]. The additional links required for the 4 MHz trigger operation must be accommodated in the local supports although initially only those links required for 1 MHz operation will be used. Activation of the additional links is controlled via the aggregator circuits which allows to change to a 4 MHz trigger operation at a later stage. The resulting layout of the uplinks for both trigger scenarios is shown in Figure 10.5 (for simplicity, only the multiplexing for the flat sections of the barrel layers is shown; the full multiplexing scheme is listed in Table 10.2).

As a consequence of the multiplexing scheme, the average raw data rate per uplink in most layers exceeds the input data rate of the envisaged lpGBTx chipset of 1.28 Gb/s. Therefore the multiplexed data of the aggregator chip (see Section 6.2.2) will be transmitted directly on the uplinks without further aggregation. The electrical uplinks are directly connected to

[1] The FE chips can send data in multiples of 1.28 Gb/s, i.e. at speeds of 1.28 Gb/s, 2.56 Gb/s, and 5.12 Gb/s

[2] The data rate in End-cap 4 at 4 MHz trigger rate is slightly higher than 70% of the link bandwidth. Further data compression measures as referred to above can be considered to mitigate, or alternatively, operation of affected modules in fast clear mode.

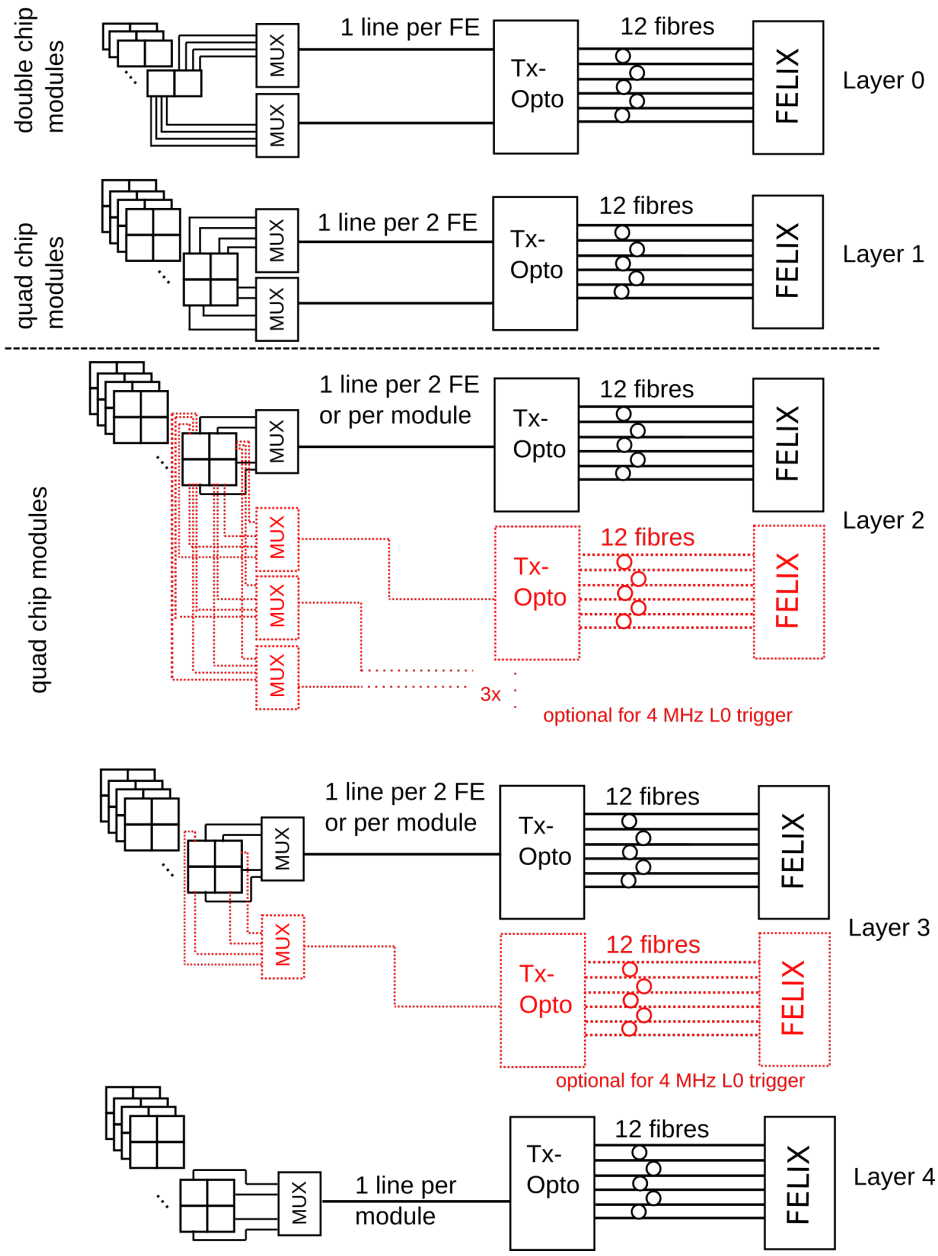


Figure 10.5: Drawing of the uplink layout, exemplarily shown for the flat part of the different barrel layers. The links between FE chips and aggregator chip (MUX) operate at a rate of 1.28 Gb/s, the links between aggregator chip and equalizer (Tx-Opto) operate at a rate of 5.12 Gb/s. The additional link at 5.12 Gb/s required to read out Layer 2 at a Level-0 trigger rate of 4 MHz is shown with red dotted lines.

Table 10.2: Multiplexing scheme of FE links into module links and resulting data rates per e-link (maximum in Z per layer is given). **Left**: Scheme for the baseline trigger mode at a Level-0 rate of 1 MHz. **Right**: Scheme for the trigger mode at a Level-0 rate of 4 MHz. The column "read-out mode" specifies if the chips in that layer will be operated in fast clear mode or fully read out on Level-0.

Layer	No. FE per link	Data rate per link (Gb/s)
Flat Barrel 0	1	3.58
Flat Barrel 1	2	1.10
Flat Barrel 2	4	1.52
Flat Barrel 3	4	1.12
Flat Barrel 4	4	0.88
Incl. Barrel 0	1	3.97
Incl. Barrel 1	2	1.78
Incl. Barrel 2	4	2.08
Incl. Barrel 3	4	1.28
Incl. Barrel 4	4	0.88
End-cap 0	1	2.15
End-cap 1	2	2.14
End-cap 2	4	2.60
End-cap 3	4	1.56
End-cap 4	4	1.08

Layer	read-out mode	No. FE per link	Data rate per link (Gb/s)
Flat Barrel 0	fast clear	1	N/A
Flat Barrel 1	fast clear	2	N/A
Flat Barrel 2	full	1	1.52
Flat Barrel 3	full	2	2.24
Flat Barrel 4	full	4	3.52
Incl. Barrel 0	fast clear	1	N/A
Incl. Barrel 1	fast clear	2	N/A
Incl. Barrel 2	full	1	2.08
Incl. Barrel 3	full	2	2.56
Incl. Barrel 4	full	4	3.52
End-cap 0	fast clear	1	N/A
End-cap 1	fast clear	2	N/A
End-cap 2	full	1	2.60
End-cap 3	full	2	3.12
End-cap 4	full	4	4.32

the input of the optical components, i.e. lpGBTx is *only* used for the downlinks, not for the uplinks.

10.3.3 Electrical Links

The electrical links (e-link) should be low mass, radiation-hard, and halogen-free. They will be connected to the flex module on one side and to the opto-box on the other side where the receiver will be placed, acting both as uplink and downlink as described above. Since the requirements for the former are more challenging, this section will focus on uplink aspects. As discussed above, the average data rate of a single FE chip in the innermost layer approaches several Gb/s which requires the differential drivers of the FE chips to be operated at their maximum speed of 1.28 Gb/s each for a total speed of 5.12 Gb/s. The same requirement is imposed by the multiplexed data on an e-link from a module in other layers. Therefore, all e-links are required to transmit differential data at 5.12 Gb/s over a distance of 5 m or less which is defined by the location of the opto-box.

In order to achieve reliable transmission, the total link loss (applicable to all the links in the system) should be kept at or below 20 dB. This value is motivated by the fact that the best FPGA receivers currently on the market can cope with a loss of 28 dB, applying the

best equalisation and signal integrity techniques. Furthermore, with such a loss, receiver equalisation will be mandatory in addition to driver pre-emphasis[3], both of which goes with the DC-balancing of the data protocol. The total link loss can be estimated by adding the losses in the full system: circuit boards (traces), connectors and cables/flexes.

Apart from this a limit on the Bit Error Rate (BER) of 10^{-12} is required for the whole (optical *and* electrical) communication chain: transmitter, channel and receiver. The limit follows requirements from the current ATLAS Inner Detector with which we adhere to defined industrial standards.

Significant effort has been invested in finding data transmission solutions that satisfy these specifications. Long flexible twinaxial and twisted pair cables have been designed as listed in Table 10.3. Kapton flexible printed circuit cables also offer a radiation-hard, low-mass electrical transmission solution. Two solutions for data transmission inside the pixel volume using Kapton flex technology with a differential embedded micro-strip arrangement and cross hatched ground plane have been developed.

Table 10.4 shows a summary of the measurement results obtained with cable and flex prototypes. Tests were performed at a frequency of 3 GHz which is higher than the actually needed Nyquist frequency[4] to add a safety margin. Assuming a loss of 1 dB per circuit board (module flex or boards in the opto-box) and 2 dB loss for each connector, the 20 dB target translates into 14 dB for the pure cable, which is met by several of the prototypes listed in Table 10.4 over the desired length (< 5 m) of the electrical links. Initial studies using passive equalization near the cable connector show an improved behaviour of cable loss versus frequency which allows transmission over cables at better quality. Further flex-based solutions as described in Section 13.4 are also considered as electrical links.

Decision and Review Path

Data transmission over twinax cables is the baseline for both barrel and end-cap local supports. The cables are laser welded to small PCBs. The PCB on one end will hold the aggregator chip while the PCB on the other end will hold an equalizer chip to form an "active cable" as described in Section 6.2.2. Electrical link candidates which are near or below the required 20 dB target, including losses on connected PCBs and connectors, will be considered for the final selection. This includes mutual optimisation of cable impedance as well as aggregator driver and equalizer design. Out of the chosen cable candidates, the solution with the least material in the detector volume is chosen. For more details on the schedule see Section 19.4.5.

[3] Pre-emphasis boosts specific frequency components of a signal in order to improve the signal-to-noise ratio for the entire frequency range.

[4] The Nyquist frequency is half of the data rate, i.e. 2.56 GHz for the data links.

Table 10.3: Cable designs considered for data transmission in ITk Pixel. CC-Al: Cu-clad Al; PES: Polyester; PE: polyethylene; LDPE: low-density polyethylene; PEEK: Polyetheretherketone; TP: twisted pair; TW: twinaxial cable; N_{cond}: number of conductors per wire; AWG: American wire gauge. All TW cables have a drain wire (TP do not), and all cables except for "TP-NOshield" are shielded.

Name	Type	AWG	N_{cond}	Wire material	Shield material	Dielectric	Insulation	Impedance (Ω)	Material (% X_0)
TP-shield AWG36_7	TP	36	7	Cu	Al foil	PEEK	Kapton	100	
TP-NOshield AWG36_7	TP	36	7	Cu	N/A	PEEK	N/A	100	
TW-shield+drain AWG28_SC	TW	28	1	Cu	Al	PE	PES	100	0.0883
TW-shield+drain AWG30_SC	TW	30	1	Cu	Al	PE	PES	100	0.0620
TW-shield+drain AWG34_SC	TW	34	1	Cu	Al	PE	PES	100	0.0537
TW-shield+drain AWG30_SC	TW	30	1	CC-Al	Al/PES	LDPE	PES	70	

Table 10.4: Summary of the measurement results obtained with ITk Pixel cable and flex prototypes. Numbers highlighted in the last column indicate that the requirement of a loss below 14 dB is passed for a cable length of 5 m.

Cable	Length (m)	dB loss at 3 GHz	dB loss per metre
28AWG Twinax	6	14	**2.33**
30AWG Twinax	6	17	**2.83**
34AWG Twinax	4	20	5.00
28AWG Twinax	8	16.6	**2.08**
30AWG Twinax	8	19.0	**2.38**
34AWG Twinax	8	32.0	4.00
36AWG TP_shield	3	12.0	4.00
36AWG TP_shield	1	5.0	5.00
Stave Flex	1	9.0	9.00
Data Flex	1	9.0	9.00
Stave Flex + 6 m 30AWG Twinax	7	25.0	3.57

10.3.4 Optical Components

The optical link between off-detector components and on-detector opto-converters should be array-based. This will save space needed for the connectors and driver/receiver circuitry and save multiplicity of connections to front-end electronics. The space constraints are defined by the location of the opto-boxes near the ITk Strips end-cap vacuum insulated lines. This location also ensures accessibility during long shutdown periods.

Two approaches are followed currently. One is based on the experience from the Run 1 Pixel Detector and one is based on the Versatile Link+ project developments. In general 12-channel optical transmitters and receivers will be used. The basic requirements are:

- The transmitter is optimised to operate at 5.12 Gb/s per channel.
- Electrical signal equalisation to properly receive the signals from the electrical cables are to be added if needed.
- The transmitter and receiver connect to a 12-way fibre ribbon each.
- The receiver is optimised to operate at 2.56 Gb/s (5.12 Gb/s),
- The transmitter and receiver operate within the environment of the ATLAS Detector.

In the following the two concepts will be described.

Versatile Link+ based development

The Versatile Link+ project is a joint ATLAS and CMS effort which aims to develop a radiation-hard optical link system. It is designed to withstand the radiation level of the trackers of both detectors during the High-Luminosity run. It has been qualified for 1 MGy Ionising Dose and for a total fluence of 10^{15} n_{eq}/cm^2. The project started its pre-production phase in 2017, while the production is expected to run in 2019 and 2020, when companies having successfully completed development (on time, in budget) will be invited to tender for the full production.

Figure 10.6 shows the Versatile Link+ architecture. The Versatile Link+ module can be interfaced with Serializer / Deserialize modules (SERDES). Each module can host a single receiver (Rx) and multiple transmitters (Tx's). For the transmission part, the Laser Driver (LDD) can work in array mode driving multiple VCSEL's (Vertical-Cavity Surface-Emitting Laser), while for the receiving part the PIN diode is coupled with a trans-impedance amplifier (TIA). The LDD and TIA are custom designed modules, while the VCSEL array and PIN diodes are commercial, but qualified within the collaboration to prove their radiation hardness property. The LDD has been designed and prototyped in 65 nm CMOS technology. The Versatile Link+ works in a Multi-Mode Optical mode and it has a data rate of 5 or 10 Gb/s for the Tx and of 2.5 Gb/s for the Rx links.

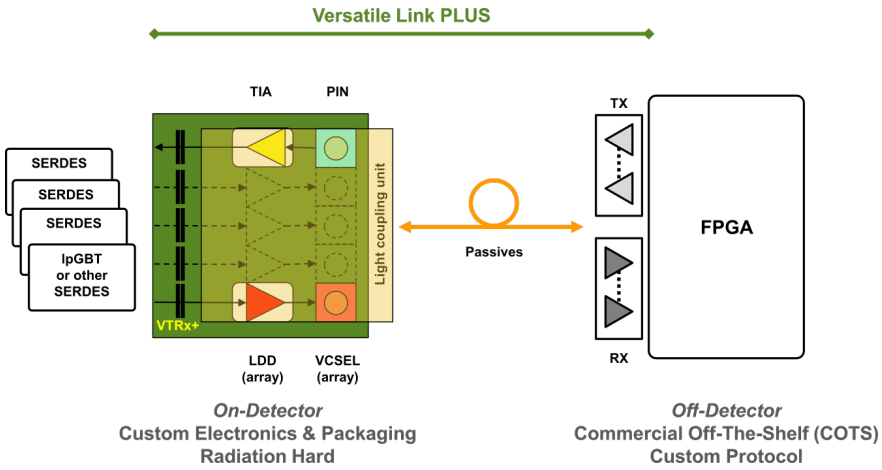


Figure 10.6: Drawing of the Versatile Link+ architecture.

Table 10.5: Summary of the custom front-end prototype of the Versatile Link + modules.

Version	Configuration	Optical I/F	Electrical I/F	Receiver	Transmitter
V1	1Tx + 1Rx	US conec: MOI	SFP	GBTIA + ULM PIN	COTS driver + ULM VCSEL
V2	1Tx + 1Rx	Low-profile	SFP	GBTIA + ULM PIN	COTS driver + ULM VCSEL
V3-V3b	4Tx + 1Rx	US conec: MOI	QSFP	GBTIA + ULM PIN	LDq10/LDQ10P + VCSEL array
V4	2Tx + 1Rx	Low-profile	Custom	GBTIA + ULM PIN	LDq10v2 + VCSEL array

At the moment four versions of the Versatile Link+ module have been produced, as summarised in Table 10.5. There are several differences between the four versions of the Versatile Link+ modules:

- The number of Tx's can go from 1 to 4.
- The optical interface can be either the Mechanical Optical Interface (MOI) by US conec or low-profile.
- The electrical interface can be done by small form-factor pluggable transceiver (SFP), quad small form-factor pluggable transceiver (QSFP) or a custom one.
- The Laser driver for the VCSEL is an LDQ10 for either a single VCSEL, or a VCSEL array.

In particular the Version V3 is the latest version tested as of June 2017. Results are presented in Figure 10.7. In the left picture the results of the Bit Error Rate test are shown; on the the horizontal axis the optical modulation amplitude (OMA) is reported while the Bit Error Rate (BER) is on the vertical axis. The test was performed at 4.8 Gb/s data transmission. In the right picture the results of the Eye Diagram test are summarised for different Tx's. In

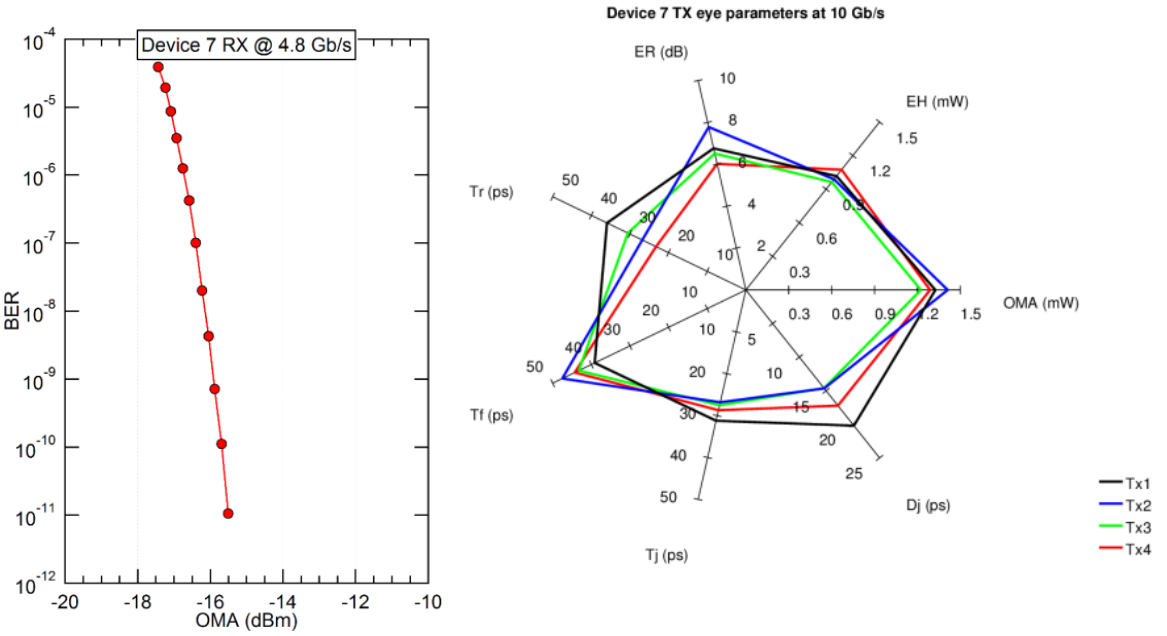


Figure 10.7: Bit Error Rate Test for Rx (left) and Eye Diagram Test for the Tx (right).

particular the OMA, the Eye Height (EH), the Extinction Ratio (ER), the Rising Time (Tr), the Falling Time (Tf), the Total Jitter (Tj), and the Deterministic Jitter (Dj) are presented. All the parameters are above threshold for obtaining a proper data transmission at 10 Gb/s.

The development of the Versatile Link+ is proceeding according to schedule and the production phase is about to start. Preliminary tests have demonstrated the possibility to operate the Rx's and Tx's links up to 4.8 Gb/s and 10 Gb/s, meeting the ATLAS ITk requirements.

Opto-board based development

The opto-board (optical module) concept is based on the two generations of optical links for the Pixel Detector of ATLAS which have been successfully deployed in Run 1 and 2. There will be two flavours of opto-boards, one for transmitting and the other for receiving optical signals. Each transmitter opto-board contains an ASIC with 12 channels of VCSEL drivers for coupling to a 12-channel VCSEL array. The ASIC will be operating at 5.12 Gb/s. Each receiver opto-board contains 12 channels of receivers to amplify the signals from a 12-channel PIN diode array. Each receiver will be operating at 2.56 Gb/s. Each received signal would then be sent to a lpGBTx (Gigabit Transceiver, see above) chip for de-serialisation into multiple 160 Mb/s signals for transmission via the e-links described above.

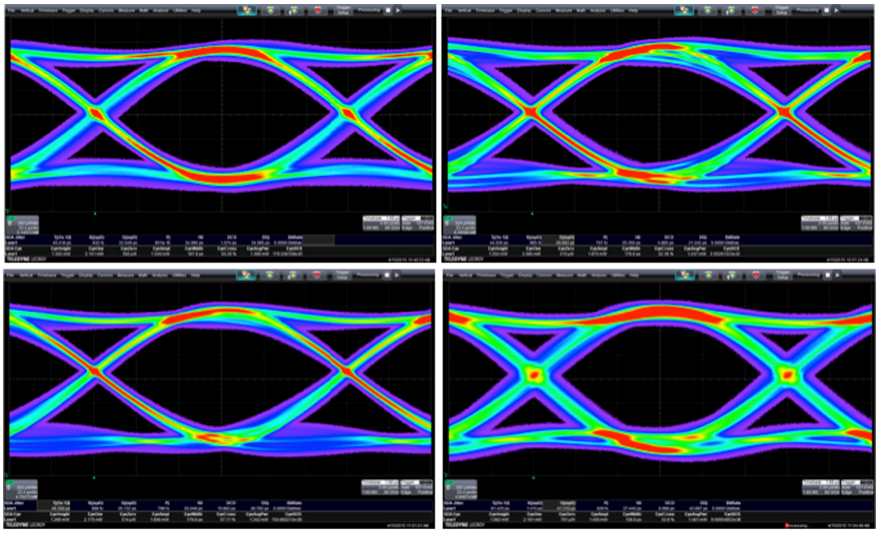


Figure 10.8: Optical eye diagrams of all four channels on an opto-board operating at 5 Gb/s [149].

The transmitter ASIC, the VCSEL driver, has been successfully prototyped in a 4-channel version using a 65 nm CMOS technology. The corresponding transmitter opto-board has also been prototyped. The optical package for the VCSEL array is very similar to that used in the second generation opto-boards and the RXs modules (the off-detector optical receiver modules) produced for the Phase-0 upgrade. The optical coupling uses commercial MTP connectors which can be readily mounted and dismounted during production testing and installation. The performance at 5 Gb/s is satisfactory [149] as shown in Figure 10.8. The plan is to lay out the ASIC in 12 channels in the near future together with an equalizer circuit in each channel. For the receiver ASIC, the plan is to take the single channel GBTIA circuitry (IP) and lay it out in array format.

Groups of opto-boards will be mounted inside an opto-box, a mini-crate similar to that used in the second generation optical links of the Pixel Detector. The use of array-based opto-boards reduces the physical size of each opto-box by a factor of two, a much needed space saving.

Equalizer Studies

In order to receive data from the electrical links to be processed by the VCSEL drivers, an equalizer will be employed. In the concept of active cables described in Section 10.3.3, such an equalizer would be part of the electrical link. Alternatively, equalizing circuits can be integrated into the VCSEL driver chip.

Development of a low-power 14 Gb/s VCSEL driver in 65 nm technology [150, 151] includes the design of a Limiting Amplifier (LA) for each channel. The LA is composed of

three differential stages, the first of which uses an adjustable equalization. A passive inductance is included to optimize the peaking frequency. Initial tests with optical components produce optical eye diagrams that pass 14 Gb/s transmission data rate with margin.

Decision and Review Path

Since the Versatile Link+ project is currently more advanced, it was chosen as baseline for the optical links of the Pixel Detector. Further development of the drivers as well as designing a full opto-box with components of the Versatile Link+ project have to go along with other services design decisions, in particular development of the electrical links. The opto-board development will be pursued in parallel, demonstrating compatibility with rate and radiation dose requirements. The final decision will be based on final performance in combination with the electrical links, the overall opto-box design, and best match to services modularity in the detector. For more details on the schedule see Section 19.4.5.

10.4 Off-Detector Electronics

The off-detector electronics for the ITk will be common between Pixel and Strips. Figure 10.9 shows an overview of the ITk off-detector electronics. The DAQ chain consists of the FELIX system as front-end interface and the Local Trigger Interface (LTI), which interfaces the ITk systems to the ATLAS-global TTC system. The backend systems will consist of several PCs for DCS, ITk monitoring, data handling and control. These systems will be described in detail in Section 12.1.

FELIX The FELIX system is the main interface between the detector and all off-detector systems and it is maintained by ATLAS TDAQ [81]. The main task of the FELIX is to handle the communication between the off-detector backend systems and the detector. Therefore, triggers coming from the LTI (see below) and configuration data from the ITk control unit are merged into a single bit stream and then encoded with the ITk Pixel specific downlink protocol (see Section 6.2.1) on a lpGBTx e-link basis. During operation of the detector the configuration has to be re-sent regularly to mitigate loss of configuration from single event upsets in the FE chips. Therefore, all configuration data will be stored inside the FELIX system and will be sent by command of the LTI during gaps in the triggering using the trickle mechanism the FE chip provides as described in Section 6.2.1. In the uplink direction FELIX will decode the custom 64b66b datastream (see Section 6.2.2) and forward it to the backend data handlers. Besides that, also some monitoring information, like timeouts, received trigger tags, decoding errors and also a prescaled fraction of events with hit data, has to be forwarded to the ITk monitoring unit.

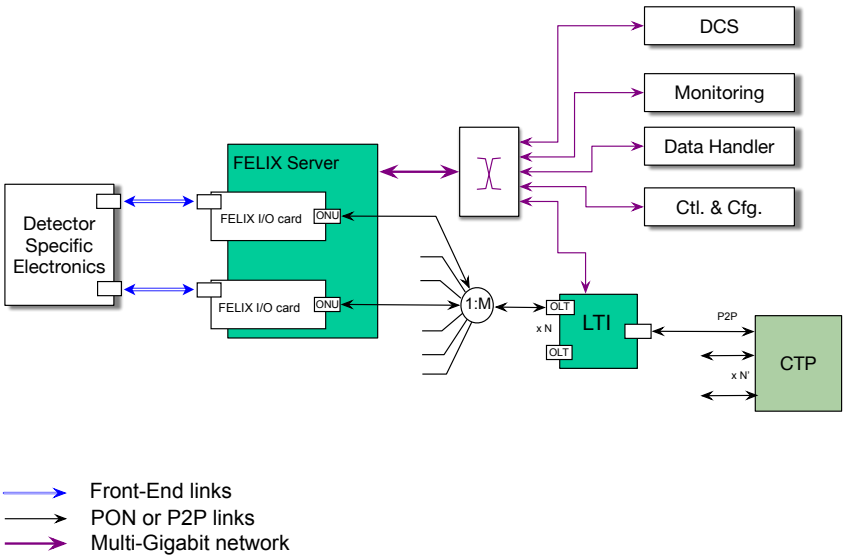


Figure 10.9: Overview block schematic of the off-detector electronics with FELIX as first-stage detector interface and LTI as trigger interface.

The current prototype for the Phase-I FELIX system is a PCIe card with 48 GBT input/output links and a PCIe Gen3 x16 interface. These cards will be hosted in a rack PC and equipped with fast network interfaces (40/100 GbE or Infiniband). A baseline design inspired by concepts of and experience with the Phase-I FELIX and based on the detector requirements at HL-LHC has been proposed in Ref. [44], with alternative options being considered as technology could significantly evolve in the next few years.

Local Trigger Interface (LTI) The Local Trigger Interface (LTI) is meant to be the interface between the sub-detector FELIX systems and the ATLAS central trigger systems (CTP). During the operation of the ITk the LTI is the only source for triggers and controls also the time when front-end configurations can be safely transmitted to the detector. The ITk Pixel front-end chip will use a trigger tag to connect data to a specific trigger and that trigger tag is also generated by the LTI. During the calibration process the LTI can be used to drive the innermost calibration loop (trigger loop) to send a specific number of triggers to all connected front-end chips (broadcast). The current design for the LTI foresees it to be an ATCA-blade with a point-to-point connection to the central trigger system and a passive optical network (PON) to the FELIX system. Therefore, each LTI would be responsible for a larger number of FELIX systems.

10.5 System Test

Even though the final on-detector electronics is not yet available, initial system test measurements were performed based on the legacy read-out chip FE-I4 [72] and read-out systems developed further from their applications during IBL [3] construction to test ITk-specific DAQ aspects such as GBT data transmission.

GBT setup A test setup for GBT read-out of FE-I4 front-end chips has been created. It uses the ATCA based RCE read-out system [152] consisting of a COB (cluster on board) ATCA carrier board, a DPM (data processing module), a DTM (data transportation module), and an RTM (Rear Transition Module) containing SFP+ transceivers. The loaded COB is shown in Figure 10.10.

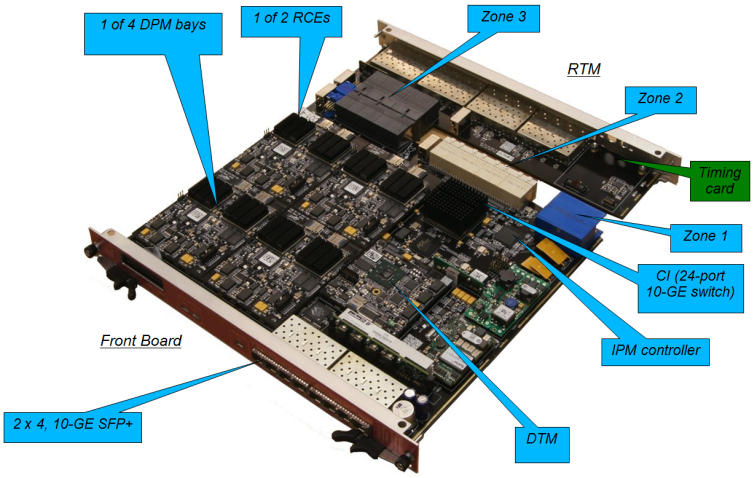


Figure 10.10: Picture of a loaded COB (cluster on board) ATCA carrier board indicating its components (DPM, DTM, RTM).

In the system test setup one RCE communicates with one Versatile Link Demo Board (VLDB) [153] over a fibre pair at 4.8 Gb/s using the GBT protocol. Since the FE-I4 front-ends have a data rate of 160 Mb/s the GBTx is configured for 20 e-ports all of which are connected to FE-I4 read-out channels via the HDMI e-link ports on VLDB. Since each RCE reads out 20 front-ends, 3 DPMs out of the 4 available DPMs on the COB are needed to read out 120 FE-I4 front-ends.

In addition to the GBT firmware the RCE contains formatting for the FE-I4 data. The data are then transferred via DMA to the ARM processor on the RCE where the calibration loops run and where results get histogrammed. The scan is controlled through a GUI (calibGui) that runs on a Linux server. The GUI also reads back the histograms from the RCE and performs analysis. The communication between the server and the RCE is done via ethernet

(1 or 10 Gb/s). All the common calibration scans are implemented since the RCE system was used for the IBL stave QA.

Stave Tests The GBT RCE system was tested with two multi-module arrangements. An old IBL stave (stave 0B) was connected via new services. Successful tuning, calibration and source scans of up to 14 out of 32 FE-I4 front-end chips on the stave was demonstrated, with the limitation in number of operated front-end chips being caused by damage to the stave and front ends. In addition a double sided stave in the UK demonstrator project was used, realised as a pair of serial powering chains, of which 16 – 18 FE-I4 front-end chips were operated. Because the RCE software was already set up for IBL staves, no changes were necessary for this test. Evolutionary further development of the RCE software towards the common ITk software (see Section 10.6) is in progress. Compatibility of GBT RCE with an early prototype of this software was already demonstrated.

In addition to the VLDB board mentioned above custom carrier boards hosting GBTx mezzanines, inspired by those used for ITk Strips, are under development. This carrier board will partially bypass the need for HDMI cabling and provide direct connection to the demonstrator. Use of the strips mezzanine board means that this read-out system can ideally also profit from the lpGBTx "drop-in" update planned for strips.

In addition to tuning, calibration and self-triggered source scans, support for cosmic data-taking and test beams are also planned with the RCE system. These setups are expected to evolve from FE-I4 to also support tests on modules and larger detector structures based on RD53A and ATLAS chips, through relatively simple hardware adaptors and the common custom Aurora 64b/66b IP for firmware.

Similar measurements will be performed on the demonstrator stave described in Section 13.4, which connects the FE-I4 links to GBT and thus allows flexible testing with the RCE system described above as well as with a read-out system based on the Phase-I FELIX prototype.

10.6 Testing and DAQ Software

10.6.1 Software Design

It is planned to use the *ITk DAQ software* as the common software architecture to support various use-cases, including sensor and module testing during production and assembly in the local sites (starting from one front-end chip read-out $O(1)$), test beams, operation of the detector in the Point-1 (up to $O(10^5)$ front-end chips), and enabling well-organised calibration and data-taking. One of the key concepts for development of the ITk DAQ software is to establish a common high-level interface to different hardware platforms, such as FELIX [81], and systems targeting module tests during production (YARR [154], RCE [152],

USBpix [155], etc.) and different front-end chip types (RD53A, see Chapter 6, and legacy front-end chips [72]). This is achieved by providing a well-defined common interface for the different hardware platforms to communicate with the higher level software which steers communication to and from the front-end.

The core of the software framework can be divided in two parts:

- The scan engine which generates the bitstream of commands to communicate with the front-end. The calibration of tracking detectors is typically performed in terms of loops with many iterations of the same kind of command which scan over a parameter range, a subset of channels or perform calibration injections. The command sets are organised as loop actions, which can be dynamically assembled into a nested loop structure to be executed by the loop engine.

- The data received from the front-end traverse a pipeline of processing steps. An important concept of this processor pipeline is its data driven manner, i.e. that all the information needed to perform the processing step is included in the data packets in the form of meta-data. The input and output data structures which are being exchanged by the processing blocks are well defined. This enables an easy exchange or integration of a processing algorithm into the chain or a hardware accelerator to perform a specific processing step; for instance histogramming is a step sometimes performed in hardware to reduce the required communication bandwidth. Furthermore this concept enables the data to be processed in a distributed manner if local processing resources are insufficient. As the processing blocks do not require communication with each other or any other pieces of the frame but only rely on the information stored in the incoming data, they can be distributed over multiple nodes and receive and send data via the network. The concept of distributing the data processing is important for the scalability of the framework. Multiple data transfer protocols, including `netIO` [156]. and `ZeroMQ`[5], and multiple data-encoding schemes (either common schemes or ITk DAQ-specific ones) can be considered for this.

With common data formats and user interfaces, expertise on operating the system for a specific task is expected to be extensible to various use-cases, e.g. an expert of the module testing in the local laboratory site can handle the common user interface in the detector operation at Point-1 with little additional training. With this model, an effective human resource sharing in the community can be achieved for sustainable detector operation and maintenance. At the software level, the common architecture enables a common data format and a storage infrastructure for calibration configurations and the output is particularly important, as the detector modules typically need to travel through several sites during construction phase before installing at Point-1. The easy sharing of data and the complete chronology record enabled by such a scheme will facilitate systematic module selection and eventual detector performance debugging.

[5] See `http://zeromq.org/`.

Configuration

Various types of configurations need to be defined in order to establish a complete read-out system. The JSON[6] format has been proposed as the candidate to describe the configuration. Examples of configurations are as follows:

- *Chip configuration* is a set of parameters that can be written to the register of the front-end chip to specify a state of a front-end chip including calibration. It is categorised into the global configuration and the pixel configuration. The global configuration is for common parameters over the chip and the pixel configuration is specific to each pixel in the chip. Chip configuration is loaded before data taking.
- *Read-out configuration* is a set of parameters that can define the behaviour of the read-out device. The definition of the read-out configuration depends on the specification of each read-out device.
- *Scan configuration* specifies the algorithm on the software to define a scan, which is the routine used in the calibration procedure.
- *Hardware connectivity configuration* specifies the administration of hardwares, including both read-out devices and front-end chips. It also specifies the software process identifier (name) that owns the control of the hardware device.
- *System configuration* describes the arrangement of the DAQ software processes over the network and their relation to each other.

Communication to front-end chips via various read-out devices

Although the communication protocol can be different depending on read-out devices, the content of the data to be sent to front-end chips (e.g. changing one global register to a specified value) is common for a specific type of front-end. Viewed from the software side (e.g. from the scan engine), the concrete detail of the protocol should be therefore be abstracted, and the software focuses on the content of the input/output data rather than the format and protocol of communication.

Scan

A *scan* is a series of sequential data taking with switching the configuration according to the specified algorithm, referred to as the scan configuration. Some scans are to be performed together with associated strobe charge injection before triggering in an adequate timing. Scans are carried out to perform specific calibrations (e.g. threshold tuning) or monitoring the goodness of calibration (e.g. ToT scan) or continuous data-taking (e.g. noise

[6] http://www.json.org/

scan), under the condition without the presence of beam collisions. A scan configuration is specified by nesting multiple loops of various algorithms, such as *parameter loop, mask loop, trigger loop, data-receiving loop* in sequence. The event data sent from the front-end chip are matched to the corresponding snapshot of the configuration setting, referred to as loop status, according to the encoding that the ITk DAQ software defines; then the data are processed in the downstream software pipelines for histogramming and analysis using the attached loop status on the data. The analysis process may generate feedback to the scan configuration to follow in order to achieve iterative convergency of the calibration. of the calibration. For some specific read-out devices, a part of the downstream process of histogramming and analysis may be performed within dedicated entities of the read-out device, which are typically implemented in the FPGAs for accelerating the scan routine. The output data type can be histograms instead of event data in this scenario.

10.6.2 Calibration Performance Requirements

As detailed above, calibration typically consists of scans realised as one or several nested loops varying parameters of the FE chips or the read-out devices. Most of these scans are based on sending a subsequent pair of charge injection and trigger commands which is repeated about 100 times. This *trigger loop* is currently run inside a loop enabling read-out or injection in only a fraction of columns or pixels for charge injection performance reasons (*mask loop*). Since trigger and mask loops are repeated within the actual calibration loop(s) modifying the scanned parameter(s), their execution is time critical. The simplest approach for executing the trigger loop is a sequence of injection-trigger commands with each pair separated in time such as to allow the FE chips to send out data before the next injection-trigger command pair is sent.

As a simplified estimate of requirements imposed by calibration scans, parameters of a typical threshold scan as used for the current Pixel Detector combined with RD53A parameters and the link layout of Layer 4 (i.e. four FE chip data links operated at 1.28 Gb/s combined to a single data link at 5.12 Gb/s) are assumed as follows:

- Each FE chip consists of $n_{\text{pix}} = 400 \times 384 = 153,600$ pixels (see Section 6.2).
- Per scanned parameter value, 100 events are generated, i.e. the trigger loop comprises $n_t = 100$ repetitions, with injection-trigger commands separated by a time Δt.
- Only a subset of pixels per FE chip is read out per injection-trigger command. From RD53A this is assumed to be a row, i.e. the mask loop comprises $n_m = 384$ repetitions.
- The charge injection mechanism can not be applied to all pixels at the same time. For RD53A injection is expected to be feasible for one row at a time and will be processed in parallel to the mask step described above (i.e. no extra loop needed).

- The parameter loop (parameter = injected charge for a threshold scan) comprises $n_p = 200$ steps. For a threshold scan, a sufficient step size is needed in order to be able to measure the slope of the turn-on curve which is a measure for noise.

Hit and ToT data are generally packed in 32 bit words for a 4-pixel-region, so that a 66 bit long word in the 64b/66b encoding (see Section 6.2.2) can contain up to 8 hits. The mask and injection patterns match this read-out pattern, such that, at high injected charge, a 64 bit data word is assumed to contain all 8 possible hits. Neglecting header information, the read-out of all enabled pixels thus results in a bit stream length of

$$N_{\text{data-bits}} = \frac{66\,\text{b} \cdot n_{\text{pix}}}{8 n_m} \approx 3.2\,\text{kb}\,,$$

transmission of which requires 2.4 μs at 1.28 Gb/s. The simple trigger loop design thus requires an corresponding waiting time between triggers, to which the time required to send the injection-trigger commands needs to be added. The latter is essentially given by the latency of $t_{\text{lat}} = 10$ μs, thus $\Delta t = 12.4$ μs. At each step of the mask loop, the registers enabling pixel read-out or injection must be changed. This is expected to be handled by a sequence of a few commands altering global registers, identical for all FE chips, thus sent as a broadcast command. Assuming $\mathcal{O}(100\,\text{b})$ for the command sequence at 160 Mb/s, this procedure requires additional $t_{\text{mask}} = 100\,\text{b}/160\,\text{Gb/s} \approx 0.6$ μs per mask step. Similarly, the parameter that is scanned requires a global register command, sent as broadcast to all FE chips, requiring t_{par} per parameter loop step. This is expected to be of order of t_{mask}. This results in the time required to collect data from the entire scan:

$$t_{\text{tot}} = n_p(n_m(n_t \cdot \Delta t + t_{\text{mask}}) + t_{\text{par}}) \approx n_p n_m n_t \cdot \Delta t \approx 95\,\text{s}\,.$$

Any additional delay within the trigger loop will increase Δt and propagate significantly into an increase of t_{tot} due to the multiplication with $n_p n_m n_t$ and should therefore be kept to the order of μs or less. Calibration procedures will also be executed between fills, requiring the time needed to fit in the available slot. The ideal timing of a more complex tuning scan which repeats the scan procedure outlined above $n_{\text{tune}} = \mathcal{O}(10)$ times is

$$t_{\text{tune}} = n_{\text{tune}} \cdot t_{\text{tot}} \approx 15\,\text{min}\,,$$

which should not be exceeded significantly by the final calibration procedures.

A similar calculation results in the total amount of data per FE chip to be decoded in the Data Handler (see Section 12.1). For simplicity it is assumed that hits are returned for half of the parameter steps, i.e. the injected charge is below threshold for parameter loop steps below $n_p/2$. This yields:

$$N_{\text{totbits}} = N_{\text{data-bits}} \cdot \frac{n_p}{2} n_m n_t = 12\,\text{Gb}\,.$$

In case of all FE chips of all modules (i.e. $4 \cdot 6572 + 2 \cdot 3192 + 512 = 33$k FE chips, see Table 8.1) being involved in a calibration scan, this corresponds to a total of approximately 40 TB of input data to be processed for histogramming.

11 Power Distribution, Grounding and Shielding, Detector Control System

This chapter describes the powering scheme for the ITk Pixel Detector. The choice of scheme, which is based on serial powering, is motivated by the fact that purely parallel provision of the high currents required by the module ASICs would require many cables, and therefore a great deal of material, inside the detector volume, which would degrade the tracking performance. Therefore a serialisation of the powering is needed. Furthermore, the outermost power cables which run between the power supplies in the services caverns and the Patch Panels 2 (PP2) in the experimental hall in the current ATLAS Detector (Type-III cables as there is no Patch Panel 3, see Figure 11.1) can and will be re-used for ITk.

In Section 11.1 an overview of the powering scheme is given followed by a description of the cables and the power supplies. In Section 11.2 the grounding scheme for the ITk Pixel Detector is presented and finally the Detector Control System (DCS) is described in Section 11.3.

11.1 ITk Pixel Powering

11.1.1 Serial Powering (LV)

The ITk Pixel Detector will have around 10,000 detector modules, which hold either one, two or four front-end chips. In this chapter we will consider a typical "powering module", which consists of four front-end chips. Therefore, for single-chip and double-chip modules a powering module is a group of detector modules with a total of four chips. In the following the term "module" refers to a powering module. These (powering) modules are serially powered for low voltage; the high voltage supply to their sensors is done in parallel and is described in Section 11.1.2. The low voltage powering is current driven by a single power supply channel for each SP chain. Commercially developed power supplies will be used which are directly connected to the SP chains.

In the concept of serial powering, the modules are grouped in serial powering (SP) chains, where n modules are connected in series and powered by a constant current source, which has a fast switching behaviour to react to loads changes (i.e. switching of modules). Within

each module, the current is distributed in parallel to the front-end chips; on each chip, two shunt low-dropout (shunt-LDO) regulators generate a constant operating voltage for the digital and analog parts from the constant supply current, while surplus current (i.e current that is not drawn by the chip) is shunted by the regulator to the local module ground.

The foreseen shunt-LDO regulator (see Section 6.2.3) is based on the regulator which is integral to the FE-I4 ASIC already installed and proven in the IBL. The regulators can shunt roughly twice the current that is needed by the analog and digital parts of the front end chip. Hence, if for some reason (broken regulators or wirebonds, for instance) one chip becomes highly ohmic, the fraction of the total current that was to be drawn from that chip can be shunted by the remaining regulators on the module while remaining operational. This is at the cost of increased power consumption on that module. This effect would be worse for modules with two or fewer front-end chips: this is why an SP chain consists of powering modules holding four front-end chips each.

In order to prevent the loss of a full SP chain in case of a single module failure, one Pixel Serial Powering Protection (PSPP) chip (see Section 11.3.2) is connected to the module low voltage line in parallel with each module as part of the on-detector DCS. Each PSPP will be located in vicinity of the detector module, which it controls, optimally as part of the Type-0 services. First tests of the PSPP as part of a serially powered chain have shown that the noise of the system is not increased by using a common return line. This chip monitors the temperature and the voltage drop across a module, and has the capability to bypass the module in the SP chain by shunting the supply current via a bypass transistor. All PSPP chips belonging to one SP chain communicate with a DCS controller chip (Section 11.3) over a single serial communication bus, which currently limits the maximum number of quad modules in one SP chain to 16.

The powering of the PSPP chips (V_{dcs}) and the DCS controller chip (V_{can}) is independent of the module powering. Nevertheless, the PSPP ground needs to be connected to the local module ground. The supply for all PSPP chips in an SP chain is via a single wire. Each PSPP chip uses an internal shunt-LDO regulator to generate its own operation voltage and protect it against the module voltage levels. Therefore, the input current for the PSPP chip needs to be in a certain operation range. To achieve this, each PSPP chip is in series to a resistor. The resistor value needs to be chosen to match the voltage values of the module, which depends on the position of the module in the chain, and to ensure an input current to the PSPP chips within the operation range. The operation range is such that in any configuration of switched on or off modules the provided input current is sufficient to operate the PSPP chip. Adding this PSPP chip to each of the module provides some virtues in case of modules need to be bypassed. On the other hand a complex chip adds risk to the system as well. This risk needs to be evaluated carefully and in case the switching is not beneficial due to too high risk factor by the chips itself, the design of the PSPP can be adopted to do only the monitoring for the DCS.

The DCS controller is powered directly from off-detector. Therefore, the communication

between the DCS controller and the PSPP chips has to be AC-coupled.

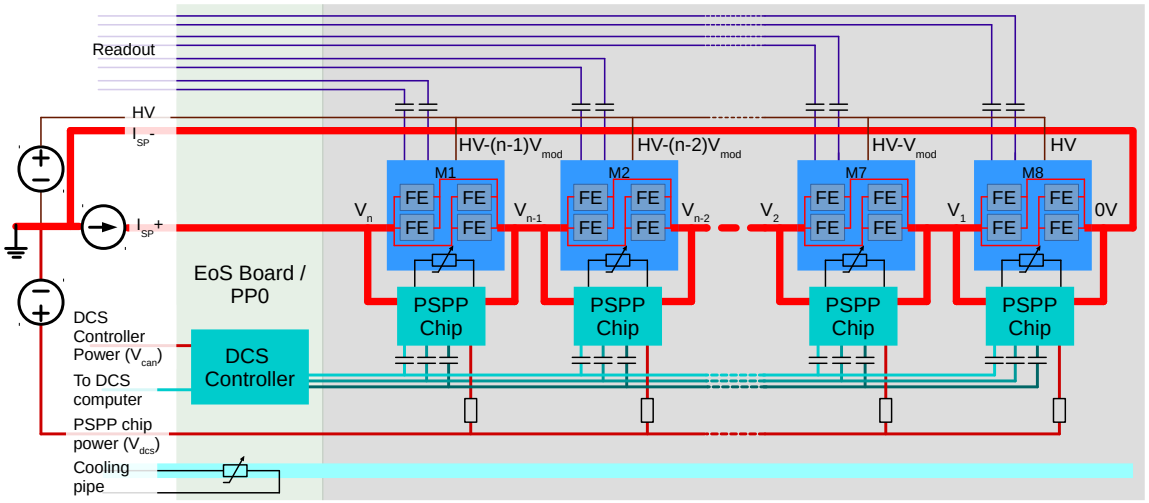


Figure 11.1: Schematic of the Serial Powering distribution on the local support.

Figure 11.1 shows the implementation of the powering lines and the PSPP and DCS controller chips (including their supply and communication lines) on a generic local support structure. The support structure itself is referenced to ground, which is the return of the supply lines. It can be seen that the data lines for the modules need to be AC-coupled because of the differing ground levels of the powering modules in an SP-chain.

The serial powering concept was demonstrated on the first generation of pixel FE chips [157, 158]. First prototypes of SP-chains based on FE-I4 have been assembled and tested [159, 160, 161]; the module performance is very promising and is not adversely affected by the novel powering approach.

Another powering chain is the powering of the optical transmission and receiving boards (opto-boards). These will not be located in the ITk volume, but further outside. Direct power lines from the power supplies in the services caverns will be connected to the opto-boards. In case the voltage drop over the long cables is too large, regulators are foreseen at patch panel 2. This also reduces the power dissipation inside the Type-III cables. The optical transceivers need two voltages, 2.5 V and 1.2 V, furthermore the GBT ASIC needs a supply voltage of 1.2 V as well. These voltages can be generated from either one or two supply lines.

11.1.2 Sensor Bias (HV) and Switch

To further reduce the total amount of material in cables, the sensor bias voltage (HV) will be supplied in parallel to all modules in one SP chain, referenced on each module to the

local module ground.

Due to the serial powering scheme described above, the local module ground is different for each module in an SP chain. This means that the local bias voltage is also different for each module in the chain and has to be set to an overall value that is high enough to ensure full depletion of all sensors in the chain without exceeding the breakdown voltage. Depending on the length of an SP chain and the type of sensor used, this might require two or more separate HV lines for a single SP chain. The LV return line could serve also as the HV return line; alternatively a dedicated HV return line could be added. The choice is currently under discussion.

This scheme introduces a potential single-point failure: if a sensor develops a short it will then draw all the available current, leaving the remaining sensors in the chain unbiased. Therefore a means to isolate each sensor must be implemented. A promising technology for this is an HV switch based on a GaN FET; this is being developed by the ITk Strips community to meet also the Pixel requirements. But until now there is implementation existing, which fits the need of the ITk Pixel system in terms of voltage to be switched, radiation hardness, and supply. Therefore, a simpler and more solid but perhaps less elegant solution is to place a resistor which is capable of withstanding only a certain current in series with each sensor. The resistor serves as a fuse, developing an open and thereby decoupling the sensor from the supply in the case of an unacceptably high current draw. The resistor fuse solution decouples a sensor permanently from the supply without reset possibility, therefore, decoupling by error must be limites as much as possible. To minimise the risk of failure of the HV fuse or switch on a working module, a normally-on solution must be used; this is naturally the case for the resistor-fuse option, but care would be needed to ensure this would be the case with a dedicated switch.

Work is ongoing to determine the best location for the switch or fuse. Space on the modules themselves is very restricted so it will have to be be mounted on the support structures or local electrical services. Due to geometrical differences there may be different solutions in the different regions of the detector: for example in the outer end-caps a dedicated HV patch card could be located on the surface of the rings between modules, while in the barrel region the fuse or switch could be located on each module pigtail or at the end of the stave structure.

11.1.3 Cables and Patch Panels

The power cabling is laid out in sections interconnected by patch panels (PPs) as shown in Figure 11.2. Starting from the detector there are Type-0 cables which run along the stave or ring. At the end of the structure, there is a local patch panel (PP0), which in the outer rings system is a collection of flexible circuits called EoS (for “Edge of Structure”) cards. From there, Type-I cables run to PP1, which is at the end of the Pixel package. At PP1 a connector break is foreseen for the powering cables; the data cables run directly towards

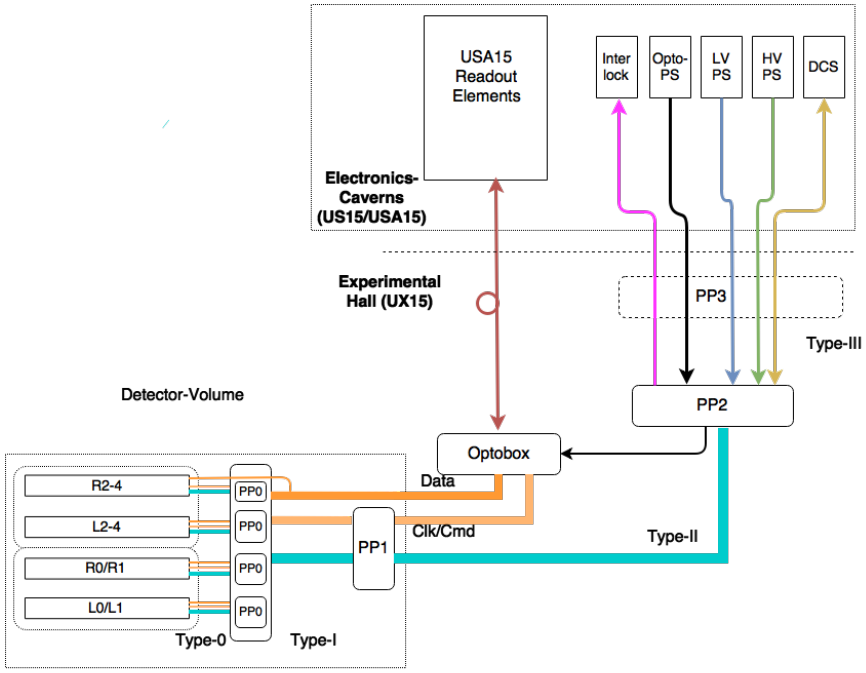


Figure 11.2: Schematic of services path between detector and US(A)15.

the optical transmitters located in "opto-boxes" in the ITk Seal Plate region. Cables from PP1 to PP2 are called Type-II cables and are routed to PP2 which is located in the region of the muon chambers. Active power management takes place at PP2; regulation for the optical transceivers reduces the power loss in the supply cables for these components. For the low and high voltage powering no active element is foreseen, for these line only passive routing is implemented in PP2. Finally, Type-III cables run to the service caverns US15 and USA15, where the power supplies will be located. As mentioned earlier, the Type-III cables from the ATLAS Inner Detector will be re-used for the ITk Pixel Detector; to adapt the grouping of the wires inside these cables to the powering needs of the ITk modules, cables will be combined by re-terminating. This re-termination will be inside the PP2 boxes. The existing Type-III cables will stay with the current connectors, which will connect to the PP2 boxes. These boxes will be located at the same place as now, so that the existing cables will fit in length. Only some DCS cables might be needed on top of the existing ones. These will be installed in addition. A list of cables with more detailed descriptions is given in Section 14.1.

11.1.4 Power Requirements and Dissipation

The main power consumption in the system is in the detector modules, largely due to the front-end chips, with small contributions from the sensors and the PSPP chips. There is an-

Table 11.1: Powering overview for the on-detector system

on-module	Nominal LV current per module	5.6 A
	LV nominal	1.4 V
	Nominal Power per module	7.85 W
	Chip power per area	0.5 W/cm^2
	Sensor power per area	< 0.1 W/cm^2
DCS power		0.15-0.28 W per 4-chip module
Cooling system capability		0.7 W/cm^2

other small contribution from powering the DCS system. The current, voltage, and power values of the on-detector components are listed in Table 11.1. The cooling system (described in Section 14.2) has been designed to have an overall capacity more than adequate to remove all the generated heat.

The supplied current produces power losses and therefore heat in the cables as well; this must be controlled to avoid high environmental temperatures inside the detector. The aim is to limit losses on the cables to approximately 10% of the delivered power in the Type-0, Type-I, and Type-II cables together, and to around 20% in the Type-III cables. This will be achieved with careful choices of cable sizes and materials, balanced with the powering strategy (e.g. the number of modules per SP chain).

11.1.5 The power supply system for the ITk Pixel Detector

The main design requirements for the power supply system are:

- floating power supplies;
- adequate modularity for the operation of the detector;
- compatibility with the grounding policy of ATLAS, particularly the avoidance of ground loops;
- support for all safety strategies including interlocks on all power supply units;
- a local processor on each power supply crate for monitoring and control;
- an interface which allows for remote control and easy integration into the ATLAS-wide DCS;
- location of all power supplies in the US/USA counting rooms, thereby avoiding radiation and magnetic field concerns and taking advantage of the local cooling; and
- modular construction from exchangeable cards, to simplify repairs.

Table 11.2: Nominal and maximum voltages and currents at the load. The numbers marked with (*) are estimated.

	nominal	max values
quad module LV	1.4 V / 5.6A	1.54 V / 8 A
quad planar HV		800 V / 1.5 mA
3D HV		250 V / 1.5 mA
V_{dcs}	2.4 V / 10 mA	2.5 V / 25 mA
V_{can}	3.3 V / 40 mA	4 V / 100 mA
V_{opto}	2.5 V / 25 mA* 1.2 V / 15 mA*	2.75 V / 40 mA* 1.32 V / 20 mA*
V_{gbt}	1.2 V / 500 mA*	1.32 V / 650 mA*

The front-end electronics require only one LV level, which, due to the serial powering concept, must be provided by a current source. Table 11.2 lists the voltage and current requirements of quad modules. The required depletion voltage for the sensors is delivered by the HV supplies, with the maximum required output voltage dependent upon the sensor type.

The on-detector part of the DCS system requires two LV levels: V_{dcs} and V_{can}. Each V_{dcs} channel supplies the PSPP chips belonging to one SP-chain, while V_{can} supplies all DCS controller chips which are connected to a particular CANbus.

Table 11.2 gives nominal and maximum design voltages and currents for the different components as currently foreseen. As the depletion voltage and current of the sensors will change dramatically under irradiation, just the maximum values are listed. For all power supply types only the power required at the load is listed. The output voltages/currents as they are required for the power supply units can only be determined once the modularity for HV, LV and consequently DCS are defined.

The powering of the opto-converter boards including the lpGBTx chips being placed in the optobox requires the following lines: V_{gbt}, V_{optoT}, V_{optoR}, always supply and return.

11.2 Grounding and Shielding

The ITk grounding and shielding (G&S) is the entire array of connected conductive elements of the ITk that attenuates electromagnetic interference (EMI) that interferes with the physics signal reception and the amplified signal data path. The equipment in the G&S system includes the service crates and modules in the service caverns, all of the metal conductor cables and shields that connect electrically with the ITk, and the detectors and data transceivers themselves. Optical fibres having no electrical conductivity are not part of the

G&S system. The discussion on the G&S scheme is based on the successful scheme used in the current ATLAS SCT detector.

The primary strategy for EMI attenuation is the full enclosure of the ITk system in a Faraday cage. The cage constitutes both the shield and the 0-volt reference for the entire ITk system. It needs to be ensured, that all the support structures and the shielding of cables have a proper connection to the Faraday cage for grounding. The cage itself is to be connected to earth ground.

The purpose of the shield is to reduce the propagation of electromagnetic fields from the outside to the inside of the system, so that EMI contribution to electronics noise is negligible. Shielding is achieved using high conductivity materials. For ITk, the shield is mainly constructed from aluminium foils and plates. This shield reduces the electromagnetic field through reflection and absorption of the incident waves, and by reducing capacitive coupling between sensitive internal conductors and external EMI sources. The shielding power is frequency dependent and for a given conductor is a function of its thickness. For ITk the minimum required thickness for copper shield is 18 μm, for aluminium 25 μm, and for carbon fibre plates 5 mm.

The ITk detector is located in an intense external static magnetic field, which is minimally distorted by the low permeability materials used. The shield material and thickness are chosen to leave the static magnetic field undisturbed. The shield EMI attenuation effectiveness is dominated by the necessary seams, joints, and connectors that build up the shield system. Therefore, the mechanical design and assembly of the system demands detailed attention, so that joining metal plates, foil or carbon fibre is continuous, leaving only small gaps or holes. All shield joints must have an inductance comparable to or lower than the shield inductance.

Non-conductive services entering the Faraday cage do so using a hole array with minimum apertures rather than a larger hole, or using a field attenuation collar as appropriate. Every service cable conductor entering the cage has an RF filter which bonds to the cage wall at the entry point. Service cooling tubes have an electrical insulator outside the cage wall as close as is practical. Electrical service cables are fully shielded external to the Faraday cage, and their shields have connector designs that RF bond the shield to the cage with a 360° connection.

Because of external cable shield connections on opposite faces of the Faraday cage, externally induced EMI currents flow on and inside the Faraday cage. An ITk module or module array will DC bond to the cage wall only using the module service cable path. These independent, single paths avoid EMI pickup caused by common impedance coupling.

EMI currents will tend to flow through adjacent modules that reference to different areas of the cage. These ground loop currents will be reduced through collaborative design of the service structures, using the conductive materials of the services themselves. Minimal additional material will be needed for EMI attenuation optimisation.

The power supplies located at PP2, PP3, or the service caverns are part of the ITk grounding and shielding system. The ITk shield skin extends up to them, so each individual power cable is fully bonded to the power supply shield enclosure. Starting from the service cavern, the service cable shields are continuous and fully bonded on both sides of intervening cabinets all the way to the Faraday cage wall. The service cables and cabinets have no earth ties: they are locally floating. The Faraday cage has a single bond to Atlas ground, line voltage earth. The shield conductors are designed so that an accidental line voltage conductor fault will reliably trip the line circuit breaker. For this safety purpose, the shield is tied to earth at a single low impedance point. No additional earth ties are necessary or useful.

In order to decrease capacitive coupling, electrostatic discharge events, and EMI antennae structures, all conductive pieces within ITk have a reliably designed bonding path to the Faraday cage. If a significant conductor is located close to a module, its tie to the cage should be made close to the detector module cage tie so as to minimise stray currents induced on the module.

The G&S design will address cable EMI emissions on data transmission within the cage. The Strip Detectors may be susceptible to the Pixel data cables and thus the emission from the pixel cables will be measured to optimise the design.

ITk power supplies are mostly switch-mode type. The outputs are floating locally, with the referencing potential being the ITk Faraday cage wall. For each detector module or module array, the inside-cage tie to the cage wall carries no DC current, so the detector array end-of-substructure tie points be at the cage wall potential. The power supply design will be tested for EMI emissions from the service cable, which implies that supply outputs will probably need common-mode chokes.

If foil alone is used for a service cable shield, the foil should be wrapped so that the foil seam is parallel to the cable run. 25 μm Aluminium foil thickness will provide sufficient shield performance for this type of construction. If spiral-wrapped foil construction is used, then supplementary techniques such as braid may be needed to achieve equivalent shielding performance to longitudinal seam shielding. Service cables that bond to the cage will be tested for transfer impedance characteristic from 50 kHz to 500 MHz frequency.

11.3 Detector Control System

11.3.1 Overview of the DCS

Operation of the detector is very demanding in terms of monitoring, control and safety. Stable data taking must be ensured as well as the safety of the equipment. The status of the power and the temperatures of the modules as well as of the environment are essential information to enable survey and control of the detector during its lifetime. To achieve all

this, the ITk Pixel Detector control system is being developed in three independent paths: safety, control and diagnostics. These paths differ in granularity, availability, and reliability level. Figure 11.3 shows a diagrammatic overview of the DCS system.

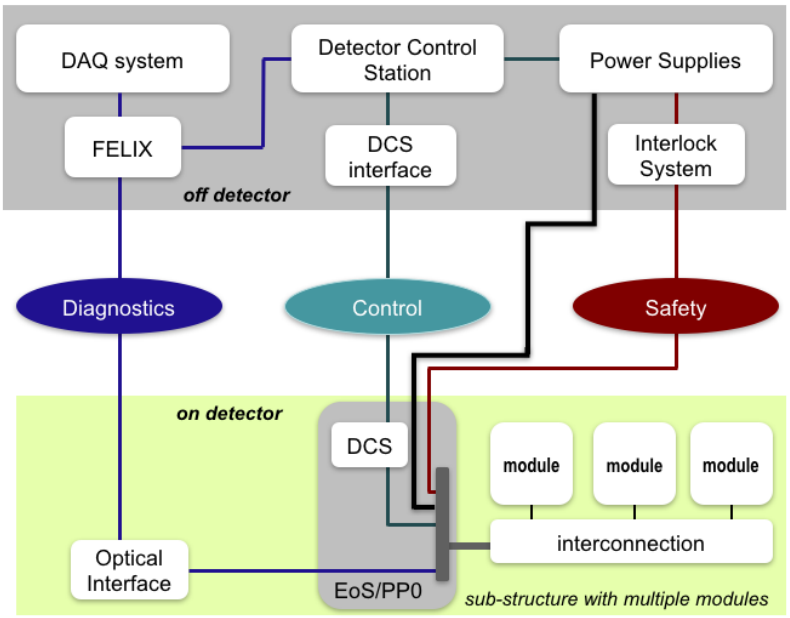


Figure 11.3: Overview on the ITk Pixel Detector Control System.

The safety path is built on a hard-wired interlock system, which acts directly on power supplies or other equipment if the safe operation of the detector can no longer be guaranteed. This system must have the highest reliability, but it does not require a high granularity. It is always in operation, even if the detector is off. One temperature sensor per serial powering chain is foreseen, which automatically provides some redundancy. The Interlock system, which is built in common for all ITk Detectors, is described in more detail in Section 12.3.

The control path is the interface between operator and detector, enabling tasks such as calibration, commissioning, and data taking. It steers all components of the detector and provides monitoring information as feedback. Its design is driven by the requirements of the serial powering. It is made of the DCS network, whose main ingredients are the DCS controllers and the PSPP chips (see Section 11.3.2). The control path is vital to the operation of the detector and therefore requires high reliability. It has its own lines for powering and communication and is therefore independent from the other paths. It must have quite fine granularity, as individual modules must be controllable to ensure reliable control over operations.

The diagnostics path provides the operator with additional monitoring values needed to debug the behaviour of the detector or tune its performance. It delivers the most detailed

information of all the paths, providing feedback from each individual front end chip. It is embedded into the data stream and is extracted at the level of the FELIX cards so no additional cabling is required.

The read-out of the DCS components is slow compared to the bandwidth of the data transmission path used by the front-end chips. For the components which are located close to the modules extensive tests for noise pick up and the impact of module bypassing by the PSPP chips have been done showing no impact on the front-end chip performance at all. To prevent the system from any EMI disturbances the communication lines for the DCS might be implemented as differential signals. Further test are foreseen to be done with RD53A chips and long SP chains.

To allow common operation with all other ATLAS sub detectors, the Pixel DCS will be integrated into the full ATLAS DCS.

11.3.2 Pixel Serial Powering Protection Chip (PSPP)

A prototype of the PSPP chip has been produced in 130 nm CMOS technology. Its main elements are a large bypass transistor and a 10-bit ADC. The ADC provides monitoring of the module's voltage and temperature. The bypass transistor is designed to switch currents of up to 8 A to disable a single module in the serial power chain. It can either be activated automatically if a module is over-voltage or over-temperature, or it can be controlled by remote command. In the current version of the PSPP, the automatic reaction can be disabled as it is not yet clear whether or not it will be required.

A dedicated protocol for PSPP/DCS communication was developed, called the SCB (Serial Control Bus). Up to 16 PSPP chips can be connected to one bus and be controlled by one SCB master, located in the DCS controller chip, which is placed at PP0. SCB was inspired by I2C; however a Hamming code for error detection and Manchester encoding for DC-balancing were added. Furthermore there are separate lines for sending and receiving data and all lines are AC coupled to the master. The PSPP chips are part of the demonstrator programs for the outer barrel and the rings. Irradiation studies of the PSPP chip are ongoing to verify operation at the dose rates foreseen for the innermost pixel layer.

11.4 Timescales

The open questions about powering, power consumption, and modularities for the serial powering will be addressed with dedicated tests in 2018 using RD53 modules. Test setups will be used to evaluate the foreseen baselines and study the effect on the supply system and vice versa. The power supply and services specifications will be checked against these and updated if needed. Decision about the HV single module failure protection, the serial

powering chain composition (location of PSPP chip, modularities, 3D module powering), and consequently power supplies need to be taken during 2018.

The powering for the optical components strongly depends on the chosen technology. First prototype tests using the chosen baseline technology (VTRx+ modules) are expected for 2018 as well, see also Section 19.4.5. These tests will influence the design of the opto part of the powering system.

The services and powering will be reviewed together, with the PDR foreseen in mid-2018, the FDR in mid-to-late 2019, and the PRR at the end of 2020.

12 Common Electronics

The electronics development for the ITk is organized such that the Pixels and Strips groups are each responsible for the electronics which pertains to their specific architectures. However, work that spans both is handled in common by groups responsible for ITk as a whole. This was described in Chapter 23 of the ITk Strip TDR. The structure has not changed but is elaborated more here, especially with regard to the ITk Read-out Group described in Section 12.1 below as well as in Sections 10.4 and 10.6 of this TDR.

Deliverables common to all of ITk, namely proper Grounding and Shielding, Off-Detector DCS, Environmental Monitoring, Luminosity and Beam Protection, are the responsibility of groups within Common Electronics. ITk read-out and its interface to ATLAS TDAQ are coordinated by a single group with representation from both Pixels and Strips. Oversight of the entire ITk Electronics effort is also handled in common with regard to specifications, QA, reliability and design reviews.

The specific components of ITk Common Electronics are covered in the sections below as well as in Chapters 10 and 11 of this TDR and Chapters 9, 12, 16, 17, and 23, of the ITk Strip TDR.

12.1 The ITk-TDAQ Interface and the ITk Read-out Group

The interface between ITk Read-out and ATLAS TDAQ is the responsibility of the ITk Read-out Group. A description of the planned hardware and functional interface is described in Chapter 16 of the ITk Strip TDR with more details specific to Pixels in Chapter 10 of this document and the section immediately below. While the hardware platform for ITk off-detector read-out and control is common across ATLAS, the ITk specific firmware and software components residing in that hardware necessary for the proper functionality of ITk are the responsibility of this group. The ITk requirements have been developed and documented by this group and form the basis for present development work along with regular meetings with the relevant ATLAS TDAQ groups to assure that the interfaces at boundaries of ITk and TDAQ responsibilities are clear.

Data as processed by the FELIX system described in Section 10.4 are distributed via commodity multi-gigabit networks. It is anticipated that at least 100 Gb/s network links will be used throughout the DAQ system. The choice of network protocols and topologies will

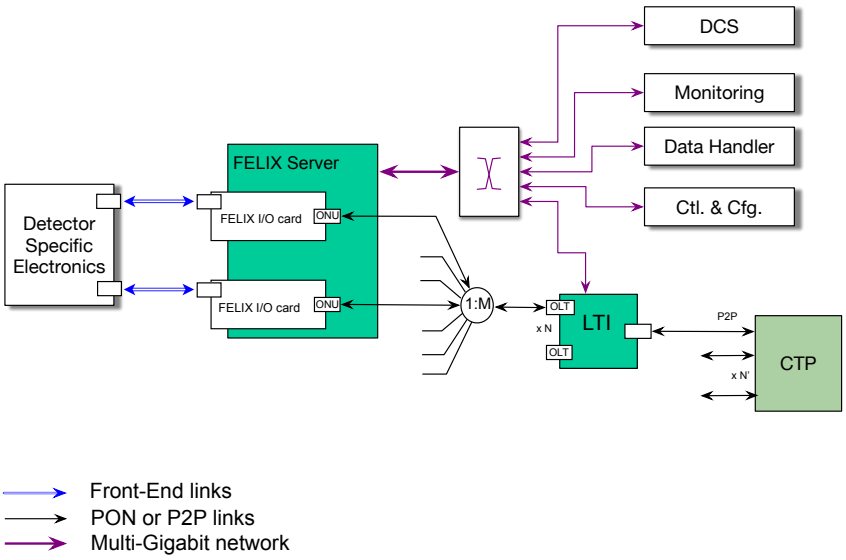


Figure 12.1: Overview block schematic of the off-detector electronics with FELIX as first-stage detector interface and LTI as trigger interface.

depend on the evolution of commodity network technologies, in particular buffering capabilities and end-to-end latencies. The box labelled "Monitoring" in Figure 12.1 relates only to monitoring of event data and performance of the data links and not the environmental or beam monitoring described in this chapter. Also, the separate distribution network from FELIX to DCS in Figure 12.1 will contain information and control mainly for Strips in addition to some Pixel information regarding read-out performance embedded in the data links. Pixel DCS information, aggregated over all modules on one serial power chain, will have a separate wired link to the DCS system. Given that the optical components must be located outside of the Pixel Detector volume because of radiation considerations, instead of using optical links a CAN-bus communication to the controller chip at the end of a structure is established, bypassing FELIX. This allows a reduction of cable mass that would otherwise have to be routed from the end-of-structure regions to the optical components. The Strips DCS design effectively aggregates all the information in a stave side or petal side resulting in 1552 channels of information. Benefiting from optical components on this location, the optical link is used for transmitting DCS information to avoid an excessive number of multi-conductor cables for Strips. The inclusion of this essential Strips DCS information and control in data passing through FELIX requires that FELIX and its network link to DCS be operational whenever ITk Strips is powered. It will be the responsibility of the ITk Readout Group to design how this information is stripped off to be transmitted to DCS and how

control from DCS will be merged with TTC signals into the downlinks to the ITk Detector.

The Data Handler receives data from FELIX through such a network. During data taking, it will decode detector specific information prior to storing them in the Dataflow and also accommodate monitoring functionality. The latter requires trigger information to be sent in addition to the actual event data received from the FE electronics. The Data Handler is also used to manage the configuration of the on-detector electronics and control calibration functionality via the ITk DAQ software described in Section 10.6.

The Data Handler infrastructure is expected to operate on a farm of commodity PCs. Needs for data taking and calibration functionality at the desired speed are estimated based on the performance of a 7^{th} generation XEON processor with about 20 cores. This results in 100 Gb/s per processor, i.e. 5 Gb/s per PC core. Counting the total number of 10 Gb/s data links for Strips and 5 Gb/s data links for Pixels the total bandwidth is expected to be the equivalent of approximately 70,000 Gb/s data links for the baseline read-out scheme with 1 MHz trigger. This implies 14,000 PC cores will be required to service the total ITk for the baseline read-out scheme. This number should be taken as upper limit, expecting significant technology evolution of processor performance.

12.2 Environmental Monitoring

The Common Monitoring system monitors all environmental parameters of the ITk volume, in particular the temperature, humidity, radiation, gas flow and pressure. Additionally, vibration and structural health sensors might be necessary. The number of required sensors varies strongly depending upon the type of sensor; an estimation of the needs is given in the table below. This table takes into account only the sensors, which are read by the common environmental monitoring. Temperature sensors, which are read by the sub-detectors specific DCS are not considered.

Table 12.1: Count of different types of environmental sensors that are planned in the ITk volume.

Sensor type	Number of sensors
Temperature	1000
Humidity	30
Pressure	200
Gas flow	20
Radiation	20
Vibration	6
Strain gauges	40

As can be seen from Table 12.1, the largest number of sensors is required for temperature monitoring. In the case of the ITk pixel detector, all sensors which are not directly part of the staves or ring elements are supervised by this system, for example the temperatures of

air volumes or cable bundles. In order to keep the services which must be routed out of the detector volume to a minimum, some local data processing is required.

CERN is developing a successor to the Embedded Local Monitor Board (ELMB) presently used in the LHC experiments. The proposal for ELMB++ aims to use components developed for high bandwidth optical links (GBTx, GBT-SCA, VTRx etc.) to realise a radiation hard monitoring system which may be deployed in the experimental caverns. As the GBTx and VTRx are relatively expensive items, it is proposed that these are integrated into "HUB-ELMB++" units, each of which may then utilise electrical links to up to 19 "Satellite - ELMB++" boards. In this way, the data for up to 1240 inputs with digitised data may be routed back to the counting room over a single, cost effective VL optical link. Whilst this scheme remains under development, it is most likely that this is going to be used for the ITk common monitoring, especially for the large number of temperature sensors. At the moment, the level of radiation hardness for the new ELMB++ is not known, therefore it is not clear whether the ELMB++ can be used in the most inner part of the Pixel Detector. Anyhow, this is not critical for the temperature sensors as long as 10 kΩ NTCs are used. Their large signals dR/dT allow for signal lines of several meters between sensor and read-out. As to whether the ELMB++ can also be used for the other sensors types, this must still be investigated for each sensor type individually.

12.3 Interlocks

The ITk Common Interlock System is a safety system which protects both the detector and personnel against any risks which may arise. It is a completely hardwired system which acts as a last line of defense for the detector safety. It must be running at all times, but has a coarse granularity and relatively low precision. In the case of the ITk pixel detector, the common interlock system operates in support of sub-detector specific interlock circuits, described in Chapters 8 and 11, which would normally be expected to operate first before the detector is switched on.

As overheating is one of the main risks to all silicon detectors, temperature sensors are located at critical points of the ITk. In the ITk Pixel Detector, each serial powered chain is equipped with a 10 kΩ Negative Temperature Coefficient (NTC) thermistor. As there is always more than one serial powered chain per cooling circuit, redundancy is provided everywhere. NTCs are chosen due to their high radiation hardness and their large signals (dR/dT) which permit the use of two-wire read-out and routing of signals back to the counting rooms.

All signal processing takes place in the Interlock Matrix Crates (IMCs) located in the counting rooms. This location is chosen such that radiation hardness is not required and that the equipment is accessible at all times. The voltage across each temperature sensor is converted to a binary signal by means of a discriminator with a predefined threshold. These interlock signals are then fed into a Complex Programmable Logic Device (CPLD) programmed

with an action matrix, mapping interlock signals onto the associated power supply channels.

In addition to temperature information, signals from the ATLAS Detector Safety System (DSS) providing information such as the status of the accelerator or of the ITk cooling plant are also fed into the CPLD. Certain events may require action upon a large number of channels to protect ITk Detector hardware against major external failures. For safety reasons a negative logic is foreseen, such that the system fails safely if any cables are removed. Also, note that all temperatures are digitised and fed into the Detector Control System for purposes of detector monitoring.

The concept of the Interlock Matrix Crate can be seen in Figure 12.2.

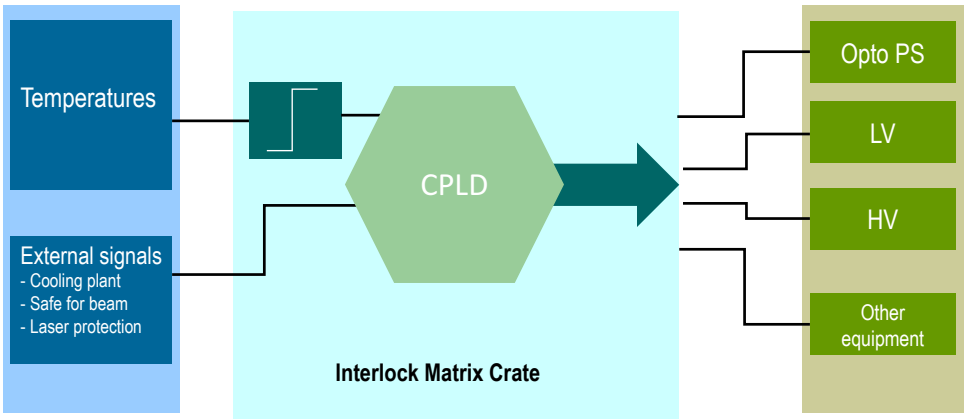


Figure 12.2: Schematic view of the Interlock Matrix Crate.

12.4 Beam Conditions monitoring and protection

This section describes the upgrade of the ATLAS Beam Conditions Monitoring (BCM') as part of the ITk. Installed on a dedicated ring in the retractable part of the Pixel system in the ITk at $r \approx 10$ cm and at the "golden" z of 1.9 m ($\eta \approx 3.6$), it shall provide a handle on the background activity in the tracker, with the aim of aborting LHC beams when danger levels are approached. Additionally it shall provide online bunch-by-bunch luminosity measurement at 1% precision. The expected charged particle flux at this location is predicted [1] to be approximately 0.03 cm^{-2} per pp interaction, or approximately 6 cm^{-2} for the nominal 200 interactions at each bunch crossing (μ-value). Half of the flux is charged hadrons, the remaining half e^+e^- pairs from converted photons, their exact level dependent on the detailed distribution of material, especially in the services, and therefore hard to precisely

predict. These fluxes result in a fluence of 4×10^{15} n_{eq}/cm^2 and TID of 3.3 MGy for the foreseen nominal HL-LHC integrated luminosity of 4000 fb^{-1}.

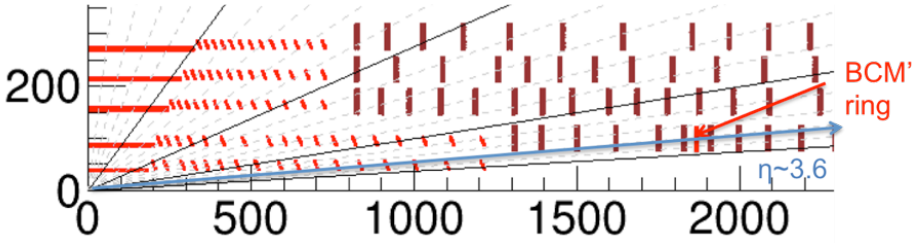


Figure 12.3: A quadrant of the Pixel Detector of the ATLAS ITk with the BCM' location. The inner two layers of the barrel and the innermost end-cap ring reside inside the inner support tube and can be replaced.

Currently, the beam conditions monitoring is provided by two systems. The fast BCM system [162] serves both as a bunch-by-bunch abort and luminosity device. It is backed up by a diamond sensor based version of the LHC developed Beam Loss Monitoring (BLM) system, integrating the charge over a minimum of 40 μs. For the BCM the two functionalities are provided by a resistive splitting of the very fast signal approximately in 1:200 ratio. This compromise leads to non-optimal performance on both tasks. For luminosity the speed results in degraded S/N, so signal amplitude variations induce efficiency drift. The luminosity requires single MIP sensitivity. This is limiting the level of the abort threshold settings, making them hard to justify, especially with only a few circulating bunches in the machine, when the slow BLM's fail to show any activity.

To remedy these deficiencies the BCM' system consists of stations with 3 fully separate devices: luminosity, fast and slow abort. All of them utilize pCVD diamond pad sensors. The 1 cm^2 diamond sensors of luminosity and abort devices are divided into 7 pads of decreasing sizes from 32 to 1 mm^2 to effectively cover the foreseen dynamic range. The time-of-flight flagging of beam induced background used in the current BCM is kept. Background-induced showers originating upstream provoke signals early by $2z/c \approx 12.5$ ns (for the 1.9 m "golden" z location) in 4 stations on the upstream side with respect to the signal from collisions, which are coincident with background on the 4 stations downstream.

The luminosity detector requires stable single MIP sensitivity. Good S/N performance of the electronics should mitigate the effect of varying signal with radiation damage. The requirements on timing can be somewhat relaxed, although a resolution of approx. 5 ns should be kept to monitor low non-collision background levels, and minimize their impact on luminosity measurement. The sweet spot for luminosity measurement for the most robust zero-count algorithm is at zero-count probability of 0.2, translating into an average 1.6 hits per cell ("visible" μ). The biggest pad exhibits a somewhat larger rate at $\mu = 200$,

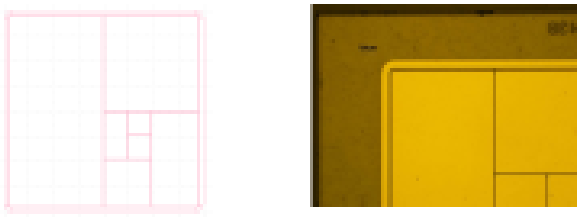


Figure 12.4: Design of the sensor pads of varying size and the top left part of the finished metallization of the prototype.

but the minimum is quite shallow. The statistical precision does not degrade by more than 25% in the range of 0.6 – 3 hits/cell; at an average of 0.2 hits the statistical error doubles.

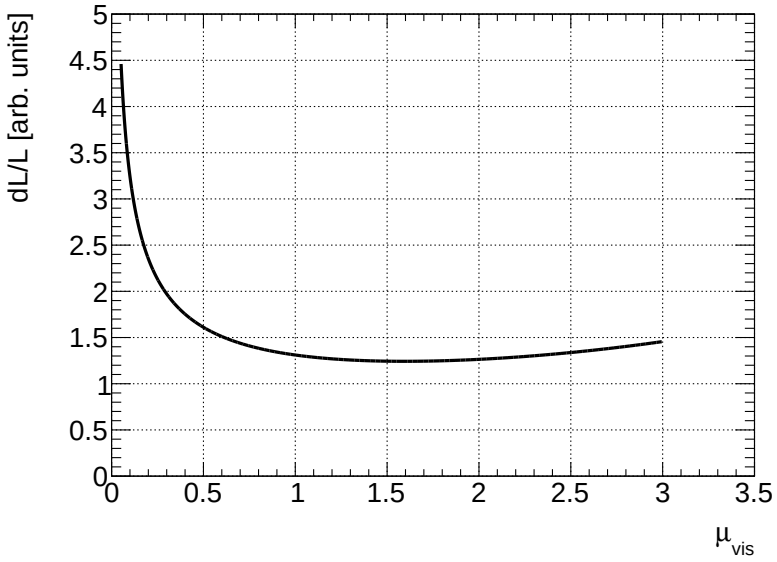


Figure 12.5: Relative statistical error on luminosity dL/L for the zero-count algorithm vs. average count on the detector (μ_{vis}).

Timing at the ns level is, however, required for the fast abort device that relies on timing to detect non-collision background. Return to baseline within approximately 10 ns is required to prevent pile-up. As the danger levels requiring abort are substantial in particle density inside a shower, the S/N requirement is not critical. The abort condition relies on a low gain amplifier feeding a discriminator with the adjustable threshold matched to ITk danger levels. The abort algorithm requires this condition be met by 3 out of 8 stations in two consecutive 12.5 ns time bins, effectively signalling an upstream background induced shower exceeding threshold first in 3/4 upstream stations and 12.5 ns later in 3/4 downstream stations. The latter condition is almost automatically satisfied for all colliding bunches, so it is vital that the signals are fast and there is no spill over into the following time bin from

collision induced signals.

The sensor design implies a detector capacitance from 0.1 to 5 pF for the standard 500 μm thick diamond. The luminosity sensor is likely to get thinned to 200-300 μm to improve radiation robustness. The sensors have to be of prime quality to work at electric fields in excess of 2 V/μm, or 1000 V for the standard thickness. In the BCM project [162] we demonstrated that with careful sensor selection and meticulous QA this is indeed possible at the scale of approximately 20 sensors.

The slow abort device is a single pad diamond coupled to the LHC machine Beam Loss Monitoring system (BLM), integrating the charge over a minimum of 40 μs (half-orbit). The logic of the abort is adapted to diamond current properties by requiring two of the 4 stations per side to cross the threshold, therefore preventing false aborts due to erratic currents in diamond.

BCM' consists of 4 stations per side, 8 in total. Sensors of the luminosity and abort devices are read by a 16-channel custom ASIC, designed in 65 nm CMOS process, and produced in multi-project runs at TSMC. The expected dynamic range needed to cover abort and luminosity is too large ($> 10^4$) for a single front end. Thus two optimized amplifier designs, 8 channels each, will be produced (for economy) on the same reticle, and the 8 non-used channels switched off. Threshold crossing time is digitized in two halves of 12.5 ns (early - upstream background, late - collisions) with 3-bit resolution (1.6 ns bin width). The 2×3 bits per 25 ns result in 2.4 GB/s of data flow for a 40 MHz 8-channel read-out synchronous with the LHC clock. The back-end design relies heavily on developments of functional blocks by CERN RD53 and ATLAS optical links. A prototype front end has been produced in 130 nm; the measurements show a S/N figure of 41 for ^{91}Sr signals from a 300 μm Si diode. Beam tests with the multi-pad structure on diamond have been on-going at PSI with intensities up to 10 MHz/cm^2 and the CERN SPS H6 beam line.

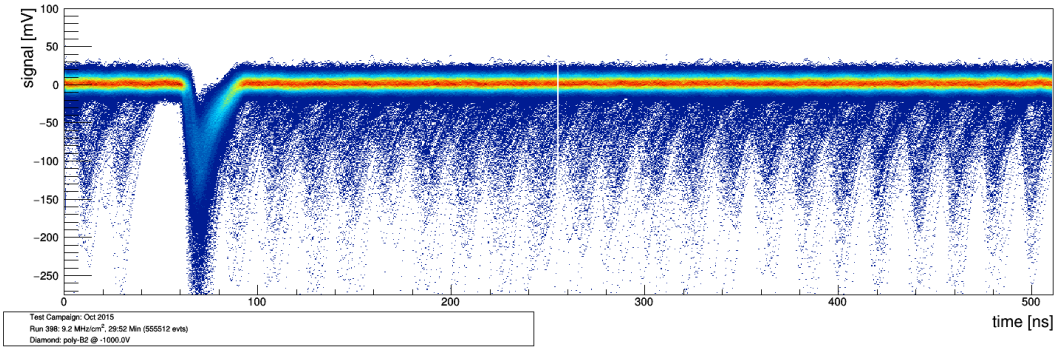


Figure 12.6: Persistency plot of the PSI beam at 9.2 MHz/cm^2 with the BCM' amplifier prototype. The approximately 20 ns time structure is clearly resolved. The absence of the bunch before the triggered one is due to trigger veto.

The services modularity is kept at individual power and data per luminosity/abort device

to minimize the risk; the number of devices to be serviced is small. The exception is the low voltage supply which serves the two ASIC's of a station in parallel. Cooling is envisaged to be able to maintain thermal neutrality; the mechanical disk construction has provision for it anyway. One micro-coax cable per ASIC is needed for transmitting the data at 40 MHz; the receiving end of clock and command can be serviced by twisted-pair links. Data links and DAQ are based on standard ATLAS solutions (FELIX) with dedicated firmware, as it is expected that they shall have sufficient FPGA resources to accommodate the luminosity and abort algorithms. The BLM device only requires a HV cable (approximately 500 V) to measure the current.

13 Local Supports

This chapter describes the support structures of the ITk Pixel Detector, starting with a brief description of the parameters which most acutely affect detector performance and the specifications to which the structures must adhere. The design of the support structures and services is then described, as well as the procedures for loading modules onto the structures. The status of the design qualification and prototyping programmes is presented, quality assurance and quality control during production are discussed, and finally a timeline for the review process will be presented.

13.1 Local Supports Specifications

One of the most relevant parameters affecting the mechanical performance of the detector is the range of temperatures to which the supports will be subjected. Different elements can have different coefficients of thermal expansion (CTEs) so that temperature changes can produce uneven deformations and induce stresses in the structure. This can cause time-dependent stability issues as the modules carried by the local supports move from their known, aligned positions, potentially degrading tracking performance. Also shear failures in the adhesives holding the disparate components together can occur if the design does not properly accommodate CTE mismatches over the specified operational temperature range (OTR). The OTR is set by the minimum coolant temperature of -35°C and the expected module interlock temperature +40°C, plus a margin of 20°C on either side, resulting in an OTR of $-55°\text{C} < T < +60°\text{C}$. The low side corresponds also to the freezing point of the coolant.

Variations in relative humidity can have a similar effect to CTE mismatches on composite structures. Additionally, relative humidity should be kept low to help mitigate galvanic corrosion on electronics and other metallic components. Humidity in the detector will be controlled by flushing the detector volume with dry nitrogen to keep the dew point of the environment at -60°C or lower.

The heat generated by the detector electronics is removed by means of a CO_2 boiling channel in which the generated heat evaporates the liquid coolant up to a maximum 50% vapour quality. The external cooling plant is protected against overpressure by means of release valves set to 130 bar; therefore this value is taken as the maximum design pressure on the detector pipework.

The radiation dose can be considered to be a load as it affects the sensors' leakage current and therefore their power dissipation, which directly affects the detector temperature. Controlling the sensor temperature is vital, as thermal runaway must be avoided at all costs.[1] The thermal performance parameter adopted for the local supports is the Thermal Figure of Merit, or TFM, which is defined below in Section 13.1.2. The required TFM value for a structure depends upon the expected total radiation dose, which itself depends upon a number of geometrical factors; for example the TFM requirement is less stringent for outer layers than it is for inner layers. It has been calculated for a lifetime integrated LHC luminosity of 4000 fb^{-1} for the outer layers, and 2000 fb^{-1} for the innermost layers as they will be replaced part-way through the Phase-II programme.

Once the loads are defined, the performance requirements can be set within an appropriate load configuration. It is beyond the scope of this chapter to describe all the specifications in detail; we will restrict ourselves to summarising geometrical, stability and thermal performance requirements.

13.1.1 Geometrical Performance

By geometrical performance we mean the ability of the structure to limit load-induced deformations. This is important for two reasons.

First, it has relevance for assembling the detector. A specification of 250 μm is set on the minimum clearance between the envelopes of the various local support structures under full loading conditions. These envelopes include the assembly tolerances as well as requiring the structures to be designed with adequate stiffness to avoid gravitational sag and oscillation, guaranteeing that the sub-assemblies can be properly assembled into a complete detector without mechanical clashes.

Second, track-based alignment algorithms require overlap between adjacent modules. Therefore the support structures are required to guarantee that a minimum number of overlapping pixels (five) between two adjacent modules is maintained under all conditions.

The time dependence of the geometrical stability is also an important parameter to control. In Run 2, time-dependent alignment is performed for each LHC fill prior to data reconstruction to determine if the detector, or individual subsystems, have moved significantly compared to a reference alignment. Such detector movements occur on different time scales, and consequently stability requirements are placed over different periods: one day and one month. The one-day stability requirement is meant to ensure that the tracking performance is not degraded by movements that can take place over the duration of an LHC fill. These

[1] Thermal runaway can occur when increasing radiation dose causes sensor currents to rise, thereby increasing their power consumption and raising their temperature, which further increases the leakage current and power, in a positive-feedback cycle, until the module reaches a point where the temperature can no longer be controlled.

are a result of variations of the thermal load in the tracking detector caused by power fluctuations of the front-end electronics due to variations in the trigger rate. The one-month stability requirement is meant to ensure that changes to the environmental conditions of the detector, such as magnet ramps, cooling system cycles, and power cycles do not lead to significant movements of the detector. Significant instabilities on such longer time scales would require an update to the baseline alignment, which serves as a best-guess basis for time-dependent alignment refinements. In other words, these constants describe the actual detector geometry to the best knowledge, decoupling purely time-dependent alignment effects.

The one-day stability requirement is ± 15 μm, ± 3 μm and ± 30 μm for δR, $\delta r\phi$ and δZ respectively. For the month timescale the values are identical with $\delta r\phi$ relaxed to ± 7 μm.

13.1.2 Thermal Performance

The metric for the thermal performance of the pixel local supports is the TFM, defined as the ratio of the temperature difference (ΔT) built up from the evaporating liquid to the hottest point on the sensor to the module's power per unit of area ϕ_{mod}. The units on TFM are $^{\circ}$C cm^2/W. TFM can be thought of as the thermal impedance of the local support: the lower the TFM, the lower the temperature of the sensor for a given heat flux.

The total TFM Γ_{TOT} is the sum of several contributions, which can be categorised as "convective" or "conductive". The convective contribution is related to the Heat Transfer Coefficient (HTC) of the boiling CO_2 in the pipe that sets the temperature rise across the boiling fluid. The conductive contributions depend upon the thermal conductivity coefficient (K) of the materials and the effects of thermal interfaces (such as adhesive layers between bonded parts of the support structure and between modules and support structures). In short one can write:

$$\Gamma_{TOT} = \Gamma_{HTC} + \Gamma_{K}$$

Γ_{TOT} can be measured experimentally on prototypes by imposing a known heat flux from silicon heaters and CO_2 boiling in the cooling pipe. The relationship between the temperature of the evaporating liquid and the temperature on the sensor is given by:

$$T_{\text{sensor}} = \Gamma_{TOT} \cdot \phi_{\text{mod}} + T_{\text{evap}}$$

where ϕ_{mod} is the (temperature-dependent) heat flux from the module in W/cm^2.

Assuming a design evaporation temperature T_{evap}, Γ_{TOT} can be set as a specification for the local support such that, at the end of the detector's life, there is still a margin against thermal runaway. W It is worth mentioning that the required Γ_{TOT} for a given local support

Table 13.1: Main Assumptions for the TFM Calculations

Variable	Value
FE Power [W/cm^2]	0.7
Max Current per Pixel [nA]	10
Evaporation T [°C]	-30
σ_{TFM} [%]	16.7
σ_{TFM} acceptance	3

depends upon a number of factors, including module geometry, module position in the detector (which determines the expected total fluence it will see), and a number of other parameters, for which the assumed values are listed in Table 13.1.

The meaning of most of the parameters in this table is self-evident. However, some of them need more explanation:

- FE Power: the power considered here is the power at the breakdown of the FE chip. Although the chip must be at an extreme and unlikely state for dissipating such a high power, the serial powering approach will force all the modules to draw the same current. It then turns out that that even a rather marginal number of chip might lead to set high power dissipation in the whole SP-Chains (Serial Powering Chain). Specifying 0.7 W/cm^2 as the reference FE power for the TFM we are implicitly calling for designing a system that can thermally cope with modules having extreme currents even this affects marginal number of SP-Chain. In other words, we can say that even if a single module has accidentally four FE chips in it drawing all of them the maximum possible current, none of the modules in the same SP-Chain will become thermally unstable.

- Maximum current per pixel: while the main reason for specifying the TFM is to protect against thermal runaway, the front-end chip is expected to have a limitation on the maximum single pixel current it can handle (10 nA). As explained below, depending upon the sensor type, this current can become the limiting factor even though the runaway limit is not reached.

- σ_{TFM} and acceptance criteria: during production there will be variation of the TFM values both along a structure's length and between individual structures. Ideally we would measure each produced structure's TFM as part of production quality control and reject any that do not have sufficiently low TFM to prevent runaway; however this is expected to be very difficult: an efficient heat load, mimicking a full complement of irradiated modules, would need to be applied to the surface of the structure without damaging it. Until such a technique is developed, target TFM values have been set by extrapolating from previous ATLAS Pixel Detector experience (including the IBL). The TFM values of individual ATLAS pixel support structures have been

measured in the experiment; plotting them in a histogram shows a roughly Gaussian distribution with a long high tail extending to as high as two times the mean value. However such high-end stragglers are very few and the overwhelming majority of the values are under 1.5 times the mean. If we assume that similar production quality can be achieved in ITk Pixel construction, a reasonably safe design specification is therefore to require the target TFM value to be 2/3 of the runaway value, and so the σ of the TFM distribution would need to be less than 16.7% of the mean in order for nearly all the structures (3σ) to have a low enough TFM to prevent thermal runaway. If the local supports prototyping programme shows definitively that a smaller σ can be achieved, and especially if techniques to measure the TFM of bare support structures can be developed, then these design specifications can be relaxed. In any case measures are being taken to ensure as far as possible that the structures' thermal performance will be adequate. Structural design and choice of materials according to key properties (e.g. glue thermal conductivity, carbon foam density) are of course very important. Finite Element Analysis (FEA) studies and prototyping are being employed (as described later in this chapter) to refine the thermal design; these studies also can indicate which features of the design are most critical to good thermal performance. Care must then be taken in production to ensure that the most critical design features are especially well controlled; thicknesses of glue layers and good thermal contact to cooling pipes are examples. Thermal Quality Control procedures to identify structural defects are under development (see Section 13.6).

Because the expected total fluence dose is position dependent, there is a different TFM requirement for each pixel layer. The TFM requirement depends also upon the type of the sensor, as planar sensors dissipate more power than 3D sensors. For 3D sensors the limiting parameter is the single-pixel current, while for planar sensors the limitation is the runaway condition. Table 13.2 summarizes the proposed TFM specifications, which have been extrapolated from the runaway TFM as described above.

Table 13.2: Specifications for the Thermal Figure of Merit expressed in °C cm^2/W. The nominal values, both for the conductive and the convective parts, are listed for each layer. Note that Γ_{HTC} is lower for Layer 0 than for the other layers because the modules in Layer 0 are half as wide in ϕ (single-chip and dual-chip modules rather than quads.)

Layer	Γ_K	Γ_{HTC}	Γ_{TOT}
Layer 0 - 3D	14.4	4.3	18.7
Layer 0 - 100 μm Planar	9.9	4.3	14.2
Layer 1 - 3D	17.4	8.6	26.0
Layer 1 - 100 μm Planar	13.6	8.6	22.3
Layer 2 - 150 μm Planar	11.8	8.6	20.4
Layer 3 - 150 μm Planar	15.1	8.6	23.7
Layer 4 - 150 μm Planar	17.7	8.6	26.3

Convection effects in the detector are not explicitly included in calculating the TFM specification as they are very difficult to estimate accurately. Instead, safety factors are placed on the module power when calculating the TFM, and on the TFM itself by requiring that the local supports be capable of removing all the heat produced by the system.

To qualify the thermal design of a particular local support, the mean value of the TFM of at least three prototypes must be within the specification for the target layer (see Section 13.3 for results).

13.2 Thermo-Mechanical Design

13.2.1 Cooling pipes for the Pixel Detector

The evaporative CO_2 is distributed through the Pixel Detector in thin-walled titanium cooling pipes. The exact geometry of the pipes depends upon the geometry of the subdetector they are serving. However generally speaking, the full titanium cooling lines embedded in the detector volume cannot be made of continuous pipes as provided by industry, so pipe segments must be separately bent to shape then connected together. The connection method of choice in the ITk pixels is orbital welding; care must be taken in designing pipe routing so that orbital welding can be used wherever joins are necessary. The use of appropriate electrical breaks is foreseen to avoid inducing potential damage to the silicon modules.

Outside the detector volume, the cooling pipes are made of stainless steel pipes. A titanium/stainless steel transition is needed, and the cooling circuits have to be globally designed to prevent background electronics noise from being transmitted inside the detector. A special fitting with a titanium/stainless-steel transition and an electrical break functionality was developed for the ATLAS Insertable B-Layer (IBL); it is shown in Figure 13.1. The electrical insulation is implemented by brazing a short ceramic tube to very compact metallic components. The breaks were successfully pressure tested at pressures up to 640 bar and their reliability has been demonstrated during the past three years of IBL operation. It is straightforward to adapt their design to the ITk pixel environment; for example in the outer end-cap they will be placed at the points where the cooling pipe exits the half-ring (see Figure 13.6).

13.2.2 Local Supports for the Outer Barrel Layers

The outer barrel region of the Pixel Detector comprises three sensing layers (Layer 2, Layer 3 and Layer 4) at different radii and each featuring three sections: a central flat part (approximately $-1 \leq \eta \leq 1$) where the pixel modules are parallel to the beam pipe; and two tilted regions, one at either end, where the normal of the active elements forms a 56° angle with

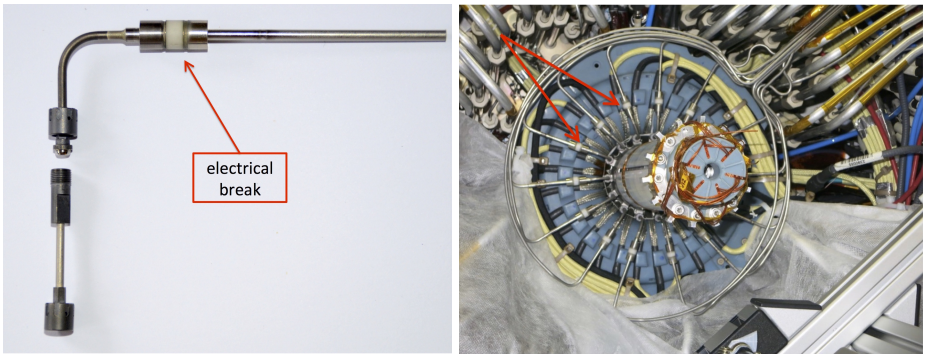


Figure 13.1: Left: Titanium fitting and electrical break developed for the Insertable B-Layer (IBL). Right: Electrical breaks in situ at the ends of the IBL staves.

respect to the beam axis.[2] The proposed local support concept for this area of the detector relies on two main design elements: "cells" to achieve the desired thermal performance, and "longerons" to support the cells and achieve the necessary structural stiffness.

The Module Cells

In a module cell, a silicon module is supported by a pyrolytic graphite plate, used as a heat spreader, which is bonded to a cooling block made of a highly conductive, lightweight material such as aluminium-carbon fibre or graphite. This principle is used in both the flat and inclined regions of the barrel outer layers, resulting in two types of cells: flat (or barrel) and inclined.

As shown in Figure 13.2 each individual cell is connected to a cooling pipe through a soldered base block made of aluminium-carbon fibre. A single thin-walled titanium pipe supplies the coolant for each row of modules in ϕ. In the prototypes to date, this pipe has 2.5 mm inner diameter and 150μm walls, although this may need to be revised to take into account final parameters of the detector. To facilitate soldering and prevent galvanic corrosion, a 5 μm-thick non-magnetic nickel-phosphorous coating is deposited on both the blocks and the pipes using electroless plating. Studies to ensure the long-term durability of the soldered joint are underway, while suitable quality control procedures will be implemented during the production phase to ensure that the coating and soldering steps are performed according to the specifications. To meet TFM requirements, the geometry of the base blocks and in particular their contact area with the cooling pipe have been carefully selected to maximise the local heat transfer coefficient of the evaporative CO_2, which is

[2] The choice of a single module inclination of 56° has been driven by material optimization for physics performances combined with a rational manufacturing. Despite the fact that this optimal angle was initially set for the 5th layer, the same value has been chosen for all the outer layers since the corresponding material increase has been assumed to be negligible.

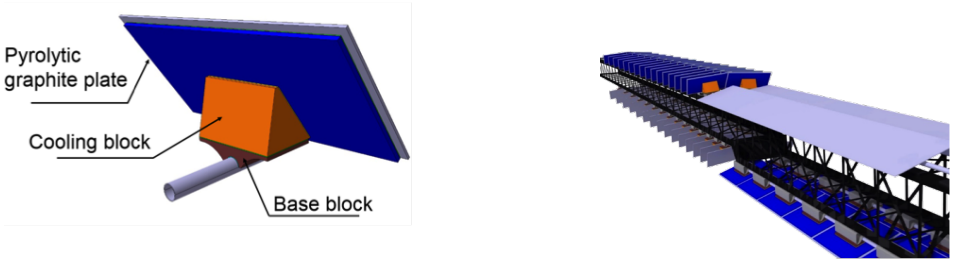


Figure 13.2: Left: Schematic representation of a tilted module cell. Right: A typical longeron (truss construction) supporting four cooling lines.

known to vary substantially with the heat flux. The base and cooling blocks are joined together employing an alignment system based on pinhole-style fiducials to control relative positioning.

The Longerons

The longerons (see Figure 13.2) are made from a blend of high and ultra-high modulus fibres. To take advantage of the radial space between sensors and to maximise the lengthwise stiffness, a single longeron can support cooling pipes from two adjacent layers. Furthermore, up to four rows of modules (i.e. two cooling pipes per layer) can be supported by a single longeron.

Three types of longeron are required to complete the detector geometry. A first type ("L23-4CL") with an approximately rectangular cross section is used to support two cooling lines from Layer 2 and two cooling lines from Layer 3; a second type ("L23-3CL") is trapezoidal in cross section and supports one cooling line from Layer 2 and two cooling lines from Layer 3; the third type ("L4-2CL") supports two cooling lines in Layer 4. The resulting coupling scheme is illustrated in Figure 13.3.

Two different types of construction have been studied for the longerons: a shell version using prepreg plies and longitudinal reinforcements, and a truss structure similar to that originally developed for the ALICE Inner Tracking System [163], and produced with a novel filament-winding process. While the initial results indicate that both types of longeron are viable in terms of stiffness, the truss version has proven to be lighter (due mainly to a more advantageous material distribution) and so has been adopted as the baseline.

The longerons are supported at either end by flanges also made of carbon-composite materials. The individual longerons are fixed to the flanges using a system of pins and screws that ensures the precise positioning of each row of modules and which constrains the rotational degrees of freedom in order to meet the maximum gravitational sag requirements.

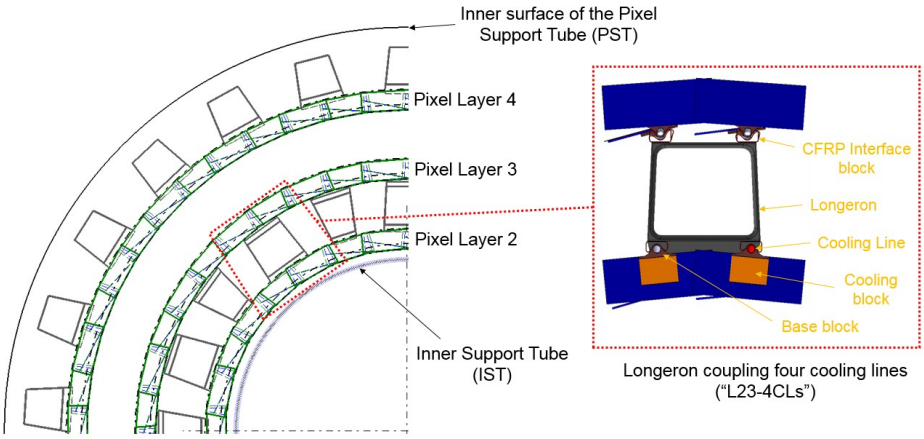


Figure 13.3: R-ϕ view of the three outer pixel barrel layers showing the cross section of the different longerons and the proposed coupling scheme.

Outer Barrel Assembly

The assembly sequence to obtain a finished local support for the pixel outer barrel is as follows (a longeron coupling two cooling lines from Layer 2 and two cooling lines from Layer 3 is taken as reference for the description):

1. The assembly of the so-called "functional longeron" begins with the soldering of the base blocks to the titanium pipes. This step is performed in a precision jig made in two parts, one for each of the detector layers to be integrated in the same support structure as shown in Figure 13.4. The nickel-coated base blocks are placed in the jig with respect to a reference coordinate system using the pinhole-based alignment system described above, while the pipes are fixed using multiple clamps. Once the soldering step is completed for the cooling lines of the two layers, they are bonded to a cured longeron using masks to apply the adhesive. Before the assembly is removed from the soldering jig, machined inserts and survey targets are glued at both ends of the longeron with respect to the same reference coordinate system used to position the base blocks. Subsequently, these inserts will serve to locate and fix the longeron to the end-flanges.

2. Following a first set of electrical tests, the stave services are then integrated inside of the functional longeron. The services, which are split at $z = 0$, are inserted from both sides and fixed to the longeron at $z = 0$. They exit the longeron at both ends though a large opening which facilitates the routing in R-ϕ. The flexible extensions used to connect to the module pigtails leave the carbon fibre structure through the space available between the spokes of the truss. The assembly is then fixed to a handling frame designed to replicate the end-support conditions found in the real detector, where it will remain until it is finally installed in the detector flanges.

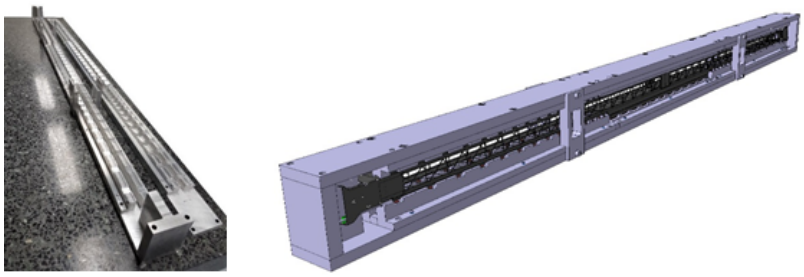


Figure 13.4: Soldering jig used to assemble to functional longeron.

3. The bare module cells are produced in batches using dedicated tooling. The cell assembly jigs rely on a machined bottom plate where the cooling blocks are positioned using the holes of the locator system. Following the deposition of the adhesive layer on the blocks using a mask, the Thermal pyrolytic graphite (TPG) plates are glued to the cooling blocks employing dowel pins for alignment. The thermal performance of the bare cells will be tested using non-destructive techniques to ensure that the bonded interfaces are sound before committing an electrical module to a given cell. A small number of cells will be also tested mechanically, measuring the deformation for a given load to ensure that the heat spreader has not been damaged during assembly.

4. The current concept assumes that loading of modules onto the local supports is a two-step process: First, the pixel modules (including the module flexes) are bonded to the individual cells in the step referred hereafter as "module loading"; then the cells loaded with the pixel modules are attached to the corresponding base blocks of the functional longeron in a step known as "cell integration". However, at the time of writing, optimisation of these procedures are under active development. For more details on this topic the reader is referred to Section 13.5 of this document. Once the cells and modules are integrated on the functional longeron, the module flexes are connected to the stave services and the electrical tests for the different serial powering chains can begin. Then, a metrological survey is carried out to measure the position of each individual module with respect to the targets bonded to the carbon structure.

5. After the metrological survey is completed, the assembly is transferred from the handling frame to the installation tooling. This tooling provides the required kinematics to place the longeron in its final position on the end-flanges while preventing collisions with the adjacent module rows. Similarly, it can be used to remove a defective support structure for repair or replacement.

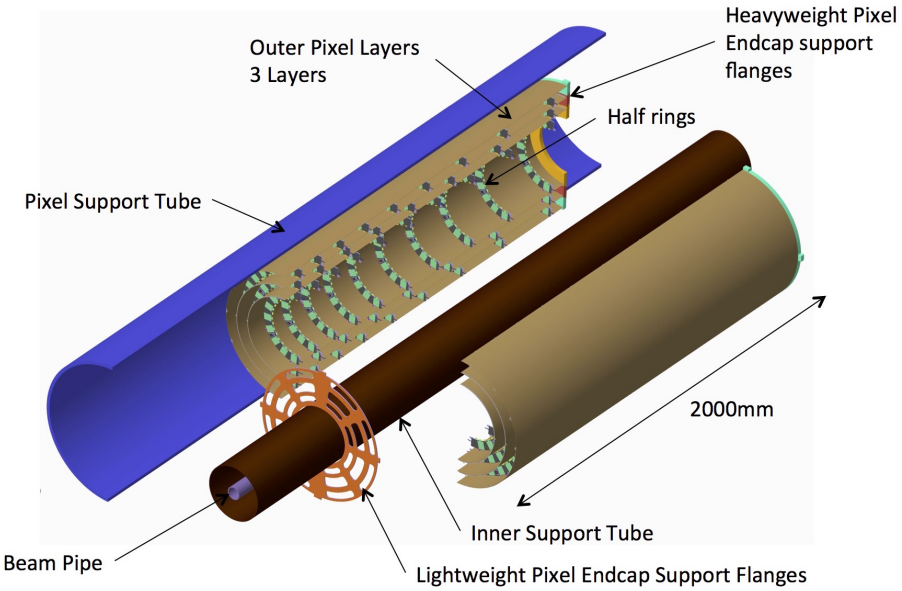


Figure 13.5: Exploded 3D drawing of one Outer End-cap.

13.2.3 Local Supports for the Outer End-caps

The outer-end-cap local supports, shown in Figure 13.5, are a modular system. Pixel modules are arranged on three layers of half-ring-shaped support structures which are held in place by carbon fibre half-cylinders. The half-cylinders are connected together at their ends with a low-mass flange at $z \simeq 1200$ mm and a heavier flange at $z \simeq 3000$ mm to form three concentric full cylinders.

The Half-Rings

The end-cap half-rings are manufactured as carbon fibre / Allcomp carbon foam / carbon fibre "sandwiches" with embedded titanium cooling pipes and copper-Kapton bus tapes (to carry power and slow controls communications) as shown in Figure 13.6. Graphite-loaded Hysol 9396 adhesive[3] is used to bond the cooling pipes and bus tapes into precisely-machined indentations in the foam. Pixel modules are placed on alternating sides of a half-ring, giving active ϕ overlap. PP0 cards are mounted on the surfaces between the modules, to transfer power and communication to the modules via the bus tapes.

[3] This is the same adhesive, doping and process used for the ITk Strip Detector; see Chapters 9 and 10 of the ITk Strip TDR.

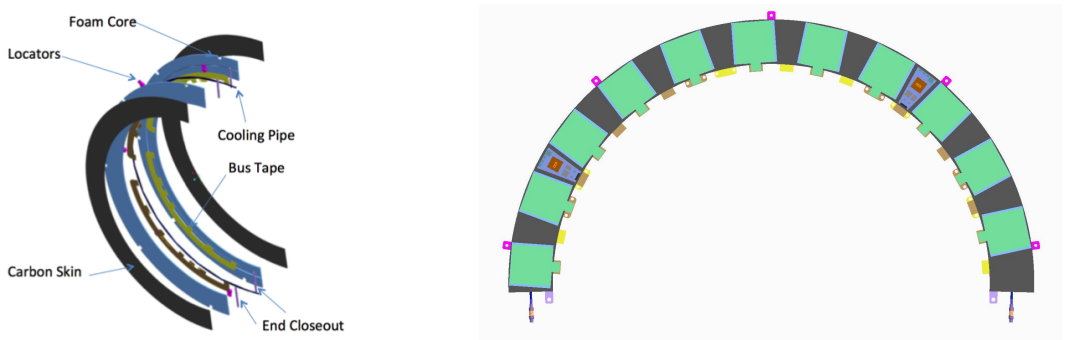


Figure 13.6: Left: an exploded view of a half-ring showing the internal components. Right: a view of the surface of a half-ring showing pixel modules (green) and PP0 or "EoS" cards (blue). The electrical breaks can be seen in the right-hand drawing, on both ends of the cooling pipe as it emerges from the half-ring.

The Supporting Cylinders

The half-rings in a given layer are mounted on a thin carbon fibre half cylinder which defines the position of each half-ring and supports the services which connect the half-rings to PP1. During assembly, pairs of half-cylinders are mated together, starting from the innermost, and attached to end supports to form a complete end-cap.

End-cap Assembly

The assembly of the pixel end-cap starts with the manufacture of the half-cylinders and is followed by the mounting of the on-cylinder services and finally the insertion of the half-rings, connecting the services and testing. The foreseen steps are as follows:

1. Each half-cylinder of the support structure will be assembled and geometrically checked. Tooling will be required to attach the various fixations and interfaces to the half-rings, seams and the end supports.

2. The type-I services will be assembled into ring-specific harnesses on a handling jig, tested, and then transferred onto the corresponding half-cylinder using the handling jigs. Beyond the end of the half-cylinders, the services will be supported on temporary structures which will provide sacrificial test connections to avoid damage to the final connections.

3. Tested half-rings will be inserted into their half-cylinder transversely and fastened into position. Connections will then be made between the modules and the high-speed links and the various on-ring interface cards for power and DCS. The connections to the cooling structures will be made using orbital welding. After each ring is installed it will have a basic test to ensure proper connectivity of all the services.

Once half-cylinders are completed they will be fully tested at operating temperature to verify the full functionality of all modules. Finally, tested half-cylinders will be integrated to form the final end-cap.

4. Once the end-cap is completed and has passed all the relevant QC steps, it will be made ready for transport, installed into its shipping container together with temperature, humidity and shock monitoring systems and shipped to CERN. At CERN the end-cap will be reception tested.

13.2.4 Local Supports for the Innermost Layers

The inner pixel system is defined as the portion of the detector which lies within the Inner Support Tube (IST). The envelope is cylindrical in shape and covers both the active volume, from -3000 to 3000 mm, as well as any eventual service volume at higher Z along the beam axis (such additional service volume has yet to be defined.)

The inner system is divided into three distinct sections which cover three zones along the beam axis:

- the barrel: ~ -240 mm $< z <\sim 240$ mm,
- the barrel rings: ~ 240 mm $< |z| <\sim 1100$ mm (each end), and
- the inner end-cap: ~ 1100 mm $< |z| <\sim 3000$ mm (each end).

Broadly speaking, the inner system has two layers (Layer 0 and Layer 1) throughout these three distinct sections, although in the inner end-cap region the boundary between the two layers becomes blurred by intermediate rings. Layer 0 will be composed entirely of single-chip dual modules with 3D-silicon sensors. Layer 1 will be composed of double-chip quad modules with either 3D or planar silicon sensors. The module technology to be used for the few intermediate rings in the inner end-cap is yet to be decided.

Due to the high data rates expected in the inner system, the baseline servicing scheme for the inner system calls for one pair of data lines per chip on Layer 0, and one pair of data lines per two chips on Layer 1. This servicing load dominates the space required and structural design for the inner pixel system overall.

There are currently two proposals for the inner system mechanics; they are similar but with two important differences:

- The "Inclined Inner" proposal (see Figure 13.7) uses a double-shell support structure in the barrel region (one shell for each of layers 0 and 1), and places its "barrel ring" modules onto inclined rings, with a slight angle of incidence (as in the outer inclined layouts). Thermal pyrolytic graphite (TPG) based tiles are used in both the barrel and ring regions.

Figure 13.7: Ring layouts in the "Inclined Inner" (left) and "Inner Alternative" (right) proposals. Modules are depicted as orange rectangles.

- The "Inner Alternative" proposal (see Figure 13.7) uses a single-shell support structure with staves and rings made of carbon foam technology; the "barrel ring" modules are placed perpendicular to the beam axis, but coupled into structures that span layers 0 and 1.

The "Inclined Inner" structures for layer 0 are similar to those in the outer system, which are described in Section 13.2.2. Layer 1 will be populated entirely using quad modules. The resulting flat section is equivalent to that found in any of the barrel outer layers, and thus it is implemented using module cells identical to those described in Section 13.2.2. Flat module cells are arranged in a half-ring configuration to implement both the inclined and end-cap regions of Layer 1. The thermal path to the boiling CO_2 is shortened by connecting the cells to semi-annular cooling lines as shown in Figure 13.7. The half-rings are built around two hollow carbon fibre profiles, which are used to support the various cells and provide the required mechanical stiffness to the assembly. An equivalent design is used for the 90° rings used in the end-cap regions.

The Inner Alternative staves and rings utilize high thermal-conductivity carbon foam to transfer heat from the module-mount surface to the titanium cooling pipe (which is the same pipe as in the Inclined Inner). The barrel staves have modules mounted on only one side. A carbon-laminate facesheet is co-cured to the carbon foam. The foam forms a triangular shape around the pipe, which is embedded with a graphite-loaded epoxy having a bulk thermal conductivity of approximately 3 W/mK. The back side of the stave covered with curved piece of 150 μm carbon fibre. In the Inner Alternative barrel rings and end-cap, the universal structure is a ring (in the barrel ring region, this is a coupled ring which spans two layers with light carbon spokes). The rings are mechanically symmetric, with the titanium cooling pipe sandwiched between two layers of co-cured carbon foam/facesheet assemblies. The modules are symmetric but rotated on the ring structure (about the beam axis) in order to provide overlap.

Table 13.3: Measurement of the Thermal Figure of Merit for the different outer-barrel-detector samples (with measurement accuracy depending on the numbers of times the cell has been tested).

Sample	Type	Target Layer	# samples	TFM [°C cm^2/W]
	Flat Cell (quad heater)	1-4	3	18.0 ± 0.5
	Tilted Cell (dual heater)	1-4	1	17.1 ± 0.6
	Flat Cell (dual heater)	0	1	11.0 ± 0.5
	Tilted Cell (single heater)	0	1	18.1 ± 0.1

13.3 Local Support Qualification and Prototyping

This section discusses design qualification using mechanical and thermal Finite Element Analyses (FEAs) and presents results of measurements on prototype structures.

13.3.1 Outer Barrel and Baseline Inclined Inner Systems

Several dedicated prototypes (thermo-fluidic, thermal, thermo-mechanical and module loading) are currently under test to qualify the inclined support structure concept used in the outer barrel and the innermost system (Inclined Inner). A prototyping campaign was launched in 2015 to demonstrate that the local support concept proposed for the outer barrel region fulfils the basic thermal and stability requirements established in Section 13.1.

A number of module cells of each type (i.e. tilted and flat) were produced to evaluate the thermal performance. To carry out the measurements, a homogeneous heat load of 0.7 W/cm^2 was applied using silicon heaters bonded on the TPG plates of the cells. A stand-alone cooling plant supplied saturated CO_2, while glued NTC sensors were used to monitor the temperature in the silicon surface at various locations. Before the thermal tests the cells were cycled forty times between -30°C and +30°C to stress the interfaces and assess their robustness. Then the TFM was measured at the most unfavourable location in the heaters. The results obtained for the flat and tilted cells are shown in Table 13.3; they fulfil the requirements established for layers 1 to 4 (assuming 3D sensors in the innermost layers). An additional number of flat and tilted cells were built using smaller heaters to replicate the dual and single FE chip modules featured in the innermost layer of the inclined layouts. The TFM results obtained with these prototypes were also compatible with the requirements established for Layer 0.

The local support as presented above relies on extracting the heat from a particularly localized source. To qualify the design a long prototype was constructed to check that the high values of HTC required for standard operation can be achieved at any point along the full

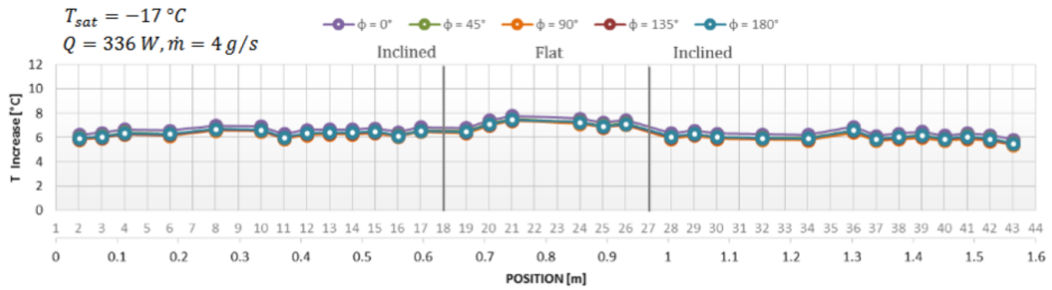


Figure 13.8: Variation of the temperature increase (i.e. the temperature difference measured by the NTCs of the blocks with and without the nominal heat load applied to the full structure) along the length of the cooling line for various azimuthal orientations of the thermo-fluidic prototype.

length of a standard cooling channel where the vapour quality will change from one location to the next. This initial "thermo-fluidic" prototype employed a 1.6 m long stainless steel pipe similar in cross section to the titanium tubes (a more realistic prototype employing a titanium tube is being constructed now - see below). A series of copper blocks were brazed to the pipe at locations corresponding to the module positions in Layer 3. Polyimide heaters and NTC sensors were glued to each copper block to simulate the power dissipation in the pixel modules and monitor the variation of the temperature along the cooling pipe. Tests were then performed for different CO_2 saturation temperatures, mass flows, heat loads and azimuthal orientations of the prototype. The results obtained were very encouraging and independent of the position in ϕ (see Figure 13.8), exhibiting minor variations of the HTC along the cooling line and reasonable temperature and pressure drops for heat loads similar to those expected at the end of the service life of the future Pixel Detector.

Following the encouraging results obtained in these initial tests, a 1.6 m long prototype featuring a single titanium cooling line populated with module cells is under construction as part of a larger "demonstrator programme" launched at the end of 2016. It will be used to evaluate the change in the thermal performance along the longeron and to get a first indication of the TFM differences expected due to manufacturing and assembly variability. To guarantee that the performance does not degrade under the normal operation of the detector, testing will be take place before and after the prototype has undergone a representative number of thermal and pressure cycles.

The mechanical performance of the longerons is also being studied. Several 1 m long prototypes of the truss and shell longerons were manufactured and tested under load to validate the corresponding finite element models, obtaining excellent agreement between the experimental results and the numerical predictions (see Figure 13.9). These FEA models were then used to predict the response of fully loaded longerons for the outermost pixel layers of an earlier hypothetical layout with similar physical parameters to the current layout, assuming constrained end-rotations (as a first approximation the mass of the electrical services was homogeneously distributed along the length of the longerons). As illustrated in

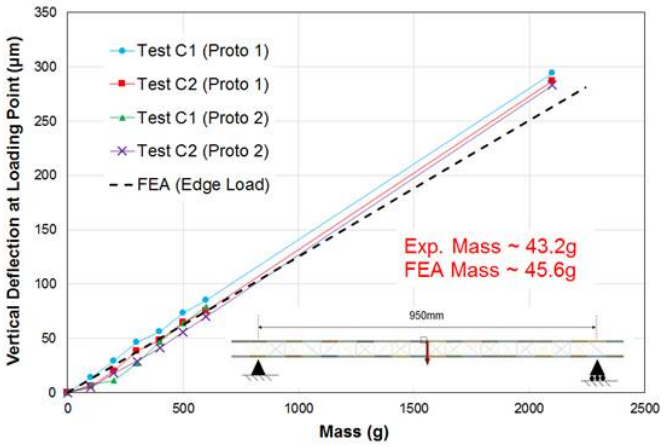


Figure 13.9: Comparison between the experimental results and the numerical estimates obtained with FEA models for truss longerons tested in a three-point bending configuration.

Figure 13.10 for the truss case the results obtained were very encouraging, indicating that the local support concept would fulfil the stiffness and frequency requirements regardless of the position in ϕ. As part of the demonstrator programme mentioned above, a large size prototype is currently under construction to study the thermo-mechanical response of the proposed local support concept for the outer barrel. Based on an earlier version of the fully inclined layout, the geometry selected for this prototype corresponds to a 1.6 m long truss longeron coupling two cooling lines from Layer 2 and two cooling lines from Layer 3 (i.e. L23-4CLs). In this case the cells will be loaded with bare silicon dummies rather than heaters to replicate the CTE mismatch between the local supports and the modules. Using an environmental chamber, this prototype will be cooled down to a pre-defined temperature while the deformations in the structure are monitored using appropriate equipment (e.g. strain gauges, camera, digital image correlation). It should be noted that while the uniform cooling provided by an environmental chamber does not necessarily reproduce the thermal load expected in the detector, it will provide a useful tool to validate the corresponding detailed finite element models so that they can then be used to optimise the design of the longeron if needed. A more realistic setup, including a CO_2 cooling plant, is under development for system tests of a full-size longeron loaded with silicon modules and heaters.

Structural performance for the inner Inclined system is still in the early stages of examination. However, models have validated the general divisions of the inner system (into barrel, barrel rings, and end-cap) and the concept of supporting each of these three sections from their endpoints (see Figure 13.11). This periodicity of supports is deemed to be feasible and to provide ample structural rigidity and stability.

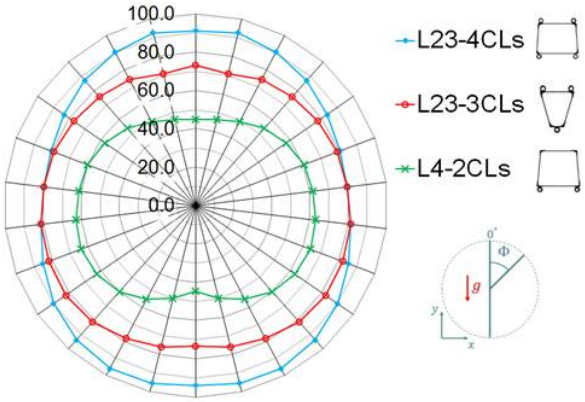


Figure 13.10: Estimates of the total deflection (in μm) as a function of ϕ for 1.6 m long, fully loaded truss longerons used to support the three layers of the pixel outer barrel.

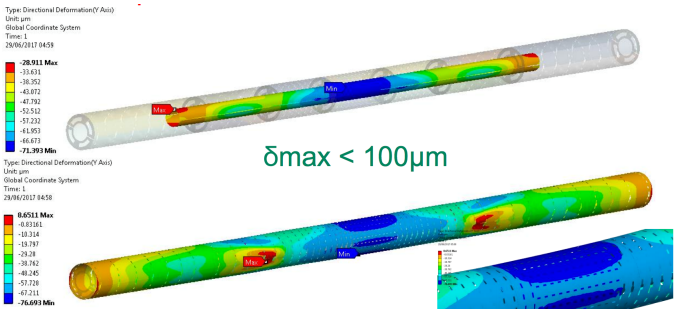


Figure 13.11: Expected deflections for the Baseline "Inclined Inner" system supported at four points (ends and two intermediate). Similar results are obtained for the "Inner Alternative" layout.

13.3.2 Outer End-caps

The thermal performance of the outer-end-cap half-rings has been studied using a three-dimensional FEA simulation, including temperature-dependent sensor power, to investigate temperature rises and headroom against thermal runaway.

In the half-rings, heat generated in the sensor and the read-out electronics is conducted through the carbon foam to the cooling pipe. A number of intermediate factors contribute to the thermal path resistance, including the small-surface-area joint between the foam and the 2.275 mm-outer-diameter cooling pipe, various thin material layers (e.g. carbon fibre facings, titanium pipe wall), and glue interfaces (module to facing, facing to foam).

Figure 13.12 shows the simulated temperature distribution on a representative azimuthal section of a Layer-2 ring.

Three layer-2 prototype half-ring structures, with varying levels of completeness, have been

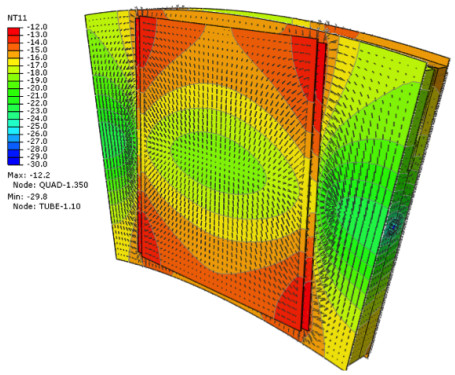


Figure 13.12: FEA Sensor Temperature bands at 4000 fb^{-1} and 3.5×10^{15} n_{eq}/cm^2, assuming sensor bias voltage of 550 V and CO_2 evaporation temperature of -30°C. It should be noted that this module temperature distribution is dominated by the read-out power density.

Figure 13.13: A prototype half-ring in its aluminium handling and transport frame.

constructed and used to set up thermal deformation and thermal performance tests, and to develop the module-loading system. A photo of a completed prototype half-ring is shown in Figure 13.13. A mini-production of four layer-3 protoype half-rings is currently underway. The first of the four is complete, has been partially populated with thermal modules, and has undergone TFM measurement with promising initial results; the TFM values measured in the areas of the half-ring most representative of the final half-ring geometry varied from 22 to 24 °C cm^2/W. This is slightly lower than predicted by FEA, but it should be noted that necessary approximations in the simulation of for example evaporative cooling and the expected power distribution across the front-end chips lead to an estimated uncertainty of about ± 2 °C cm^2/W in the predicted TFM. Another of these rings will be electrically fully realistic (including prototype EoS cards and electrical breaks) and will be used for full electrical tests with up to 12 FE-I4 quad modules, with results expected in early 2018. The other rings' TFMs will be measured, and they will be subjected to thermal cycling, applying thermal QC procedures (see Section 13.6) before and after.

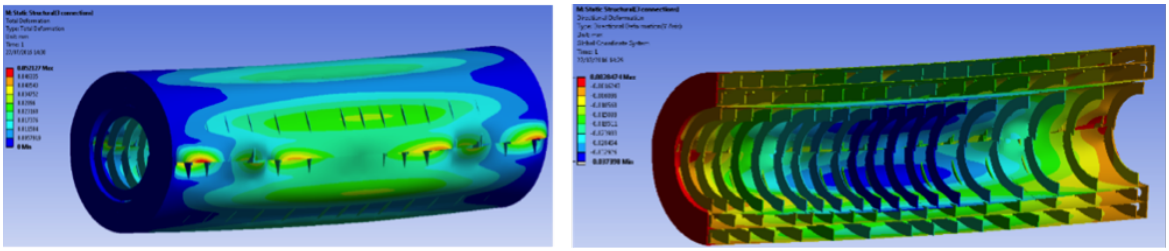


Figure 13.14: FEA static deformation results of the full pixel end-cap model with supports and splits at 3 and 9 o'clock and half-shells connected at 3 positions along the seams show (on the left) the maximum overall deformation = 0.052 mm and (on the right) the maximum gravitation sag of (inner) half-rings = 0.037 mm. For the same end-cap model with supports at 3 and 9 o'clock and splits at 12 and 6 o'clock, the maximum gravitation sag of the half-rings = 0.047 mm.

The mechanical performance of the outer end-caps is also being studied. A modal and deformational analysis of an outer end-cap has been performed to investigate the critical parameters for meeting the positional stability requirements. Inputs to the finite element analysis (FEA) included the 3D CAD model of the design, mass estimates of the half-shells, end flanges, half-rings with modules, all ancillary electronics, cables and cooling pipes, and material properties of the half-cylinders, end flanges and half-rings. The analysis used a simplified parametric model of the geometry with nominal material properties and boundary/global support conditions.[4]

The initial analysis showed that full-cylinder shells supported on a horizontal plane have 30% less static deflection compared to the same shells supported vertically and that half-cylinders showed the least static deflection when split horizontally, although this effect is largely mitigated by adding connection points along the length of the half-shells. Radially fixed half-rings have 5-9% higher resonance frequencies compared to radially free half-rings; inner and middle rings require three fixations to achieve a resonant frequencies >100Hz, with the outer ring requiring four.

A full end-cap model with the best features from the earlier sensitivity studies was then developed. The results of this analysis showed that the full end-cap model has less than 100 μm half-ring displacement when there are at least three connection points between half-shells along the seams between the end flanges, and when the various half-rings have the above-mentioned numbers of radial connections to their shells. (see Figure 13.14).

The first resonant mode is axial at 27 Hz and the second resonant mode is a bending of the inner half-shells between connections along the seams at 38 Hz. Assuming the measured long-term averaged acceleration spectral density of less than 10^{-9} g^2/Hz is reproduced in the ITk, the minimum resonant frequency of the end-cap structure exceeds the few-Hz level at which the modal deformation would approach the positional stability requirement.

[4] Note that an earlier ITk layout with larger z coverage and more half-rings was used for these investigations; the analysis will be repeated with the updated layout in early 2018.

Table 13.4: Summary of results of vibrational measurements on four M55J laminates, compared to FEA

Lay-up	Layers	Thickness (mm)	Modal Frequency (Hz)					Simulation or Test
			1st	2nd	3rd	4th	5th	
[0,45,-45,90]s,	8	0.62	3.5	10.1	21.1	36.1	55.7	*ANSYS*
			3.3	11.3	22.5	38.5	58.8	*TEST*
0,90,90,0,90,90,0	7	0.55	5.1	14.8	31.0	52.2	81.1	*ANSYS*
			5.0	14.5	31.2	52.8	81.5	*TEST*
90,0,90,0,90,0,90	7	0.55	7.1	20.5	43.0	60.6	112.5	*ANSYS*
			6.8	19.9	42.8	73.3	111.3	*TEST*
[90,45,-45,0]s	8	0.62	7.9	22.9	48.0	68.5	125.5	*ANSYS*
			7.8	22.5	48.3	82.8	126.0	*TEST*
100GPa solid	1	0.55	5.5	16.0	33.5	57.4	87.6	*ANSYS*
100GPa solid	1	0.62	6.2	18.0	37.8	64.7	98.7	*ANSYS*

A series of prototype 600 mm long middle half-cylinders have been manufactured with different carbon fibre lay-ups. The pre-preg carbon fibre material used is M55J fibre in cyanate ester resin with an areal weight of 80 g/m^2. The vibrational response of these shells have been measured and their CTEs estimated using classical laminate theory. In general, lay-ups with circumferential fibres at the outer surfaces of the laminate lead to higher modal frequencies. Quasi-isotropic laminates give rise to near-zero CTEs with minimal directional variations. Table 13.4 shows a summary of the measurements made on four prototype laminates together with the results of FEA simulations using a full laminate definition based on manufacturer's data for the properties of a unidirectional lamina. The preferred laminate is [90,45,-45,0]s. In summary, the prototyping results show that the detailed FEA model of half-cylinders is reasonably accurate and increases the confidence in the global FEA simulation.

13.4 Local Electrical Services

13.4.1 Outer Barrel

For the outer pixel barrel layers services, one of the options being evaluated for electrical servicing is based on two independent flexes: one to carry the modules' serial power and one for data transmission. This choice of two independent flexes is the result of optimising the combination of currently available technologies, industrial processes and cost.

The power flex is designed to supply the serial current up to 8 A with limited loss. This flex includes the DCS lines and the return path for the powering current and will hold the PSPP chips (see Section 11.3.2).

The data flex carries the high-voltage lines, as well as the very high-rate data transmission lines. It is desirable to maximise the number of module transmission lines per flex in order to reduce the number of flexes to be inserted inside the longeron.

To reduce the amount of material in the services, the thinnest double sided copper-polyimide laminate industrially available is used: 9 μm copper on 35 μm Kapton. The initial design is based on a maximum radiation length of $X/X_0 = 0.3\%$, smeared over a 20 mm wide flex. To further reduce the amount of material, selective plated holes will be implemented for both types of flexes. As explained in Section 10.3.3, twisted pairs are considered as well as a backup solution in case of insufficient performance of data transmission lines on the flex.

For modules on a single cooling line, four sets of four-layer flexes are needed: one each for the inclined and the barrel on both sides. The flexes run inside the longeron in the z direction, towards the patch panels at either end. Small flexible service extensions exit the carbon fibre truss structure though the openings between the spokes and are connected to flexible pigtails on the module flexes using separate connectors for data and power; see Figure 13.15. The module flexes will be bent to connect to the stave flex on the side of the longeron; see Figure 13.15.

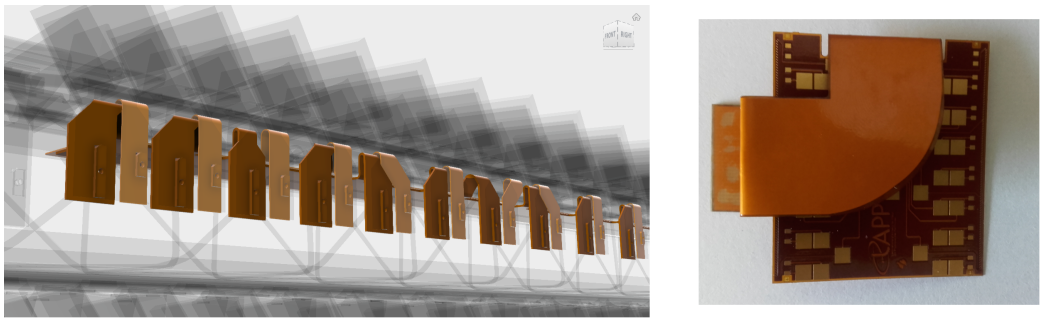


Figure 13.15: Left: Mechanical layout of the data (dark/orange) and power (light/yellow) flexes for the layer 3 inclined C-side. Each flex has independent tails with dedicated connectors exiting in front of each module location. Right: Dummy Flex Module bending test.

To ensure modularity and simplify the integration and the reworking capabilities, the stave flex will be equipped with connectors. There will be two Hirose connectors on the module side for power (BM25 series) and data (BM24 series), and a Samtec Firefly connector at the end of stave.[5]

Dummy modules with bare silicon pads and realistic module flexes are being produced and will be equipped with the Hirose connectors to perform a large panel of qualification tests on thermal cycling, bending, electrical test before/after irradiation and mating and de-mating cycles.

[5] Hirose Electric Co, Ltd. and Samtec are companies specializing in the manufacture of electrical connectors.

The transition between the electrical flexes and the Type-I cables at PP0 is done through a FireFly Samtec connector. This connector is qualified as radiation hard and gives the possibility, when needed, to include additional active electronic components such as signal repeaters. For the pipes exiting the staves at PP0, fittings and electrical breaks are described in Section 13.2.

13.4.2 Outer End-caps

As in the outer barrel, the data chain and the power/DCS chain for the outer end-cap system are separate. Clock and commands and data will be carried directly between PP1 and the modules on individual Type-I cables, as described in detail in Chapter 10 of this document.

The power/DCS chain (carrying low voltage for the module ASICs, sensor bias, DCS chip supply voltage, DCS controller voltage, and the CANbus data interface to the DCS controller) consists of several components: a flexible multi-layer copper-Kapton bus tape embedded in the centre of each half-ring (see Section 13.2.3), PP0-style patch cards (referred to as "EoS" or "End of Stave" cards) glued to the surface of the half-ring in the spaces between the modules, and Type-I cables which lead from the EoS cards along the inner surfaces of the supporting half-cylinders and through the high-z end-cap end flange to PP1.

The bus tapes are connected to the modules and to the EoS cards via connectorised tabs which extend outside the volume of the half-ring and which connect to extensions of the module hybrids and to flexible extensions of the EoS cards (see Figure 13.16). The bus tapes may also carry the PSPP chips.

13.4.3 Innermost System

The services for the inner system represent a challenge in both space management and integration as thousands of connections are required. Detailed estimates of the volume required for services are underway, and prototypes of service bundles are being constructed. Adjustments may have to be made to the existing envelope between the inner and outer systems to make the best use of the space available.

13.5 Module Loading and Replacement

The fixation of modules on local supports with thermal glue ("module loading") poses several constraints. Nine thousand modules will have to be loaded in two years' time; this will represent seven times the loading done for the current ATLAS Pixel Detector. Assembly rate and parallelisation of this activity become key points for matching the ITk schedule.

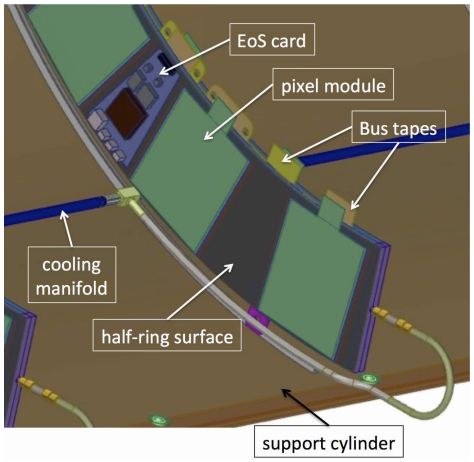


Figure 13.16: Conceptual drawing showing the interconnection of bus tapes (shown in yellow and gold), EoS cards (blue), and modules (green) in the outer end-cap system. Type-I cables (not shown) connect to the EoS cards and modules at the outer rims of the rings (grey) and run along the inside of the support cylinder (brown). The cooling pipe manifold is shown in dark blue.

Since each inclined structure can hold up to 52 modules, damage during assembly must be strictly guarded against in order to minimise the need for risky and difficult repairs. Repeatability and accuracy of tooling and processes are fundamental requirements. Experience gained from the IBL and ATLAS-Pixel projects suggests that the assembly process should be compatible with rework; this is one of the main considerations in the module glue qualification campaign which, in addition to examining the thermal and mechanical properties of glues before and after irradiation, must also demonstrate that removal and replacement of a module after loading will be possible.

13.5.1 Module Loading for the Outer Barrel and Innermost Systems

Module loading on the barrel structures will be carried out at several sites in parallel. The local supports for the outer barrel will be assembled in a handling frame (see Figure 13.17) which will support the structure during services assembly, module loading, and services connection and testing, to minimise mishandling risks. This frame will also be used to ship the structure between assembly sites, store it safely, and support it during all QC procedures.

Module loading will be performed using a Coordinate Measuring Machine (CMM), with contact and contactless measurement capabilities. The QC done during loading will comprise measuring the local support and module geometry, the glue deposition uniformity, and the module placement accuracy. Services integration and testing will be done prior to module loading, to minimise services-induced failures.

Modules and services will be different for the Outermost and Innermost local support. However the type of glue, the glue deposition technique, and the module pick-up and placement tools will be similar in order to efficiently control the effects of tooling on the quality of the loading process. Each local support will be equipped with fiducial reference marks which will be measured and related to the structure assembly frame reference system. As the module's fiducial marks are engraved on the sensor but not on the visible part during loading, wire bond pads or sensor edges will be used to locate the module in the reference assembly frame.

Two different placement techniques are under development. The first technique consists of using the CMM itself to pick up and place modules on the local support; this offers high precision and repeatability. The second technique uses a holding jig with reference pins to locate and position local supports and modules (IBL-like loading). This technique is easier to duplicate and therefore offers greater potential for increased assembly rate. Both module placement techniques will be used for outer barrel loading: the jig assembly technique will be used for inclined module loading and the CMM (Figure 13.18) will be used for the flat barrel section, where clearances between adjacent modules will require more accuracy.

Three different glue deposition techniques are being investigated: a stamp technique, a mask deposition technique and an automated syringe dispenser. The relative suitability of these procedures is highly dependent on glue characteristics such as viscosity and pot life. Depending on the polymerization time of the glue, the addition of UV glue dots to stabilize the module and increase the assembly rate may be considered.

Recall that the outer barrel layout is based on a main support structure which holds cooling cells which in turn hold the module. Loading modules on cells and then cells on the main support is likely most suitable for inclined modules; loading cells on the main support and then modules on cells is probably more suitable for the barrel section. Both assembly schemes are being considered for further development.

The connection of services to modules is done sequentially after loading, so no electrical test will be performed on a stave until it is fully loaded. A temporary EoS connection board will be used at the PP0 location during testing and qualification to minimise the number of mating cycles on the final electrical connectors. These boards will be directly attached to the handling frame. A survey will be performed after module loading to locate each module with respect to the local support frame. This will enable determination of the module positions after each future integration step into the whole Pixel Detector. A full functionality test and burn-in on the local support structure will be performed following module loading; this can happen in parallel with the loading of other supports.

13.5.2 Module Loading for the Outer End-caps

Loading of modules to outer-end-cap half-rings will be carried out at a different location to ring assembly. Bare half-rings will be shipped to the loading site, each in its own test and

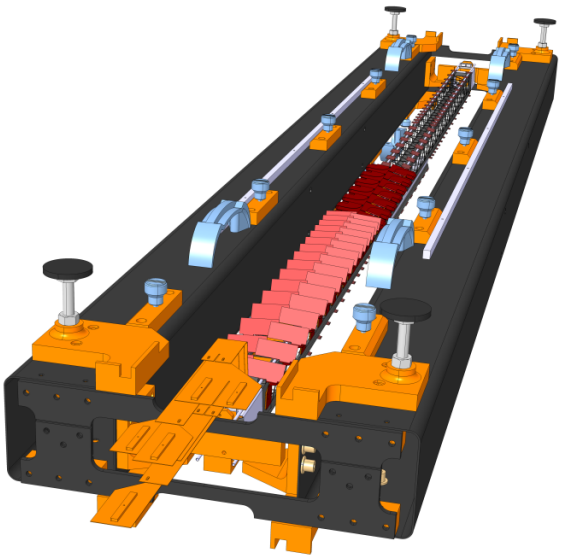


Figure 13.17: Outer layer local support structure in its handling frame.

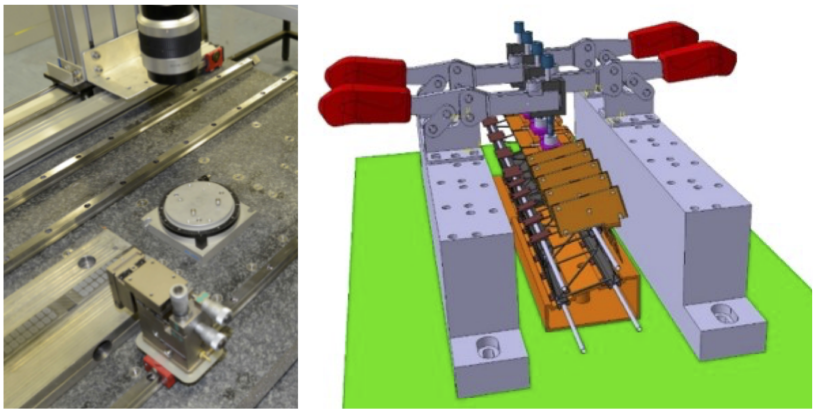


Figure 13.18: Left: jig, module handling tool, glue deposition tool for inclined-module loading. Right: Clamping tool concept for loading vertical inclined modules.

handling frame which incorporates three fiducials (precision optical pinholes); the position of the half-ring mounting lugs is referenced to these when the frames are made. Tested quad modules and EoS cards will also be shipped to the module loading sites from the manufacturing sites.

Acceptance tests will be performed on the received parts to ensure that no damage has been sustained during shipment. The handling frames and half-rings will be inspected for damage, using a microscope and camera. It may be necessary to re-check the surface topography of the half-rings before module loading takes place. The modules and EoS cards will be tested with the minimum subset of tests which can guarantee full functionality. The bus tapes will undergo a simple electrical continuity test and possibly a simple HV breakdown test. The modules and EoS cards will be inspected visually using a microscope.

EoS cards will be mounted first; as they do not require highly precise placement, they will be positioned using simple custom jigs.

The module mounting system is based on a custom linear motor gantry (see Figure 13.19). It is equipped with a camera, magnifying optics, and software and so can measure the fiducial positions and calculate the required module positions.

The half-ring is placed on an aluminium baseplate and put under the gantry. Modules are picked up using a movable bridge with a vacuum chuck on manually adjustable stages; coarse alignment is achieved by dowelling the bridges to the baseplate (again see Figure 13.19). The stages then allow precision alignment of the module to the camera crosshairs. Once the module is aligned, the bridge is withdrawn (leaving the module in the chuck), adhesive is applied to the the half-ring surface using a syringe dispenser built into the gantry, and the bridge replaced and left until the adhesive has cured. UV-cured tags could be used to allow the bridges to be withdrawn earlier.

Once mounting is complete, module positions are surveyed using a laser-based measurement system which is built into the gantry. The module and EoS tails are then connected to the bus tape tabs and the completed half-ring is tested for functionality, using a dark box with dry gas purge and CO_2 cooling. Again the minimum possible subset of electrical tests to determine functionality will be performed; any failing module will be removed from the half-ring and replaced. Fully functional half-rings will then be shipped to the relevant institute for integration into the end-cap.

13.6 Local Support Quality Assurance and Quality Control

Quality Assurance (QA) and Quality Control (QC) measures must be applied appropriately to the local support structures (see Section 19.1 and Section 14.1 of the ITk Strip TDR for the definition of and distinction between QA and QC.)

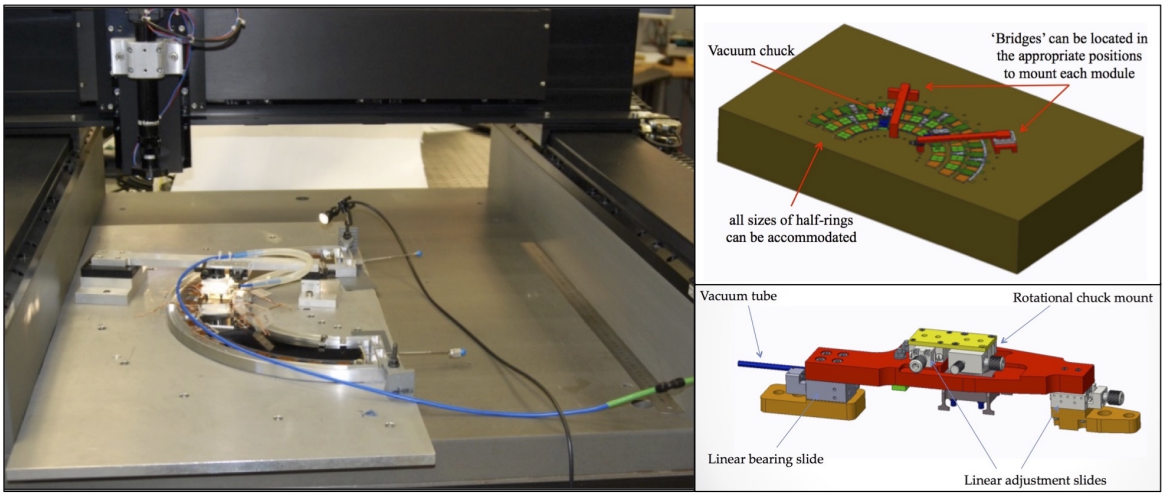


Figure 13.19: Left: Gantry with inner half-ring in its handling frame. Upper right: the half-ring-loading concept. Lower right: a drawing of a module placement bridge.

Design Qualification is performed on prototypes during the R&D phase and is reported on above in Section 13.3; also system-level test setups are being prepared in various production sites, see for example Section 10.5. In addition, materials like glues for detector assembly are under qualification to the expected total radiation doses (see Section 2.3) in a material irradiation campaign.

Quality Assurance requires production-quality parts; thorough systematic and destructive tests are planned in the pre-production phase, and during production small batches will be tested with the same methods.

Quality Control refers to the process of confirming that every production item meets specifications. Individual components such as cooling pipes, cells, carbon structures, electrical modules etc. will be fully qualified before being assembled into larger structures which are then themselves subjected to QC tests. Mechanical, thermal, and electrical tests are foreseen, optimized to balance potential additional risk and time with the need for quality control. All QC results will be stored in a database.

Items that were assembled at other sites must pass a reception test (electrical test at room temperature) upon arrival to the assembly site. Before insertion into the overall structure an additional test is conducted (electrical and optical, connection tests of pressuring cooling loops at room temperature), after which temporary cooling fittings and electrical connectors are removed.

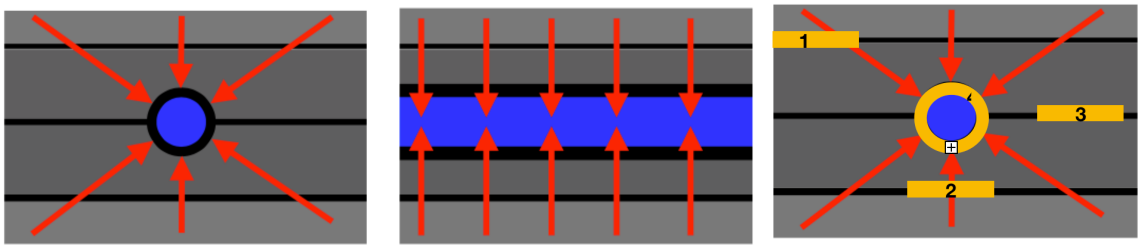


Figure 13.20: Expected heat flow (red arrows) in the radial (left-hand plot) and azimuthal (center plot) transverse sections: the CFRP facesheets are shown in light grey, the carbon foam is shown in dark grey. The cooling pipe is shown in blue and the black lines indicate glue layers. The right-hand plot shows possible construction defects as described in the text.

13.6.1 Thermal Quality Control

Before populating with pixel modules, bare structures should be carefully analysed to reject any that are defective. Two different techniques to detect defects are under development on outer-end-cap half-rings, based on measuring the temperature distribution on the surface of the half-ring using an infrared fast-video camera during the cooling process.

Transverse cross-sections of a half-ring, together with arrows depicting the internal heat flow when modules are mounted on the ring surface, are shown in Figure 13.20; also shown are several types of internal defects which can degrade the thermal performance: 1) delamination of the carbon fibre facesheet from the carbon foam, occurring near the edge of the half-ring; 2) the same sort of delamination occurring immediately above the cooling pipe; 3) a defect in the glue joint between foam layers; and 4) a defect in the glue joint between the cooling pipe and the foam.

In the first technique under development to detect such defects in bare rings, the half-ring is placed in a heated (50°C) climate chamber to provide a heat load, and a valve is opened suddenly in the coolant supply (5°C) going to the pipe, producing a rapid change in the temperature profile on the surface of the ring, which is recorded by the thermal video camera. This technique is sensitive to defects on and immediately above or below the pipe. The second technique uses a Peltier element underneath the ring rather than coolant through the pipe, and is sensitive to delaminations that are not aligned with the pipe.

The techniques have been demonstrated using small ring sections on which defects have been included deliberately during production. A drawing of one of the pieces, which has three different types of defects, is shown in the left-hand diagram of Figure 13.21. The piece was tested using the cooling-pipe technique described above; the center and right-hand plots in Figure 13.21 shows the results of this measurement for both sides of the structure. The delamination just above the cooling pipe is clearly visible. A software technique has also been developed to analyse the temperature profiles (coloured arrows in Figure 13.21)

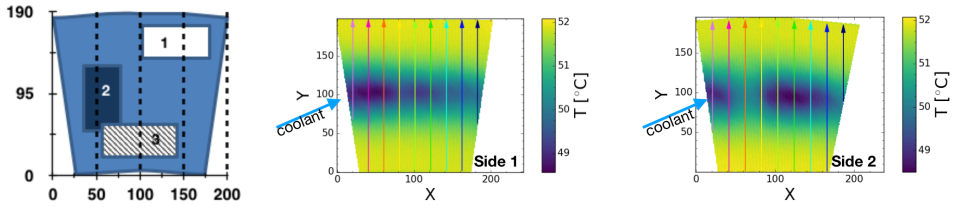


Figure 13.21: Left: a ring test piece incorporating three types of defects: 1) CFRP-foam delamination on side 1, 2) CFRP-foam delamination (above the cooling pipe) on side 2, and 3) no glue between foam layers. Center: thermograph of side 1. Right: thermograph of side 2. A clear temperature gradient is seen along the pipe in both thermographs; this corresponds to the delamination above the cooling pipe.

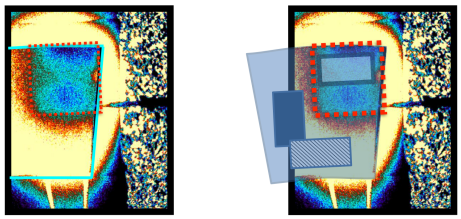


Figure 13.22: Infrared images obtained by applying the Peltier technique described in the text. The Peltier element area is highlighted in red and the ring piece is outlined in light blue. In the right-hand image the ring-piece defect 'map' is overlaid with the infrared image, showing that the temperature non-uniformity overlaps with the delamination defect.

in the direction transverse to the pipe, fitting them to Gaussian functions. Plotting the minimum values of the Gaussians as a function of the direction along the cooling pipe, the defects appear as maxima in the distribution. This enhances the visibility of the defects beyond the sensitivity of the human eye and also has potential for automatic defect flagging.

The Peltier technique described above is able to identify delaminations that are not aligned with the pipe. A 2×2 cm^2 Peltier element was placed underneath the same test piece, in direct contact with side 2, opposite to the delamination but aligned with it. The result of this measurement is shown in Figure 13.22 where the delamination is visible in the infrared camera images.

These techniques are being optimised in both software and hardware for application to full half-rings. The goal is to have an automised setup that can scan over a half-ring, and analysis software that can identify defects, minimising the time and the person power required.

13.7 Decision path and timeline

The specification review of the local supports is tentatively scheduled for April 2018 and will be followed by the Preliminary Design Review in Q3 2018.

The Final Design Review will take place in Q2 2019, using the experience accumulated with RD53A modules and the first results from ITkPix-V1 modules; this review will launch the pre-production of loaded local supports where pre-production modules will be used.

The qualification process for the local supports is rather complex and covers the thermo-mechanical, hydraulic and electrical aspects of the detector. Section 13.3 addresses the prototyping plan required for the qualification of the design.

The Production Readiness Review is scheduled for the end of 2019; this early date is chosen to be able to launch the production of the mechanics at the beginning of 2020 and avoid an excessive overlap with the loading phase, starting in Q2 2021. Production of loaded supports is scheduled to finish in mid-2023.

14 Services

This chapter describes the ITk services outside of the ITk Detector volume. Services for Pixels inside the detector volume are covered along with Local Supports in Chapter 13 and their patch panels as well as power supplies are covered in Chapter 11 to complete the description of the full powering system of the ITk. Powering for the Strips component of ITk was described in Chapter 17 of the ITk Strip TDR and cooling in Chapter 19. More information is now available about the cabling needs of ITk than was available at the time of the writing of the ITk Strip TDR and so that is further elaborated in Section 14.1 below. Likewise, the space available for cooling pipes and the needs for cooling cable trays and patch panels are now better described in Section 14.2 below.

14.1 Cable Inventory

A list of all external cables required to service the ITk is shown in Table 14.1 along with some commentary on each cable run. Currently, some cable counts are awaiting final choices of the Pixel community regarding the number of modules to be placed on each serial powering line. By convention, Type-II cables run from Patch Panel 1 (PP1), at the entrance to the ITk detector, to Patch Panel 2 (PP2), inside the Muon Spectrometer volume, thus running along the end plates of the cryostat. Type-III cables either run from PP2 to PP3 or to the service caverns USA15 and US15. Type-IV cables run the last segment from PP3 to USA15 and US15. The ITk will reuse all Type-IV and most Type-III cables, replacing the SCT Type-III cables and all the Pixel and Strip Type-II cables. The SCT Type-III cables are to be replaced because the present cables do not reach PP2 and would require splicing a short extension onto each cable, a procedure that will cost significant amounts of time during Long Shutdown 3 and also represent a reliability concern. All the Type-II cables will be replaced because they will be activated at the end of Run 2, especially the cable segments and connectors nearest the detector, making safe handling problematic. In addition, the overall reliability of these cables may be questionable given their long exposure to radiation. It is not yet confirmed that the new cables as listed in Table 14.1 will fit in the available space, especially the new Type-II cables. However, a back-up plan exists to purchase cables with smaller diameter (but with larger cable count) if the cables as listed will not fit into the available space (due to either cable diameter or allowable bending radius). Note that if cables as listed are split into multiple cables, the run of cables formed from one cable in Table 14.1 will need to be kept in close proximity to each other in order to prevent electrical

Table 14.1: ITk cable inventory

Cable Name	Number	Origin	Terminus	Diameter (mm)	Notes
SCT Type-IV	1552	PP3	USA15	13.75	Reuse these cables in situ
SCT Type-IV	1552	PP3	US15	13.75	Reuse these cables in situ
ITk-Strips Type-III	776	PP2 half A/half C	PP3	14	New cables
ITk-Strips Type-II	68	PP1 half A/half C	PP2 half A/half C	26.5 or 20	New cables for two inner barrel layers (SS)
ITk-Strips Type-II	320	PP1 half A/half C	PP2 half A/half C	18.2 or 14	New cables for two outer barrel layers (LS) and end-cap
ITk-Strips Fibres	24	PP1 half A/half C	PP2 half A/half C	9	Assumes circumferential services for barrel; combines barrel and EC fibres in one cable.
ID-Pixels LV Type-III	144	PP2 half A/half C	USA15	18.7	Reuse these cables in situ
ID-Pixels LV Type-III	144	PP2 half A/half C	US15	18.7	Reuse these cables in situ
ID-Pixels LV Type-III	144	PP2 half A/half C	USA15	16.3	Reuse these cables in situ
ID-Pixels LV Type-III	144	PP2 half A/half C	US15	16.3	Reuse these cables in situ
ID-Pixels LV Type-III	144	PP2 half A/half C	USA15	5.9	Reuse these cables in situ
ID-Pixels LV Type-III Optoboxes	144	PP2 half A/half C	US15	5.9	Reuse these cables in situ
ID-Pixel HV	152	PP2 half A/half C	USA15	5.8	Reuse cables from USA15 to PP2. Cut cables at PP2; discard from PP2 to detector.
ID-Pixel HV	152	PP2 half A/half C	US15	5.8	Reuse cables from US15 to PP2. Cut cables at PP2; discard from PP2 to detector.
ID-Pixel DCS	664	PP2 half A/half C	PP3	12.8	Reuse these cables in situ
ID-Pixel DCS	332	PP2 half A/half C	USA15	12.8	Reuse these cables in situ
ID-Pixel DCS	332	PP2 half A/half C	US15	12.8	Reuse these cables in situ
The following 4 cable types can only be defined as a total cross section. Exact cable count will have to await final decisions on Modularity.					
ITk-Pixels LV ASICS		PP1 half A/half C	PP2 half A/half C	76.615	New cables; exact number depends upon the modularity decided for the detector.
ITk-Pixels LV Optoboxes		Optoboxes half A/half C	PP2 half A/half C	2.968	New cables; exact number depends upon the modularity decided for the detector.
ITk-Pixels HV		PP1 half A/half C	PP2 half A/half C	8.877	New cables; exact number depends upon the modularity decided for the detector.
ITk-Pixels DCS		PP1 half A/half C	PP2 half A/half C	18.912	New cables; exact number depends upon the modularity decided for the detector.

pickup from stray electro-magnetic emissions due to the common connections of the cable shields. This will complicate the cable pulling and cable inventory to some extent. Current estimates for the power dissipated inside the Muon Spectrometer volume by ITk cables and patch panels are considerably less than that due to the present ATLAS Inner Detector, however, some cooling, especially of the PP2 area will still be required.

14.2 Cooling

The cooling plant described in Chapter 19 of the ITk Strip TDR [1] connects at PP1 to the cooling pipes of the local supports described in Section 13.2.

Since the time of the Strip TDR in early 2017, ITk have re-evaluated the requirements of the CO_2 cooling system based on the most up to date measurements. The Pixel total is reported in Table 14.2. The total for the strip system (Barrel plus end-caps) is 94 kW. The total ITk requirement, without safety factors, is 191 kW.

14.2.1 Cooling Modularity and Mapping

The cooling system must remove all the heat generated inside the detector volume. There are three heat contributions to be considered within the detector volume:

- **Heat generated by the FE chip:** In Paragraph 13.1.2 the FE chip power assumption has been given for specifying the thermal performances of the local supports: The value was set to 0.7 W/cm^2. As said, this extreme power should not be used for estimating the overall cooling budget. It is in fact unrealistic that a large fraction of the modules in the whole detector dissipates the maximum power. It is therefore worth to the scope setting the average FE chip power as:

$$\overline{P_{FE}} = \frac{1}{N_{FE}} \sum_{i=0}^{N_{FE}} P_{FE}^{i}$$

  Where:

  $\overline{P_{FE}}$ = Average FE chip Power
  N_{FE} = Total number of FE chips in the whole detector $\simeq$ 33.000
  P_{FE}^{i} = Single FE chip power

  The expected power distribution among the FE lead to set the Average FE power of 0.5 W/cm^2.

- **Heat generated by the Sensor:** The sensor could potentially dissipate up to 0.25 W/cm^2. However, this is the power at the thermal runaway. A module (with its sensor) is not operational in this condition. A reasonable but still conservative way to define the average sensor power is to estimate its dissipation at the end of the detector's life assuming the TFM's specifications (given in Paragraph 13.1.2) are met. Therefore, assuming that the thermal performances of the local supports are as specified, the maximum sensor power will be less than 0.1 W/cm^2

- **Dissipation along the services up to PP1 (Patch Panel 1):** The heat generated in the services includes contributions from:
  - Module flex
  - Type0 services (along the local support up to PP0)
  - TypeI services (from PP0 to PP1)

  Such an estimate depends also upon the minimum SP-chain modularity (also set > 7.5 modules per SP-chain), upon the conductor' cross section that can be accommodated in the available services gaps and, finally, upon the average current of the module. It turns out that a conservative budget leads to account for the services up to 20% of the total power dissipated by the FE: 0.1 W/cm^2 (0.5 W/cm^2 $\cdot$ 20% = 0.1 W/cm^2).

The sum of the three contributions, that already includes convenient safety factors, gives a total power dissipation equal to:

0.5 W/cm^2 (FE-Chip) + 0.1 W/cm^2 (sensor) + 0.1 W/cm^2 (services) = 0.7 W/cm^2.

Which, multiplied by the total detector active area, sums up to less than 100 kW

Reader should notice that the power dissipation used for the TFM (also 0.7 W/cm^2) is only accidentally equivalent to the power estimate for the cooling budget. In the first case, we were interested in the maximum FE power in order to design a local support capable to handle extreme FE current consumption. Services contribution was not considered there since the heat from the cable follows different path and it does not contribute significantly to the temperature of the sensor. Here, vice versa, we are interested in the total heat generated inside the detector volume that must be based on the average power dissipation.

Parameters of the cooling loops
Reliability requirement imposes to avoid removable connections on the cooling lines inside of the detector volume. The Pixel system will have a limited number of fittings at PP1 (28 in total; see Table 14.2). The coolant is therefore distributed via welded manifolds inside the PP1 volume or via the so-called common rail. Figure 14.1 shows the concept for the case of the Outer Barrel. The coolant is delivered subcooled at the inlet line at PP1 at -35°C [point (a)]. Its enthalpy is increased providing heat through the "Warm Nose Heat Exchanger". At the HeX outlet [point (b)] the fluid is still subcooled but its enthalpy is such that, after the pressure drop induced by the restriction [point (c)], the coolant will be already boiling[1] when entering the local support. From (c) to (d) the heat generated by the modules is collected by the coolant increasing the vapour quality. In this case four local supports are connected in parallel. The saturation temperature at PP1 is guaranteed at -35°C but the pressure drop budgeted along the section (c)$\longrightarrow$(e) is 2 bar ($\sim$ 5°C in saturation temperature). It turns out that the temperature at the inlet of the boiling channel [point (c)] cannot

[1] This artefact solves the boiling initiation problems experienced in IBL.

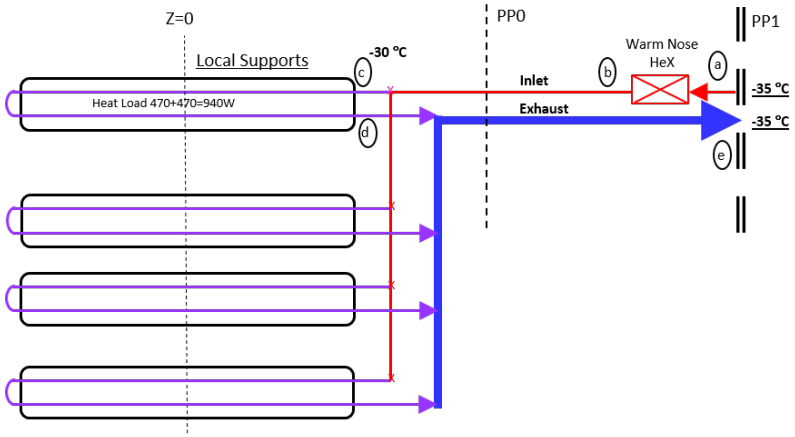


Figure 14.1: Schematic of the Pixel Outer Barrel cooling loop.

Table 14.2: The cooling manifolding concept for Pixel Barrel layers Layer 0. . .Layer 4 (L0. . .L4) and End-cap rings Ring 0. . .Ring 4 (R0. . .R4).

Layer	No. of Loops entering PP1	Loop Power at PP1 [W]	PST End Plate					At the Dry Barrier at PP1		Flex Lines			Splitting Box			Plant Power [W]		
			Feeding lines		Exhaust lines			# Vacuum Insulated Fittings										
			Side C	Side A	Side C	Side A	Notes	Side C	Side A	Side C	Side A	Power	Side C	Side A	Split Ratio	Side C	Side A	TOTAL
L0+L1	4	2831	2	2	2	2	Counterflow. L0 and L1 manifolded per US/USA15	2	2	2	2	2831	2	2	1:1	18099		97386
R0+R1	4	1694	2	2	2	2	Each End-cap manifolded together	1	1	1	1	1694	1	1	1:1			
L2+L3	10	3048	5	5	5	5	Two evaporators are coupled in series and then four of them in parallel	5	5	5	5	3048	5	5	1:1			
L4	4	3933	3	3	3	3		3	3	3	3	3933	3	3	1:1			
R2	2	3615	1	1	1	1	Full rings of one End-cap manifolded together	1	1	1	1	3615	1	1	1:1	39643	39643	
R3	2	3884	1	1	1	1	Full rings of one End-cap manifolded together	1	1	1	1	3884	1	1	1:1			
R4	4	2553	2	2	2	2	Half rings of one End-cap manifolded together	1	1	1	1	5106	1	1	1:1			
TOTAL	32	97386	16	16	16	16		14	14	14	14		14	14		3		
			32		32			28		28								
			64															

be lower than -30°C. For this reason -30°C is the value indicated in Table 13.1 for specifying the requirements on the TFM.

The mapping of the cooling lines is layout dependent. Hereafter we refer to the so-called LAYOUT1 (NeN_V94) for which the mapping has been developed. There is a total of 324 boiling channels in the whole detector.

The grouping must respect the maximum cooling power of the single flex line reaching PP1, which should not exceed 5 kW. There are three main places where the manifolding is located: inside the detector volume between the evaporators and the detector End-Flange, in the PP1 dry volume, and at the splitting box.

Figure 14.2 and Table 14.2 show the mapping and how the grouping is carried out.

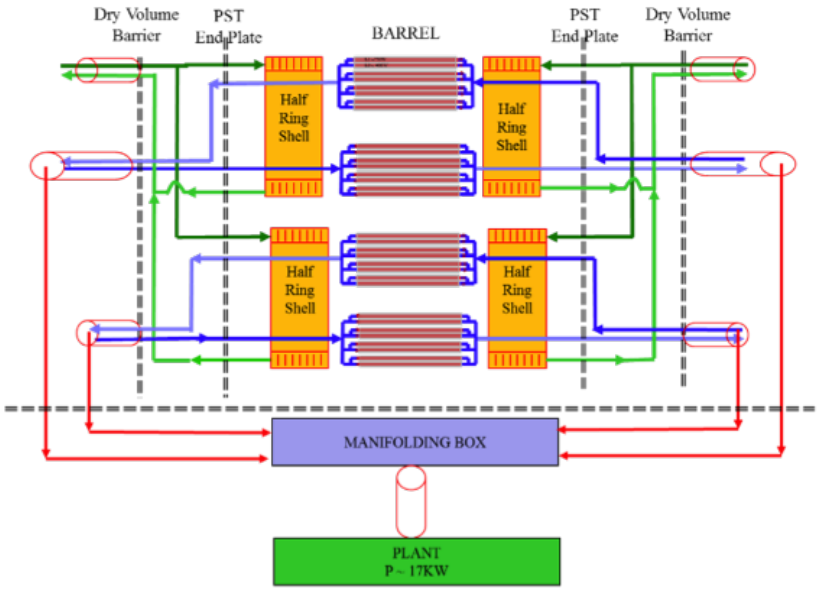


Figure 14.2: Schematic illustrating the cooling distribution for the quadrants of Inner System barrel (Layer 0 and Layer 1). Lines in blue describe the "counter-flow" approach where the inlet line of one quadrant is coupled to the exhaust line of another quadrant. Inner End-caps, lines in green, have the inlet and outlet coupled in the standard configuration that also reach the manifold box (not shown in the figure).

Focus for example on the Innermost assembly mapping as shown in Figure 14.2: two feeding lines entering the PST end-plate are split to serve all the barrel evaporators, a third one is dedicated to the End-cap. The exhaust lines are manifolded similarly collecting the vapour near the exit at the opposite side of the detector.

From PP1 the cooling lines are grouped into a single transfer line at the manifolds box reaching a dedicated plant in the cooling room about 100 m away. The innermost layers (Layer 0 + Layer 1 and Ring 0 + Ring 1) need to be cooled at the lowest possible temperature to guard against thermal runaway and a single low power cooling plant is a favourable option. The last column of Table 14.2 shows that the plant will have to deliver only approximately 20 kW.

The rest of the detector follows a similar grouping. In the outermost layers (Layer 2+Layer 3 and Layer 4) the feeding lines are on the same side of the exhausts. The entire Pixel Detector will need a total of three cooling plants with a power below 50 kW each for a total of approximately 100 kW.

15 Common Mechanics

The Common Mechanics WBS covers a diverse set of deliverables; many of these have a well defined core value, while others have zero core value but require a significant amount of design effort." The WBS items are shown in Table 15.1. The Common Mechanics WBS was ordered in a way that deliverables with core value appear at the top and items with no core value appear at the bottom such that a PBS roll-up is easy to do. 2.3.1 “Surface Integration and Commissioning” and 2.3.2 “Installation in the pit” are sufficiently complex to be described in separate chapters of this TDR – Chapters 16 and 17 respectively. 2.3.7 “Service Integration and Installation” will also be covered in Chapter 17. 2.3.7 has no core value but is a significant effort and is tracked in this WBS. 2.3.8 “Beam Pipe Interface” is included here to assure an appropriate effort is assigned to the machine interface even if there is no core allocation. What will be described in this section are primarily structures or systems and their requirements. In addition, the last Section deals with 2.3.6 “CO_2 cooling system” the design of which was described in the ITk Strip TDR [1]. This is updated here with results from the “Baby-DEMO” project.

Table 15.1: Common Mechanics Level 3 WBS.

WBS	Deliverable
2.3.1	ITk Surface integration and commissioning
2.3.2	Installation in the pit
2.3.3	Common Structures
2.3.4	Polymoderator
2.3.5	Outer Service Volume
2.3.6	CO_2 cooling system
2.3.7	Service Integration and Installation
2.3.8	Beam Pipe Interface

15.1 Common Structures

The ITk is designed to be lowered into the ATLAS pit as a complete “Package” which can be inserted into the Inner Warm Vessel (IWV) of the Argon Barrel directly. This follows the same philosophy as when the previous Pixel Detector was installed in the current ID, aimed at minimizing time required to connect previously installed external services.

The ITk package is assembled in the "Outer Cylinder" (OC) and is enclosed by "Structural Bulkheads" (SB) at the ends of the OC, they provide support to help hold the OC round at its extremity, and provide seals and supports for various sub-subsystem services. The SB also supports the ends of the "Pixel Support Tube" (PST) which is composed of 3 cylinders, a barrel section and two forwards that allows for independent insertion of the Pixel system. The OC, SB, and PST also define the Faraday cage and gas vessel for the Strip system.

The services are also designed to minimize time to connect and qualify them after delivery to the pit.

The Common Structures of ITk are the primary integration structures for the detector. The Outer Cylinder supports directly the Strip Barrel Shells, and the Strip End-caps via rails. The PST is supported via the interlinks of the Strip Barrel Shells. The Strip Barrel Shells are provided in a separate WBS, but are largely based on the design of the PST which is a thin wall cylinder with eccentric stiffeners (hat stiffeners) at the locations of the lock points of the Strip Staves. These shells are terminated in flanges that interface to the interlinks and in the case of the PST, also allow the forward extension to be attached.

The ITk Detector is assembled very much like the current Inner Detector (ID) was in the pit, with an outer (strip) barrel installed and serviced first. Then Pixel Support Tube extensions (PST forwards) prior to outer (strip) end-cap installation. Followed by insertion of the Pixel Detector and its replaceable sub-system. The primary difference is that all of this occurs on the surface to minimize work in the pit. The Outer Cylinder is the primary integrating structure on the surface. It is an analog of the IWV of the Barrel Cryostat (Argon Barrel). In the previous installation, full length services were installed starting well inside the bore of the IWV for the TRT (Transition Radiation Tracker) and the SCT (Semi-Conductor Tracker) and then dressed out to US and USA caverns. The precision required to meet envelopes in this volume with such long cables slowed installation. The current plan for the Strip Barrel is to install "Service Modules" that are much shorter, easier to meet precision packing, and with a break at the end of the OC called Patch Panel 1 (PP1) which will also provide gas-tight and EMI seals at the boundary of the ITk. The Strip Detector volume, bounded by the OC, PST, and SB is its own Faraday cage and gas volume. The Pixel Detector volume is split similarly, but into two separate volumes. The Pixel Detector is split into an outer system and an inner insertable system, both with corresponding barrel and end-cap sections. The outer Pixel Detector system is bounded by the PST on the outer radius and the IST (Inner Support Tube) on the inner radius. The insertable system is bounded by the IST at high radius and the VI (Vacuum Inner) beam pipe at low radius. Both outer and insertable systems have PP1 (Patch Panel 1) structures that independently seal their volumes at high $|Z|$. The outer Pixel Detector volume is separate from the insertable system, such that the eventual replacement of the insertable system does not disturb the sealed volume of the outer pixel layers. Pixel Detectors are not as susceptible to EMI, so the Faraday cage aspect of each of the two volumes is not aimed at protecting the detector from EMI, rather protecting the neighboring detectors from Pixel noise. There is no specific requirement for a Faraday cage between the outer and insertable pixel systems, so the IST is not specifically a field cage.

Experience from the IBL (Insertable B-Layer) shows that EMI protection from the beam is not required, i.e. there is no internal Faraday cage on the current VI, which is planned for continued use in HL-LHC.

This methodology has been adopted by all sub-systems. Strip Barrel has Service Modules that end and seal at the extent of the OC in conjunction with the Structural Bulkhead (SB). The Strip End-caps are delivered with the SB and their PP1 is sealed with and penetrates the SB. Similarly, the Pixel PP1 for both Outer and Insertable systems are supported by and seal to the SB. The ITk Package will be presented in the pit with bulkhead connectors sealed and tested on the surface ready to terminate in the pit after insertion in the IWV.

There are three separate volumes for the detector; Strips, shared between Barrel and End-cap, then two separate Pixel volumes: Outer system, and Insertable. The Strip volume is bounded by the OC, SB, and PST. This forms a Faraday cage as well as a separate gas volume. The two Pixel volumes are separate from this. They are primarily separate gas, but not EMI volumes. Pixel Detectors are not viewed to interfere electromagnetically; gas volume separation is only required for humidity control. See Figure 15.1 of the envelope model.

A fourth volume is the "Outer Service Volume" (OSV). This volume is external to the ITk Detector volumes, but internal to the "ITk Seal Plate" (ISP). This volume is between the OC and IWV and at 3.2 m extends to 2.15 m radius from beamline to the service penetrations. The ISP provides an intermediate dry environment for the various service penetrations of the ITk volumes.

15.1.1 Envelopes and Interfaces

The Outer Cylinder is 6.4 m long and 2.15 m in diameter as shown in the envelope drawing. The Structural Bulkhead mechanically holds the OC round, and supports various service penetrations. It also supports the Pixel Support Tube. These three global mechanics deliverables in WBS 2.3.3 (2.3.3.1 Outer Cylinder, 2.3.3.2 Structural Bulkhead, 2.3.3.3 Pixel Support Tube) are separate deliverables with tightly coupled interfaces. The Strip Barrel interlinks support the PST Barrel and are connected to the OC at $Z = \pm 1.4$ m. The PST also forms the inner surface of a Faraday volume and hygrothermal barrier. The OC and SB need to perform as components of a hygrothermal barrier and Faraday cage as well as supporting the Strip Barrel and End-caps mechanically. The OC is directly supported by rails inside the Inner Warm Vessel (IWV) of the Liquid Argon Calorimeter Barrel (AB). These rails are directly incorporated onto the inner surface of the IWV, along with a 3 cm thick layer of poly-moderator. An additional 3 cm of Polymoderator is incorporated on the inside of the OC in the barrel region, i.e. $Z = \pm 1.4$ m.

The OC is split into 3 segments in length, joined via flanges at the end of the "Barrel" region ($|Z| = 1.4$ m). This facilitates precision placement of mounts for the Strip Barrel Shells, as

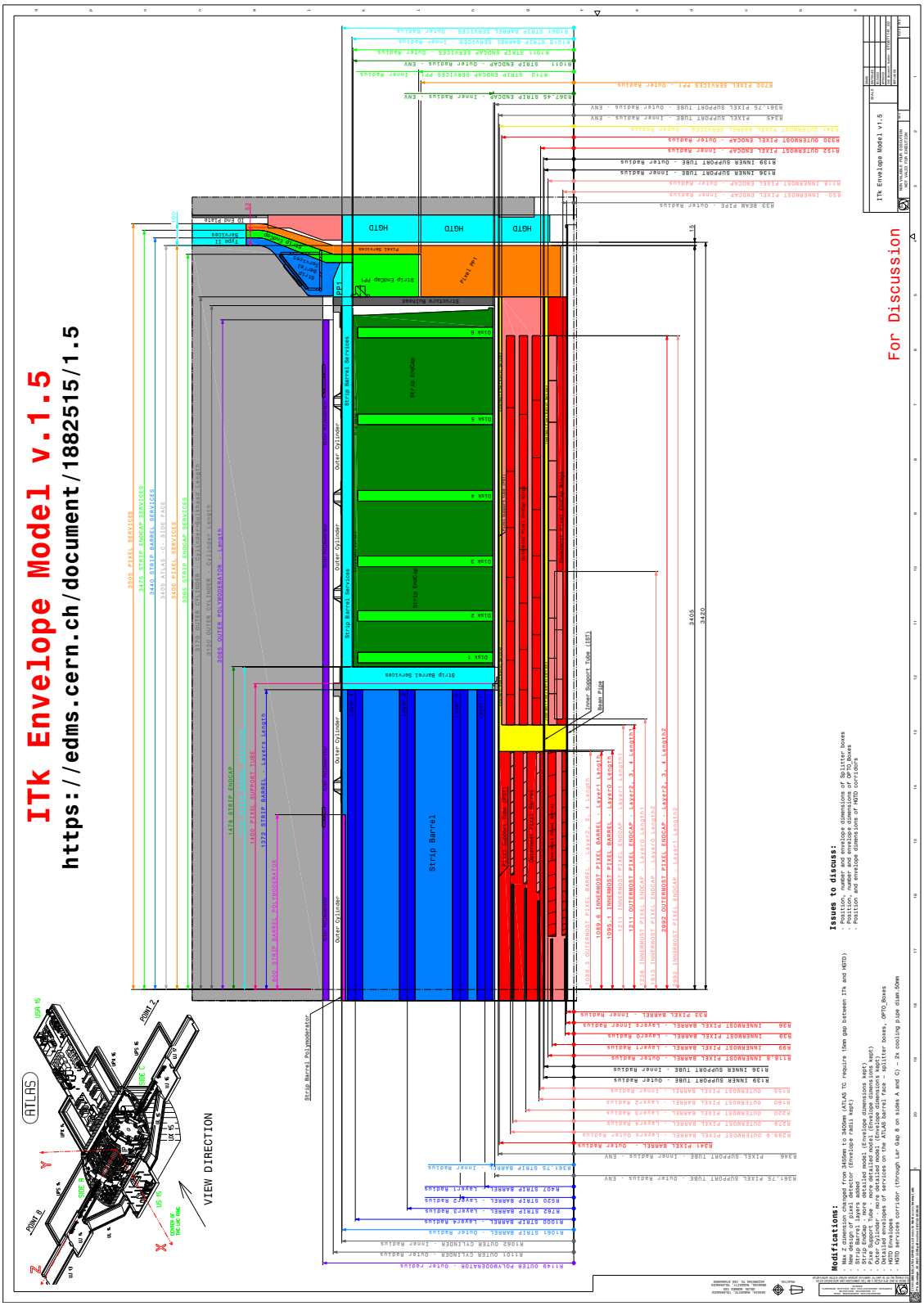


Figure 15.1: Envelope Model of ITk.

well as placement of the rails required in each forward section to support the Strip End-caps. The flanges required for joining the segments will also stiffen the shell of the OC at the locations where detectors are supported within it, and where it is in-turn supported by the rails in the IWV. This split also reduces fabrication risk by making 3 smaller shells; this also allows for shorter tooling, and a re-use of the tools required to place the flanges at the end of each section – a technique developed for the original Pixel Support Tube.

The ITk is assembled on the surface inside the OC and lowered into the UX cavern (pit) as a unit. The aim of this configuration is ALARA, and to allow rapid connection of services in the pit. This also allows for significant commissioning/testing on the surface prior to lowering.

The Outer Cylinder and Specifically the Structural bulkhead have significant interfaces to the ITk Services, nominally via the Patch Panel 1 penetrations, but also, in envelopes, the Type-II services. These are illustrated in Figure 15.1 and will affect the overall length of the detector.

15.1.2 Support Hierarchy

Section 15.2.2 describes how the Pixel Detector is supported inside the PST and is not covered here. The PST is supported via the interlinks described above in a plane at $|Z| = 1.4$ m, as well as at its extremities $|Z| = 3.2$ m by the structural bulkhead. The Strip Barrel shells are all supported also by these interlinks to the flanges on the barrel section of the Outer cylinder.

The primary external interface for the Outer Cylinder is the Inner Warm Vessel of the Argon Barrel. The Outer cylinder is inserted into the AB IWV via a set of rails at $Y \sim 0$, $\pm X$ (3 and 9 o'clock). These rails also support the ITk via the OC in the operating condition. One of the rails, on the -X side (USA), is a "Vee" i.e. provides constraint in the X direction. The opposite rail is "Flat" to allow for both mis-alignment in the X direction of the Vee rail, and also allow for radial expansion/contraction of the IWV. The envelope (gap) between the OC and IWV, as well as the Horizontal (X) extent of the Flat rail is sized to allow for catastrophic Liquid Argon leak inside of the AB – which could cause the IWV to shrink approximately 10 mm on diameter. The vertical (Y) alignment of the rails is expected to be within 0.25 mm parallel to each other – this provides the vertical position, alignment, and support for the OC. The OC will have 4 engagement points per rail; at $|Z| = 1.4$ and 3.2 m on each side. This is not a kinematic arrangement. The OC will be flexible, on the order of the vertical alignment of the rails assuring load sharing along the rails. The Rails are assumed to be aligned/co-planar to a similar tolerance as the current Inner Detector, which is co-planar to 0.5 mm. The deflection of the OC, if supported by just its end rollers will be approximately five times that of the IWV which is 10 mm thick Aluminum. The Z constraint is on the C-side of the Vee rail.

15.2 Global Mechanics

Sections here specifically describe the design and construction of the Outer Cylinder, Structural Bulkheads, and Pixel Support Tube.

15.2.1 Outer Cylinder and Structural Bulkhead

Will describe the OC and its performance with the SB in place subjected to the loads of the detectors. A brief discussion of possible fabrication methods will also be included to support the cost methodology.

The Outer Cylinder is the primary integration structure for the ITk. It is a composite structure approximately 2 m in diameter and approximately 6.5 m long. It will be split into 3 cylinders, joined by flanges, with a barrel section and two forwards allowing for better control of various internal interfaces, e.g. interlinks for the Strip barrel shells and rails for strip end-cap insertion into the forwards. The design effort includes preliminary tooling design, and access platforms that will be reused during barrel integration on the surface. The OC will be an eccentrically stiffened shell. Along with the flanges additional eccentric stiffeners, including rings and various pad-up regions around load introduction points. This is similar in philosophy to how the PST is designed, but will mostly use Intermediate Modulus fibres (under 400 GPa) for most of the structural shells to reduce cost.

The Structural Bulkhead closes the cylinder at the end providing structural stiffness and seal interfaces to various patch panel penetrations. There are 2 SB, 2 m diameter stiffening plates with integrated seals for service penetrations. It supports all of the Patch Panels for ITk barrel and end-cap strips as well as Pixels. They are each located at the ends of the OC. Their primary purpose is to stiffen the Outer Cylinder, while also providing the primary environmental seals (gas, electromagnetic field, humidity).

15.2.2 Pixel Support Tube

The Pixel Support Tube (PST) constitutes the primary mechanical interface between the Pixel Detector and the rest of ITk. The PST, supported by the Strip barrel and structural bulkheads, creates a clear bore through the ITk for the insertion and housing of the Pixel Detector. It also creates an electromagnetic and gas barrier between pixels and strips, provides interfaces for support of the Pixel Detector and services and support for Strip Detector Layer 0 staves in the barrel section. The PST is a Carbon fibre Reinforced Plastic (CFRP) tube assembly divided into three sections: a barrel and two forwards. Each assembly consists of a continuous shell, a flange on each end (for bolting both the barrel and forward sections together, as well as the PP1 ends of the forwards to the structural bulkhead) and hat stiffeners for both rigidifying and supporting strip staves. In addition, mount pads on the

barrel and forward sections provide support from the Strip barrel and Structural Bulkhead, and rails guide the insertion of the Pixel Detector, Strip Barrel Supports and Interlinks.

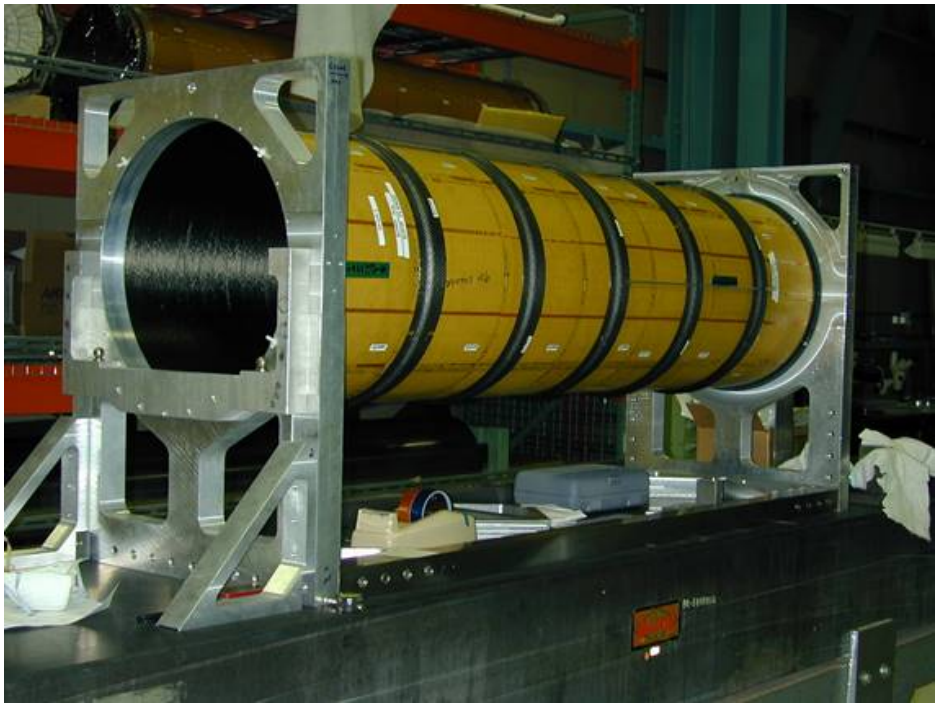


Figure 15.2: Pixel Support Tube from current ATLAS Inner Detector.

The PST is parametrically based on the design of the PST which is currently installed in the ID, see Figure 15.2. This paradigm uses Ultra High Modulus Graphite fibre (UHM) for the shell, with fibre modulus in the 800 GPa range, similar to YS80A or K13C2U (TBD during final design). The shell laminate takes most torsion loads and is optimized for local flexure. The shell is stiffened eccentrically, by way of hat-stiffeners (hoops with a "top-hat" cross-section). Generally the optimization of hat-stiffeners drives them to be as tall as the envelope allows. The remaining optimization space available is the position periodicity along the length of the shell of these stiffening elements. Generally they are placed at a distance such that their added mass just less than doubles the mass of the shell they stiffen, or in this case, they are placed to coincide with specific mount points of the Strip Staves in the barrel section of the PST. These load points are the primary eccentric (local bending) load applied to the PST. An eccentrically stiffened shell can be optimized to take discrete loads, such as the stave mounts, rather than a honeycomb shell (concentrically stiffened) which gives flexural stiffness everywhere, rather than just the discrete locations required. This paradigm is also used for the Outer Cylinder which has discrete load introduction points e.g. the support rollers on its exterior, and the internal rails which will support the Strip End-caps. The PST will similarly have internal loads applied by the Pixel system both during insertion, likely via rails, and perhaps discrete lock points for the Outer Barrel and

End-caps of the Pixel Detector.

15.3 External Mechanical Interfaces

This section describes external interfaces, e.g. Type-II patch panels, and nearby envelopes, e.g. HGTD, service routing at radii under 1.2 m, and the ID Seal Plate. An overview is given of Strip and Pixel Detector service routing via muon chambers to the HX structures with PP3 and the penetrations(chicane) to the US(A) caverns.

Except for the bore of the IWV, the volume external to the ITk has many envelopes, most of which are services.

15.3.1 External Envelopes for services

The ITk Package is the object that is lowered into the pit from the surface and is mostly described in Section 21.4.1 of the ITk Strip TDR [1]. While the envelope for lowering is the primary driver allowing the ITk to be inserted as a whole, there are several envelopes post installation that need to be considered.

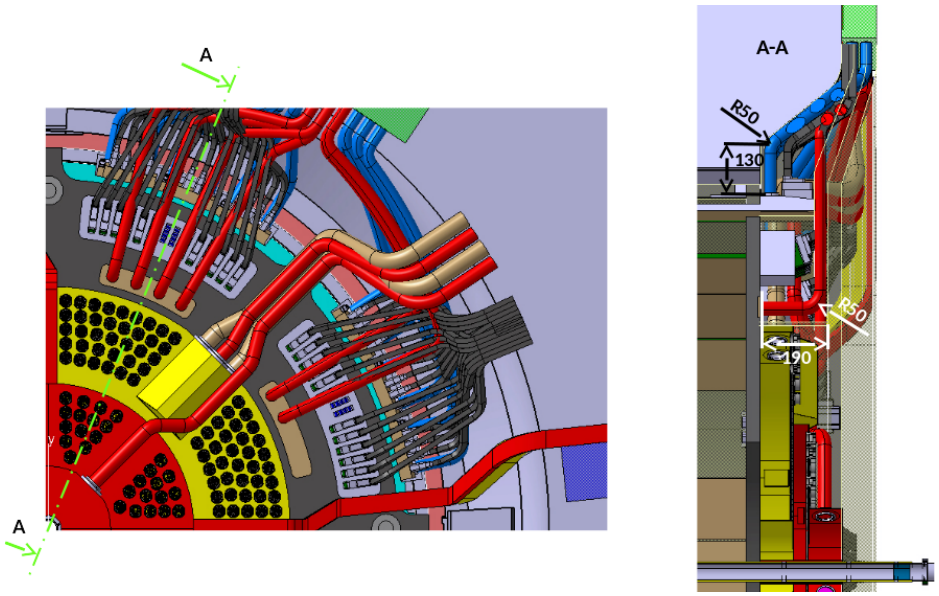


Figure 15.3: **Left**: front view towards the Interaction Point and ITk chamfer region. **Right**: section view along the line A-A in the left picture; the grey area near the label "R50" indicates the HGTD.

The Patch Panels for each of the ITk sub-systems need to interface and allow space for the services that will eventually connect the detector to the service plant. These services are still being finalized and optimized. Envelopes have been assigned to them, but detailed

routing to assure that all services can reach various routing requirements is still ongoing (see Figure 15.3). It has been shown that the net service cross-section is proportional to the current Inner Detector, and that envelope is the base-line for the ITk. Work to demonstrate routing of these services at high radius is still more than a year away. This represents some risk to the detector, but is no different in scale to the risk the previous detector experienced at this stage of the design.

15.3.2 Service Routing on Inner Detector End Plate

The ITk Services are routed from PP1 to PP2 in the Outer Service Volume (OSV). The OSV is defined by the ITk Seal Plate (ISP). The envelope is tightly defined in $|Z|$ to be 10 cm including the ISP, leaving mostly 97 mm, but with occasional reductions to 93 mm for lap joints in the ISP. In two sectors, 1 and 9, services for the HGTD will require a 5 cm incursion

The HGTD is a newly proposed detector that will impinge upon the existing envelope. Significant effort has been spent to define a conservative envelope for the HGTD and its services. These have been included in a 3D model of envelopes. The primary impact of the HGTD is to subtract 6.5 cm from the ITk envelope, with a likely consequence of shifting the last disks of the Pixel and Strip End-caps by at least that amount. The HGTD is currently going through an IDR, and the space requirements are preliminary, but conservative and unlikely to be exceeded based on a Task Force that also includes ATLAS TC and ITk. This along with the previously mentioned work to define ITk Type-II Service routing (the services that plug into the Strip and Pixel PP1's) mean that the envelopes for the ITk can only be finalized at the time of the OC FDR.

It was originally desired to maintain "ϕ-symmetric" envelopes, but this is not possible with the size of some of the services, particularly CO_2 cooling transfer lines.

15.4 Baby-DEMO low temperature CO_2 research

15.4.1 The challenges of CO_2 cooling at low temperatures

The ITk Pixel needs cooling temperatures around -40°C at the level of the cooling pipes inside the Pixel staves. The cooling flows from and to the cooling plants far away in USA15 is via the transfer lines and local distribution. The fluid transfer is subject to losses, which in a 2-phase system appears as a saturation temperature drop on the return line due to the frictional pressure drop of the flowing media and static height differences. Figure 15.4 shows a typical temperature distribution of the cooling system from plant to detector and back.

The cooling lines inside the detector (PP2-PP1-PP0) are typically designed to small diameters to minimize mass and to ease integration. The performance of these small lines are

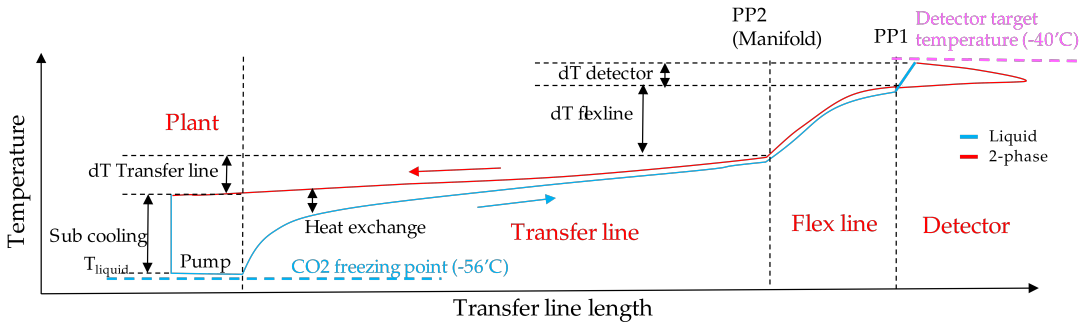


Figure 15.4: Typical temperature distribution in a CO_2 cooling system.

subject to higher losses and are critical in the design as they increase the detector temperature. A distribution with high losses needs a colder cooling system to achieve still the temperature requirements on the detector. The system with the lowest operational temperature of all running systems is the IBL cooling which can achieve -35°C at the plant. Stave temperatures of -40°C need therefore a cooling plant temperature in the order of -45°C if a 5°C temperature loss in the distribution and transfer is assumed. Up to now typical CO_2 pumps of the brand LEWA need to pump pure liquid with a margin towards evaporation (sub cooling) of about 8°C minimum. When taking a -45°C cooling plant temperature in mind the pumped fluid need to be in the order of -53°C. This becomes dangerously close to the CO_2 freezing point, which is at -56.6°C.

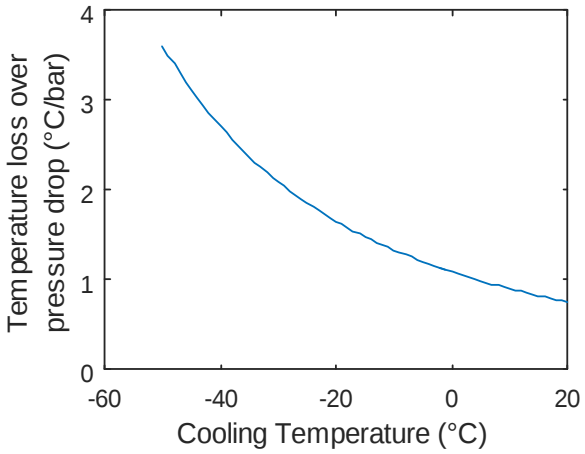


Figure 15.5: Temperature loss in a 2-phase cooling tube as a function of pressure drop and temperature.

High pressure evaporative CO_2 as coolant for detectors is superior above other low-pressure refrigerants as the high pressure allows for small tubes, as pressure drops are less significant with respect to the system pressure. The produced vapor volume stays com-

pressed at high pressures, so the volume flows remains low and hence the pressure drop. The benefit of the high pressure in a CO_2 cooling system is most beneficial at high temperatures and start losing more and more these superior properties at low temperatures. Figure 15.5 shows the relation of the temperature loss as a function of pressure drop. The need for colder CO_2 cooling for Pixel is not only a problem for the system and the pump in particular but also the losses in distribution and transport start to play a major role in the overall performance of the entire system.

15.4.2 Baby-DEMO cold temperature R&D system

In order to investigate all the important aspects of reducing the temperatures on the detector as low as -40°C, the total performance from the plant towards the detector with real scale geometry and components was proposed. A cooling plant with a low temperature chiller was built by CUT-Ponar in Poland under supervision of CERN EP-DT. The challenge of the low temperature chiller is to provide a stable cooling close to the freezing point of CO_2 (-56.6°C). The temperature must be stable not to freeze the CO_2 when going too low and not too high to lose the pump sub cooling. The system is equipped with a LEWA membrane pump similar to what is expected to be used in the future core plants. The goal of the tests is too see what typical minimum sub cool levels can be adopted for the pump in order to see what the lowest possible plant temperature is. This research was originally planned in the development of the pre-production unit called DEMO, but as these questions needed to be answered in a short time, it was decided to build a smaller prototype first, which was therefore called Baby-DEMO.

15.4.3 Real scale cooling distribution

The Baby-DEMO plant is installed next to the ATLAS 1:1 Mock-up in B180 to connect real size and space oriented distribution lines. Figure 15.6 shows an overview picture of the Baby-DEMO plant behind the ATLAS mock-up. For the PP2 to PP1 distribution a flexible concentric transfer line with vacuum installation is under development. This flexible approach is a scaled up technology from ATLAS-IBL and must match the complex integration inside the detector. Figure 15.7(left) shows the flexible vacuum insulated transfer lines which are built in Germany by the Witzenmann Company and which are designed by MPI-Munich.

The design cooling power per flex line is 5 kW. The triple concentric line consist of a 5 mm ID inner hose for the liquid inside a 16 mm ID outer hose for the vapor return. The outer CO_2 pipe is insulated with Muli Layer Insulation (MLI) and placed inside a flexible vacuum hose with an outer diameter of 50mm. The flex lines are 10 m long. The vacuum level inside the hose needs to be smaller than 10^{-4} mbar to exclude convection. The vacuum is achieved by a turbo molecular pump station. Figure 15.7(right) shows the design in a longitudinal

Figure 15.6: Baby-DEMO cooling plant during installation in B180 behind the ATLAS 1:1 mock-up with flex line installed.

cross-section of the flex lines with three concentric flexible metal below hoses. The high pressure CO_2 hoses are strengthen by a metal mesh, the vacuum hose is a normal plain bellow. The full assembly including the end pieces is fully produced by industry taking serial production in the future already into account.

The flex lines will terminate in the manifold boxes in PP2 which will be installed at the Z-level of the ID end plates between the inner and middle muon chambers. Two locations have been foreseen which are in sector 5 and sector 13. The Baby-DEMO set-up on the ATLAS mock-up is equipped with manifolds in both locations so that the effect of gravity of upward and downward routed flex lines can be studied. For the initial tests of which the results are presented in this chapter the flex line was connected to the sector 5 manifold on top of the mock-up. The manifolds are connected to the plant with stationary concentric lines of about 17 m long with a 3/8″ diameter tube for the liquid supply concentric inside a 1″ return line. The insulation is standard armaflex with a metal protection. A dummy load of 6 kW was installed in the center of the ATLAS mock-up to simulate the detector load per

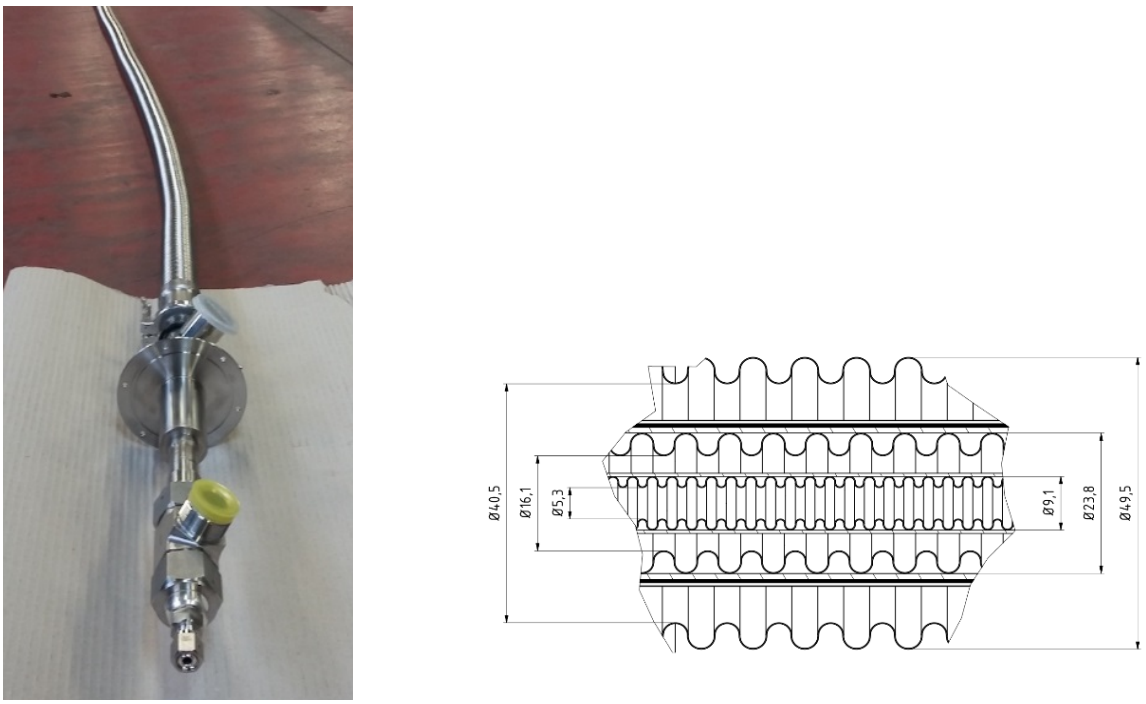


Figure 15.7: **Left**: Picture of the 5 kW ITk flex line. **Right**: Longitudinal cross-section of the 50 mm ITk flex line.

flex line in a realistic location.

15.4.4 Baby-DEMO test results

In December 2017 the Baby-DEMO plant was run successfully for the first time and evaporative cooling temperatures of -47°C were achieved at the plant level. Figure 15.8 shows the test cycle which was made to evaluate the performance of the full system. Accumulator saturation temperature set-point cycles (ST4080) from -47°C to 10°C were made with different heat loads from 1 to 6 kW. The cycle speed for the measurement was as low as 6°C/h so that the results can be treated as being steady state values.

After the first cycle with 5 and 3 kW a cold record attempt was performed manually by the expert operator around 42 hours. During this attempt, the sub cooling of the pump was lost two times (green upward spikes). A loss of sub cooling has often resulted in a full and unrecoverable stop of the flow in many previous cooling systems. This stop was believed to be more critical for cold temperature operation. In Baby-DEMO the pump showed not to be sensitive to this and recovered without a problem when sub cooling was returned. This is a very important result as it allows the system to operate with lower sub cool margins and hence colder evaporation temperatures can be achieved. During the record attempt, a

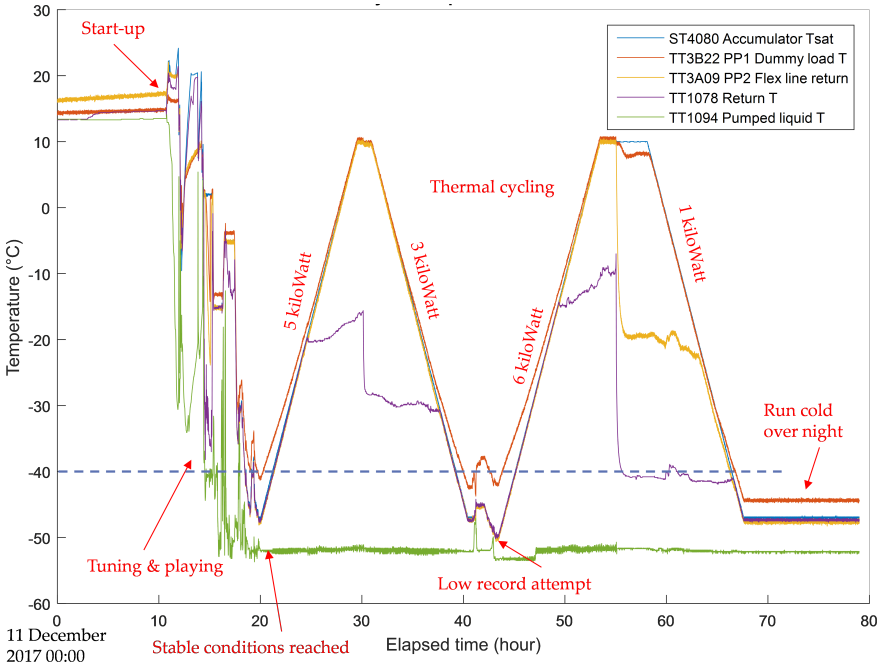


Figure 15.8: Thermal cycling tests of Baby-DEMO under different heat loads.

temperature of -50°C at the plant was achieved. It should be noted that this low temperature is not an operational temperature for future as it was achieved manual without safety margin. However it was good to see that the pump can handle these cold temperatures so it has margin towards the achieved -47°C run over long time as done after the cycling, starting at 68 hours.

With a plant operational temperature of -47°C a temperature in the dummy load below -40°C was achieved so the goal of the Baby-DEMO to prove an operational temperature on the detector at -40°C was fulfilled. The gradient of 7°C was lost mainly in the flex line. Figure 15.9(left) shows the measured gradients of the flex line as a function of heat load and temperature. Clearly visible is the loss of performance at lower temperatures which is due to the lower pressure as explained in Figure 15.5. Figure 15.9(right) shows the losses measured over the long transfer line which are negligible compared to the flex line losses. The negative losses shown are due to the suction by gravity of the downward flow when in full liquid state. Once evaporation was present the suction effect disappeared resulting again in positive frictional losses only.

15.4.5 Future aspects

The Baby-DEMO successfully demonstrated the ability of achieving a -40°C evaporative cooling at the outlet of the pixel cooling pipes as required. The observed gradients in the

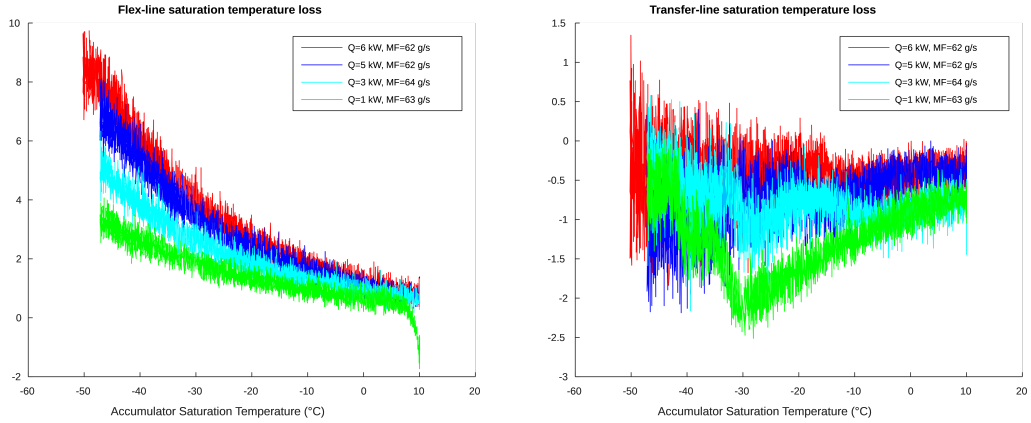


Figure 15.9: **Left**: Measured flex line gradients. **Right**: Measured transfer line gradients.

flex line are subject to improvements. A larger diameter flex line of 60 mm instead of 50 mm is under prototyping and will be tested in Baby-DEMO in 2018. The flex lines as tested are usable for the Strip Detectors where the requirements are less strict compared to Pixel.

Baby-DEMO will be extended in 2018 with prototype manifolds and with so-called warm nose circuits to demonstrate the pre heating concept needed for boiling enhancement. Baby-DEMO will also be the system to test real scale detector prototypes under realistic integration conditions.

16 Surface Integration, Commissioning and Associated Testing

In this chapter we explain the sequence of integration events that will end with the completed ITk.

16.1 Commissioning activities and Schedule

The integration and surface commissioning schedule for the ITk is designed to have a fully integrated and commissioned ITk ready for installation in ATLAS in April 2025. All integration and commissioning steps build towards this goal and the start and end times of these activities are set so that we achieve this target when appropriate time scales are allocated to each of them, and added.

Counting back from this date we allow for a float of two months between ITk installation readiness and the actual scheduled date for lowering the detector into ATLAS. Allowing for disconnection and preparations for the transport from SR1, and considering holidays, this means surface commissioning should end by the end of December 2024. Surface commissioning, which comprises a full test of the entire system achieved by the sequential operation of about 1/8th of the ITk across subsystems, is broken into two periods of about three months each. The first 3-month period will encompass the system tests considered essential to verify the proper operation of the ITk. The second 3-month period is intended to allow for more advanced studies of system performance and the collection of additional data, such as cosmics to be used for a first alignment of the ITk. This second period is auxiliary and can be scoped or phased if required by late changes in the lowering schedule.

Surface commissioning starts in June 2024 after the insertion of both the outer pixel barrel (including its end-caps) and the inner replaceable pixel systems into the Strip Tracker. These insertions, with their associated QC tests are estimated to take two months. Prior to the insertions of the pixel systems, the strip end-caps will be inserted into the ITk and tested in their final position. These activities are also estimated to take two months to complete. The backdating outlined here gives the required arrival dates for external deliverables at CERN, e.g. the pixel or strip end-caps, and defines the necessary completion dates to meet the overall ATLAS integration schedule underground. The ITk integration schedule is given in detail in Figure 16.1.

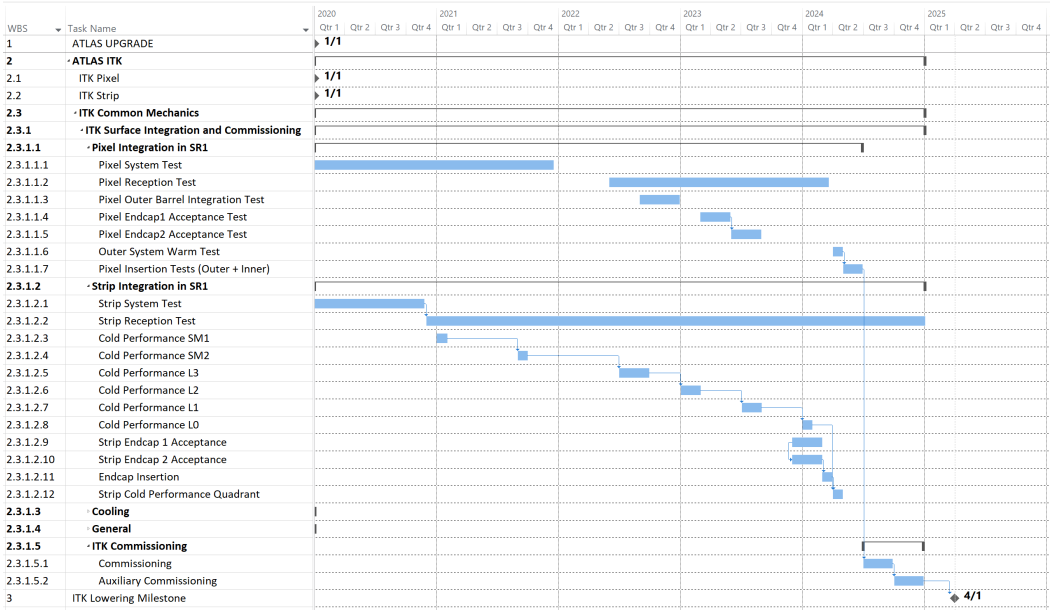


Figure 16.1: Schedule for Surface Integration.

The integration of the different subsystems will proceed in parallel. In the following we will first present in more detail the integration activities for the pixel systems, followed by a discussion of the integration of the strip systems, and then of the subsequent operations until the completion of the ITk.

16.2 Subsystem integration

16.2.1 Outer barrel pixel integration

Outer barrel integration is the process by which local supports are assembled together to form a complete outer barrel sub-detector. Local supports are populated and tested by both CERN and off-site institutes. These local supports are reception-tested in SR1 and then stored locally. As enough local supports become available they are integrated into half-shells in SR1 on a specific integration tool with the services to PP1 being supported on a framework on each side. The end of pixel outer barrel integration is marked by the performance verification of the two fully-populated half-cylinders.

For integration purposes, the outer barrel will be split in two halves. Each will be integrated with the corresponding type-I services and tested separately. Then, both halves will be mounted around the End-caps to build the Outer System (see Figure 16.2).

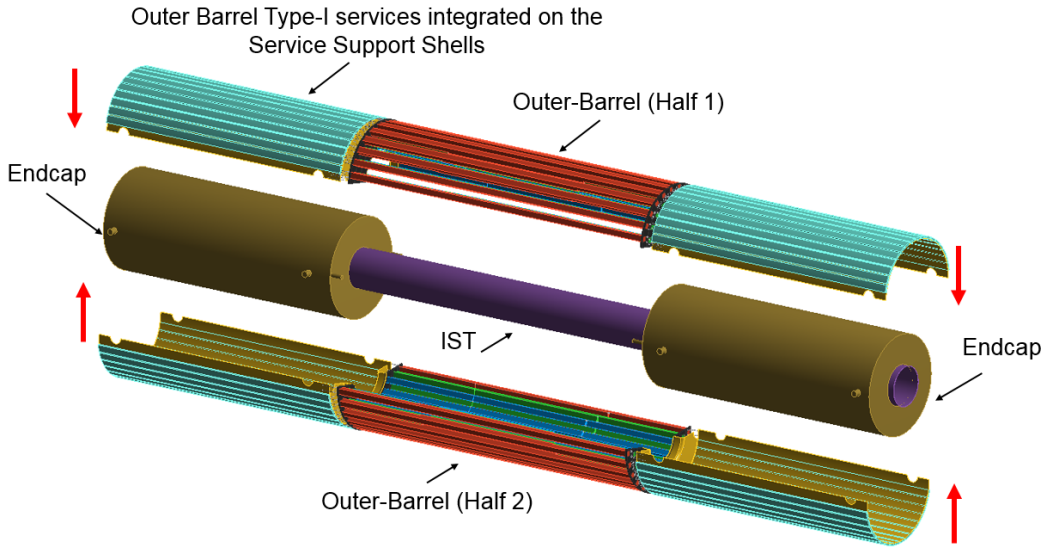


Figure 16.2: Schematic representation of the integration scheme of the two halves of the Pixel Outer Barrel.

For each half of the outer barrel the Type-I services and the manifolds for the cooling lines are first integrated on two CFRP service support shells (i.e. for sides A and C respectively). These two structures are then placed on the integration tool for the half barrel, and connectivity and leak tightness tests are carried out.

In parallel, the individual longerons are mounted on the end-flanges, creating three separate assemblies for Layers 2, 3 and 4. Next, the half-layers are transferred to the integration tool and connected to the Type-I services in steps. Testing of the longerons in a given half-layer proceeds by sectors, following the grouping of the cooling loops by PP1 feedthroughs. The next half-layer is transferred to the integration tool once testing of the previous half layer with the Type-I services has been completed.

16.2.2 End-cap pixel integration, transport and reception

Pixel end-cap integration is the process by which the half-ring local supports are assembled together to form a complete pixel end-cap. The pixel end-caps are integrated from an assembly of six half-cylinders, which are tested off-site and then installed into a transport enclosure and made ready for shipment to CERN. On reception at CERN they are tested in SR1 individually in their self-contained shipping containers to check for transportation damage. This container will comprise a thermal enclosure, which allows safe operation of the end-caps cold (at temperature below the dew point in the integration area). Once the reception test is complete, the shipping containers are removed leaving the two end-caps

supported on cradles compatible with inserting/integrating the pixel end-cap into/with the outer barrel.

The end-cap is formed from an assembly of six half-cylinders each populated with a number of half rings. Each assembled half-cylinder can be operated as an autonomous unit and encompasses the CFRP support shell, the half-ring mounting fixations, the Type-I services harnesses and the half-rings. The integration of a half-cylinder starts with the installation of the CFRP half-cylindrical shell into an assembly jig. The Type-I services assemblies are mounted onto the half-cylinder in pre-assembled bundles using custom tooling. Once positioned on the half-cylinder the services are secured in place and the excess length between the end of the half-cylinder and the PP1 location is secured to a temporary handling frame. Before any half-rings are mounted a full geometric survey of the positions of the half-ring fixation points is taken and an envelope-check on the positions of all the services bundles is made to ensure there is adequate clearance for the installation of the half-rings.

Tested half-rings are supplied from the module mounting site in transport/test enclosures which can be disassembled after reception testing leaving the half-ring attached to a handling jig. A custom set of tooling picks up the half ring via the handling frame and places it at the correct z-position along the length of the half-cylinder. Using micro-adjusters the position of the half-ring relative to the half-cylinder is set and the half-ring is then translated side-ways into the half-cylinder. Once the half-ring has been attached to the half-cylinder it is disengaged from the handling frame and the tool withdrawn. The rigidity of the fixations is verified and the position of the half-ring surveyed. Next, the electrical connections between the Type-I services and the half-ring services patch-panels are made. Where applicable, simple loop-back tests using low-power modes of operation which do not need CO_2 cooling are used to verify the connectivity of the cabling. Finally, the connections to the cooling system are made using in-situ orbital TiG welding. Once each half-ring is fully connected the cooling lines can be evacuated and checked for leaks. A test enclosure is placed around the half-cylinder and the environment de-humidified. High temperature CO_2 cooling allows the first round of electrical testing to be undertaken whilst the humidity of the test enclosure is being reduced to the level required for long-term cold testing. After a full set of connectivity and basic functionality testing has been undertaken, a full characterization at operating temperature is made. The half-cylinder is then subject to unpowered thermal cycling down to low temperature to stress all services interconnections. Finally, the half-cylinder is subjected to a second full-characterization and the results are compared to identify any failures. Completed half-cylinders are then stored in a clean dry environment until their partner has been assembled and tested.

When pairs of half-cylinders are ready for integration they are mounted onto a pair of assembly jigs which allow the two sides to be brought together in a controlled manner. Each pair of half-cylinders is brought together around the previous pair. When each pair is mated together the seams of the CFRP half-cylinders are joined and the half-cylinders are attached to the front end-flange and the rear end-flange-assembly. Once integrated together, the position of the pair of half-cylinders is measured relative to the end-cap support feet attached

to the front and rear supports. The integration of each pair of half cylinders proceeds in turn until all three layers have been assembled together. After each pair of half-cylinders is added, the Type-I services have to be re-laid to attach them to the temporary services extension shells on which they will be supported until after the integration into the PST.

After all three layers are assembled, the connectivity of all services will be validated. Sections of the end-cap corresponding to the availability of DAQ and power supply systems will be connected and all modules tested. Once all the testing is complete, the end-cap will be installed into a transport enclosure and made ready for shipment to CERN. Prior to the transport of the end-cap there will be a trial shipping of the transport enclosure and end-cap mock-up to validate all the tooling and handling procedures. The transport will be a dedicated load on an air-sprung, temperature controlled lorry. During the transport, environmental and vibration monitoring systems will be used to ensure that as much information as possible is available should the end-cap suffer any damage in transit.

16.2.3 Inner pixel integration and reception

The inner pixel system will arrive in SR1 in 12 pieces, 4 quadrants each for the barrel and two end-cap regions. Each quadrant will undergo a standard reception test to check for service connection integrity (as with the other pixel subsystems), which will be performed with cooling, but at room temperature. Quadrants will then be assembled into halves, and eventually into the three individual sections (barrel and two end-caps). Finally, the three sections will be joined into a train (maintaining Z position but with flexible joints) and the services will be dressed over the entire length in order to packaged them for insertion into the Inner Support Tube (IST) in the Pixel Outer Barrel. At this stage, the final tube manifolds are welded, and the entire Inner System undergoes a cold connectivity and performance test. In order to allow for space considerations, the bulk of this work takes place after the outer end-cap reception and while the outer end-caps are being integrated with the outer barrel.

16.2.4 Barrel strip integration

The integration of the barrel strip tracker is described in the ITk Strip TDR [1]. The barrel strip staves are reception-tested at CERN upon receipt and again later just prior to inserting into the global structures as they may be stored for several months prior to insertion. These are similar tests and are performed warm (above the dew point in the integration area) to reduce the risk of condensation, but with cooling to extract the heat. The power per stave is 200 W for the full test suite. The boxes used for protection of staves during the shipping are compatible with this test and also with the insertion tooling.

The staves are inserted axially from the end of the support structure and engage with mount points on the Barrel. This insertion takes place within the confine of the OC. It starts on

the layer with the largest radius and proceeds inward. There is a limited test, without cooling, performed immediately after the insertion of each stave to assure that no damage was incurred. No further test is done until after a set of eight staves is installed and ready to connect to the Type-I service module. This activity progresses on both sides (A and C) of the outer cylinder, eventually in parallel.

The major unit of assembly for the strip barrel is a service module which services eight staves. There are six services modules per quadrant per end. Connecting a service module to the staves involves welding the cooling pipes to the staves, pressure and leak testing the welds, and connecting the electrical and optical services. After the first service module is installed, the OC volume will be sealed and a full cold test will be run with the first eight installed staves. A similar cold test will be performed after the service module that serves the staves on the next layer in is installed, and will include both ends. Figure 16.3 shows the assembly sequence of service modules and the number of staves and service modules installed between cold tests as indicated by the coloured frames. The two Layer 3 services modules (purple and olive) are installed first followed by the two covering Layer 2 and Layer 3 (blue and green), then the one for Layer 1 (orange) and finally the one straddling Layer 0 and Layer 1 (red). These first two cold tests are to verify the noise environments inside the outer cylinder and potential coupling between layers and ends in the performance of the strip barrel.

After the first two tests, the OC will be closed four more times during the strip integration to test all the staves and service modules on a given layer once the layer has been completed on both sides. The two cold tests described in the previous paragraph are called SM1 and SM2, the subsequent layer tests are Layer 3, Layer 2, Layer 1 and Layer 0, named for the layers that are tested. The durations for the layer tests decrease from three months to two, and finally to one month as the number of staves tested decreases and our experience grows.

Following the completion of strip barrel integration, one quadrant of one end will be coupled up to the test system and the performance of all staves will be characterised. This test will be repeated immediately after the insertion of the end-cap on that side to allow a comparison of the performance before and after end-cap insertion to be made to check for any system-level performance degradation. After completion of this test, the detector could stay connected in this way through the surface commissioning.

16.2.5 End-cap strip integration and reception

The strip end-caps will be assembled at two different sites (NIKHEF and DESY). After shipment to CERN they will be accepted at SR1 in parallel. The acceptance test will be run with warm cooling and is approximately timed to overlap with the strip barrel quadrant test. This test will power a service duct in the end-cap at a time and verify that no petals or connections have developed a fault during shipping. Prior to installation in the end-cap support structure the petals have been tested cold as part of the local support assembly. Follow-

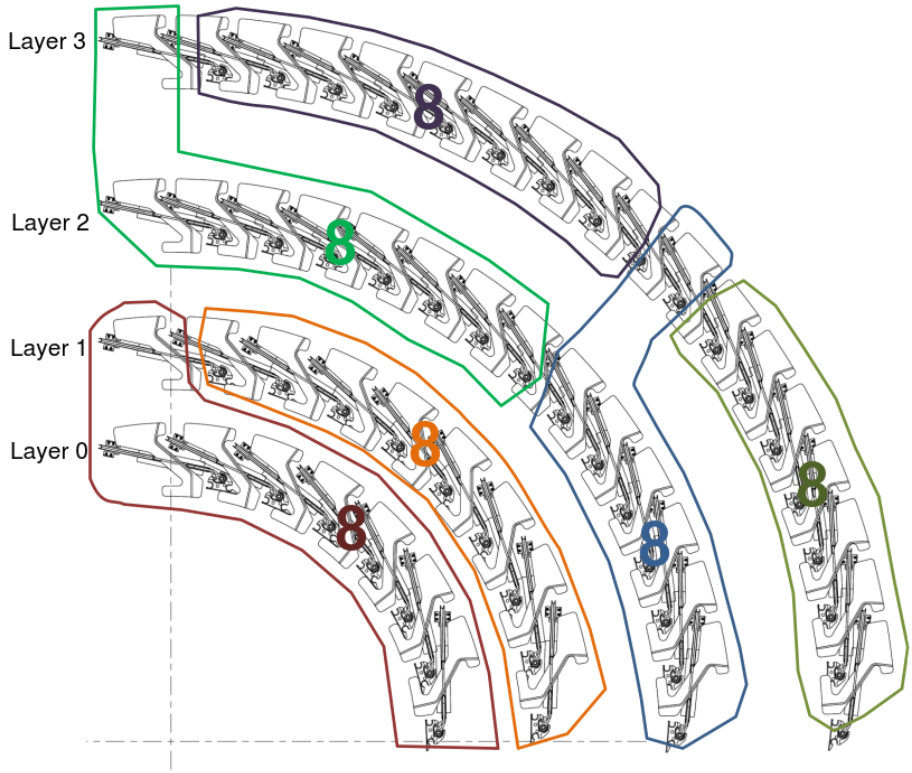


Figure 16.3: Assembly Sequence of Strip Staves in the Barrel Shells. The coloured frames indicate groups dealt with in the same assembly step.

ing the reception test, the two strip end-caps will be made ready for insertion into the OC. The reception tests and preparations for integration are foreseen to take three months.

16.3 ITk integration

16.3.1 Strip EC insertion and cold test of strip systems

Once the testing of the barrel trip tracker and the reception tests for the strip end-caps are complete, the strip end-caps will be inserted into the outer cylinder. The end-cap insertion is straightforward. In preparation for the end-cap insertion the forward extensions of the barrel PST are mounted, and rails on the inside of the outer cylinder are installed. These rails will align with similar rails on the shipping cradles that the end-caps arrived and were tested in. The outer cylinder and the end-cap cradles are registered and aligned to rails in the floor of the SR1 extension. This provides rough alignment of the different structures.

A small rotational stage, similar to what will be used in the cavern, is required for fine alignment and orientation of each end-cap.

Each end-cap arrives with one of the structural bulkheads, which also supports the Type-I services and the PP1s. The structural bulkhead will be fixed to the end-cap until after reaching the final position inside the OC. Once the end-cap is locked in this position, the structural bulkhead will be decoupled from the end-cap so that it can register properly to the outer cylinder and seal the interface surfaces provided by the strip barrel service modules. The structural bulkhead is also bolted on its inner radius to the PST forward extensions, providing a z-constraint to the strip barrel.

Once both strip end-caps are installed the outer cylinder is fully sealed at its ends, both electrostatically and for gas tightness. Quality assurance tests of these seals, particularly for gas/humidity tightness, are required before the following test, which is testing the end-caps (and barrel) strip systems cold.

First, the quadrant test of the strip barrel is repeated with the detector in the final configuration of the Faraday cage and with each end-cap covering the barrel service gap. Then both end-caps will be tested cold. This test is the first large scale cold test of the end-caps with a large scale cooling plant. The effort to extract an end-cap at this stage is viewed as relatively small, which is why we will not test the end-caps cold as part of their reception test. Finally we will connect and test up to 12.5% of the Strip Detector, measuring potential cross-talk between barrel and end-cap.

It is essential that the strip end-caps are thoroughly tested and signed off prior to installation of the pixel system, as access to a strip end-cap after pixel insertion is extremely undesirable.

16.3.2 Insertion of the pixel systems and tests

The outer pixel system with its components, the outer barrel and the end-caps, will be integrated into an insertable package with the services folded in to allow them to pass through the PST. After insertion into the PST, the services need to be unfolded and laid in along their final routing to PP1. The unfolding of these services, re-routing them and mounting into PP1, which is supported off of the structural bulkhead, is sequential, and covers services internal to PP1 as the operation progresses. Intermediate testing will be made to ensure all connections have been properly made before continuing to the next step. As a similar number of connections as in the current Pixel Detector are required a six week period for this task is foreseen, which was the time required for the connection of that system. It is planned to take eight weeks to insert both outer and inner pixel systems into the ITk on the surface. Insertion for each system is accomplished with a simple cable and winch (as in the current Pixel) that pulls the system from its integration tool directly into ITk on the insertion rails (located in the PST for the outer system, and in the IST for the inner system). Following each insertion, services are arrayed into their PP1 positions

in order to give space for the subsequent operations (either insertion of the inner system or transport to the cavern). Both the outer and inner systems ride and are permanently supported on the insertion rails, with only a Z stop near Z=0 to define final position of the detector. The exact locking mechanisms for this final fixation are expected to be similar to the current pixel (i.e. spring operated) but this remains to be defined.

The inner system is planned to be inserted into the IST on the surface using the same tooling that could be used in the pit for its eventual replacement. Should the inner pixel system be delayed, it is possible to insert it in the pit, but that is not the baseline plan. After insertion of the outer system and inner system into ITk a 12.5% slice test is foreseen. Electrical connectivity tests are planned In sections of the manifolding and with Type-I services connected to PP2. The cooling system will be connected in the same sequences to allow enough cooling to operate the modules at room temperature but also give the possibility to perform cold tests. In total 130 days are scheduled for these tests.

16.4 Surface commissioning

During surface commissioning significant sections from all subsystems will be powered together for the first time. This will also provide a possibility to test close-to-final data and control chains prior to installation of the detector in the pit. The first three month of surface commissioning is viewed as essential testing of a fixed 1/8th slice of the ITk. This operation, unlike the previous cold tests, is also aimed at assessing some of the performance parameters of the ITk, and perhaps start alignment of some elements with cosmics. It is to be similar in scope to the commissioning of the current Inner Detector before turn-on of the LHC.

There is an additional three month period currently scheduled to perform additional testing, either by powering a different slice of the detector or gathering more statistics. Should the lowering date be delayed, the detector can stay in this configuration until it is required in the pit. Alternatively, if there are delays in the ITk integration, or in case that the lowering date advances, this portion of the testing period can be scaled down.

16.5 SR1 preparations

Building 2175 (SR1) at point 1 is being expanded to allow for parallel integration of the barrels of the strip and pixel systems. The end-caps for both systems are assembled elsewhere and will only be received and inserted into the ITk in SR1. For the ITk integration the SR1 cleanroom will be re-configured and expanded (see Figures 16.4 and 16.5 for naming details).

The current layout of the SR1 clean room has two areas, the radiation lab and the main floor area. The main floor area will be divided to isolate the current system test setups for the Inner Detector, which must stay operational until the end of Run 3. This separation will allow the new clean room expansion to run cleaner, and more controlled. The radiation lab will be set up for ITk pixel and strip system tests, which will run through local support acceptance testing. A caveat for use of the radiation lab is that any setup must be able to be removed within two months, in case this area is needed for work on activated objects from the current ATLAS Detector.

For reference, the three main areas of the future clean room are the radiation lab (207 m^2), the main floor area (270 m^2) and the (new) SR1 extension (250 m^2). The latter two will be further divided into three sections, south, mid, and north, to describe where specific activities are located, and to define servicing requirements (patch panel locations, cooling lines, etc.), which need to be routed to semi-permanent positions. These services can move if required, but not without cost and schedule impacts.

The extension adds 250 m^2 to SR1, compensating for a similar amount of space lost to the current ID system tests. One main innovation of the extension is inclusion of rails in the floor with an extended concrete pad outside of the building, which will allow for easier transfer of the completed ITk to SX1. Improvements to the HVAC systems will be made to ensure the upgraded room will reach ISO Class 7 and have better environmental control. Additional outlets for 2- and 3-phase power will be included in the extension as well as upgrades to the network.

The primary integration locations for the strips and pixels are in the middle of the main floor and the extension areas. Patch panels for electrical services (PP2) for strips and pixels can be located near the middle I-Beam column which allows the Type-II cables to reach both ends of either the ITk strip systems (which are integrated inside the outer cylinder), or the Pixel Detector which is similar in length and will be integrated side-by-side with the OC. Splitter boxes for cooling are required at both ends of the tracker ($\pm$3 m), close enough for the short flex lines. A detailed layout of SR1 is underway to determine the optimal positions for these services.

Other more mobile activities such as pixel and strip local support reception testing are distributed about SR1. Currently they are planned for the radiation lab, but may move to either a portion of the ID system test room or to the south end of the extension. This may require either re-routing of cooling transfer lines, or a separate cooling system.

16.5.1 Cooling system requirements during integration

The cold tests during integration are defined in the schedule above. These are sub-system level tests that for the strips verify noise parameters and potential self-interactions between subelements of the strip system and the structure. As more of the detector is assembled the power requirements (and correspondingly mass flow) required to cool larger portions

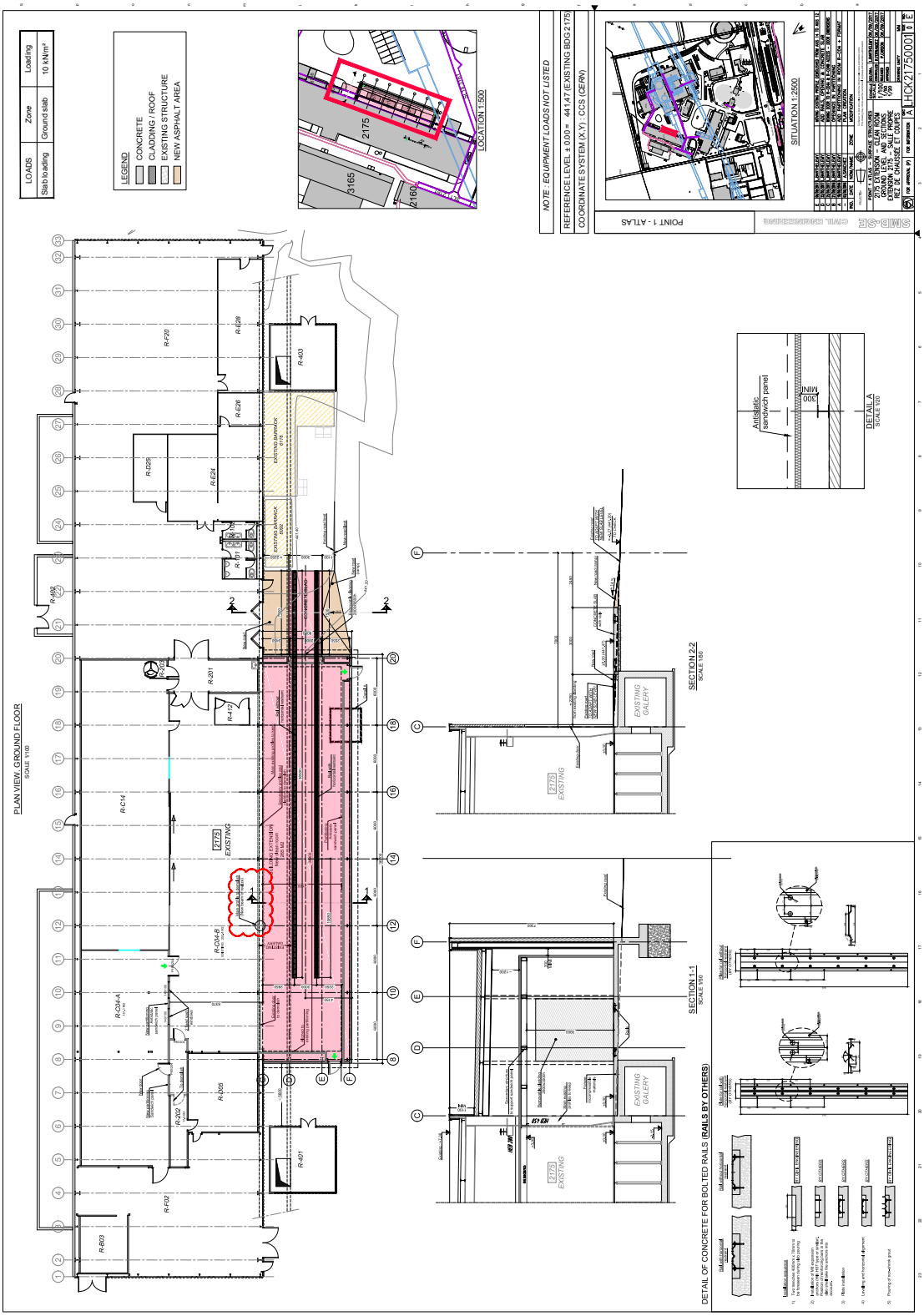


Figure 16.4: SR1 Expansion showing rail locations.

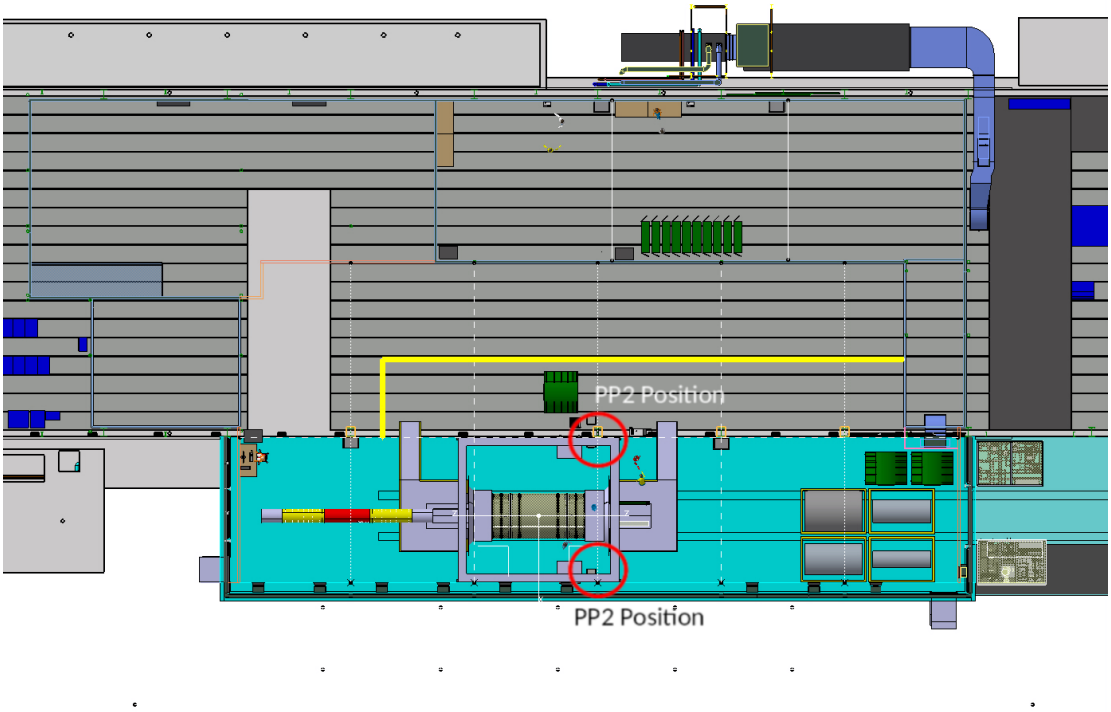


Figure 16.5: SR1 Expansion showing approximate Patch Panel locations.

of the detector will increase. This is not a strong function of the fraction of the detector completed at later stages. A lower power system can be used in the early tests, but for the strip SM2 test at least two long strip service modules must be powered simultaneously. Subsequent tests can be performed with the same cooling power, but it is necessary to ramp the cooling capacity to approximately 10 kW in time for the full quadrant test.

16.5.2 Long term use of SR1

There will be services for the operation of 1/8th of the detector installed in SR1. Most of the active components (power supplies, voltage regulators, FELIX boards, etc.) will be moved down to the pit after the surface commissioning. The cable and piping infrastructure will remain. Some portion of pre-production active components can be used with local supports that were not eventually installed in the ITk on the surface as an ongoing system test, much like the ones currently operating for the ID in SR1.

By the time this occurs, the ID system tests can be removed and the ITk system can be installed in their place to maintain the upgraded SR1 clean room as a clean space. This will

necessarily require re-configuring PP2 locations and re-routing Type-III cables and transfer lines.

17 Installation

The installation of the ITk is the sum of all activities and procedures that start with departure of the ITk from the SR1 surface building, that is immediately followed by the lowering and maneuvering of the ITk in front of the face of the Liquid Argon Cryostat that continue to the end of the beam pipe bake-out. The beam pipe bake out is the formal hand-over of the ITk to ATLAS and the start of in-situ commissioning ready for first beam.

17.1 Overview over the ATLAS Area

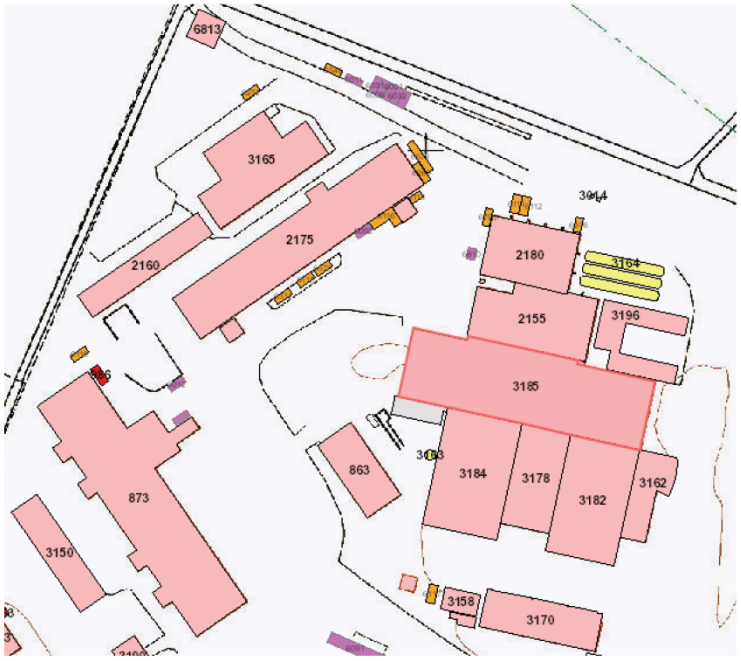


Figure 17.1: Surface map of the ATLAS experimental areas. SR1 is building 2175, building 3185 is the shaft access to the pit.

A surface plan of the ATLAS experimental area is given in in Figure 17.1. The most important areas for the integration and installation of the ATLAS ITk will be SR1 (building 2175), where the surface integration of the ITk will take place and building 3185, which houses

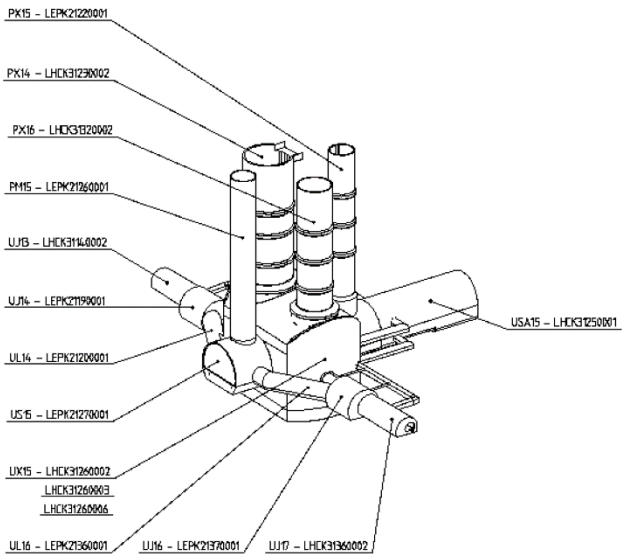


Figure 17.2: ATLAS underground areas. The accelerator is housed in the UJ tunnels. The experiment is in UX15 and the main service areas for the experiment are located in USA15 (main counting room, cooling plant etc.) and US15. The ITk will be lowered on the C-Side of ATLAS.

the access shafts to the underground cavern. A sketch of the underground areas is shown in Figure 17.2.

The ITk is assembled on rails inside of the SR1 cleanroom extension that are aligned with a door to the outside, see Figure 17.3. This door has a temporary exterior wall that is removable to allow the ITk to roll outside on these rails to an exterior level pad. This pad is in the same location used to lift and transfer the Inner Detector Pixel system with a long boom crane for transfer from this pad to a waiting transport flat-bed truck just outside the access door of 3185. The same method will be used to deliver the ITk from SR1 to 3185, with known logistics. The boom crane is positioned between 3185 and 2175 with its boom extended to lift and transfer from the pad location to the truck with no boom-extension operations. This is necessary as boom extension imposes undesired acceleration. The waiting truck has special suspension and steering to allow it to safely position itself under the ITk and transfer it from outside to underneath the gantry crane inside 3185 that will pick it from the truck and lower it into the UX15 Cavern.

17.2 ATLAS Opening Configuration and Infrastructure

Because of the size of the Outer Cylinder the movement to the inner bore of the Barrel cryostat will require ATLAS to be in the “Large Opening” configuration, which is the only one that provides a gap between the end-cap and the barrel Toroid which is large enough for the Tracker to pass. Temporarily access platforms, called Minivans, will be installed

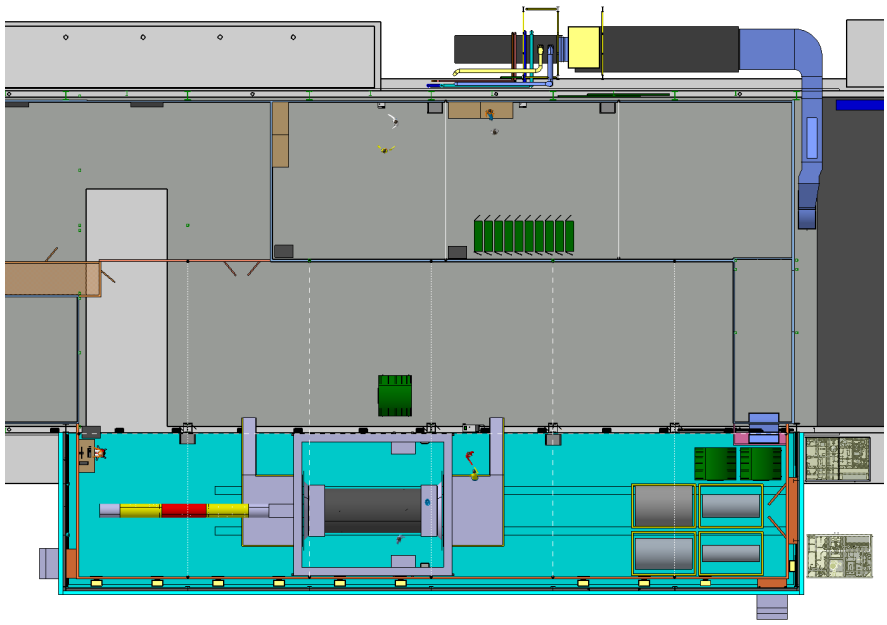


Figure 17.3: ITk assembly site in SR1 building 2175. Grey area shows the original space while the blue area shows the extension of building 2175 where the ITk Detector will be assembled.

on the ATLAS rails to provide a work platform inside the area, together with dedicated access tooling (rails, scaffolding, etc.). This configuration has been used to install the Inner Detector in 2007 and more recently the IBL detector in 2014.

Six minivans are installed in between the barrel and end-cap calorimeters, providing a work area of about 11 m $\times$ 6 m. Two rails are installed parallel to the beam axis in order to move the ITk on its insertion tooling (see Section 17.4.1).

17.3 Preparations of the Cryostat before the ITk Insertion

The ITk is supported and guided during its insertion into the inner warm vessel by the ITk rails (see Figure 17.4). This new aluminium rail system is dimensioned such that it can take the load of the new tracker (about 5 t). The ITk rails are installed on both sides of the inner warm vessel on the same rail support that are used by the current Inner Detector, which is called the tracker support rail. The geometrical shape of the ITk rails will be defined with the interface support of the Outer Cylinder once its design is more advanced.

The Tracker Support Rails (tracker support rail) contain M5 threaded holes distributed every 60 mm along its length, which will provide the anchoring points and the vertical and horizontal references for the new rails. To be able to limit the traction forces on the M5 bolts, the lever arm to take the torque created by the load eccentricity is increased at the

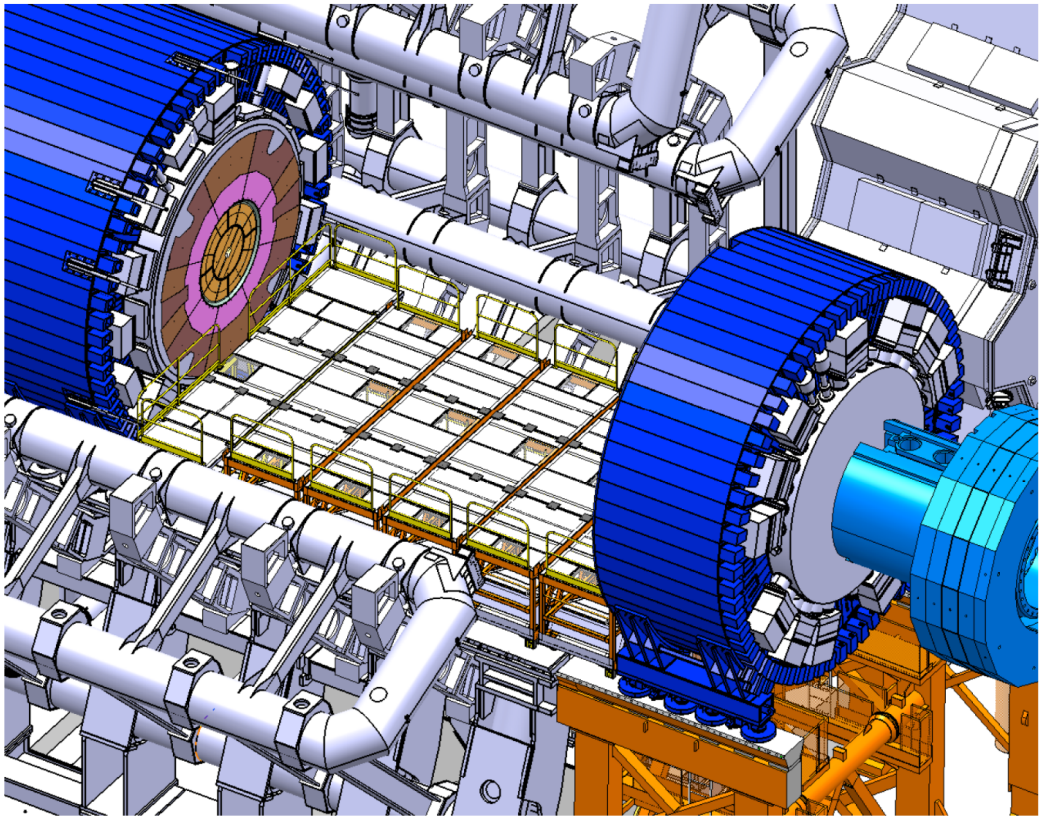


Figure 17.4: ATLAS Large Opening configuration. The end-cap calorimeter is moved as much as possible toward the Target Absorber Secondaries (TAS), six Minivans are positioned in between the barrel and end-cap calorimeters

bottom part of the rail by a fixation point on the inner warm vessel. Both rails are brought inside the inner warm vessel as a single element. Their weight (about 50 kg) will allow a manual manipulation and installation on the tracker support rails.

Once installed on the inner warm vessel rail support, a survey operation is done:

- to adjust the vertical position.
- to adjust the horizontal position at the level of the V-shape rails (Figure 17.6).

The expected range of positioning is in the order of 0.2 mm as achieved on the ID rail. The eccentric point of the rails will be brought close the inner warm vessel with a controlled gap of about 0.2 mm. Further analysis is required to finalise this gap value.

Access to the inside of the inner warm vessel over the full length will be possible on a platform supported at both extremities on the minivans as it was done during the installation of the ID rails. If the activation (see next chapter) in the inner warm vessel is such that a shielding or any other tooling is required to allow access for work specific access these

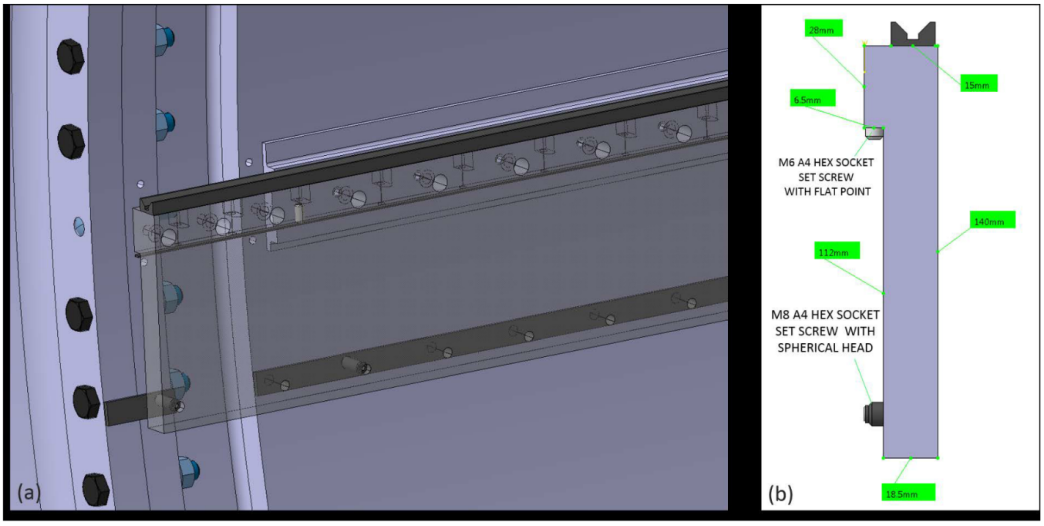


Figure 17.5: (a) ITk rail connected to the Inner Warm Vessel and (b) ITk rail cross section

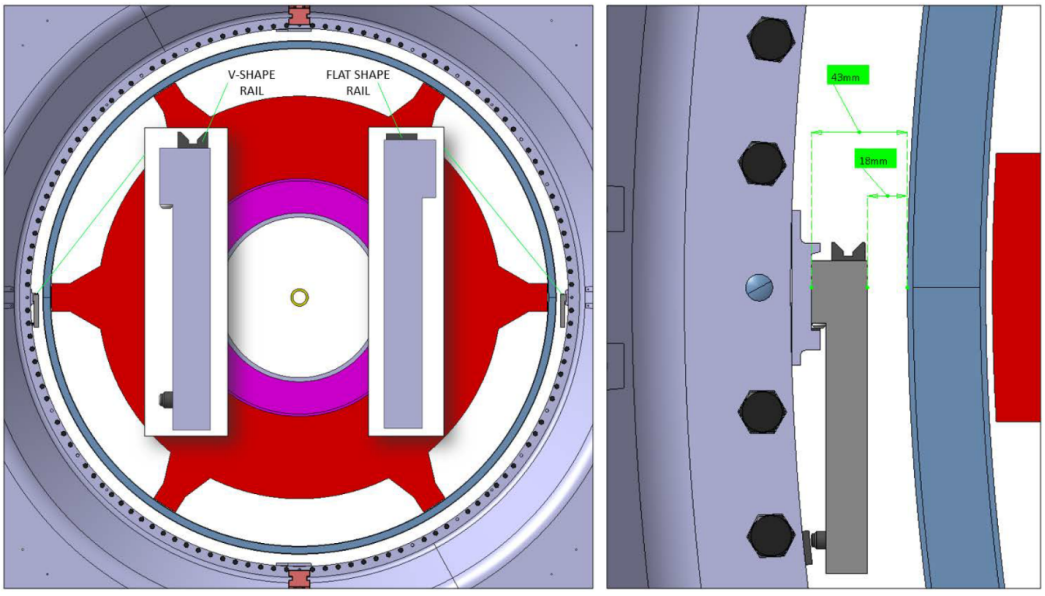


Figure 17.6: V-shape and flat shape rail guides on the ITk rails. Rectangles in the left drawing are enlargements showing details of the V and flat shapes.

means will be developed during the decommissioning phase of the ID, which will remove the current rails for the ID.

Figure 17.7: Access platform inside the inner warm vessel during ID construction.

The time required to perform the installation and the adjustment operation will be measured on a scale one mock-up.

17.4 ITk Transport

At the current stage of the project it is not yet decided if the integration support structure that will be used for the integration activities in SR1 will be used also as the transport structure for the transport to building 3185 (SX1). It would make sense that a common support structure with both functionalities of integration and transport exists to minimise the manipulation and load transfer of such delicate detector. The functionality and feasibility details will be discussed and worked out during the tooling definition, once the architecture of the Outer Cylinder is better defined. Several specific tools are needed to perform the transport and positioning of the ITk into the barrel cryostat inner bore. All these tools are still under design at a conceptual stage.

We can therefore not give a detailed description of these items here, but we present a list of these tools as well as their main functions.

- Transport Frame: The main function of the Transport Frame is to allow the lifting and the manipulation of the ITk with overhead and mobile cranes between the surface buildings and from the surface (Bldg. 3185, SX1) to the underground experimental cavern (UX15). The secondary function of this frame is to provide environmental protection for the ITk while it is transported out of clean and controlled environments.

- Support Cradle: The function of the Support Cradle is to support the weight of the ITk. The ITk Detector is similarly interfaced with the Support Cradle as it is with the calorimeter bore rail system. The adjustment of the Support Cradle is allowing the positioning of ITk prior to its insertion into the calorimeter bore.

- Rotating Table: Whatever the lowering scenario will be, the ITk will be unloaded on the Minivans with its axis perpendicular to the beam axis. There is a need for rotating it by 90°. This is the primary function of the rotating table. The table will also be used for the translation movement from the lowering point to the insertion point using wheels or rollers interfaced with the rails installed on the top of the minivans. The Rotating Table must be capable of supporting the weight of all the objects resting on it: The ITk, the Support Cradle and the Transport Frame. The preliminary estimate for the total weight of these objects is about 7 t.

The Transport Frame is interfaced with the Support Cradle; they can be combined such that they create a single tooling with both individual functionalities. Further study will define if a combined design makes sense with respect to the integration and transport constraints.

17.4.1 Crane Operation

The overall dimensions of the package that is possible to be handled, including attached services are defined in the envelope drawing; the outer diameter is 2,216 mm and the length is 8,000 mm. One should note that the Transport Frame for the Outer Cylinder needs to be added to the envelope in order to define the overall transport envelope. This work is ongoing and will be updated regularly, as the definition of the Transport Frame will progress. A conservative estimate of the ITk weight is about 5 t. Therefore even with the addition of the Transport Frame the total weight will stay below 7 t. The transport operation from the Surface building (SX1) to the experimental cavern (UX15) will be done by the overhead 20 t crane of SX1 building. Although the operation could be performed either on side A or on side C of the experiment, the baseline has been defined to be on side C. To access the Minivan platform two paths are identified currently:

a) Direct from the surface: The ITk is lowered by the 20 t crane directly from the surface to the Minivans, through an open space at the top sector of the Barrel Toroid. The Inner tracker passes in between the end-cap calorimeter and the top toroid coils nearly vertically on top of the beam axis (Figure 17.8). The advantage of this solution is that the operation is direct with the 20 t crane and does not need any load transfer. However, the clearance between the Outer Cylinder and the various obstacles on its way is as small as 30 mm at the most critical place. This entails not only specific constraints on the design of the Transport Frame and Support Cradle but also a lot of care during the lowering operation. Among other constraints, this option requires the provisional removal of two main obstacles: the Forward Platform in sector 3 and the Barrel Toroid vacuum pipe as shown in Figure 17.8.

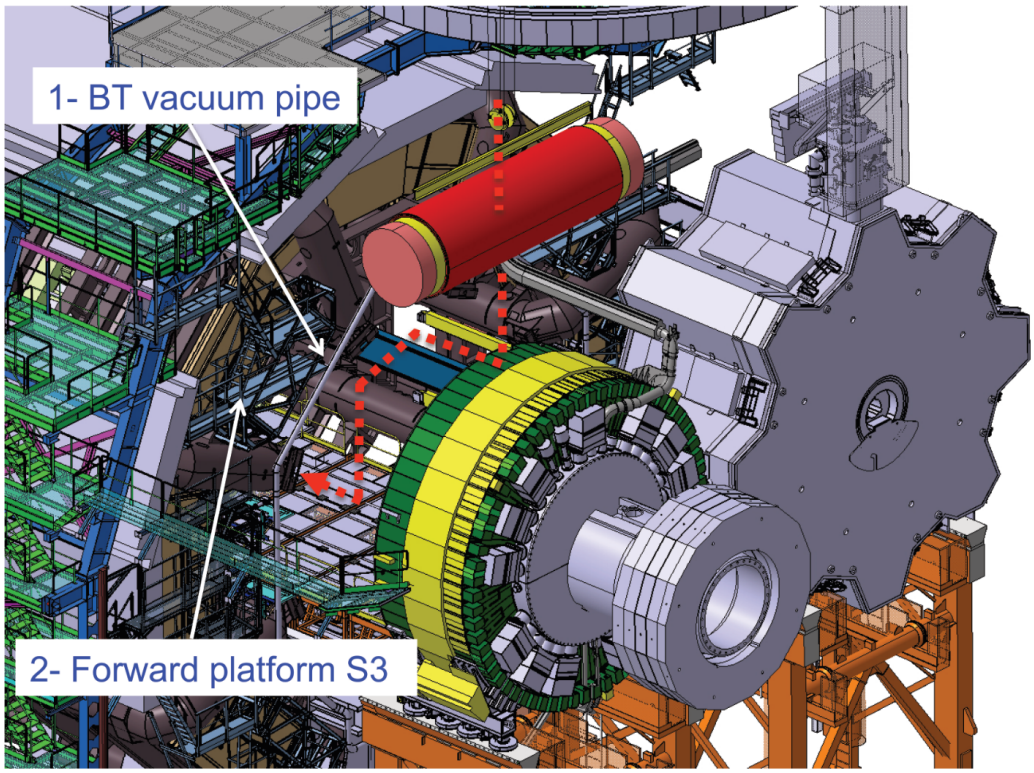


Figure 17.8: Path a: The ITk is lowered directly from the surface onto the Minivans; the red dotted line indicates the path.

b) Sideways lowering: In this scenario, the ITk is inserted onto the Minivans platform from the US side (Sector 1). This path is incompatible with the coverage of the surface crane; a load transfer is required inside the experimental cavern (UX15) so that the operation can be performed using the local underground crane (65 t capacity). The only possible location for this load transfer is on the top of the end-cap calorimeter which needs to be equipped with a resting platform to allow for this operation. Once the transfer is done, the ITk is lowered beside the calorimeter to the beam axis height and is then moved side-

ways until it can be unloaded onto the insertion tooling (Figure 17.9). This scenario has the main drawback that it requires the load transfer on the top of the calorimeter, which entails the design and manufacturing of an additional platform, including access means and personal protections. Nevertheless, the clearance between the Outer Cylinder and the various obstacles on its way is about 90 mm at the most critical place, which is a clear advantage of this option. As for the previous scenario some conflicts have to be resolved by removing some items temporarily. Three main obstacles have been identified: the Forward Platform in sector 1, the Barrel Toroid vacuum pipe and the arch stairs as shown in Figure 17.9.

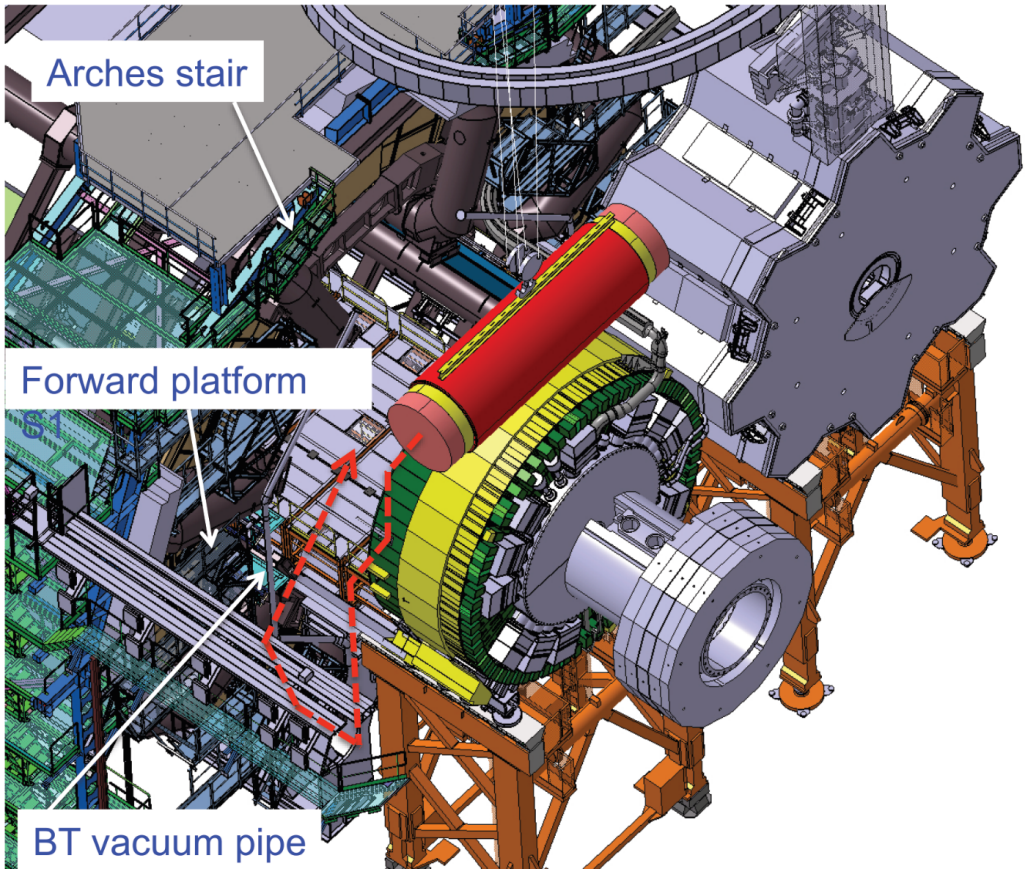


Figure 17.9: Path b: The ITk is lowered in 2 steps: first onto the top of the end-cap Calorimeter then sideways to the Minivans; the red dotted line indicates the path.

Option a) is more straightforward and is the preferred one despite the very small clearance involved. However, it is mandatory to ensure that the ITk can pass through such a small clearance. The opportunity to study the geometry of ATLAS in a Large Opening configuration is not frequent: a Large Opening was performed on side C during Long Shutdown 1 (2013-2014) and the next Large Opening will happen on both sides during Long Shutdown 2 (2019-2020). During LS1 an accurate survey has been done, in particular a 3D scan. The data from this survey has been used to create an “as built” 3D CAD model of this region of ATLAS. This model is being used to study the lifting scenario and the installation tools.

In order to mitigate the risk related to the very small clearance, it has been decided to perform a blank test of the ITk lowering during LS2, which is the next opportunity when a Large Opening of ATLAS will take place. A dummy Outer Cylinder will be manufactured, including space reservation for services, together with a dummy Transport Frame and Support Cradle. The use of a spreader beam may be required. The dummy package will be moved to the Minivans without unloading it, as the installation tooling will not be available at that time. However, no showstopper is expected in this step.

Both lifting scenarios will be tested in order to check that all conflicts have been detected.

In both scenarios, the BT vacuum pipe needs to be modified to allow its local removal to free the passage of the ITk package. It will be the right time during LS2 to implement the modification on the vacuum line to anticipate the required LS3 configuration and to test the insertion paths with the dummy ITk package.

The preparatory work is the key to the success of such the installation process. Once the end-cap Calorimeter has been moved to the Large Opening position, the six Minivans will be lowered and rails positioned ready to receive the ITk. The position of the rails are surveyed with respect to the inner bore of the Liquid Argon Cryostat. The Rotating Table will then be lowered and installed onto the rails of the minivans, ready to host the ITk package

Due to the access constrains, the ITk Detector with its Support Cradle are released on the Rotating Table perpendicular to the beam axis close to the end-cap calorimeter at about 13,400 mm from the IP (Position 1) as shown in Figure 17.10.

17.4.2 Rotation and Translation

To reach the insertion position, the ITk on its Support Cradle needs to be successively translated towards the IP at about 9,400 mm from the IP (Position 2), and rotated by 90° to be coaxial with the beam axis (see Figure 17.11). Then the package is translated up to its insertion position at about 6,775 mm from the IP (Position 3) as shown in Figure 17.12.

The translation movement is done on a rail system installed on the minivans, parallel to the beam axis, similar or identical to the one used by the ID. The rotation to bring the ITk axis onto the beam axis will be done on a Rotating Table similar or identical to the one that has been used for the Inner Detector.

At this stage of the project it has not been decided if these translation and rotation movements are manual or motorised using actuators. Several parameters need to be evaluated before taking that decision:

- The weight of the overall translated object.
- The activation in the environment that may limit the presence of operators during the operation.

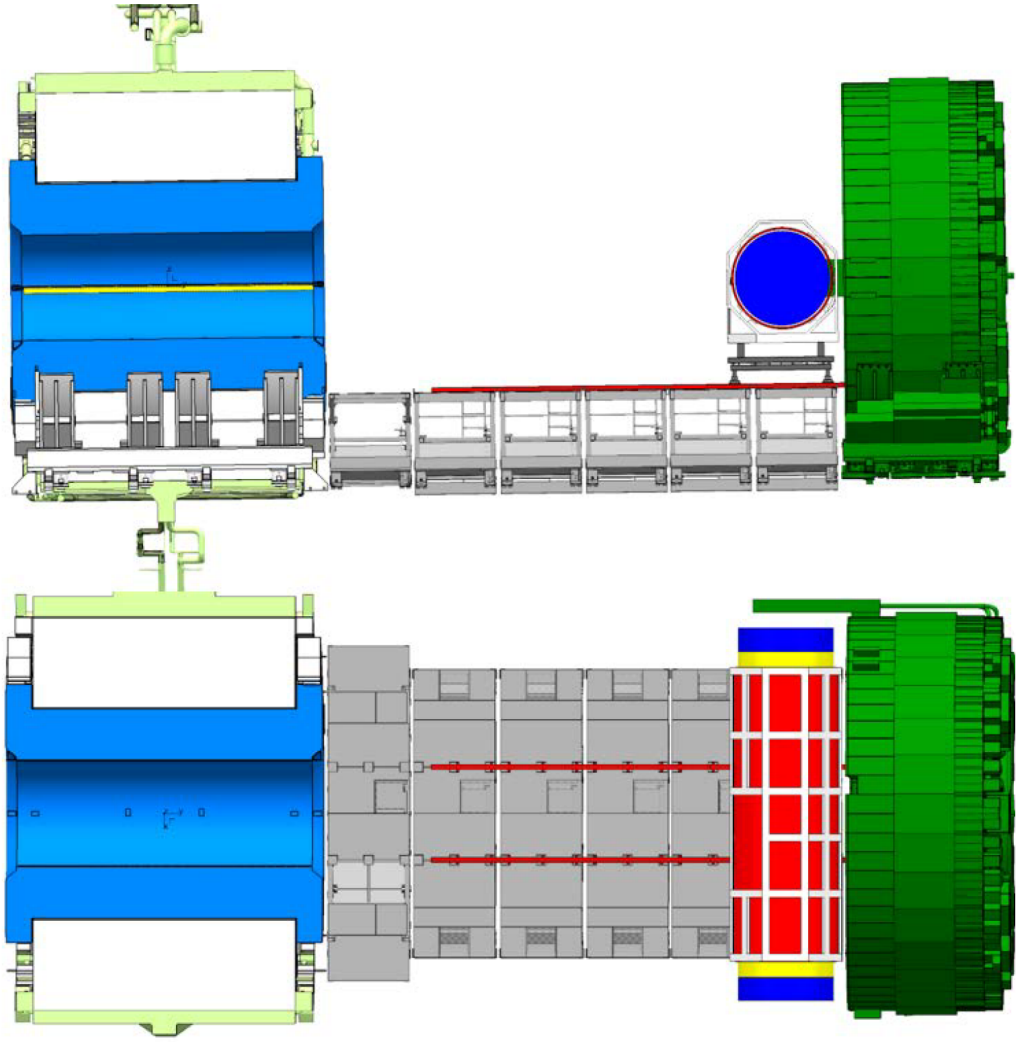


Figure 17.10: Position of ITk on minivans platform after release from the crane (Position 1). Top drawing is side view and bottom drawing is top view.

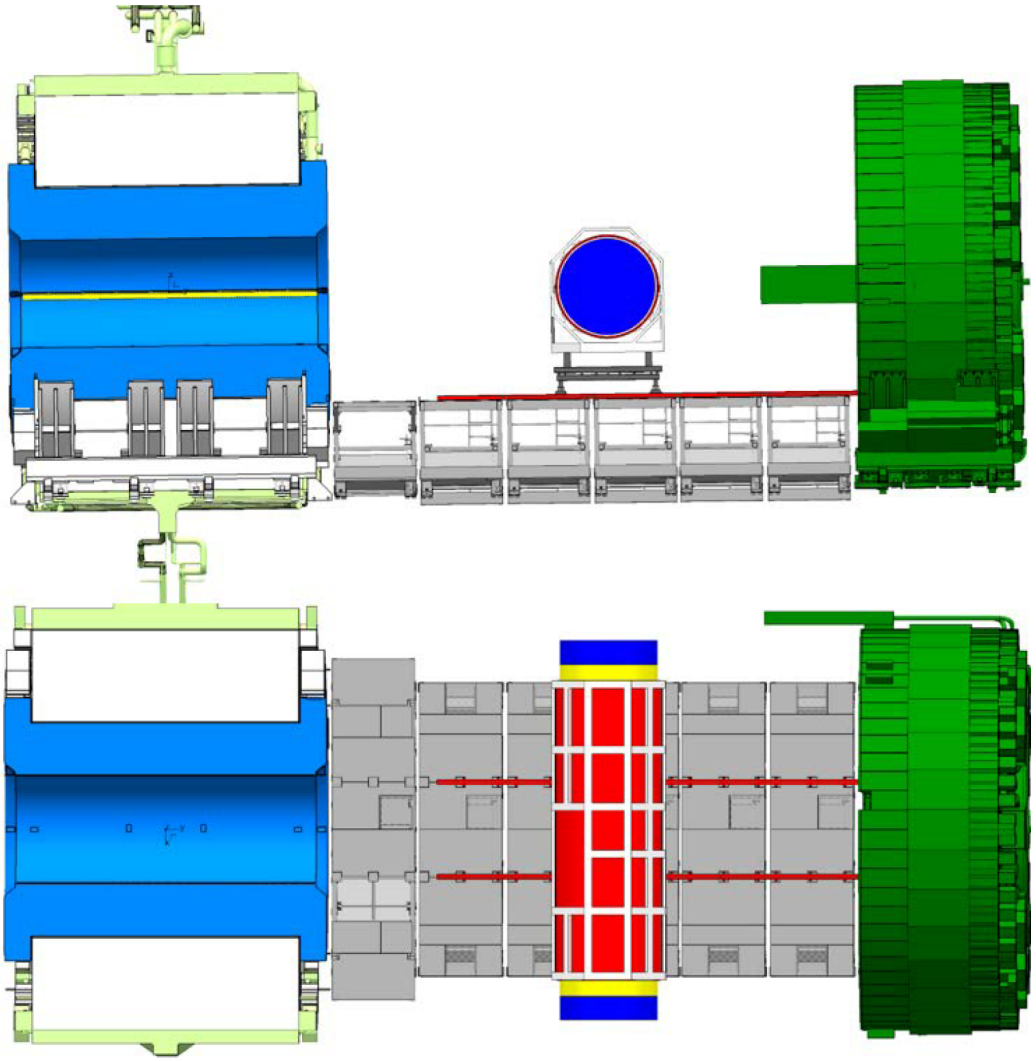


Figure 17.11: ITk Rotation position (Position 2) at about 9.4 m from the IP.

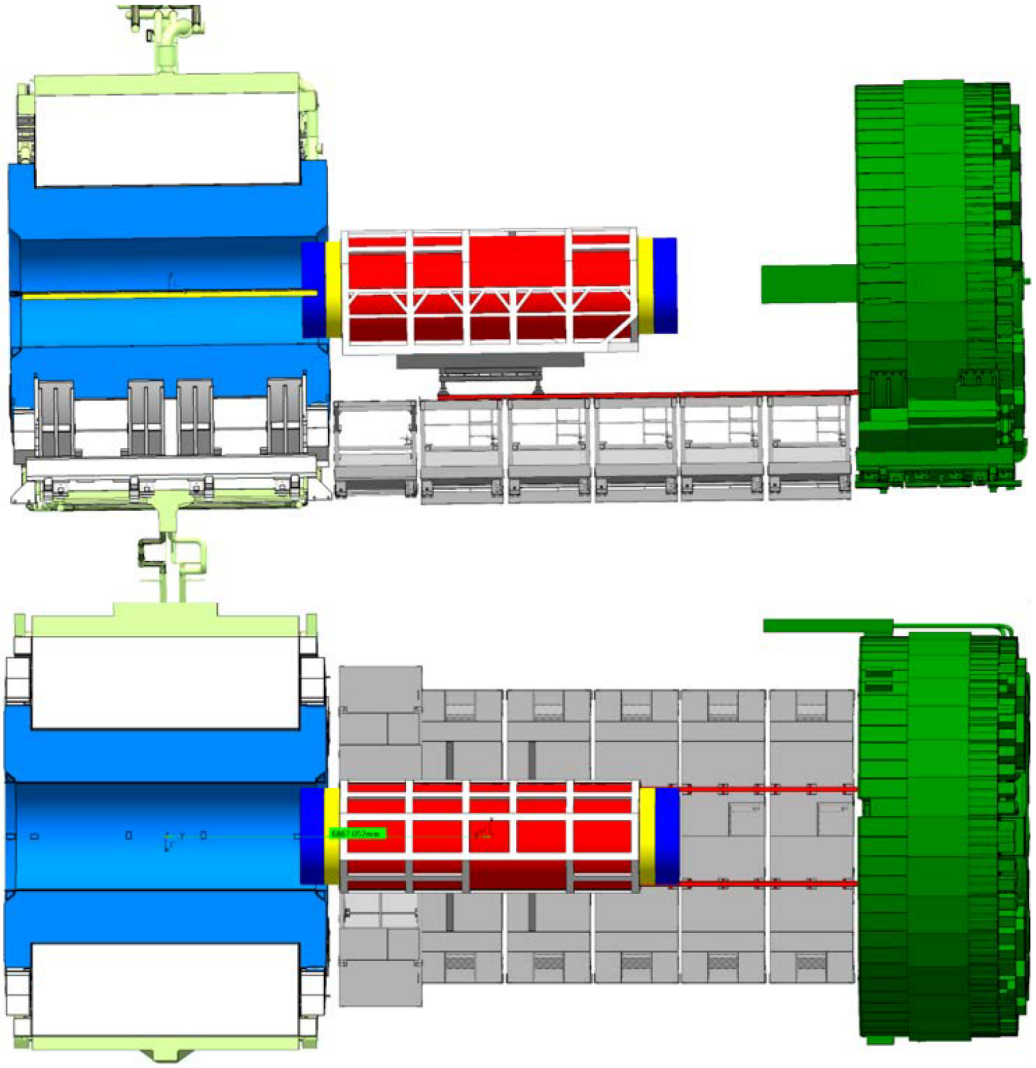


Figure 17.12: ITk ready for insertion (Position 3) at about 7 m from the IP.

- The precision needed for the control of the movement parameters like position, speed and acceleration.

17.4.3 Insertion of ITk into the Cryostat

At the end of the translation and rotation steps described in the previous section and prior to the insertion of ITk into the calorimeter bore, a precise positioning will be done to bring the ITk package co-axial with the inner warm vessel tracker support rails. This positioning will be done with the help of the survey team and using adjustment mechanisms on the support structures (Rotating Table and Support Cradle).

The Support Cradle will have a matching rail system that will be connected to the inner warm vessel tracker support rails for continuity. After the mechanical connection of both rail systems, the tracker will be moved on the rails into the calorimeter bore. The insertion stroke is about 7 m (see Figure 17.13). The rails are acting as a guide and as the support of the tracker during its insertion. The tracker translation is foreseen to be motorised, to control the insertion force, position, speed and acceleration. The rail system has the advantage to reduce the ITk dynamic envelope during its insertion into the calorimeter bore. This dynamic envelope still has to be defined. The complete insertion mechanism and tooling will be designed to allow both, the insertion and the extraction of the tracker. This means in particular that it will be designed to move the detector towards or against the ATLAS beam slope of 0.708°.

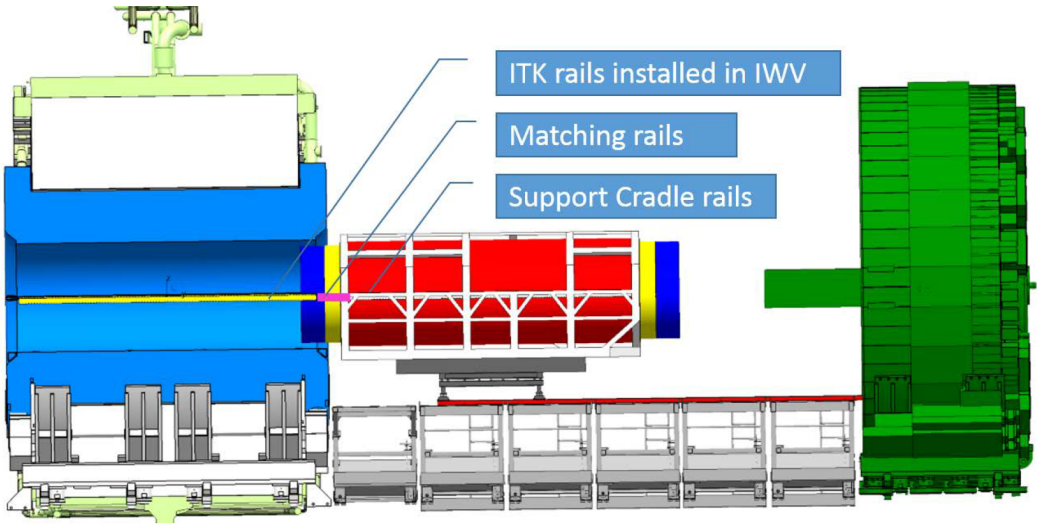


Figure 17.13: ITk ready for insertion (Position 3) at about 7 m from the IP with matching rails.

The insertion tooling will be motorised to control the insertion speed, the acceleration but also to control the power consumption of the stage. For all parameters, maximum acceptable values will be set and once reached the movement will be stopped. The threshold

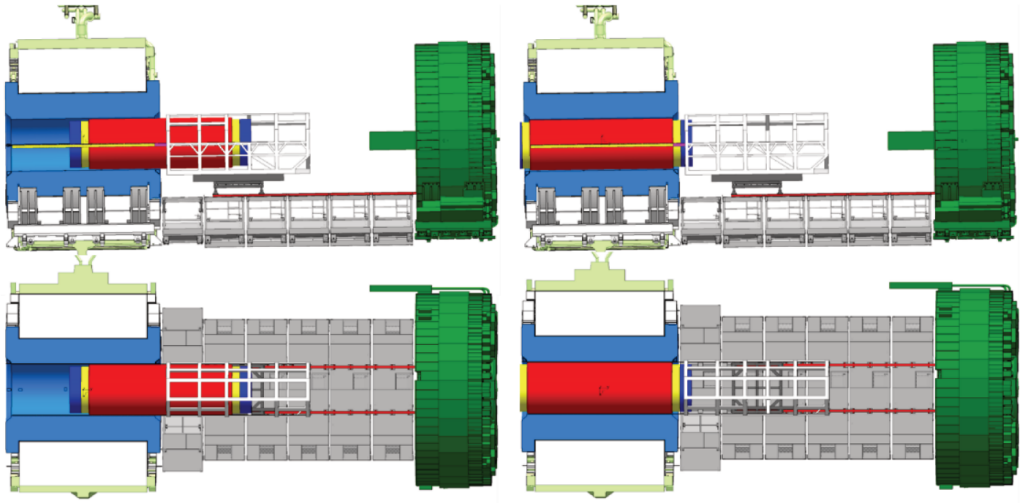


Figure 17.14: ITk insertion into the inner warm vessel.

values will be adjusted during commissioning work with one mock-up on the stage. In particular the power consumption will be optimised to detect any holding points or conflict during the insertion or extraction operation.

The ITk final position is defined in the following way:

- In Z (along beam axis) the translation movement is stopped when the tracker reaches its target operating position (given by the survey team). To guarantee no movement over time, the tracker is fixed to the calorimeter. The geometry of the fixations on Side A or C and their position on the OC shall be decided in conjunction with the internal architecture and fixation points of the different ITk sub-systems.
- In Y (vertical) and X (horizontal) the positioning is done at the assembly stage by the vertical and horizontal positioning of the interfaces (V-shape rail and Flat-shape rail as well as the position of support wheels with respect to the tracker). Therefore no adjustment is foreseen during the insertion of the tracker into the calorimeter bore.

17.5 Service Installation

The service plant for the ITk will be installed in parallel with Inner Detector Decommissioning. Where envelopes are shared or interfere with ID Services, their removal must complete before onset of ITk service installation. This is most directly the case for the Type-II services. These run from the type 1 patch panels (PP1s) that are part of the ITk package, and run along the cryostat wall through gaps in Tile fingers, LAr power supplies, and Muon chambers to reach various Patch Panel 2 (PP2) locations which are shown in Figure 17.15. The envelopes along the cryostat wall and through the various gaps are very tight, and require

accurate positioning of fibre, cable and pipe routing and controls to assure envelopes are maintained.

From PP2, services are routed outward radially to either US15 or USA15, or to patch panels (PP3) on the HX Platforms in ATLAS. These are the external platforms surrounding ATLAS in the UX15 cavern providing various access points to the detector volume, and populated with equipment racks. All services leaving PP2 are called Type-III services, regardless of destination. Cables running from PP3 to either US/USA15 are called Type-IV services.

The ID Services will be removed by sector, starting possibly at the top. This is preferred because the PP2 cooling boxes for the majority of ITk are in sector 5 which is on top. Its desired to install the CO_2 cooling lines near the beginning of service installation because they have the largest single cross-section (50 mm diameter flex-lines). Installation of services by sector will allow a complete service chain to be installed and commissioned prior to connecting to the ITk. This work will interact with many other activities in the cavern, most importantly refurbishment and upgrades to the Muon chambers, so advancing on multiple sectors in parallel will be required to fit around other complex work packages ongoing in the cavern.

While the work to complete service installation will be completed by sector, the installation environment is divided radially. The Type-II services will be installed by ITk personnel, up to the tile fingers, and ATLAS TC technical personnel are responsible for routing beyond that. Termination of services at patch panel locations; connecting and testing are the responsibility of the sub-systems, e.g. Pixel and Strip communities.

17.5.1 Type-II Service Installation on the Cryostat Wall

Type-II services run from the ITk PP1 to the various PP2 locations, with the exception of the optical fibres which run directly to the counting room in USA15 with no breaks. All Type-I services are delivered with the ITk Package. Most are terminated in bulkhead connectors mechanically mounted to the ITk, some few are "pigtails" that arrive with the ITk package and need to be dressed out onto the cryostat wall – most notably the Pixel Data Cables, which will route to "Opto-boxes" located on the cryo wall.

The service layout for Type-II services is preliminary. Envelope studies to place opto-boxes and splitter boxes required for the CO_2 cooling system are ongoing. The guidance for all service envelope studies is that the ITk plans to re-use all envelopes from the ID, this includes most of the cryostat face and named gaps in tile fingers. Services are mostly routed out radially from low radius where there is little room for re-arrangement in phi. Phi-rerouting occurs at larger radius for the services to reach the named routing gaps. It is desired to minimize cross-overs of services when possible. Services that are installed late, or for new subsystems such as the Insertable B-Layer (IBL) in the current ID are the exception seen in Figure 17.16.

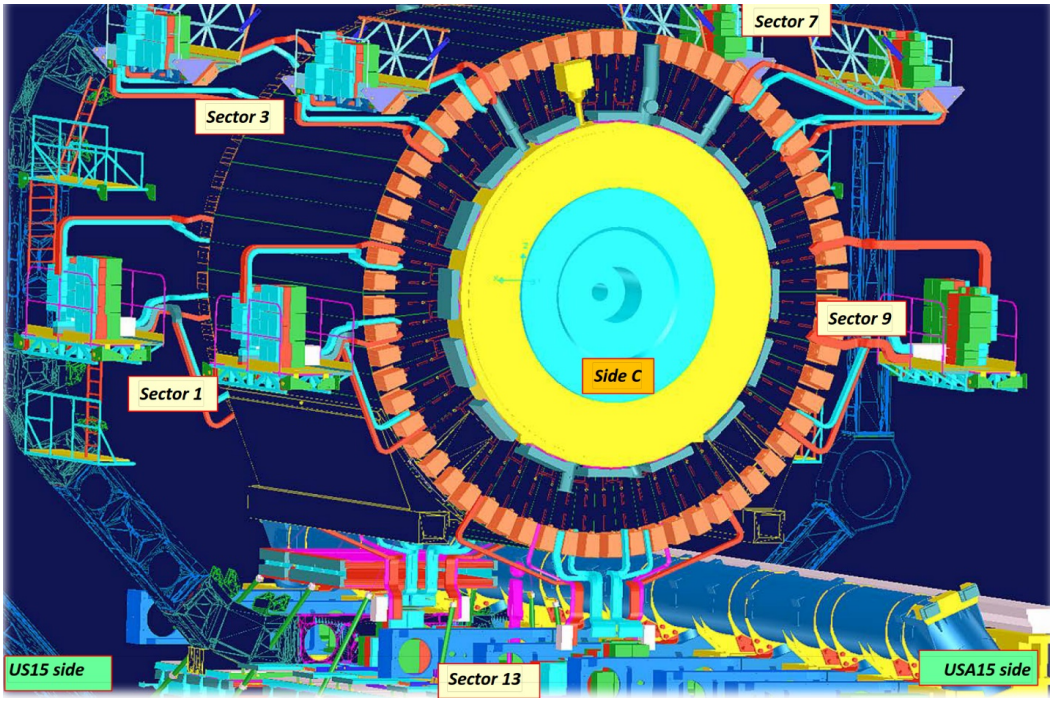


Figure 17.15: Patch Panel 2 locations are distributed in named sectors around ATLAS on both Sides A and C and are located between Muon Chamber layers

Type-II services for the ID are probably the most complex routing environment. The same will be true for the ITk. There is little to no space for excess cable storage on the cryostat face. To install Type-II services, mockups of the ITk PP1s will be required. These dummy patch panels will be installed prior to ITk insertion and allow dressing of services from their locations radially outward through the tile fingers where excess length will be stored until ATLAS TC is ready to continue routing to PP2 through the Muon chambers. These gaps are shown in Figure 17.19.

After Type-II services are installed, at low radius, they will need to be folded back and temporarily supported to allow for ITk insertion. Type-II services will not be connected to the ITk until after completion of the service chain in that sector to allow for complete qualification of the services' response to all controls. A programmable dummy load is planned which can emulate the ITk sub-systems, and exercise the DCS, DSS, and all interlocks. This test is required before connecting the external service plant in the cavern to the ITk.

17.5.2 Patch Panel 2 Installation and Connection

The patch panel 2 locations shown in Figure 17.15 will be preserved, but on modified platforms. The Inner Barrel Muon chambers will grow slightly in thickness requiring that the PP2 platforms be removed and modified. This can happen as soon as decommissioning

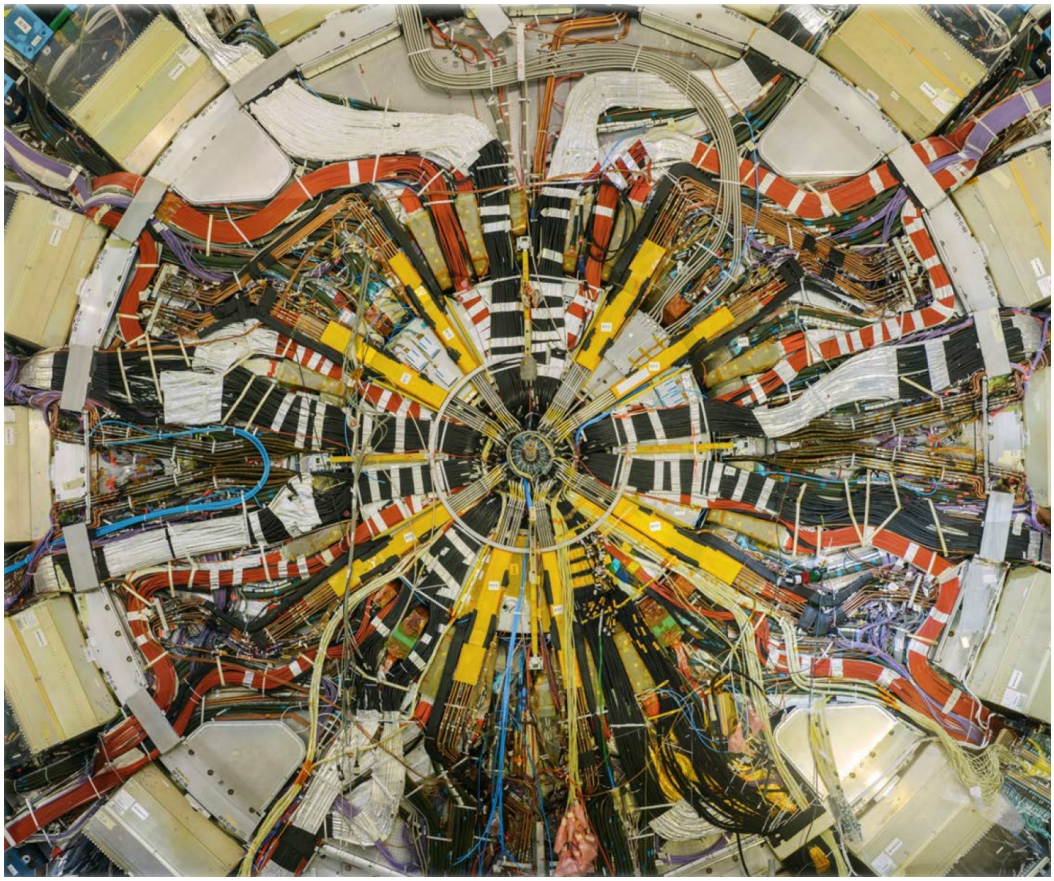


Figure 17.16: Inner Detector services on the Argon Barrel Cryostat wall after installation of the Insertable B-Layer (IBL).

starts so should be completed prior to routing Type-II services to the PP2. The PP2 shown in the figure are primarily for ITk electrical services, so will refer mostly to cables in this section. The cooling services come from an independent PP2 in Sector 5 and are described in the cooling chapter. Some few other services are not routed to PP2, but directly to USA15, such as the optical services. Additionally, some of the patch panels will require cooling – this service is provided by TC already at these locations and will be connected during patch panel installation.

The Pixel system plans to re-use most of the Type-III cables that service the current PP2. These cables were installed by plugging them into the current ID Pixel PP2, then pulled from there to US/USA15. There is no excess cable length on the Pixel Type-III cables at PP2 meaning that the ITk Pixel PP2 must either have the same connector layout, or plan to re-terminate all of their Type-III cables prior to PP2 installation.

The ITk Strip system plans to install new Type-III cables from PP2 to PP3. This allows for installing the Strip PP2 first, then pulling cables from it to PP3. In both cases not much space is required to store excess Type-III cable length. This means that the installation of

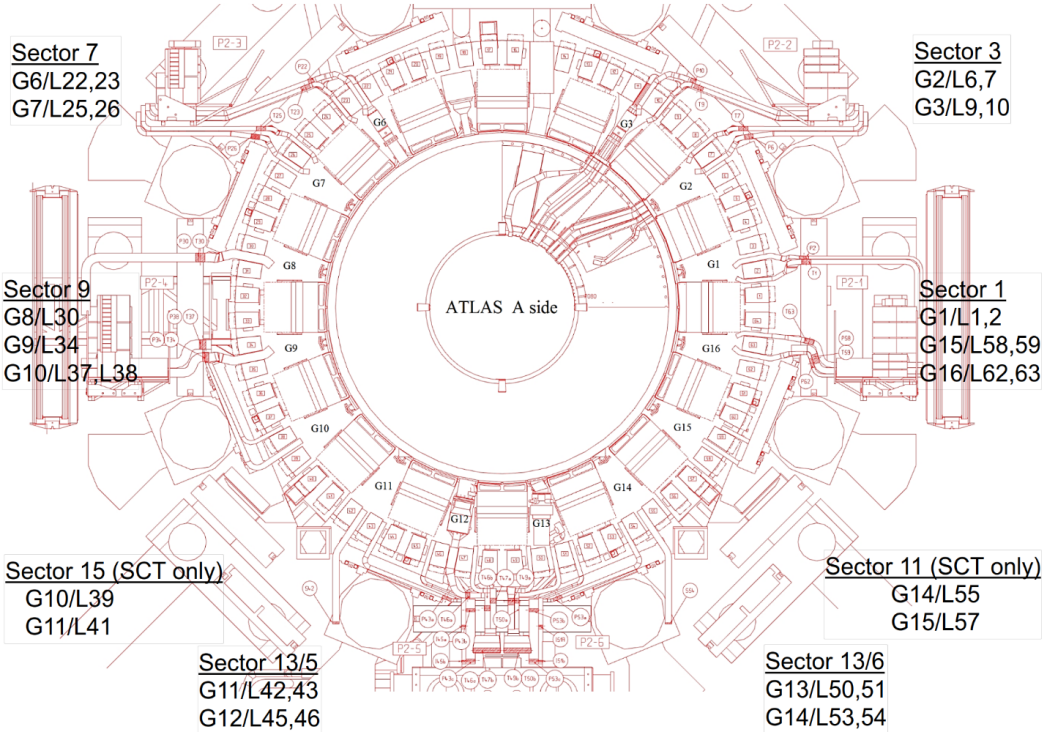


Figure 17.17: Tile Finger gaps used by the Inner Detector and re-used by ITk. Gaps on the top in Sector 5 have not been defined, but are under-utilized.

the PP2 boxes, is independent of Type-II cable installation in schedule and can proceed in parallel. The installation order of Strip versus Pixel PP2 will depend on the work that may be required to re-terminate Pixel Type-III cables. It is also Sector dependent – each PP2 platform is configured differently so order will be configuration dependent.

There is space under each of the PP2 locations, with exception of the Sector 13 location to store excess Type-II cables, which will be utilized once TC is able to route these services to the various PP2 locations. The primary schedule conflict for routing Type-II cables to PP2 is Muon Chamber installation.

The ID services must be removed to allow Muon chambers movement in $|Z|$. ITk Type-II services can be installed at lower radius, but cannot be routed to PP2 until after completion of work on the Muon chambers. While this is a clear physical conflict, the auxiliary work on Muon chambers may require other chambers to move into ITk service routing gaps for their access.

ITk Type-II service cross-sections are intended to be identical, but many of the cables will be larger in diameter. Bend radii of larger cables during installation may necessitate changes in routing or gap selection. This will be tested on the 1:1 mockup installed in Bat. 180. CAD Modelling of the ID services, and many other sub-systems is incomplete or not wholly updated in CATIA. This work was started in EUCLID, the CAD package that ATLAS was

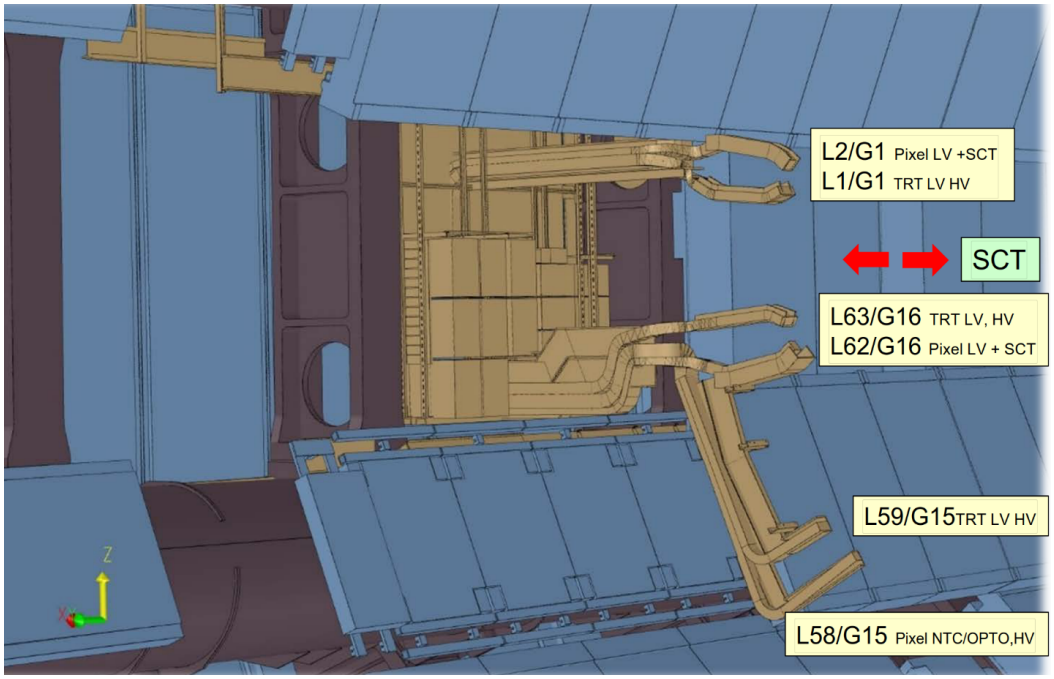


Figure 17.18: ITk Type-II Services penetrate gaps in the Muon Chambers obstructing access to the chambers at low $|Z|$. Red arrows indicate chambers that must move to higher Z.

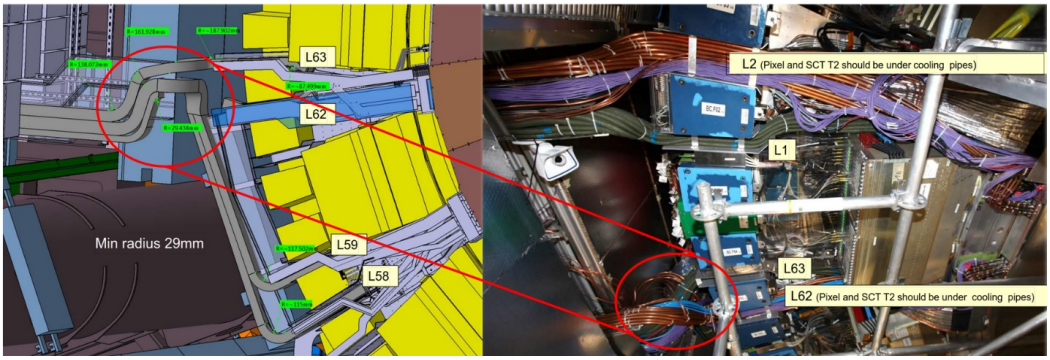


Figure 17.19: Type-II service routing through gaps. Circled region is through the muon chambers.

originally designed in, then ported to CATIA. This CAD model is quite detailed, but a significant portion is unverified, particularly between PP2 and PP3, but also between the tile fingers and PP2 regions. As noted in Figure 17.19, many services are covered by others that were installed later. It is likely that as the ID decommissioning advances, changes to detail design of service routing may change as un-documented services are uncovered. Engineering and designer effort is planned during this phase of the project to keep up with new information and update the modelling and planning as required.

17.5.3 Type-III and -IV service installation

For the ITk Pixel Detector no significant work is planned to install cables beyond PP2. Some auxiliary cables may be required for Pixels, e.g. High Voltage, and some auxiliary control cables, but these are few, e.g. under 100. Some may be routed to PP2 or directly from PP1. The ones which are installed to PP2 can likely be installed along with the Strip cables which will be replacing the entire service chain from PP3 inward.

The Strip Type-III cables will be installed in the current ID SCT service envelope where it can be made available. This task will start at PP2 with pre-terminated cables which are pulled and dressed into the cable trays vacated by ID SCT cables, or in newly installed cable trays. This work, both design and installation is controlled by TC and is a work in progress. Investigation into currently installed services has begun during the last EYETS (Extended Year End Technical Stop) and will continue during LS2 where some more access will be available to verify currently installed services and to develop plans to remove those that are no longer required.

The ITk Strip Detector plans to re-use the ID SCT Type-IV cables from PP3 to US/USA15. No significant work is planned to remove any of the type 4 cables in the service chicanes up to USA15, or the penetrations into the US15 cavern. Some few new cables may need to be installed in existing cable trays/penetrations to reach US/USA15, as mentioned above for HV, fibre optics, and some control cables.

17.6 Radioprotection and Personal Safety during Installation

As for any activity on the CERN site concerned by radiological risk, the radiation protection ALARA (As Low As Reasonably Achievable) principles will need to be implemented [164, 165].

Those guiding principles are:

- Justification,
- Optimisation,

- Limitation.

To do so, the ITk Project Leader will need to ensure that the ALARA process is followed according to the General Safety Instruction [166]. The first step of the ALARA process will consist of a Provisional Interventions List (PIL) made in collaboration with all potentially intervening parties. As the installation of the ITk will occur during long shutdown LS3 the process will start the latest during LHC Run 3.

To establish this list, each intervening group will provide the following information:

- Short description of the intervention
- CERN group responsible of the intervention
- Description of the status of the intervening personnel: external company, Member of Personnel
- Information on the location of the intervention
- Estimation of the intervention duration
- Estimation of the expected dose to people based on simulations

Once the Large Experiment Group Leader in Matters of Safety (LEXGLIMOS) of ATLAS and Radiation Safety Officer consider the Provisional Interventions List sufficiently documented, they will contact the CERN Radiation Protection group, as well as the intervening parties to determine the radiological nature of the interventions. The interventions can be qualified as permanent, repetitive or unique. In the case of the ITk installation the interventions will be classified as unique. The interventions will also be classified according to a radiological criteria: level I, level II or level III as described in Section 18.3.4.

The ALARA process to be followed will depend on this qualification. The Radiation Protection service will inform the intervening parties about the expected content of the file to be provided for interventions in a radioactive environment, in French Dossier d'Intervention en Milieu Radioactif (DIMR).

Level I and II are not submitted to the ALARA committee, only level III intervention shall be approved by the ALARA committee as mentioned in the General Safety Instruction [167]. DIMR Level I and II will be prepared and discussed between the intervening parties, the ATLAS LEXGLIMOS, the RSO, and a representative of the radiation protection service several days before the start of the intervention. Discussions will be organised regularly all along the intervention with the presence of the representatives listed above. Before any intervention, the DIMR shall be approved. An intervention cannot start without an approved DIMR.

A complete discussion of dose rates for decommissioning is given in the following chapter.

18 Inner Detector Decommissioning

18.1 Introduction

This chapter describes the decommissioning of the Inner Detector (ID) in order to enable the installation of the ITk during Long Shutdown 3 (LS3). In particular, it describes the removal and storage of the beam pipe, the removal of the IBL, Pixel, SCT and TRT detectors as well as the removal of all services from the cryostat volume and the ID endplates, up to the cable connections at Patch Panel 2 (PP2). It includes general consideration of radiation protection, dose mitigation planning and radioactive waste management and presents updated radiation simulations. These calculations will form the basis on which the decommissioning procedure will be optimised during the coming years. We present the foreseen work on different mockups to test and optimise the extraction procedure, the different training campaigns currently foreseen as well as the planned dose optimisation procedures. In addition, a first concept for possible shielding to lower the collective dose of personnel involved in the decommissioning process is proposed.

18.2 Sequence of the Inner Detector Extraction

18.2.1 Preparation Work & General Guidelines

To begin the decommissioning process, access to the Inner Detector End Plates (IDEP) on both sides is needed. Therefore, the ATLAS Detector must first be brought into a configuration that allows access for tools and the transport of material to and from these regions. The begin date of the decommissioning is envisaged to fall 10 weeks (70 days) after the beginning of the LS3, with the exception of work on PP2, which can start earlier. This timing leads to a cool down period of 98 days, assuming 4 weeks (28 days) of Heavy Ion running at the end of Run 3.

The beginning configuration will be as follows :

- Side C [1] in "Large Opening" to allow the usage of the crane to bring in various transport tooling

[1] Inside the ATLAS cavern UX15, Side C refers to the cavern side following the LHC clockwise (towards Point 2 - ALICE) while Side A refers to the side following the LHC counterclockwise (towards Point 8 - LHCb).

- Side A in an "Extended Standard Opening", increasing the distance to the End-cap calorimeter
- Minivans (a set of moveable platforms that can be placed on the main ATLAS rails to create a working platform in front of the Inner Detector) and scaffolding installed on Side C
- Scaffolding installed on Side A
- The outer beam pipe parts removed, only the beam pipe inside the Inner Detector (VI) still present
- ID outer end plate cover removed, services along the ID end plate are accessible

Figure 18.1 shows the working environment on Side C during the Pixel removal in LS1, with the Pixel support and transport tool visible. The area will be almost identical during the extraction of the beam pipe, IBL and Pixel for the decommissioning during LS3.

To minimise the general radiation background in the areas concerned, and therefore reduce the collective personnel dose, the decommissioning procedure will follow the general rule to remove potentially radioactive material as early as possible from the work area. As an example for this rule, it is proposed in the detailed sequence mentioned below to remove the IBL as soon as possible[2] (right after the extraction of the beam pipe), thereby reducing the activated material close to the work area during the Pixel service removal. Further radiation analysis and measurements will have some impact on the decisions made here, but given the current understanding of the general radiation environment, and of the most highly activated components, the stepwise approach listed below is deemed to be the most practical approach until more information is known.

18.2.2 Proposed Sequence of Decommissioning

In this section, the overall procedure for the removal of the Inner Detector is presented. The full schedule of this sequence can be found as a Gantt chart in [EDMS 1838361] and a high level summary can be found in Section 18.2.4.

The overall approach has been developed in consultation with sub-system experts, engineers involved in the original installation, and the ATLAS Design Office, which was responsible for the beam pipe and IBL installation. In addition, the times required are heavily informed by experience gained (and well documented, both manually and on video) of the removal of the Pixel Detector, which was performed for refurbishment during LS1. This previous removal process gives precious experience with the working conditions, manipulations to be made, and time required for the analogous (and partially identical) full ID decommissioning.

[2] The IBL could also be removed together with Pixel, if further analysis proves that this would be the better option regarding the exposure of personnel.

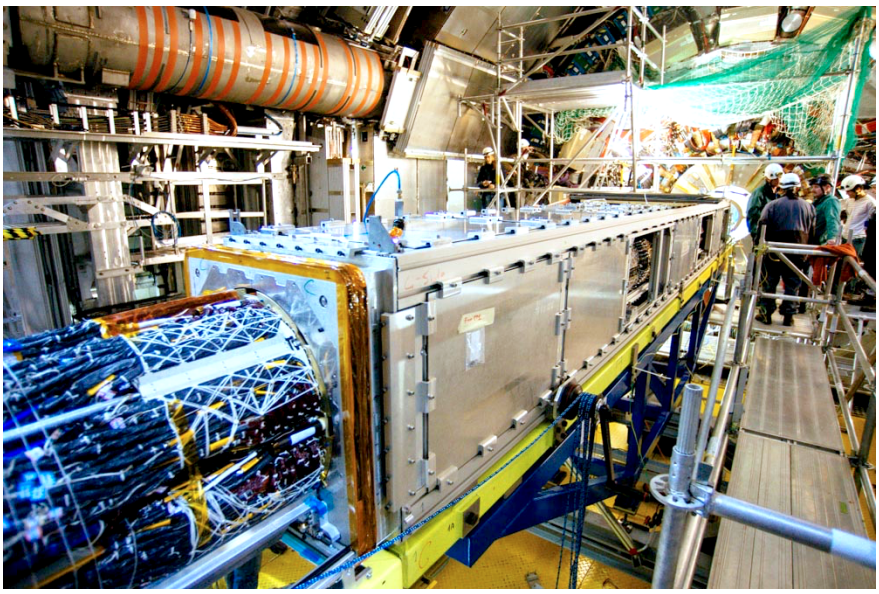


Figure 18.1: Work environment during the extraction of the Pixel Detector in LS1, with the Side C in large opening configuration. The Pixel support and transport tool is visible on the Minivans.

Broadly speaking, the beam-pipe is removed first, followed by the IBL and its low-radius services. The Pixel Detector follows next, combined with its low radius services, followed by the ID Endplate nose, End-cap and Barrel services at the cryostat chamfer, and finally the End-caps, followed by the Barrel. Lastly, the services on the bore of the cryostat barrel are removed. Higher radius services on the cryostat faces are removed either in parallel to or after their preceding activities (they do not highly impact progress made at lower radius, and are thus not critical to the schedule).

The disconnection of cables at PP2 can start as soon as the areas are accessible, since no activation of concern in these regions is expected, and work can progress in parallel to the main decommissioning campaign. Any cables and pipes can be cut downstream of PP2 as needed. The dismantling of the individual patch panels will begin immediately after the disconnection of the cables. This work may begin before the full opening of ATLAS occurs.

The currently proposed sequence for decommissioning is as follows :

1. Service Removal of non-radioactive services from the ID endplate up to PP2 : This initial step involves disconnection at PP2, an initial cut of cables and pipes at a specific radius on the face of the ID endplate, and removal of cables running up to PP2, as permitted by other work in the region.

2. Removal of VI beam pipe via Side C : The beam pipe pit table and transfer tool (designed, not yet manufactured) must be lowered and aligned, services cut, and the

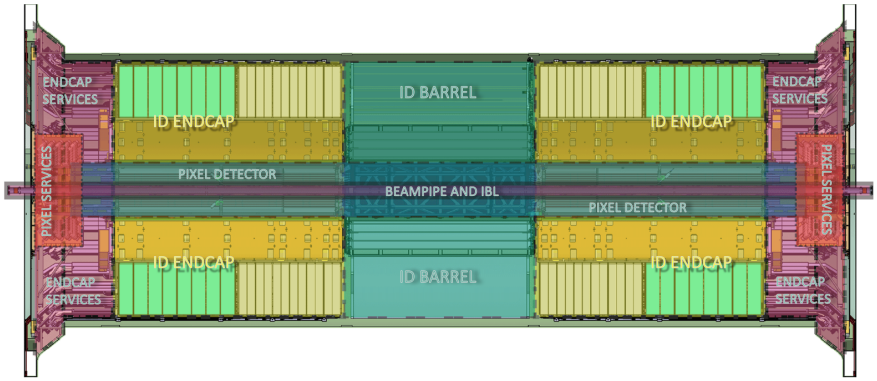


Figure 18.2: Detailed CAD model of the existing Inner Detector, with labelling of terms used in this chapter.

beam pipe extracted from the IBL to its protective container. It is then immediately delivered to the beam pipe group and will be reused.

3. Removal of IBL via Side C : After disconnection of the IBL services on both sides, the IBL can be extracted using the same tooling table and alignment as the beam pipe.

4. Removal of Pixel package via Side C : In order to access the Pixel package, service disconnection must be performed on both A and C sides. Heaters must be removed, cables cut within the Pixel nose, and the Pixel package extracted to the dummy support tube for transfer to the surface.

5. Removal of ID Endplate Nose and related supports from ID Endplate, sides A and C

6. Removal of ID services from cryostat face, Sides A and C. This step involves removing the remaining services from the face of the cryostat, thereby liberating access to the cryostat bore.

7. Removal of ID End-cap, Side C : The ID End-cap trolley must be lowered and aligned to the ID bore, allowing extraction and raising of the ID End-cap on Side C.

8. Removal of ID End-cap, Side A : The ID End-cap trolley must be lowered and aligned to the ID bore, allowing extraction and raising of the ID End-cap on Side A. This process requires a large opening on Side A.

9. Disconnection of ID Barrel services inside cryostat bore, Sides A and C : Now that the ID Bore has been cleared of all but the ID Barrel, work must commence inside the bore to cut and remove services holding the ID Barrel in place. In addition, the rails must be changed on the A side in order to allow the extraction of the ID Barrel.

10. Removal of ID Barrel, Side A : The ID Barrel trolley must be lowered and aligned to the cryostat bore for removal and extraction of the ID Barrel.

11. Removal of services from cryostat bore, Sides A and C : Now that the full detector has been removed, the cryostat bore must be cleared of all services and service trays.

12. Removal of all services from cryostat face, Sides A and C, and final cleaning.

18.2.3 End of Decommissioning Sequence

At the end of decommissioning, the cryostat bore will be clear of all services and trays, except for the barrel ID connection panels (PPb1) inside the cryostat which are laminated to the cryostat bore and have a thickness of approximately 3 mm. These will be left in place, as the effort required to remove them will be substantial, and the envelope gained will be small. The service trays, on the other hand, are easily removed, as has already been verified on the cryostat prototype. In addition, the ID rails will be removed, and the cryostat face completely cleaned of services and mechanical attachments. It has not yet been decided whether there will be a chemical cleaning of the bore and face of the cryostat before beginning installation of ITk.

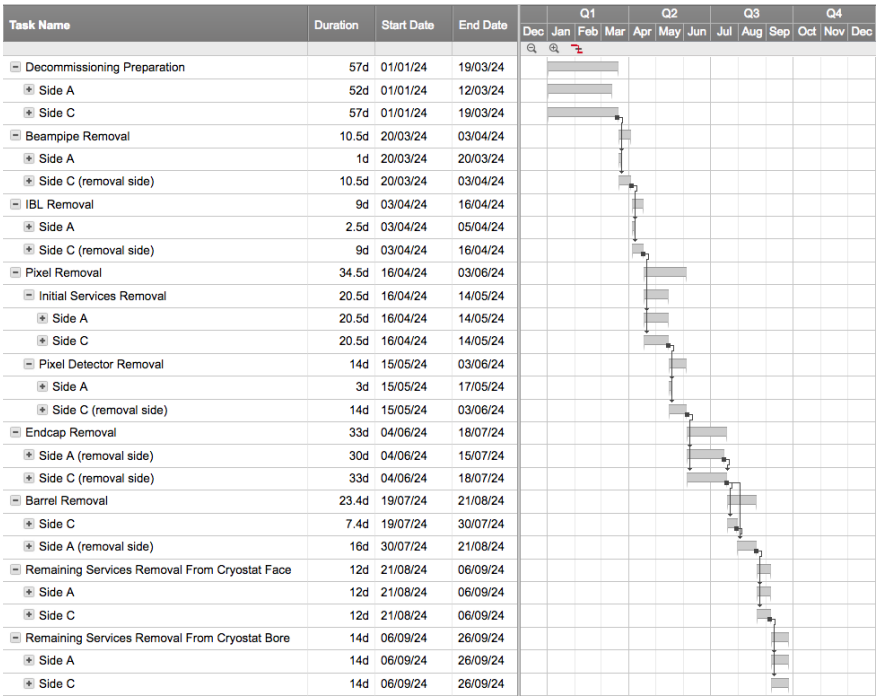
18.2.4 Estimated Time Schedule

As shown in Figure 18.3, the decommissioning process begins approximately three months after the beginning of LS3, which amounts to mid-March of 2024 in the current schedule. The beampipe and beampipe services are first disconnected in preparation for beampipe removal. IBL removal begins approximately two weeks later, followed by the Pixel disconnection and removal over the following eight weeks. Removal of both End-caps takes place over the next six weeks, arriving at the four month point in the decommissioning process (currently planned for mid-July). The final large item for removal, the ID barrel, is extracted in the next three weeks. Final removal of all services and attachments from the Cryostat bore and faces leads to a final completion date approximately 6 weeks later (or just over 6 months into decommissioning), providing for clean access for ITk from that point onwards, currently October 2024.

18.3 Radiation Protection Simulations and ALARA Considerations

18.3.1 Comparison of Simulated Radiation Levels to Measurements

In-situ radiation measurements were made during the End of Year Extended Technical Stop (EYETS) in 2016. The results can be found in Figure 18.4. These measurements were com-



Task Name	Duration	Start Date	End Date
Decommissioning Preparation	57d	01/01/24	19/03/24
Side A	52d	01/01/24	12/03/24
Side C	57d	01/01/24	19/03/24
Beampipe Removal	10.5d	20/03/24	03/04/24
Side A	1d	20/03/24	20/03/24
Side C (removal side)	10.5d	20/03/24	03/04/24
IBL Removal	9d	03/04/24	16/04/24
Side A	2.5d	03/04/24	05/04/24
Side C (removal side)	9d	03/04/24	16/04/24
Pixel Removal	34.5d	16/04/24	03/06/24
Initial Services Removal	20.5d	16/04/24	14/05/24
Side A	20.5d	16/04/24	14/05/24
Side C	20.5d	16/04/24	14/05/24
Pixel Detector Removal	14d	15/05/24	03/06/24
Side A	3d	15/05/24	17/05/24
Side C (removal side)	14d	15/05/24	03/06/24
Endcap Removal	33d	04/06/24	18/07/24
Side A (removal side)	30d	04/06/24	15/07/24
Side C (removal side)	33d	04/06/24	18/07/24
Barrel Removal	23.4d	19/07/24	21/08/24
Side C	7.4d	19/07/24	30/07/24
Side A (removal side)	16d	30/07/24	21/08/24
Remaining Services Removal From Cryostat Face	12d	21/08/24	06/09/24
Side A	12d	21/08/24	06/09/24
Side C	12d	21/08/24	06/09/24
Remaining Services Removal From Cryostat Bore	14d	06/09/24	26/09/24
Side A	14d	06/09/24	26/09/24
Side C	14d	06/09/24	26/09/24

Figure 18.3: High level schedule for decommissioning during LS3.

pared to the so-called Run 2 FLUKA[3] model of the Inner Detector. In most cases, the ratio of radiation calculated to radiation measured was within a factor of two from unity, validating the material and physical model. The ratio was slightly low (more radiation than simulated) for zones near the Pixel and ID services area.

The FLUKA models used for Figure 18.4 did not include the full set of services at high Z and low radius areas of the Inner Detector. Consequently, approximately 1.5 t of material have been added to the models. This material was calculated from existing models that had been made for Liquid Argon Calorimeter radiation studies, and then extrapolated to the size and shape of the routed service area. In addition, an estimation was made for the missing services in the Pixel-specific volume by scaling from existing masses and densities. An average density has been calculated for each side, and the material has been added as radial symmetric disks with varying thickness. This addition brings a 20% increase of simulated radiation dose in previously underestimated regions near the barrel calorimeter / ID endplate region. The final simulations are therefore well within a factor of 2 for all measured values.

Another large part of the increased accuracy of the new FLUKA simulations comes from the use of a new simulation method. Previous simulations considered the various detector elements individually during decay, with the surrounding volume set to vacuum. The re-

[3] http://www.fluka.org/

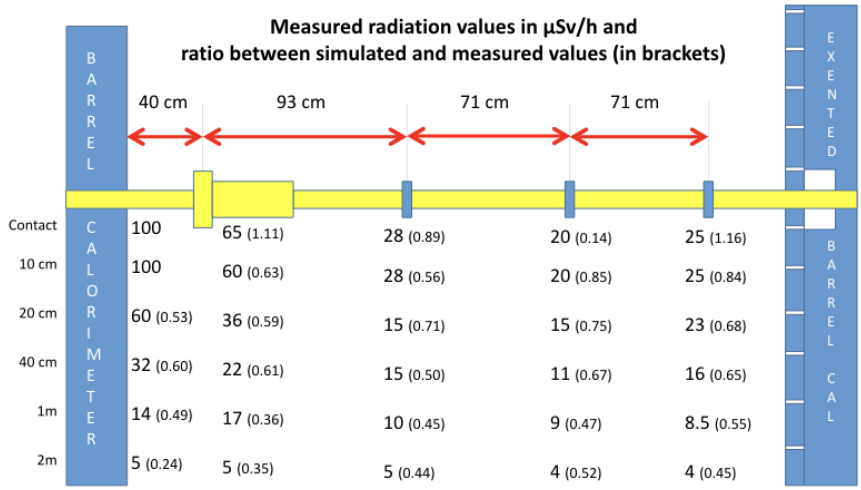


Figure 18.4: Comparison between simulated and measured radiation values for the region between the ID Endplate (left) and the End-cap Calorimeter (right) during a standard opening scenario in the EYETS 2016/17. The measured values (given in μSv/h) have been taken after 51 days of cool-down on 15.12.2016. The ratio of simulated over measured values is given in brackets.

sidual dose was then calculated from the distance of each detector element in the various opening scenarios. This method neglects any self-shielding effects from these detector parts or from material in between them. The new method (SESAME) [EDMS 1520812] now simulates the prompt radiation in the closed geometry and stores the nuclides produced into a file. The detector parts are then moved into the open geometry, and the decay is calculated after the displacement of the nuclide produced, that follow the regions they belong to. Therefore the material between the decaying nuclei and the accessible area is accounted for correctly.

It should be mentioned that the present simulations give reliable values at some distance from the source of the radiation. For the FLUKA model, materials are often smeared into an average composition with an average density distributed with radial symmetry around the beam axis. In close proximity, the actual radiation can therefore be higher given specific local material composition. We plan to have a dedicated measuring campaign, together with the CERN Radio Protection group (RP), at the beginning of LS2 along the ID cover plate and, if possible, with the ID cover plate removed and the services accessible. Any hot spots found will be documented, marked and addressed in the dose optimisation procedures described below.

18.3.2 Radiation Simulations prepared for LS3

With the updated FLUKA model and the new SESAME method, the following simulations have been calculated by RP, covering the essential steps for the decommissioning:

- Large Opening work environment at the beginning of the decommissioning
- Extended Standard Opening environment at begin of decommissioning
- Radiation activation levels along the services on the ID end plate
- Work environment with IBL/VI removed
- Work environment with Pixel services removed
- Work environment with Pixel Detector removed
- Work environment with one end-cap SCT/TRT removed
- Work environment inside cryostat with services in place
- Radiation activation levels of IBL/Pixel/SCT&TRT in stand-alone geometry on surface, and in storage after several years

All new simulations concentrate on ID surroundings instead of the full detector, giving higher precision in the anticipated work environment. These simulations will be used to estimate the expected dose for each decommissioning step, and are the basis of all optimisation and training efforts foreseen to take place on the mock-ups.

We present here two example results: In Figure 18.5, we see the boundary lines between different radiation levels two weeks before the start of decommissioning, with the inner beam pipe still inside the ID. Most of the working platform on the Minivans is in the 0.5–3 μSv/h range. In the area near the scaffolding around the ID face we reach the limit for a supervised area of 3–10 μSv/h but only within one meter of the end of the beam pipe we reach the limit for a simple controlled radiation area of more than 10 μSv/h. Figure 18.6 shows the simulated radiation levels after 224 days of cool down, during the removal of the services inside the cryostat bore. In this scenario, the beam pipe, IBL, Pixel, and the ID end-cap are already removed. As one can see, most of the working area will be in the 1–5 μSv/h range, with the exception of the area close to the ID barrel centre.

18.3.3 Radioactive Waste Management

The expected quantity of radioactive waste needs to be declared to RP well in advance, since during LS3 RP will need to deal with material from all over CERN for storage/disposal. With the help of simulations of the radiation activation levels along the services on the ID end plate mentioned earlier, it is possible to define a Radius R_{Rad0} on the ID face that will separate the potential radioactive waste from the conventional waste (see Figure 18.7). To simplify the separation, the radius will be considered as common for all service (cables, pipes, etc.) and will be based on the most activated services. All services inside R_{Rad0} will be treated as radioactive waste. The possible reuse of the detector parts from inside the cryostat volume is taken into consideration if a temporary storage area is found and a final

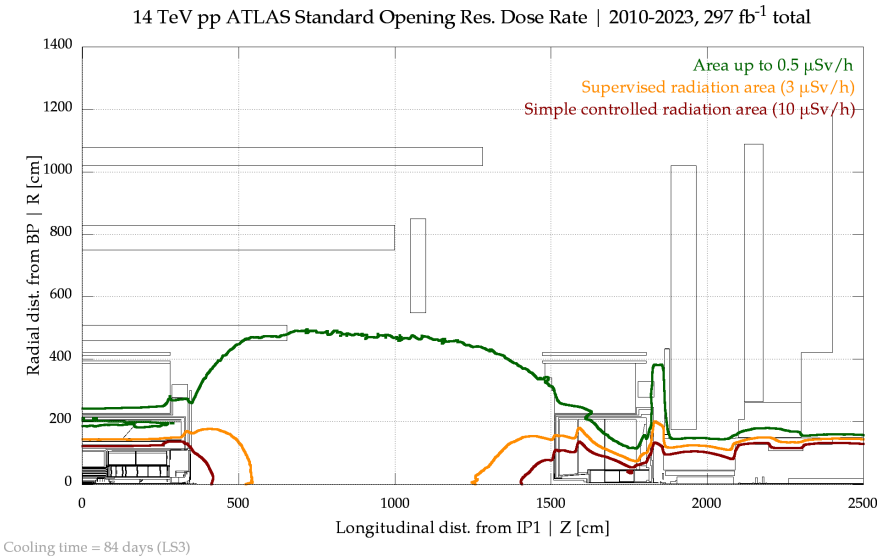


Figure 18.5: Radiation simulations for the large opening scenario, after 84 days of cool down, showing the boundary of different radiation classification zones 2 weeks before the start of decommissioning.

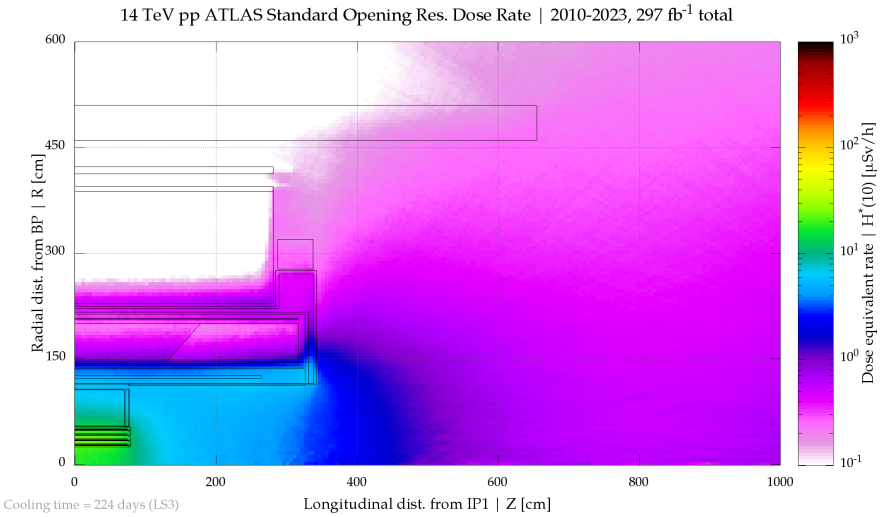


Figure 18.6: Simulated radiation levels after 224 days of cool down with the SCT/TRT End-cap removed. The ID barrel is still in place.

destination (museum or exhibition) is defined at the time of the removal. Otherwise, these components will be considered as radioactive waste. It is foreseen to validate these simulations with measurements at the beginning of the LS2 during the proposed removal of the ID End Plate cover. The final radius will be defined at the beginning of decommissioning by direct measurements from RP. With the currently assumed R_{Rad0} of 2–3 m, it is estimated that 2,000 kg (approximately 10 m^3) of services will be handed over to RP for disposal (excluding the detector parts).

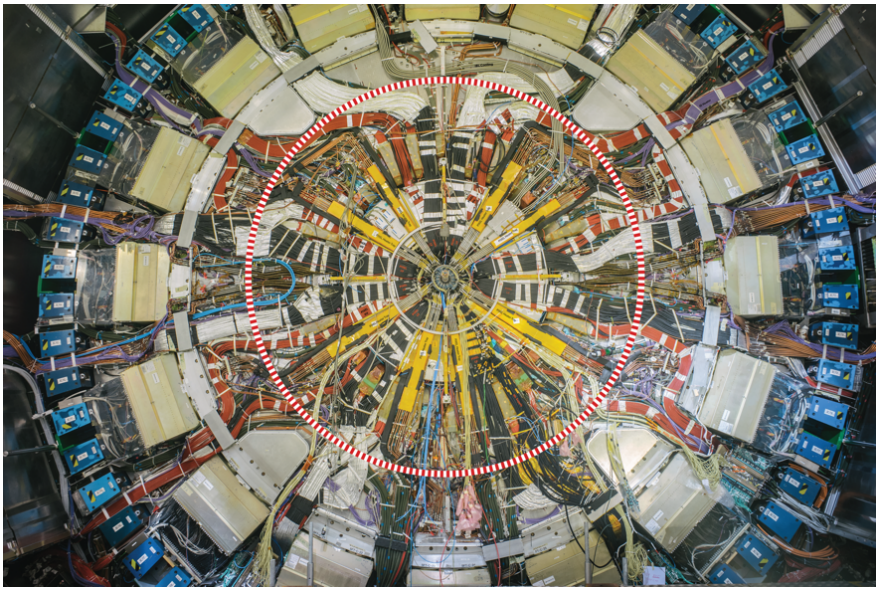


Figure 18.7: The Inner Detector Endplate with the services visible. The red circle symbolises the expected boundary condition between conventional waste (outer radius) and radioactive waste (inner radius). The precise radius will be adjusted by RP measurements during the beginning of decommissioning.

It is foreseen to cut all services at R_{Rad0} at the beginning of decommissioning. This allows the quick removal of a cable or pipe, as soon as it gets cut/disconnected at the detector side, and also allows the easy separation of the waste into different containers. Samples from cables at the extremity disconnected/cut from the detector will be collected for waste characterisation and sent to the radioactive waste section of the RP group.

Following the guidelines of RP radioactive waste handling, the cables will be delivered to RP in 1 m segments, separated into different types of cables according to their composition (power cables, multi wire cables, fibre optics, . . .) and without connectors.

18.3.4 ALARA Considerations

Following the general guidelines of the ALARA[4] principle, special care has to be taken to minimise the individual and collective dose for the entire decommissioning team over the full period of work. According to CERNs ALARA rule applied to inventions at CERN, the limits separating the different classifications are :

Individual dose equiv.	Level 1	100 μSv	Level 2	1 mSv	Level 3
Collective dose equiv.		500 μSv		**5 mSv**	
Ambient dose equivalent rate	Level 1	50 μSv/h	Level 2	2 mSv/h	Level 3
Airborne activity in CA		5 CA		200 CA	
Surface contamination in CS		10 CS		100 CS	

Where the exposure to Surface Contamination (CS) of 1 CS is equivalent to 0.5 mSv effective dose per year and the exposure to Atmospheric Contamination (CA) of 1 CA is equivalent to an internal exposure of 10 μSv/h. Since airborne activity (and most likely also contamination) can be ruled out during the work, the ALARA level classification will be mainly determined by individual and collective dose. As seen from the above table, the decommissioning work should be situated at the boundary between ALARA Level 1 and Level 2 from the ambient dose. However, early dose estimations for LS3 (based on experience gained in LS1) show that the collective dose for all persons involved during the whole 6 months work could approach the Level 3 threshold of 5 mSv. In the Level 3 scenario, the dose planning and work optimisation is reviewed by the ALARA committee, who will make further recommendations for optimisation. The relevant discussions with RP have already begun.

18.4 Training and Optimisation

18.4.1 Upgrade to the ATLAS Mockups

Currently we have two mockups available that will be used for decommissioning, one based on the original ID service mockup, and one on the existing IBL installation mockup. In addition, we have a spare Inner Warm Vessel (IWV) available, an exact copy of the currently installed Liquid Argon (LAr) IWV. The current state of these mockups is shown in Figure 18.8. During the next 1-2 years, the mock-ups will be significantly upgraded and expanded.

The ID service mockup will be used to simulate the decommissioning processes on the cryostat face, at the cryostat chamfer, inside the bore of the cryostat, and at the SCT-TRT Barrel. This mockup will include:

[4] As Low As Reasonable Achievable

- Printing of a high-resolution full size (1:1) photo of the current ID endplate services for lamination on the mockup
- Electrical and cooling services (each 3.5 m long, four sets for iteration of cutting operations) for one quadrant of the cryostat face
- Mockup patch panels for SCT and TRT services
- Mockup SCT/TRT barrel face
- Mockup flex tapes for the barrel ID services
- Mockup shielding and tooling
- Cutters/tools/and other equipment for services removal

The existing IBL installation mockup will be extended to simulate the full radius of the cryostat bore (location of all Pixel patch panels) and the Pixel service disconnection. It will include:

- Printing of a real size (1:1) high-resolution photo of the current Inner ID endplate services for lamination on the mockup
- Electrical and cooling services (2 m lengths, and four sets for iteration of cutting operations) for one quadrant of the Pixel nose
- Mockup patch panels for Pixel services (with one octant of connectors)
- Mockup Pixel heater trays
- Mockup shielding and tooling
- Cutters/tools/and other equipment for services removal
- The spare IWV will be used to validate some aspects of the SCT/TRT end-cap and barrel extraction as well as testing various shielding for their usability inside the bore.

It has been assumed that a significant number of cables for the mockup will need to be re-ordered, as some types are no longer available or are potentially needed for ITk. In addition, several sets of cables (as noted above) have been assumed in order to allow for iteration in the fine tuning of cutting and disconnection operations.

The planned work in 2018-2019 includes at least one simplified process validation on the 1/4 and/or IBL mockups. It is clear that this optimisation process, including ALARA documentation and dose minimisation, will need to continue throughout the following years. A final validation campaign is foreseen approximately two years before the start of the LS3 (2021-2022). This work will focus on the availability of all required tools and supports as defined in the procedures written so far. During the last year before LS3, it will be necessary to train the selected technicians directly on the mockups. This work would probably focus

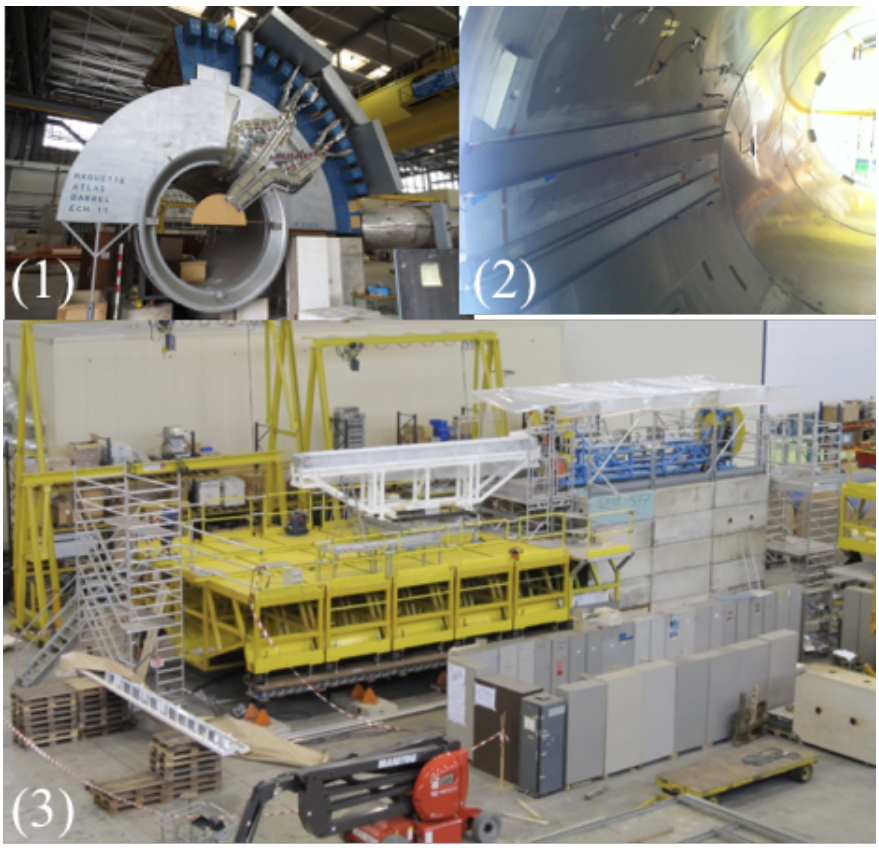


Figure 18.8: Pictures of the existing mockups as they are today. (1) ID service mockup, (2) spare Inner Warm Vessel, (3) IBL installation mockup. The planned improvements to each mockup are described in the text.

on the IBL mockup (IBL and beampipe removal, Pixel removal) and the IWV mock-up (removal of the SCT/TRT barrel and End-caps). For this final training, a realistic environment simulating the access constrains inside the toroid region (as it exists already today on the IBL mockup) will be needed. If possible, the mockups should be kept in a state where we can validate procedures to cope with unexpected problems that may occur during the ongoing decommissioning work in 2024.

18.4.2 Dose Optimisation

Calculating the dose from the average position of a person, the number of persons and the duration of a task is known to lead to significantly overestimating the dose. Experience on the Pixel extraction during LS1 showed that the measured collective dose was approximately four times lower than the predicted one (350 μSv instead of 1.5 mSv). This is caused

largely by the rough estimation of time and position that each person spends in the radioactive environment. In absence of a detailed workflow and position for each individual person, a worst case scenario has to be applied both for the duration of each task and the position of each person. To get a more realistic estimation of the actual exposure of each person, it is envisaged to establish a dose-prediction system to use on the mockups, based on video surveillance. This system employs several motion detection sensors linked to a computer acquisition system, and is based on algorithms already largely developed by the CERN media lab. In combination with the radiation maps from the simulation, this system would allow to optimise the individual and collective dose. Different type of shielding can be simulated to judge their effectiveness, and the position of people in respect to different radiation sources can be optimised. It is also foreseen to use the mockup to test various tools to remove the services as efficiently as possible (e.g. different types of electro-hydraulic cable cutters, as used by EN-EL in similar tasks).

The optimisation will continue even during the actual decommissioning. Given that the source of the radiation will not be evenly distributed, as described in the FLUKA model, but will rather be concentrated in specific parts of the services (e.g. connectors), it is planned to mark these hot spots clearly (e.g. by spray paint) during a dedicated measuring campaign with RP as soon as the ID End Plate cover has been removed. The development of live radiation monitoring systems (e.g. gamma cameras) will be closely followed during the coming years and their potential usage for the decommissioning phase will be evaluated. Training and procedures will be adapted according to any new findings to further reduce the exposure of personal.

18.4.3 Proposed Shielding

The new RP simulations described in Section 18.3.2 suggest that local shielding could be useful in order to reduce dose from lower radius materials (i.e. Pixel, IBL, beam pipe, and associated services below radius of 0.6 m). As a possible shielding concept, a set of shielding half-disks are proposed, of diameter approximately 1.2 m, which can be placed in front of the ID during operations on the cryostat face. The two disks, covering slightly more than 180° each, could be mounted on a common support such that they are independently rotatable, and can cover either the whole face of the ID (when no work is required in the inner radii) or expose the necessary segment (0–170°) while still providing coverage on the rest of the area. After the removal of the outer services and subsequently the removal of the SCT/TRT End-cap, these disks could either be remounted on the ID rails inside the bore during operations within the cryostat, or they could be replaced with a second set of shielding disks, depending on the final design. It is assumed that two sets of shielding will be necessary, one for A and one for C side, as the current schedule requires working on both sides of the ID in order to complete decommissioning within the time window allowed. Depending on the available access paths during shielding installations, the shielding might need to be assembled in situ near the ID endplate.

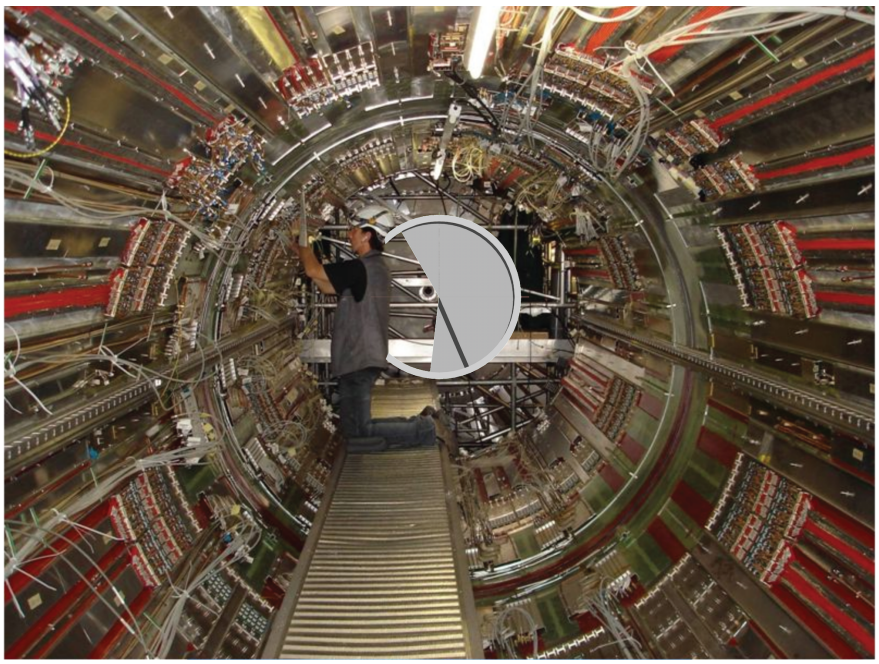


Figure 18.9: The bore of the Solenoid vacuum vessel during installation, with a sketch of a possible shielding disk (consisting of two half disks) superimposed. The disks can be rotated to either allow work in a segment up to 180°, or to cover the whole area for maximum protection.

The exact material and total weight of the shielding elements will depend on the reduction factor needed and can only be defined after a more detailed analysis. A rough first estimation, however, shows that a shielding disk of 1.2 m diameter that provides a reduction factor of 5 for 1.25 MeV gamma radiation (e.g. lowering the dose from 10 μSv/h to 2 μSv/h) would require 6.9 cm of steel or 3.4 cm of lead. Therefore the shielding could consist of two half-disks of around 220 kg (Pb) to 310 kg (Fe) each.

The second area identified for potential shielding is the face of the End-cap calorimeter, located at roughly 15 m on the beam axis (see Figure 18.5). While this area is far from the actual decommissioning work, it is the only area reachable by the main crane. Therefore the radiation could be an issue during transport of detector components, transport tools, etc. In this case a simple flat shielding wall could be placed against the face of the calorimeter to further reduce the dose during any material handling in this area.

18.4.4 Conclusion

During the last year, discussions with experts from all groups involved in the decommissioning have started, ranging from detector mechanics to radiation waste management. New FLUKA simulations for the different extraction steps are now available, based on

an improved detector model and simulation method. The requirements for adapting the existing detector mock-ups have been defined, and will be implemented in 2018. These mock-ups will be used for a more accurate dose estimation and dose optimisation in the coming years. A step-by step analysis of the decommissioning work (both in CAD and on the mock-ups) will show the effectiveness of different tools and procedures. A first concept for shielding has been presented. Lastly, a baseline extraction sequence has been defined which is compatible with the overall LS3 schedule.

19 Production Model and Schedule

19.1 Introduction

In this chapter, the production of the ITk Pixel Detector is described. Particular emphasis is given to the module construction and stave and ring loading that consume significant financial and human resources. The production of the Pixel Detector is a complex logistical process that is geographically distributed between multiple ITk institutes and several industrial partners and will take several years to complete. After an introduction to the Pixel production process, the ITk schedule and the Pixels part in it, are described.

The ITk Pixel Detector is considerably larger than the current ATLAS Pixel Detector. The total silicon area has increased from 2.1 m^2 to more than 12 m^2, the number of pixel modules has increased from 2,024 to more than 10,000 and the number of channels has increased by over two orders of magnitude. The production model used for the production of the current Pixel Detector would not scale to the greater demands of the ITk. The required rates of component production and the loading of modules to local supports need to be streamlined and carefully managed to make good use of the numerous available resources. In many cases, multiple vendors are required to ensure sufficient throughput of specialised components and processes during the construction phase. Significant experience will be gained during a period of component pre-production that will be the same as the main production that follows one year later. During this period, procedures will be exercised and the process streamlined. Multiple vendors will be used for the production of silicon sensors. Multiple vendors for the hybridisation phase are also mandatory to guarantee the production flow required to complete on time. In calculating the numbers of components required for the combination of the limited-scale pre-production and bulk component production, we have used a component yield model which uses a combination of experiences gained in the production of the existing Pixel Detector, yields measured in ITk prototyping and assumptions about yields that can be achieved when fabricating the finer pitch modules required for ITk. The most important technical considerations driving the calculation of the yield were illustrated in Chapters 7 and 8. The estimated cumulative yield for modules, taking into account losses in all the production phases, varies between 65% and 73% depending on technology, sensor thickness and module size. The losses at each stage are propagated through the different stages of production to calculate the number of purchased components taking into account break points in bulk purchases and the need to be able to terminate contracts in the case of failure to meet agreed quality control requirements.

The techniques used to construct the pixel modules are based on the experience gained in the construction of the existing Pixel Detector, including the Insertable B-Layer (IBL). Bare modules (without flex) consisting of a sensor bump-bonded to a Front End chip will be shipped from vendors performing the hybridisation to module assembly centres, where the module flex will be added. Assembled modules will be tested and shipped to local-support loading centres. To meet the required production rates, we will commission approximately 15 module production and testing sites. It is likely that the individual module production sites will be required to be able to fabricate and test multiple "flavours" of module, and particular attention will be devoted to the optimization of the assembly and test procedures with the aim of reducing as much as possible the differences.

The techniques used for the loading of the modules on to the local supports will also be based on previous experience. This loading will take place at 5 loading sites for the Outer Barrel, 3 loading sites for the end-caps and 1 loading site for the Inner System.

A critical aspect of this complex production will be the assessment of the quality over all the assembly steps. The ITk-wide approach to Quality Assurance (QA) and Quality Control (QC) was set in the ITk Strip Detector TDR and is described in its Section 14.1 [1]. QA tests are carried out during the development and pre-production phases and on a batch basis during production. The aim of QA test is to guarantee that all the produced parts are compliant with the specifications and that the quality is not affected by variations or problems in the fabrication procedures. QC tests are performed on all production items, to ensure full functionality. Both QA and QC of the different detector components are described in the technical chapters. The results of all the QA and QC tests will be logged in the ITk production database throughout the pre-production and production periods. Automated analysis procedures will be implemented to monitor production rates, quality and uniformity across the production sites. This analysis will help in identifying bottlenecks in the production flow, quality variations, consistency with the programmed production schedule. The ITk production database was described in Section 13.5 of the Strip TDR.

19.1.1 Work Breakdown Structure

The Work Breakdown Structure (WBS) for the ITk Pixel Detector is shown in Table 19.1. It defines the deliverables at Level 4 (e.g. 2.1.1.1 for Planar Sensors). The most important milestones and ATLAS reviews during the development, pre-production and production phases are listed in Table 19.2. The ATLAS reviews procedure, followed by the ITk, was presented in Chapter 23 of the Strip TDR on Project Management. Each major system component must undergo a Specification Review at the beginning of the design, a Preliminary Design Review (PDR) before the fabrication of the first large scale prototype, a Final Design Review (FDR) before the beginning of the pre-production and a Production Readiness Review (PRR) before the beginning of the production.

Table 19.1: Work Breakdown Structure (WBS) for the ITk Pixel Detector

2.1	**Pixel Detector WBS**	
2.1.1	Pixel Sensors	
	2.1.1.1	Pixel Planar Sensors
	2.1.1.2	Pixel 3D sensors
	2.1.1.x	CMOS sensors
2.1.2	Pixel ASICS	
	2.1.2.1	Front-end read-out chip
	2.1.2.2	Data concentrator chip
	2.1.2.3	PSPP chip and peripherals
	2.1.2.4	DCS Controller Chip and peripherals
	2.1.2.5	Opto Amplifier AISC (i.e. GBT-TIA)
	2.1.2.6	VECSEL driver
2.1.3	Hybridisation and module assembly	
	2.1.3.1	Bare module hybridisation
	2.1.3.2	Module flex
	2.1.3.3	Module assembly
	2.1.3.4	Module testing
	2.1.3.5	Test beams
2.1.4	Services	
	2.1.4.1	On stave/ring cables (Type-0)
	2.1.4.2	Patch Panel 0 (PP0)
	2.1.4.3	Type-I Services
	2.1.4.4	Patch Panel 1 (PP1)
	2.1.4.5	Optical drivers/receivers
	2.1.4.6	Optical patch panel
	2.1.4.7	Optical fibres
	2.1.4.8	Type-II Services
	2.1.4.9	Patch Panel 2 (PP2)
	2.1.4.10	Type-III Services
2.1.5	Local Supports	
	2.1.5.1	Local Support cooling line
	2.1.5.2	Local support Mechanical Structure
	2.1.5.3	Module loading on local supports
2.1.6	Global Mechanics and installation tooling	
	2.1.6.1	Inner layers Support Tube (IST) – Insertion system
	2.1.6.2	Outer Barrel mechanical structure – Support points
	2.1.6.3	Inner Barrel mechanical structure and insertion tooling
	2.1.6.4	Outer End-cap structures
2.1.7	Integration and system test	
	2.1.7.1	Integration of Inner Replaceable Layers
	2.1.7.2	Integration of Barrel Outer Layers
	2.1.7.3	Integration of End-cap rings to Cylinders
	2.1.7.4	Integration of End-caps to Barrel
	2.1.7.5	Integration of Inner Layers to End-caps and Outer Layers
	2.1.7.6	Barrel local support system testing
	2.1.7.7	Inner local support system testing
	2.1.7.8	End-cap local support system testing
	2.1.7.9	12.5% or slice system test in SR1
	2.1.7.10	DAQ for test setups
2.1.8	Off-detector electronics	
	2.1.8.1	LV (Modules – Opto)
	2.1.8.2	HV
	2.1.8.3	DCS
2.1.9	Support	
	2.1.9.1	DAQ test setups Hardware
	2.1.9.2	Test beam
	2.1.9.3	Irradiation

Table 19.2: Main review dates for the ITk Pixel Detector

Major Pixel reviews associated with production				
WBS	What	PDR	FDR	PRR
2.1.1	Planar Sensor	Q2 18	Q1 19	Q2 20
	3D sensor	Q2 18	Q1 19	Q2 20
2.1.2	FE chip	Q1 18	Q4 18	Q4 19
	Data concentrator	Q4 18	Q4 19	Q4 20
	PSPP chip	Q2 18	Q4 18	Q4 19
	DCS controller chip	Q2 18	Q1 19	Q3 20
2.1.3	Module Hybridization	Q2 18	Q1 19	Q3 20
	Modules Assembly	Q2 18	Q2 19	Q4 20
2.1.4	Services	Q3 18	Q4 18	Q3 19
2.1.5	Local Support	Q3 18	Q2 19	Q4 19
2.1.6	Global Mechanics	Q3 18	Q2 19	Q2 20
2.1.7	Integration	Q3 19	Q3 20	

19.1.2 Production Responsibilities Flow

During the production phase, the ITk Pixel Detector project will appoint a Production Logistics Coordinator to track and manage the overall flow of parts to ensure optimal production rates and quality.

One cluster of institutes will be responsible for the assembly and integration of the outer barrel, two clusters of institutes will be responsible for the assembly and integration of the two outer end-caps and one cluster will be responsible for the assembly and integration of the inner system. When complete, the four parts of the Pixel Detector will be delivered, ready for integration into the ITk in the surface building at the ATLAS pit at CERN. The work will be locally coordinated by a Cluster Production Manager and centrally by the Production Logistics Coordinator. Reporting to the ITk Pixel Project leader will happen in regular production meetings.

Each cluster will receive parts from collaborating institutes and industrial partners and will load modules and services on to the local support mechanics (staves and rings). Within each cluster, the loading of the local supports may be shared between several participating institutes. Having more than one institute helps to reach and maintain the production rate required to meet the production milestones. In order to benefit from the expertise established across the entire ITk Pixel community and to optimise development time and resources, the loading, Quality Assurance and Quality Control procedures and tools will be the same at all participating clusters. Institutes participating in the construction process will be required to satisfy a production-qualification process which is a demonstration of

capabilities, equipment and quality-control techniques including the use of the production database.

19.2 Global Production Plan

The production phase ends with the delivery of fully assembled and tested staves and rings for the final integration of the four main Pixel deliverables (the outer barrel, the two outer end-caps and the inner system).

The bulk production of three distinct types of components will run in parallel:

- Module Production.
- Construction of the local supports (staves and rings).
- Services for the Local Support (Type-0).

The production of the components that are not directly mounted on the local supports, but needed for integration, will also be launched at the same time as module construction. These include: Type-I and Type-II cables, cooling tubes, data transmission lines and HV and LV power supplies and cables.

The module production will require the assembly of several components that will be delivered by industry. These include: sensors, front-end chip ASICs, inter-connection of sensors and front-end chips (to produce bare modules) and module flexes. The coupling, which will involve the gluing and wire-bonding of bare modules to module flexes to form assembled modules, will be performed in-house at module assembly sites. No industrialisation is currently foreseen of this part of the process.

The local support mechanical structures will be made from carbon fibre composite material sourced through qualified vendors. Carbon foam and titanium tube for cooling will be preformed for fabrication into local supports at participating institutes. Mechanical structures will be shipped to local-support loading sites, where they will loaded with modules and Type-0 services (unless already embedded in the local supports as for the outer end-cap half-rings).

Type-0 services will also involve several components, most of which will be produced in industry: cables for data transmission, DCS and power supplies providing low and high voltages to the modules.

The module production or assembly flow is outlined below:

- Sensors: Planar and 3D sensors will be fabricated by industrial partners who will have been qualified prior to pre-production. A sub-set of sensors will be probed prior to being connected to the front-end chips. In the case of standard high-resistivity planar

sensors, the purchase contracts will be placed through CERN following a market survey. The market survey was launched in Q4 2017. The contracts for the 3D sensors will be placed by local contacts in participating countries.

- Front-end chips: All wafers will be probed using semi-automatic wafer probe stations as part of the reception process. The purchase of the FE chips will take place through CERN using established frame contracts with the CMOS foundry.
- Bump-bonding: Sensors and front-end chips will be shipped to bump-bonding vendors to produce bare modules. Testing of bare modules prior to assembly with module flexes can be considered if possible defects identified in this phase can be be repaired in a cost effective way. Individual vendors will not be tied to specific sensor producers or module assembly sites, although, in some cases it is conceivable that such a direct link might be put in place to optimize the production flow and rate. The contracts for the bump-bonding will be negotiated through CERN. Market surveys for the bump bonding will be launched in Q1 2018.
- Flexes: Module flexes will be produced by commercial vendors and tested in-house at participating institutes. The contracts for these will be negotiated and managed through participating countries.
- Module assembly and testing: Bare modules and modules flexes will be shipped to module assembly sites. Module flexes will be glued and wire-bonded to bare modules (to the front-end chips) to produce fully assembled modules which will then be tested before shipping them on, in batches, to local support loading sites. As described in Chapter 8, several types of modules are required to populate the Pixel Detector.

Given the large number of modules to be assembled and the relatively short production time, the module production will have to be shared between many institutes in order to achieve the required rates. Based on previous experience and the need for more than 10,000 completed good modules to be assembled during a period of two and a half years, the required rate is 100 modules per week. However, two additional factors have to be taken onto account which will significantly affect the ability of the project to reach the required maximum sustained rate:

- A finite amount of time will be required to reach the maximum production rate and this needs to be taken into account when calculating the total number of modules available at a given time. It is foreseen that module production sites will be brought on stream in a way that minimises risk of loss of components. This is time consuming but necessary to control quality.
- Bump-bonding may represent a significant bottleneck for the production: it is a low volume industrial process and for this reason tends to be batched and the maximum capacity available is not continually exploited. Based on previous experience, delays in bump-bonding can occur for many reasons, so it would be prudent to anticipate needing that excess capacity. The current planning is based around our expectations

of the available resources and 200 modules per week (at peak performance) have been assumed.

The current module assembly model assumes the following:

- 10 Module Assembly clusters, with one or more sites taking care of assembly and QC.
- A time-averaged production rate of 20 modules/week/cluster.

Previous experiences have shown that the testing phase is the bottle-neck in the module assembly procedure. Some additional sites, dedicated to module testing and not performing assembly, will be put in place once the whole module assembly procedure is better understood. The module assembly production flow is shown in Figure 19.1 and the expected module production rates for the three sub-detectors are shown in Figure 19.2. Module loading sites will receive modules from module assembly sites, as well as Type-0 services and local-support mechanical structures from various production sites.

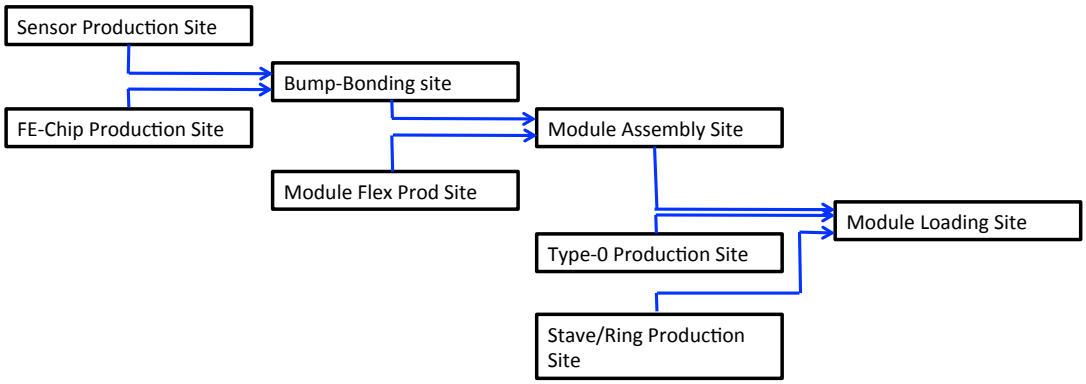


Figure 19.1: Module Assembly Production Flow.

Efforts are in progress to qualify five or six bump-bonding vendors. In addition to the investigations of the technical characteristics of the different processes, a significant effort will be made to verify the maximum production rate each vendor can achieve. The aim would be to select at least three vendors with a peak capacity of 20 modules/day each: this would ensure a large margin above that required to reach the required rate, hence a safe handling of fluctuations and possible problems at one vendor. At the same time, the possibility of using automatic flip-chip machines available at different institutes in the Pixel collaboration to alleviate the load on the industrial partners is being explored. Bump-bonding qualification is already on-going, using the previous generation of front-end chip (the FE-I4, used in the IBL) coupled to new sensors or dummy test structures. However, the final step of the qualification, including going to the smallest pixel pitch and to the full chip size, will only be possible at the beginning of the pre-production. Another aspect that can

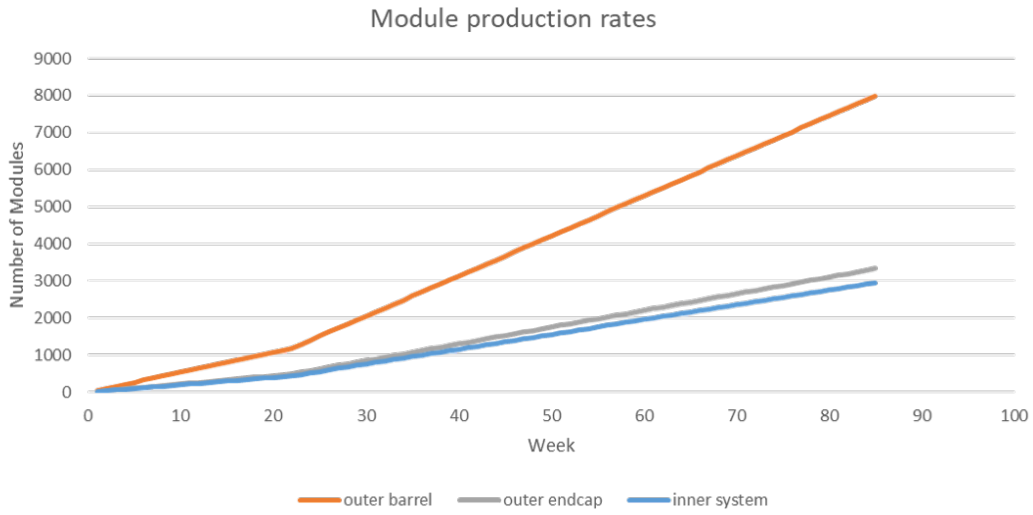


Figure 19.2: Expected module production rates for the three subsystems of the Pixel Detector.

have a significant input on the schedule is the decision process to select between alternative sensors and/or module inter-connection technologies.

One recent development, and active area of research, which could have a significant impact on the schedule is the use of monolithic CMOS. In this case, the simplification in module production and an important reduction of the load on the bump-bonding vendors may have a beneficial effect on the overall production schedule. On the other hand, the effect of postponing a decision on the technology may generate large delays elsewhere in the project. It is clear that the selection of the baseline technology to use in each layer of the detector cannot be postponed beyond the beginning of the pre-production phase to avoid interference with the tendering and procurement procedures. In particular, the decision on CMOS will not affect the development of standard planar hybrid modules up to the level required at the FDR. CMOS modules will only be considered for outer layer, while the remaining part of the detectors will be built with standard hybrid modules. Moreover, each alternative technical solution to be considered after the Pixel TDR must be compatible with the local-support thermal and mechanical specifications listed in Chapter 13. This mandates that the new technologies are a "drop-in" solution replacing the de-selected technology. In Q2 2018, before the submission of full size prototypes, the CMOS project will be reviewed. At this stage, together with the evaluation of the status of the monolithic chip design and of the compliance with the requirements (as usually done in a PRR), the overall impact on ITk and ATLAS will be evaluated. Possible benefits in terms of cost and production schedule will be analysed and a detailed risk analysis will be performed to spot possible negative impacts on the rest of the project. If the recommendation will be to continue the development of a monolithic CMOS solution for Layer-4, a fully functional CMOS module will be evaluated in a FDR in the second half of 2019 (on the same time-scale of the hybrid module FDR)

and a final decision on the selected technology for the outer layer will be taken before the beginning of the module pre-production to avoid perturbations in the sensor procurement process.

19.3 Module Loading on Local Supports

As introduced above, the assembly of fully equipped local supports includes the following:

- Modules: assembled modules will be provided by module assembly and testing sites. Functionality tests will have been performed on each module prior to loading on the local support.

- Supports: qualified supports will be provided to the loading sites by the sites producing and qualifying them. The qualification includes thermal and mechanical functionality as well as electrical functionality in case of embedded services in the supports as for the outer end-cap. A receival test must be foreseen before loading modules.

- Type-0 services: Type-0 services include cables and flexes for LV, HV, DCS, data and clock/command and will be provided by the various production sites or vendors. There will be different flavours of all services depending on the type of the local support.

The loading sites will be organised within each loading cluster. It is anticipated that the two outer end-caps will have at least one loading site each, the inner system will have a single loading site, while the outer barrel will require at least five loading sites (see Table 19.3).

Table 19.3: Organisation of loading sites.

Detector Subsystem	**Number of Loading Sites**
Outer End-cap 1	1
Outer End-cap 2	2
Outer Barrel	5
Inner System	1

The local supports, once fully assembled and tested, will be shipped to integration sites.

19.4 Production Schedule

In this section, the schedule of the ATLAS ITk Pixel system is discussed in the context of the global ITk schedule.

19.4.1 Overall Schedule

The ITk Tracking Detector construction schedule is based around the CERN Medium Term Plan (MTP) for the period 2016-2020. This was presented at the CERN Council session [168] in June 2015. The ITk will be installed during Long Shutdown 3 (LS3), which starts at the end of 2023, and is expected to last for 30 months with colliding beam operation expected to start in mid-2026. Figure 19.3 shows the high-level development of the pixel schedule.

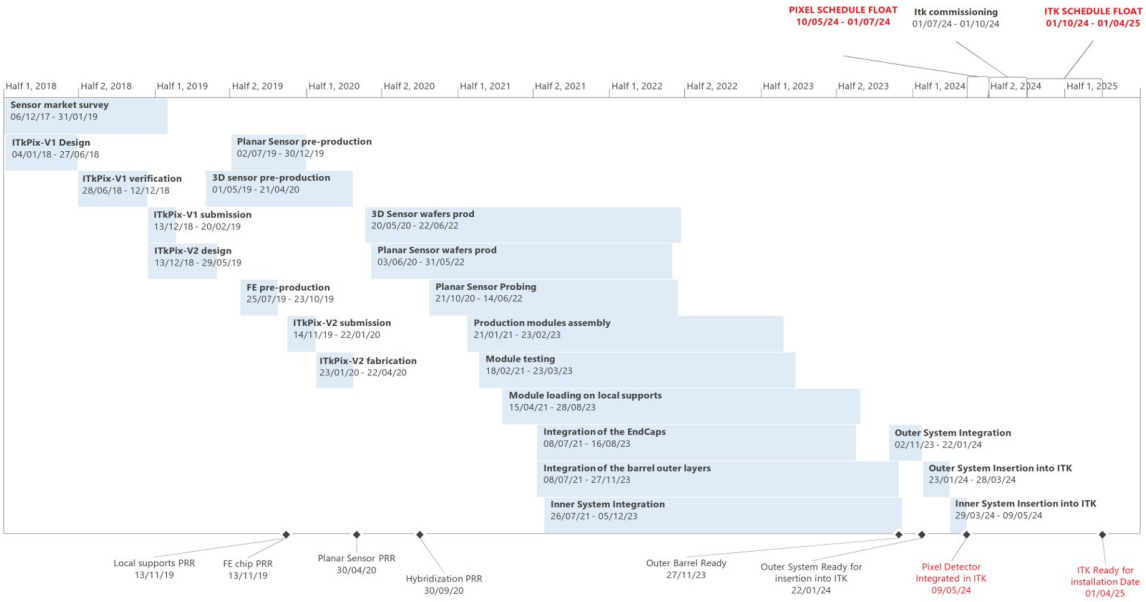


Figure 19.3: Top-level Pixel Detector production schedule.

19.4.2 Market Surveys, Pre-production and Production

Market Surveys have been launched with CERN procurement to identify potential suppliers for the major cost items that will be purchased through CERN. This will allow greater confidence in the accuracy of the prices for these items ahead of the preparation of the MoUs. It is also important to qualify the potential suppliers for the long lead-time components before the final tendering process. When preparing the specifications that are part of a market survey and tendering process for many of the components that will be purchased

for the ITk, the main difficulties are the requirements that relate to radiation hardness, which cannot be easily captured in commercial Quality Assurance procedures. This places the burden on the ITk for extensive preparatory R&D followed by demands on the vendors for written assurances that device processing is kept identical to that of pre-production devices built to final specifications which have been through the full radiation qualification process. A qualification phase of early procurement of enough devices designed to final specifications to demonstrate these requirements is essential given the timescales required for adequate irradiation and test beam studies. For the Semi-Conductor Tracker of the Inner Detector (SCT), there was a pre-production procurement of a small fraction of the final order with contractual break-points to allow the SCT collaboration to be able to withdraw from the purchase in case problems were encountered either in terms of radiation tolerance in sample testing, QA difficulties or delivery schedule issues. Another issue is that some sensor suppliers require separate early procurement of masks and polished wafers to mitigate cash-flow problems. Following previous procedures, after the TDR, the ITk will place contracts for a pre-production of 10% the total volume with pre-negotiated break points that enable the ITk community or its representatives to terminate the contracts if the parts do not meet the specifications. Pre-production modules also need to be built and tested to the final specifications including a series of irradiation tests. These components are used to: qualify the vendors production procedures, capabilities, ITk reception and Quality Assurance procedures, streamline the component flow between sites including part-tracking and to bring the production sites through site qualification to production readiness. Based on experience gained during the construction of the ID, it is expected that this process will be time consuming. A slow ramp up to full production is anticipated, taking care to guarantee the highest quality of the large number of mass produced parts. This will also be true for the ITk where a significant number of production sites are planned. The pre-production phase indicated on the schedule covers the pre-production phase after the TDR. Because this phase of the project is so critical it is likely that it will be necessary to collect funds for the qualification of vendors and to pay for the pre-production phase before all of the formal phases of the financial review are complete. This bridging between pre-production and production will require an interim Memoranda Of Understanding (iMOU).

19.4.3 Preparation for the Installation of the ITk

Before the installation of ITk Detector into the ATLAS experiment, the Inner Detector (ID) must be safely removed from the cryostat to the surface and handed over to the Radiation Protection group for consolidation, storage and eventual disposal. The schedule for the removal of the ID and installation of the ITk requires detailed planning with ATLAS Technical Coordination who must take account of the requirements of multiple sub-systems. Preparation is ongoing within the ID and ITk-Mechanics group to understand the details of the process, the required tooling and personnel and the associated timeline.

The ITk is scheduled to be available for installation in the ATLAS pit by Q2 2025 and de-

signed for rapid connection once installed in the ATLAS cryostat. The combined operation of installation and service connection is assumed to take no more than six months.

Furthermore, the ITk should be available for an extended period of commissioning on the surface at Point-1 nine months before it is required for installation. This requirement is based on the experience gained with the current tracking detector, with the intention to minimise exposure to radio activation during or after installation of the ITk and to minimise the time to full operation before physics data taking. By the time the ITk is fully integrated into the outer cylinder on the surface, all components will have been tested stand-alone as part of a sub-system. The integration of the ITk on the surface will be complete by June 2024 and this will be followed by 3 months of combined testing of up to one eighth of the final detector at any one time. Six months of float have been added at the end of this process.

WBS	Task Name	Duration	Start
2.1.2	**Pixel ASICS**	**1459 days?**	**Mon 09/01/17**
2.1.2.1	**Front-end readout chip**	**1443 days**	**Mon 09/01/17**
	RD53-A	**413 days**	**Mon 09/01/17**
	RD53-A design verification	168 days	Mon 09/01/17
	RD53-A submission	0 days	Thu 31/08/17
	RD53-A fabrication	65 days	Thu 31/08/17
	Chip level tests	45 days	Thu 30/11/17
	Irradiation assemblies preparation	25 days	Thu 01/02/18
	Irradiation assemblies test	25 days	Thu 08/03/18
	Chip irradiation	45 days	Thu 12/04/18
	Irradiated chip tests	40 days	Thu 14/06/18
	Fabrication of chips for modules	65 days	Thu 12/04/18
	ATLAS FE Chip	**1332 days**	**Tue 13/06/17**
	FE spec review	0 days	Tue 13/06/17
	FE spec review 2	0 days	Wed 28/02/18
	FE chip PDR	0 days	Fri 30/03/18
	ITkPix-V1 Design	125 days	Thu 04/01/18
	ITkPix-V1 verification	120 days	Thu 28/06/18
	FE chip FDR	0 days	Wed 12/12/18
	ITkPix-V1 submission	50 days	Thu 13/12/18
	ITkPix-V1 fabrication	65 days	Thu 21/02/19
	Chip level tests	45 days	Thu 23/05/19
	Irradiation assemblies preparation	25 days	Thu 23/05/19
	Chip irradiation	45 days	Thu 27/06/19
	Irradiated chip tests	20 days	Thu 29/08/19
	FE pre-production	65 days	Thu 25/07/19
	wafer probing	50 days	Thu 24/10/19
	ITkPix-V2 design	120 days	Thu 13/12/18
	FE V2 FDR (optional)	0 days	Wed 02/10/19
	ITkPix-V2 verification	120 days	Thu 30/05/19
	FE chip PRR	0 days	Wed 13/11/19
	ITkPix-V2 submission	50 days	Thu 14/11/19
	ITkPix-V2 fabrication	65 days	Thu 23/01/20
	Chip level tests	45 days	Thu 23/04/20
	Irradiation assemblies preparation	25 days	Thu 23/04/20
	Chip irradiation	45 days	Thu 28/05/20
	Irradiated chip tests	45 days	Thu 30/07/20
	Chip production - Wafers	65 days	Thu 30/07/20
	FE Probing	450 days	Thu 29/10/20
	FE production done	0 days	Wed 20/07/22

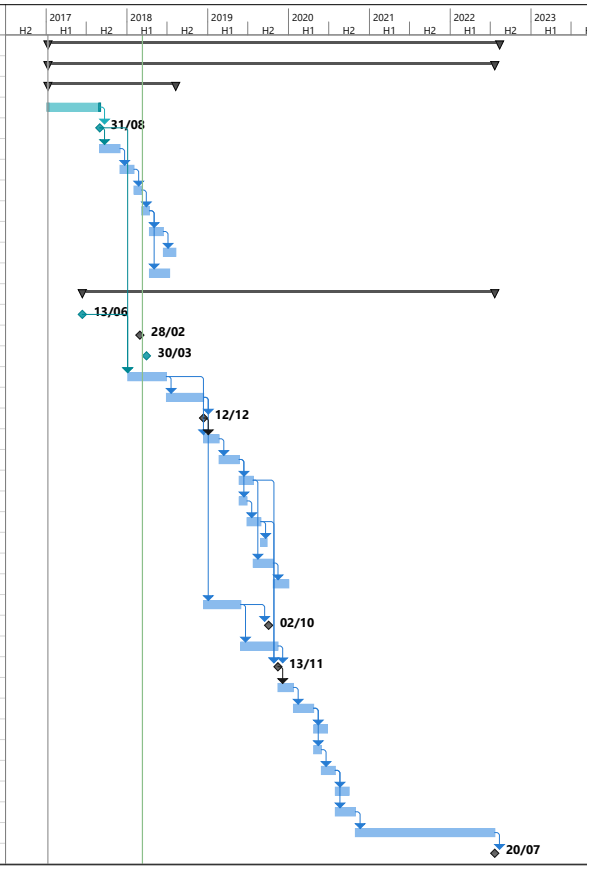


Figure 19.4: Pixel FE chip production schedule.

It is important to stress that any work carried out in the ATLAS Detector once it has been installed into the cryostat will be heavily constrained by the radiation environment in the cavern in general and the cryostat in particular. The removal of the Inner Detector, described in Chapter 18, is likely to be particularly difficult and the development of the required tooling

and training of manpower and procedures will take several years. The removal will be a partnership between the ID and ITk communities and ATLAS Technical Coordination.

WBS	Task Name	Duration	Start	Finish
2.1.1	Pixel Sensors	1368 days	Fri 31/03/17	Tue 28/06/22
	Sensor spec review	0 days	Fri 31/03/17	Fri 31/03/17
2.1.1.1	Pixel Planar Sensors	1337 days	Mon 01/05/17	Tue 14/06/22
	Production for RD53-A modules	120 days	Mon 01/05/17	Fri 13/10/17
	RD53-A modules evaluation	220 days	Thu 01/02/18	Wed 05/12/18
	Sensor market survey	302 days	Wed 06/12/17	Thu 31/01/19
	Market survey step 1	31 days	Wed 06/12/17	Wed 17/01/18
	Market survey step 2	80 days	Fri 09/02/18	Thu 31/05/18
	Planar Sensor PDR	0 days	Mon 30/04/18	Mon 30/04/18
	Market survey step 3	175 days	Fri 01/06/18	Thu 31/01/19
	Planar Sensor FDR	0 days	Fri 01/02/19	Fri 01/02/19
	Planar Sensor tender	20 days	Thu 28/02/19	Wed 27/03/19
	Planar Sensor pre-production order	0 days	Mon 01/07/19	Mon 01/07/19
	Planar Sensor pre-production	130 days	Tue 02/07/19	Mon 30/12/19
	Planar Sensor PRR	0 days	Thu 30/04/20	Thu 30/04/20
	Planar Sensor Order	0 days	Mon 01/06/20	Mon 01/06/20
	Planar Sensor wafers prod	520 days	Wed 03/06/20	Tue 31/05/22
	Planar Sensor Probing	430 days	Wed 21/10/20	Tue 14/06/22
2.1.1.2	3D sensors	1347 days	Mon 01/05/17	Tue 28/06/22
	Production for RD53-A modules	120 days	Mon 01/05/17	Fri 13/10/17
	RD53-A modules evaluation	220 days	Thu 01/02/18	Wed 05/12/18
	3D Sensor PDR	0 days	Mon 30/04/18	Mon 30/04/18
	3D Sensor FDR	0 days	Thu 31/01/19	Thu 31/01/19
	3D Sensor pre-production order	0 days	Wed 01/05/19	Wed 01/05/19
	3D sensor pre-production	255 days	Wed 01/05/19	Tue 21/04/20
	3D Sensor PRR	0 days	Wed 22/04/20	Wed 22/04/20
	3D Sensor order	0 days	Tue 19/05/20	Tue 19/05/20
	3D Sensor wafers prod	546 days	Wed 20/05/20	Wed 22/06/22
	3D Sensor Probing	450 days	Wed 07/10/20	Tue 28/06/22

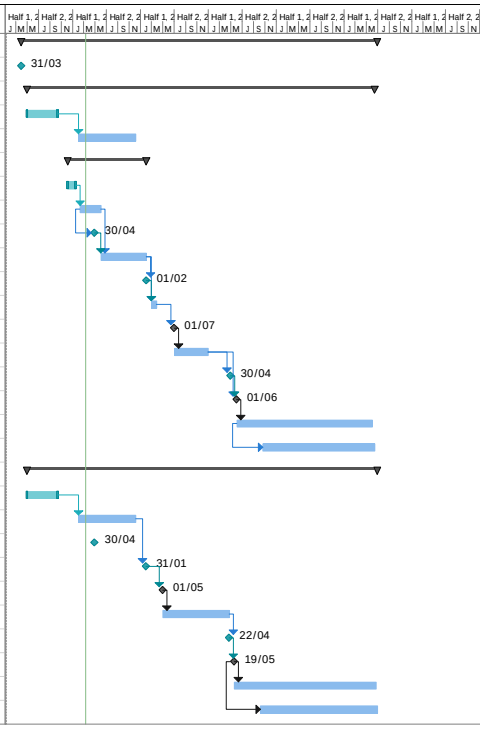


Figure 19.5: Sensor production schedule.

19.4.4 The ITk Pixel Detector Schedule

The design, development and qualification of the Pixel Front-end Chip is the key schedule driver in the years running up the start of module pre-production that starts in October 2019 and lasts for one year before launching bulk production in early 2021. The schedule (see Figure 19.4) assumes two iterations of the front-end chip design, module development and testing including irradiations. The RD53A chip was submitted in August 2017 and the first prototypes were available for the fabrication of modules in December 2017. The RD53A chip, described in Chapter 6, is not the final production chip but does support most of the functionality required in production. The design of the first complete ATLAS chip (ITkPix-V1) that is expected to meet all specifications starts in Q1 2018 and will be complete one year later. Based on experience gained in 2017, six months of comprehensive verification is foreseen ahead of the first submission at the start of 2019. The first chips should be available for testing in May 2019 and it would be possible to start the FE wafers pre-production in July 2019. However, based on previous experience, we have foreseen the need for a second iteration that includes five months of additional design and approx-

imately five additional months of verification. This would be followed by submission, in January 2020, performance evaluation and irradiation studies. The final production run of the ITkPix-V2 production wafers is scheduled for July 2020.

WBS	Task Name	Duration	Start
2.1.2	Pixel ASICS	1459 days?	Mon 09/01/17
2.1.2.2	Active Cable Components	1247 days	Wed 01/11/17
	Active cable chips (aggregator-driver and equalizer-receiver)	1217 days	Wed 01/11/17
	Prototype design	282 days	Wed 01/11/17
	PDR	0 days	Thu 29/11/18
	Prototype submission	50 days	Fri 30/11/18
	Prototype fabbrication	65 days	Fri 08/02/19
	Prototype testing	120 days	Fri 10/05/19
	FDR	0 days	Fri 25/10/19
	Pre-prod submission	50 days	Fri 25/10/19
	Pre-prod fabrication	65 days	Fri 03/01/20
	Pre-prod tests	120 days	Fri 03/04/20
	PRR	0 days	Fri 27/11/20
	Production chip submission	50 days	Fri 27/11/20
	Chip fabrication	65 days	Fri 05/02/21
	Active Cable Chips production done	0 days	Thu 06/05/21
	Wafer probing	300 days	Fri 07/05/21
	Active cable assembly	1075 days	Fri 29/06/18
	Active Cable Market Survey	0 days	Fri 25/10/19
	Passive/rad soft prototype	0 days	Fri 29/06/18
	Active prototype with ATLAS chips	0 days	Thu 02/04/20
	pre-production 6/20	100 days	Fri 03/04/20
	production 6/21	300 days	Fri 18/06/21
	Active Cable Production done	0 days	Thu 11/08/22
2.1.2.3	PSPP chip and peripherals	987 days?	Thu 05/10/17
2.1.2.4	DCS Controller Chip and peripherals	1025 days?	Mon 02/10/17

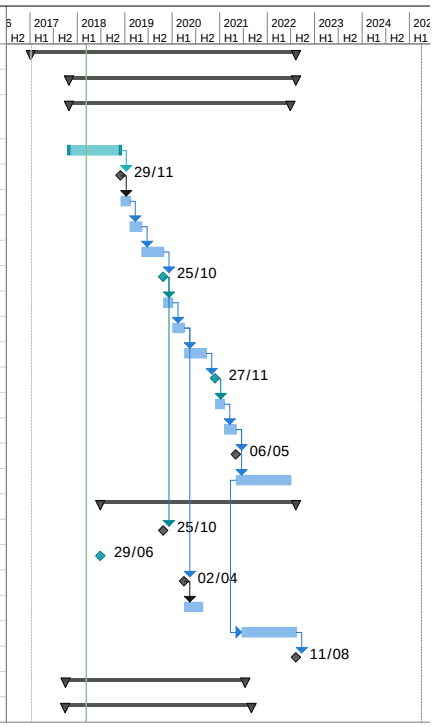


Figure 19.6: Data aggregator production schedule.

The schedule for the ITk Pixel high resistivity planar sensors is presented in Figure 19.5. The sensors will be ordered through CERN. A market survey was launched in Q4 2017 and is expected to be complete at the end of January 2019. Following the call for tender, it will be possible to place the orders for the pre-production sensors in July 2019. The bulk order for planar sensors would be launched in June 2020. It is anticipated that 3D sensors will be purchased from two or three vendors through representatives in the countries where they are produced. The pre-production orders will be placed in May 2019 and the production order one year later.

The data aggregator chip and equaliser receiver chips, which are not part of the module, but part of the testing, will be designed and prototyped by the end of 2018. A first submission is foreseen at the end of 2018, with the return and testing between February and May 2019. Pre-production orders will be placed in Q1 2020 and the bulk production order will be placed in Q1 2021. The PSPP chip and the Detector Controller System chip (DCS) follow similar timelines (see Figure 19.6).

The preparation required to establish module production starts with a market survey, launched through CERN for the contract to do the bump bonding. This will be launched in

WBS	Task Name	Duration	Start
2.1.3	Hybridization and module assembly	1506 days	Thu 15/06/17
2.1.3.1	Bare module hybridization	1410 days	Thu 15/06/17
	Hybridization spec review	0 days	Thu 15/06/17
	Bump-bonding RD53-A modules	250 days	Thu 01/02/18
	Hybridization market survey I	151 days	Mon 02/10/17
	Hybridization PDR	0 days	Fri 29/06/18
	Hybridization market survey II	194 days	Tue 01/05/18
	Hybridization FDR	0 days	Mon 28/01/19
	Hybridization tender	65 days	Mon 28/01/19
	Hybridization pre-production modules	240 days	Thu 24/10/19
	Hybridization PRR	0 days	Wed 30/09/20
	Hybridization production modules	500 days	Thu 10/12/20
2.1.3.2	Module Flex	424 days	Thu 01/08/19
	Frex Pre-production	2 mons	Thu 01/08/19
	Flex Production	6 mons	Wed 30/09/20
2.1.3.3	Module assembly	1486 days	Thu 15/06/17
	Module spec review	0 days	Thu 15/06/17
	RD53-A Module assembly and test	325 days	Thu 01/02/18
	Module PDR	0 days	Mon 30/04/18
	Module FDR	0 days	Wed 01/05/19
	Module PRR	0 days	Wed 30/09/20
	Assembly sites qualification	302 days	Mon 25/03/19
	Assembly Sites Qualified	0 days	Tue 19/05/20
	Pre-prod modules assembly and test	240 days	Thu 24/10/19
	Production modules assembly	546 days	Thu 21/01/21
	Barrel modules assembly	546 days	Thu 21/01/21
	Outer Barrel Modules 10% completed	0 days	Thu 22/07/21
	Outer Barrel Modules 50% completed	0 days	Thu 17/03/22
	Outer Barrel Modules 100% completed	0 days	Thu 23/02/23
	End-cap modules assembly	546 days	Thu 21/01/21
	EndCap Modules 10% completed	0 days	Thu 22/07/21
	EndCap Modules 50% completed	0 days	Thu 17/03/22
	EndCap Modules 100% completed	0 days	Thu 23/02/23
	Inner modules assembly	546 days	Thu 21/01/21
	Inner Modules 10% completed	0 days	Thu 22/07/21
	Inner Modules 50% completed	0 days	Thu 03/03/22
	Inner Modules 100% completed	0 days	Thu 23/02/23
2.1.3.4	Module testing	546 days	Thu 18/02/21
	Barrel modules test	546 days	Thu 18/02/21
	End-cap modules test	546 days	Thu 18/02/21
	Inner modules test	546 days	Thu 18/02/21

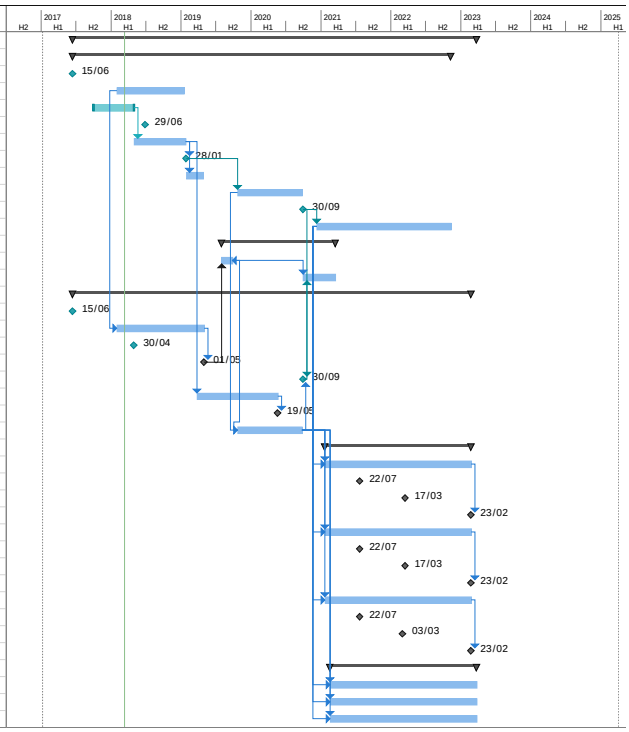


Figure 19.7: Module production schedule.

January 2018 and will be complete by the start of April 2019. Module pre-production starts in Q4 2019 and bulk production starts at the end of 2020. It is foreseen that the production of all module types start simultaneously as they are required to establish the loading process. Module loading on to staves starts as soon as the modules become available at the start of 2021 and is complete at the end of 2022. Detector integration starts in Q4 2022 and is complete by the end of 2023. The module construction is expected to continue for 25 months, as illustrated in Figure 19.7.

19.4.5 Production of the services for the ITk Pixel Detector

The preparation of the Type-0 and Type-I services for the Pixel Detector (including cables, fibres, patch panels, tubes) will take place between Q2 2017 and the middle of 2020. For each component, there is a significant period of capturing the requirements and reviewing the specifications. A short period of pre-production and qualification, during the first half of 2019, is followed by the final production starting in Q3 2019. For the electrical-optical conversion stage of the data lines, in Q3 2017, the ITk Pixel community chose the VTRX++ as the baseline solution. This is a joint ATLAS-CMS venture based on commercially available components. Pre-production of the components is scheduled to start in Q2 2020, followed

rapidly by bulk production. Orders will be placed for the GBT transmitters in the middle of 2020 and is complete one year later.

19.4.6 Local Supports

The process of capturing the requirements and specifications for the Pixel Local supports has been in progress for several years and has strongly influenced the demands of the detector layout. This has been explained in detail in Chapter 13, where the design, construction and results from the first prototypes have been described. This process will be brought to a formal conclusion in Q2 2018 with the presentation and review of the specifications documents. A Preliminary Design Review in Q3 2018 will be followed rather quickly by a Final Design Review in Q2 2019. The production of the local support structures will take place from the beginning of 2020 to the beginning of 2022. Loading of modules on to the supports starts in Q2 2021 (Figure 19.8). It is worth noting that the module production and the module loading activities must almost completely overlapped, in order to complete the loading phase (especially of the outer barrel) by Q3 2023.

WBS	Task Name	Duration	Start
2.1.5	Local Supports	1408 days	Thu 05/04/18
	Spec review	0 days	Thu 05/04/18
	PDR	0 days	Thu 23/08/18
	FDR	0 days	Thu 30/05/19
	Local supports PRR	0 days	Wed 13/11/19
	Loaded Local Supports pre-production	6 mons	Thu 30/05/19
2.1.5.1	Local Support cooling line	240 days	Thu 14/11/19
2.1.5.1.1	Outer Barrel Local Support Cooling Line	12 mons	Thu 14/11/19
2.1.5.1.2	Outer Encap Local Support Cooling Line	6 mons	Thu 14/11/19
2.1.5.1.3	Inner Barrel Local Support Cooling Line	6 mons	Thu 14/11/19
2.1.5.1.4	Inner Encap Local Support Cooling Line	6 mons	Thu 14/11/19
2.1.5.2	Local support Mechanical Structure	550 days	Thu 06/02/20
	First Mechanics from each subsystem delivere	0 days	Thu 06/02/20
2.1.5.2.1	Outer Barrel mechanical structure	550 days	Thu 06/02/20
2.1.5.2.2	Outer Endcap mechanical structure	350 days	Thu 06/02/20
2.1.5.2.3	Inner Barrel mechanical structure	250 days	Thu 06/02/20
2.1.5.2.4	Inner Endcap mechanical structure	250 days	Thu 06/02/20
2.1.5.3	Module loading on local supports	618 days	Thu 15/04/21
2.1.5.3.10	First OB Loaded local support delivered	0 days	Thu 15/04/21
2.1.5.3.11	50% OB Loaded local support delivered	0 days	Tue 21/06/22
2.1.5.3.1	Outer Barrel Module Loading	618 days	Thu 15/04/21
2.1.5.3.12	First EndCap Loaded local support delivered	0 days	Thu 15/04/21
2.1.5.3.13	50% EndCap Loaded local support delivered	0 days	Tue 03/05/22
2.1.5.3.2	Outer Endcap Module Loading	546 days	Thu 15/04/21
2.1.5.3.14	First Inner Loaded local support delivered	0 days	Thu 15/04/21
2.1.5.3.15	50% Inner Loaded local support delivered	0 days	Tue 03/05/22
2.1.5.3.3	Inner Barrel Module Loading	546 days	Thu 15/04/21
2.1.5.3.4	Inner Endcap Module Loading	546 days	Thu 15/04/21

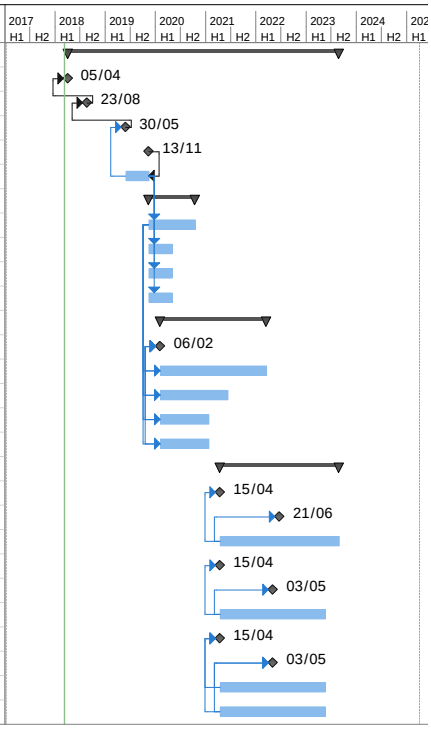


Figure 19.8: Local support production and loading schedule.

19.4.7 Integration of the ITk Pixel Detector

The planning of the integration of the Pixel Detector is illustrated in Figure 19.9. The Pixel Detector integration starts in Q3 2021, as soon as the first loaded staves and rings are available. The outer barrel is expected to be completed by November 2023. The two end-caps will be delivered at CERN in October 2023. The inner system will be delivered at CERN in quadrants in October 2023 and assembled by the end of 2023. The different phases of the Pixel Detector integration (integration of end-caps and outer barrel, insertion of the outer system in ITk, insertion of the inner system) will proceed in sequence from November 2023 till May 2024 and will be interleaved with test periods to verify the integrity of the subsystems. Form July 2024, a six months commissioning phase will start. During this period it will be possible to operate up to 12.5% of the ITk. The ITk must be ready for installation in ATLAS on April 2025.

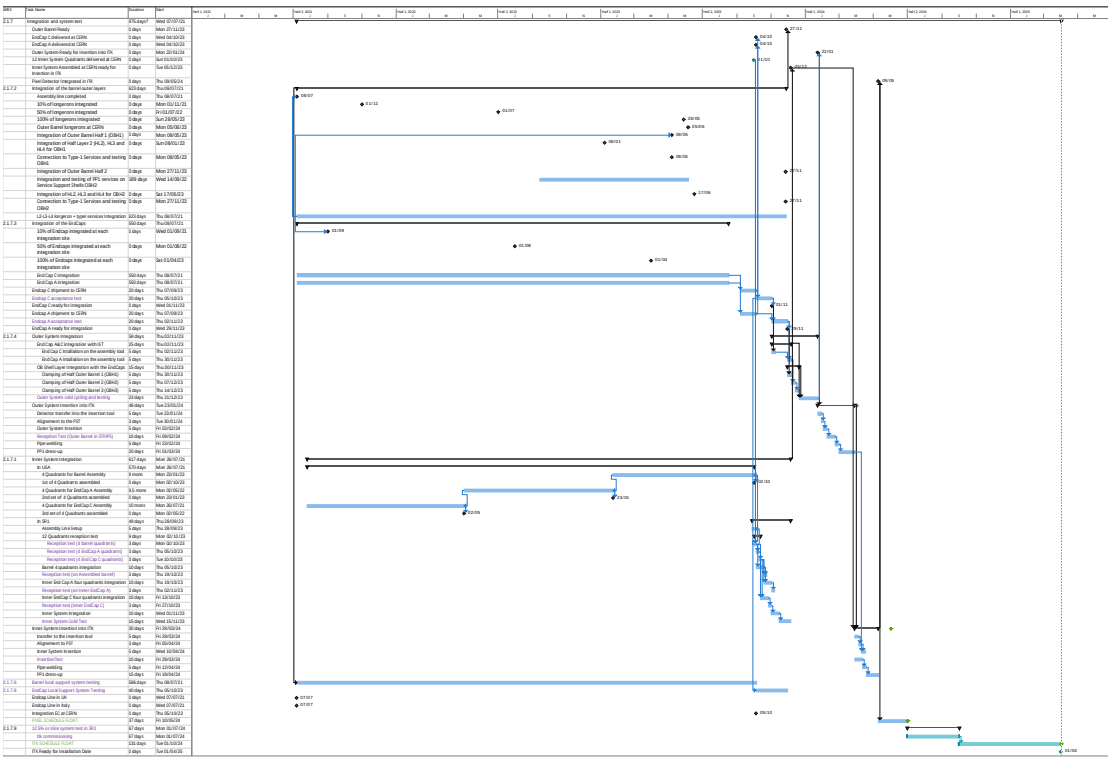


Figure 19.9: Pixel Detector integration schedule.

19.4.8 Common Structures for the ITk

The schedule for the common structures (outer cylinder, structural bulkheads and associated barriers) is driven by the need to have these components available at the start of the

integration of the strip systems beginning 2021. The outer cylinder is needed to allow for the assembly of the barrel strip structures including the Type-I services in their final location inside the ITk. Whereas the structural bulkheads are not mechanically linked in the final configuration, they are so closely related to the Strip end-caps that they need to be included in the construction of the end-caps. This would allow for a compact end-cap package including services. Other common structures, such as the Pixel Support Tube and the Inner Positioning Tube (that defines the inner radius of the Pixel volume), will be needed at a later stage of the ITk integration. An integration cradle, that provides support during the integration process and later transport to Point-1, is needed at the beginning of the Strip integration phase. A volume mock-up of this structure will be built so that it is available during LS2 (2019) for insertion trials into ATLAS to verify the envelopes for ITk and cradle, and the approach paths.

A key milestone for the next few years is the demonstration that the low evaporation temperature of -35° C, which is needed primarily for the Pixel system, can be achieved with a realistic feed and return pipe network and distribution. Because of the crucial importance of this issue for technology choices in the pixel system, a test facility ("baby demonstrator") is being set up, which is scheduled to provide results at the beginning of 2018. Because of the larger thermal headroom in the Strip system, the ultimate achievable evaporation temperature is much less critical for the strip system. However, use of the baby demonstrator facility will be made to verify the designs for evaporators and Type-I services in the strip system. As the goal of the baby demonstrator is to demonstrate low-temperature operation, it will only supply a limited amount of cooling power (5 kW). It is anticipated that the final cooling plants will be larger by about a factor 10 (50 kW) and the design and performance of such a close-to-final plant will be investigated in a demonstrator plant to be available in 2020. After that the design of the cooling plants, the ITk will be finalised and production will be commenced.

19.4.9 Power supplies

The development and purchase of power supplies for Low Voltage, High Voltage and DCS starts with small numbers of demonstrators between 2018 and 2019. This will be followed by an extensive period of testing. It is anticipated that a 10% advanced purchase of these items will be complete in early 2024 to support the ITk commissioning on surface. The bulk purchase will be launched about one year later.

19.4.10 ITk DAQ Schedule

A description of the ITk off-detector read-out and its interface to ATLAS TDAQ is contained in Chapter 10. At the time of this TDR, the work focuses in two separate areas which will start to converge in 2018. Work is ongoing on DAQ systems required to be able to test Pixel

and Strip modules as they start to be produced. These systems will evolve into production test systems. In parallel, a group representing the Pixel and the Strip systems are working with a group from the TDAQ organisation to define the hardware, firmware and software requirements needed to meet the ITk read-out and control specifications. Eventually, the components of the test DAQ systems will be incorporated into the online DAQ system interfaced to the ATLAS TDAQ. While it is important to understand the requirements of the online DAQ system soon, the actual purchasing of hardware can be delayed for some time until it is needed and when it is hoped that the costs will have decreased.

In the context of the Pixel demonstrator programme, several read-out solutions will be tested during 2018, and the solution to be used in the test sites will be identified. The procurement of these components will happen at the beginning of 2019, to allow the qualification of the production sites and the beginning of the module pre-production at the end of 2019. Larger systems, like the ones needed for the integration of the detector, will be likely based on pre-production series of the final read-out boards. The read-out of the 12.5% slice of the ITk at the end of the integration phase will be based on the production version of the DAQ hardware and software.

20 Costing

20.1 Introduction

The core-cost of the ITk Pixel Detector and the ITk common items (Common Mechanics and Common Electronics) are presented. The structure of the cost estimate and the uncertainties in the estimate are discussed. This is followed by a presentation of the spending profile that spans the production and loading of the Pixel Detector and integration and installation of the complete ITk Detector. The costs presented are consistent with the 4 MHz read-out-solution of the Trigger and Data Acquisition architecture presented in the TDAQ-TDR.

The spend profile is driven by the needs of the production and loading sequences presented in Chapter 19 and the need to make timely, staged purchases. The core values presented are based on bottoms up estimates of the different parts of the detector. In preparing the total core costs the Pixel Detector has been divided into three parts: an inner section, containing two barrel layers (Layer 0 and Layer 1) and two sets of rings (Ring 0 and Ring 1); an outer barrel section, with three barrel layers (Layer 2, Layer 3, and Layer 4); and two end-caps each with three sets of rings each (Ring 2, Ring 3 and Ring 4). The inner section is designed to be extracted and replaced during a long shutdown of the LHC and, being designed to be radiation tolerant up to a total integrated luminosity of 2000 fb^{-1}, it will have to be replaced at least once during the lifetime of the LHC phase II program. The pixel costing is based on a layout presented in Chapter 2 that includes a five-layer barrel configuration with a disk arrangement in the forward direction covering the pseudo-rapidity range up to $|\eta| = 4.0$. The construction of the different sections of the Pixel Detector will be shared between consortia of funding agencies who will produce the inner system (Layer 0, Layer 1, Ring 0 and Ring 1), the outer barrel (Layer 2, Layer 3, and Layer 4) and the two end-caps (Ring 2, Ring 3 and Ring 4) respectively. The core cost estimate is based on standard sensors bump-bonded to the front-end chip fabricated in a 65 nm CMOS process. The sensors in the inner layers will be 100 μm thick n-in-n or 3D. In the outer layers the sensors will be n-in-p. The cost of the hybridisation includes the cost of bump bonding. The cost of the bump bonding, which is a significant fraction of the cost of the module, is based on quotes received from different vendors in 2015. The uncertainty in the cost of bump bonding is one of the key-risks in the pixel module production. A market survey for the planar sensors was launched in Q4 2017 and another one for the provision of the bump-bonding process will be launched in Q1 2018. It is important to identify multiple (perhaps as many as five or six) bump bonding vendors for the production period. The front-end chips will be purchased

through CERN using existing frame contracts. The values quoted include the cost of the mask sets for production and a one year pre-production period when 10% of the modules will be fabricated ahead of bulk production.

20.2 The Yield Model

The number of components required at each stage of the process has been calculated based on a yield model that is used to propagate the effects of losses of individual component and component-assembly losses at different stages of the production, loading and testing. The yield values in the yield model are based on a combination of experience gained in the construction of the existing Pixel Detector, the IBL and measurements made in prototyping ITk parts.

20.3 Pre-production, NRE, Exchange rates and Quality Factors

The pre-production components will be fabricated using final tooling and staff, and will increase confidence in the readiness of the sites for the volume production. The pre-production parts are also used in the qualification of the individual production sites. The costs of infrastructure, prototypes, and spare components are not included in a core costing and are not presented here.

Custom ASICs have significant non-recurrent engineering (NRE) costs that are included in the estimate of the core cost. Based on previous experience, it has been assumed that two complete mask sets will be required for each submission (sensors and ASICs).

When components will be purchased in a country other than Switzerland, the exchange rate of those countries to Swiss Francs (CHF) have been fixed to the same values used in the preparation of the Strip TDR. This was calculated as the 3 month average at the end of 2016. The price estimates for all the individual items are based on the most accurate information available at the time of writing. The level of cost certainty of individual items depends on the amount of technical development and understanding of its procurement process.

Cost quality factors have been assigned to each of the components according to the following definitions:

QF1 Items for which there is a recent (< 1 year) catalogue price or quote on a nearly completed design and for which there is more than one potential vendor.

–OR–

Items that are a copy or almost identical to an existing design for which there is a recent (< 1 year) catalogue price or quote and for which there is more than one potential vendor.

QF2 Items that just fall short of satisfying the QF1 criteria: Items that have only one potential vendor.

–OR–

Estimate that are based on a detailed but not completed design.

–OR–

Items that were adapted from an existing design with minor modifications.

QF3 Items with quotes > 2 years.

–OR–

Items whose cost estimates are based on a conceptual design or adapted from existing design with extensive modifications.

–OR–

Items whose costs are estimated using physicist or engineering experience regardless of the maturity of the design.

QF4 Items that have unproven fabrication yields or for which there are unique issues e.g. a special-order item and/or a single preferred vendor

QF5 Items that are still in a conceptual stage with no detailed specifications or design.

The most precise current estimates (QF1) are those that are purchased through the CERN frame contracts. The prices depend on the number and size of the ASICs and these are now fixed. A number of items have had multiple prototyping cycles using one or more vendors. The cost estimates have been provided for a full-scale production (QF2). There is more uncertainty for these costs as the vendors used for production cannot be determined before a full tendering process. Additionally, the details of the quality control processes to be performed by the vendors have not been finalized, which can influence the cost. This category includes items such as: sensors, flexes, and carbon fibre materials Items with an uncertainty of QF3 typically have had multiple prototyping cycles. The details of the global supports for the barrel are also at the engineering design phase. Other items with QF3 are off-the-shelf items for which the final models have not been chosen (low voltage and high voltage power supplies).

20.4 Current core cost estimates and the spend profile

The cost estimates presented here are broken down to the third level of the WBS shown in Table 19.1. The costs of common mechanics and common electronics are 12,434 kCHF and 931 kCHF respectively. We also include the cost of developing an ITk production database developed in industry. Also shown are the cost profiles for the different level 3 WBS items.

20.5 The core cost of an ITk Pixel Module

The cost of the module is relatively well known as it is based on considerable experience accumulated with other detectors and on a robust R&D program targeted at the development of a Pixel module for HL-LHC carried out in the ITk Pixel community over the last three years. Most of the module components have a relatively mature design and the cost of the front-end chip is well known.

A hybrid Pixel module consists of two principle elements: a bare module comprising the sensor and the read-out chip that are connected via a high density interconnection technique (flip-chip bump bonding) providing a conductive connection for each pixel; a flexible PCB (module flex) glued to the bare module and providing the connections to the read-out and power distribution systems.

The same front-end chip is used throughout the entire detector. It will be implemented in 65 nm CMOS technology. The chip size will be 20×19.2 mm^2, and the assumed pixel cell size 50×50 μm^2. The cost of the FE chip is well known, as the chip will be purchased through a CERN frame contract with the selected foundry. In calculating the costs the two submissions of this chip are foreseen in 2018 and 2019 respectively. The large scale prototype that was submitted in August 2017 (RD53A) contains most of the features required for the final chip, and, for this reason, a single submission might be sufficient to have a production grade chip. The cost of each submission is 920 kCHF. The cost per cm^2 of each chip takes into account a yield factor, derived from the experience with the construction of similar devices implemented in the same technology

Different types of sensors, with different level of radiation tolerance, will be used in the different parts of the detector: 3D sensors and thin (100 μm) planar sensors in the inner section, 150 μm planar sensors in Layer 2, Layer 3, Layer 4 and End-caps. The costs used in this estimate are derived from preliminary quotes from several vendors, and, as in the case of the FE chip, include a yield factor. The cost of the bump-bonding includes the complete post-processing of the FE and sensor wafers (under bump metallization, bump deposition, thinning and dicing) and the flip-chip process to bond the two components. Different yield values are assumed for the different types of sensors which reflect the complexity in handling the wafers and the complete assembly.

The bump-bonding estimate is based on preliminary quotes from three vendors. Interconnection is one of the potential choke-points in bulk module production and requires careful monitoring. The cost of the flex circuit is small, compared to the other components, and it is estimated on the basis of similar design in the previous generation of Pixel Detectors.

Given the cost of the individual components, the cost of a complete module is 1000 CHF for the 3D single chip modules used in Layer 0, and around 2,400 CHF for the quad modules used in the rest of the detector. The total module cost, including the 10% of pre-production accounts for 50% of the total cost of the Pixel Detector.

20.6 The core cost of the local supports of the Pixel Detector

The design of the mechanical structures used to support the modules is in the preliminary phase, but several prototypes have been produced and tested. The techniques that will be used in the fabrication of the local supports in the various regions of the Pixel Detectors have been defined, and the cost evaluation of each component is based on experience accumulated in different laboratories in building support structures with composite materials for the prototyping phase. The local supports account for 12% of the total cost.

The Inner Support Tube (IST) is costed separately. Its design is not yet complete and has a cost quality factor QF4. The design does not include a thermal barrier to isolate the outer part of the Pixel Detector during the replacement of the inner section. The possibility that we will need a thermal barrier has been captured in the risk register with an associated cost. The IST cost is estimated to be 411 kCHF.

20.7 The core cost of the Pixel Read-out and associated services

A complete design of the pixel services is not yet complete. A preliminary design has been presented in Chapter 14, but several of the proposed solutions still need to be demonstrated in a comprehensive system test. For the costing presented here, the evaluation of the ON and OFF-detector services is based on the preliminary design and depends on the number of modules and staves to be powered and the total amount of data that must be extracted from the detector. The assumptions used to determine the number of cables and read-out-fibres are realistic and based on the most recent results of our R&D program and on ATLAS requirements on trigger rate and maximum trigger latency, while the cost uncertainty depends on the lack of a final design and of a market survey to identify the best technological solutions. The total cost of the services accounts for 21% of the total pixel costs.

20.8 The core costs of Pixel loading and integration

Based on the experience accumulated during the construction of the existing ATLAS Pixel Detector, we have estimated the core cost for the module production, module loading and integration phases. This cost covers the tools needed to position the modules on the supports and to assemble the complete structures, as well as the specific equipment needed for QA and QC. Loading and integration represents 4% of the total core value of the Pixel Detector.

20.9 The total core cost of the Pixel Detector

The total core cost of the Pixel Detector is summarized in Table 20.1. The cost of the inner section, that will need to be replaced once during the HL-LHC program, is 8.8 MCHF. The uncertainty on the overall cost, based on the estimated fluctuations of the cost of individual items is around 25%. Cost estimates will improve as the design matures and the remaining parametric estimates are replaced with a detailed cost estimate.

20.10 ITk Common Items

A list of the common ITk items with core values that will be covered by the institutes participating in the construction of the ITk is presented in the cost summary table. Only WBS items with a finite core value are presented. The core values have been determined from estimates based on experience with previous constructions (ATLAS ID and IBL) and in some cases scaling by area from previous costings has been applied. The existing dry-gas system used for the Inner Detector will be reused with a small amount of pipe connection at the detector end of the supply lines. It is also assumed that the existing cable cooling system serving electronics at PP2 and cables inside the detector volume will also be reused. The latter will need some modifications to eliminate the use of fluorocarbon liquids. The estimates of the value for the common structures, including the outer cylinder and the pixel support tube, are based on previous experience building large scale carbon fibre support structures (for example the existing pixel support tube) and correcting for inflation to arrive at 2016 values. The CO_2 cooling system is still in development. A small-scale prototype system (5 kW at -30°C) has been constructed ahead of the Pixel TDR and tests results will be available in early 2018. A full-scale development system of the cooling system will follow. The value presented here is based on experiences from the construction of similar systems for ATLAS, CMS and LHCb. The FELIX-I read-out covers the purchase of a limited number of Phase I FELIX read-out systems to be used during integration and commissioning at the Institutes and CERN surface building. The environmental monitoring estimate is the sum of a significant number of small-scale monitoring systems (temperature, humidity, radiation

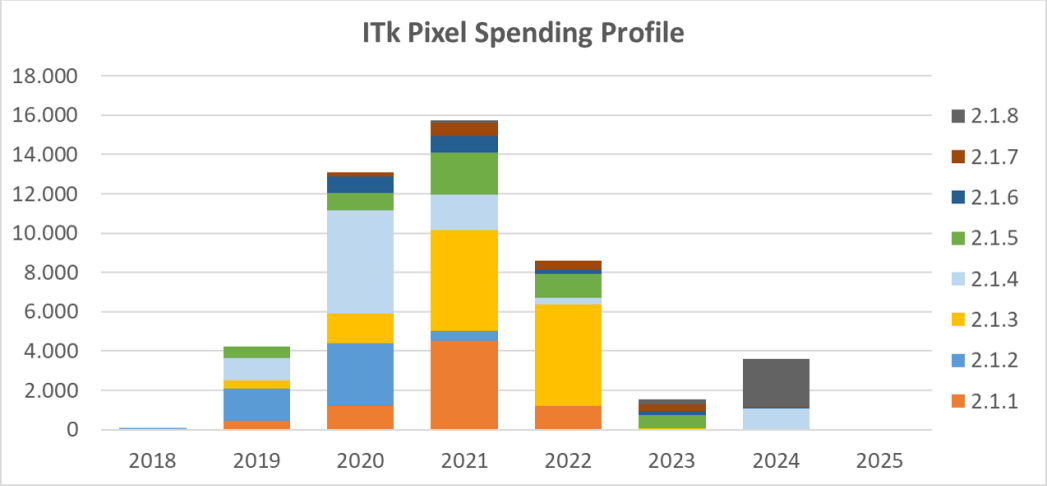


Figure 20.1: The cost profile in kCHF of the ITk pixels from 2018 to 2025.

backgrounds etc.). The estimate of the core costs come from quotes for individual parts. The core value of the interlock system is based on estimates on the construction existing systems in ATLAS.

20.11 Total Cost of the ITk Detector

Table 20.1 presents a summary of the total costs of the ITk for the Strip and Pixel Detectors and the common mechanics and common electronics.

Also shown are the cost profiles for the core spending for: pixel, common mechanics and common electronics (see Figures 20.1, 20.2, and 20.3).

Table 20.1: The total costs of the ITk. The costs of the pixels, common mechanics and common electronics are detailed with the WBS number.

WBS	Description	Costs/kCHF
2.1.1	Sensors	7,339
2.1.2	ASICS	5,403
2.1.3	Hybridization and module assembly	12,325
2.1.4	Services	9,615
2.1.5	Local support	5,492
2.1.6	Global mechanics and installation tooling	2,119
2.1.7	Integration and system test	1,767
2.1.8	Off-detector electronics	2,823
Total for pixels		46,882
2.3.1	Surface assembly and commissioning	2,695
2.3.2	Integration and insertion in the pit	300
2.3.3	Common Structures including PST	2,534
2.3.4	Poly moderator	99
2.3.5	Outer Serices	387
2.3.6	CO_2 cooling plant	6,419
2.4.1	Environmental monitoring	244
2.4.2	Interlock and protection system	380
2.4.3	Grounding and shielding	14
2.4.4	Luminosity and beam protection	293
2.4.5	Phase I FELIX Read-out	777
2.5.1	Production database	303
Total Common Items		14,445
Strip Tracker		60,637
Total for ITk		**121,964**

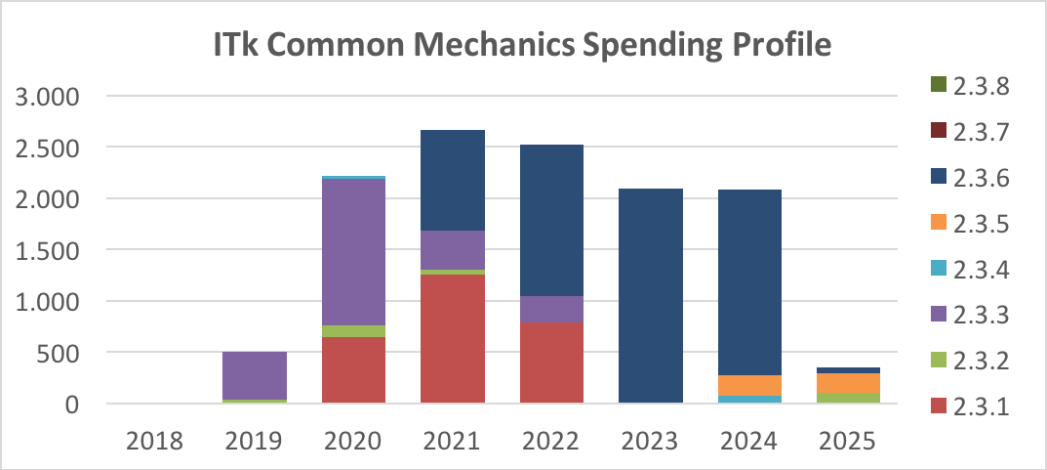


Figure 20.2: The cost profile in kCHF of the ITk Common Mechanics from 2018 to 2025.

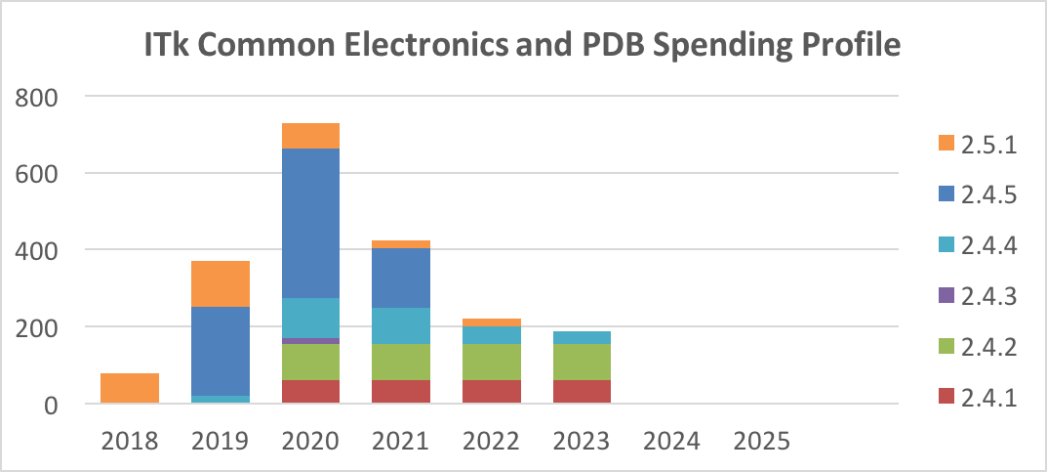


Figure 20.3: The cost profile in kCHF of the ITk Common Electronics from 2018 to 2025.

21 Risk Analysis and Risk Mitigation

21.1 Introduction and overview

The scope of this section is to describe the process developed to assess, manage, mitigate, and, if necessary, respond to risks associated with the ITk pixel project and to summarise the status of the work at this point in time. Risk management has been fully integrated into the ITk project following broadly accepted risk management protocols outlined in DOE G413.3 [169] and "Project Management Body of Knowledge" [170].

Knowledge and experience from other large projects (CMS, The Upgrade to the Argonne Advanced Photon Source, DESI-II) has been studied and the risk management process has evolved as understanding improved following its implementation for the ITk Strip project as described in the ITk Strip TDR [1].

As shown in the ITk organization section (Chapter 23) of the Strip TDR, risk management is conducted by a Risk Management Committee (RMC), which reports through the ITk Steering Committee to the ITk Project Leader. The responsibility of the RMC is to manage the identification of potential project risks, the analysis of these risks, the response planning, the development of mitigation strategies, and monitoring and tracking of the risks and mitigation plans. In this context, a risk is any event not included in the project plan which can have a potential impact (positive or negative) on the ITk project. The full risk management process is documented in the ITk Risk Management Plan [RMP]. The typical five-step approach to risk management (outlined below) is being followed:

I. Identify potential project risks.

II. Analyse the risk.

III. Plan risk mitigation and response strategies.

IV. Execute risk mitigation and response strategies.

V. Monitor and track the results, revising the mitigation strategies as necessary.

In the sections below, we summarise the ITk RMP, describe the status of the pixel risk management process, and illustrate the content of the ITk risk register for some examples of risks identified in the pixel project context.

21.2 Risk Management Plan

Following accepted practices, the ITk Risk Management Plan has been prepared and approved by the RMC, the ITk Project Engineers, and the ITk Project Leaders. The RMP defines the roles and responsibilities of the members of the ITk project organization with regard to risk management, the documents to be prepared as part of the RMP, the thresholds used to characterise risk probability and impact, and the process of monitoring and controlling risks throughout the project. Of particular note, the RMP defines the role of the Activity Coordinators to identify and characterise risk elements in their areas of responsibility and to review these in the Risk Management Committee. This plan takes into account the special international nature of the ITk project with, for example, contributions and commitments to the project made through negotiations involving multiple national funding agencies and the resulting implications for transfer of risk. A separate failure mode and effect analysis (FMEA) is being implemented which addresses such characteristics as single point of failure. The FMEA is considered to be intrinsic to the system/component design and the FMEA report will be reviewed as part of the PRR and FDR.

21.3 Risk Register

The process of identifying Pixel risk has followed the procedures described in the ITk RMP (top down identification, brainstorming sessions, risk workshop, Activity Coordinator follow-up on probability and impact, RMC review, quantitative risk analysis). The ITk project management (Project Leaders, Project Engineers and Deputies) have performed a top-down high-level risk assessment. Elements identified at this stage as potentially of particular significance included: low bare module yield in production and flip-chipping due to worse mechanical stability of thin sensors; the cost of depositing UBM and the opportunity provided by performing this at the sensor vendor; the yield of 3D sensors; and the rate at which planar sensors can be fabricated. Following the high level identification of risks, the Activity Coordinators have prepared a more detailed set of risks as well as additional material on the risk mitigation and response plans. Approximately 50 risk elements have been identified through discussions at a risk workshop and have been captured in the risk register. These have been reviewed in more detail by Activity Coordinators and members of the RMC to provide a preliminary set of pixel risk elements. The level of detail captured through this process is presented below for a number of risk elements (chosen for their significance to the pixel project): bare module yield; flip-chip volume, cost and schedule; thin wafer processing and the impact on cost for bump bonding; planar sensor biasing structures; FE chip production.

1. Bare module yield
   The bare modules defined in Section 4.3 have a risk of low yield in production and a longer production schedule. Production in smaller batches and engaging multiple

vendors will be used to mitigate the production risk. Use of many test structures to check quality will be used to monitor and mitigate the risk of a low production yield. The bare module yield is dependent on the fraction of good wafers and chips following bump deposition and flip-chip processing to bond the sensor to the front-end chip. The most pessimistic yield was estimated from discussions with several vendors and has a low probability; the most optimistic yield is from experience with processing wafers for the FE-I4 and has a medium probability. To complete the risk assessment a document describing the risk probability and impact of this risk and the basis for these numbers has been prepared, reviewed by the RMC and linked to the Risk Register. In the event that this risk is realized, the consequence is that the production schedule may be longer and there may be a cost increase. This is dependent upon whether any delay is absorbed with an increase in through-put at vendors or whether the decrease in yield is contained within the vendor production contract.

2. Flip-chip volume cost and schedule
   The design specifies the use of thinned FE wafers in layers 0 and 1. Due to the greater mechanical fragility, the use of such wafers decreases the yield of FE chips successfully bump-bonded to sensors resulting in a higher cost due to the need to process additional wafers to offset the reduced yield of good bare modules. Additionally fewer vendors are capable of processing such wafers (applying the UMB, bumps and performing the bump bonding of sensor to FE chip). R&D is being performed to qualify additional vendors and design specifications will be reviewed following the production of the RD53 chips. The impact on yield and thereby cost is obtained using engineering judgement and will be updated following the experience with the RD53 chips. Should the yield be wholly unacceptable, this risk may be mitigated through use of 400 μm chips with a resulting negative impact on physics performance due to the additional material (0.3% radiation length at normal incidence).

3. Thin wafer processing and impact on price and schedule for bump bonding
   Thin FE wafers have been specified in the module design to provide minimum material in the tracking volume and thereby maximum tracking performance. The use of thin FE wafers results in lower yields of successfully bump-bonded chips plus sensors due in part to the lower mechanical stability of such wafers. The opportunity of a reduction in cost is presented by the use of thicker (400 μm) FE chips. The thicker wafers present an additional 0.3% of a radiation length at normal incidence. Simulation studies will be carried out to estimate the impact of this additional material on performance over the full acceptance, and a value engineering decision will be made based on the results of the performance studies and the potential cost reduction resulting from the use of 400 μm rather than 100 μm FE chips. Note that this risk element is correlated with point 2 above (flip-chip volume cost and schedule) since both derive from the use of thinned FE wafers.

4. Planar sensor biasing structures

R&D testing is providing hints that biasing structures implemented in pixel cells for testing before interconnection lead to excessive efficiency loss for small RD53 pixel cells after irradiation. It is possible to use instead temporary conductive layers to contact the pixel implant for QA before interconnection. The additional process mask implies a cost increase for sensor production. These results will be rechecked for the RD53 chips, which have a lower signal threshold. If a response is necessary, more resources will be required for sensor production to cover the additional processing steps.

5. Front End chip production
   The project plan foresees the development of the ATLAS FE chip (ITkPix) based on the RD53A chip. ITkPix will meet all all ITk requirements including 5.12 Gb/s serial transmission. Two design iterations are included in the project plan. There is a risk is that a third cycle is needed which will impact cost and schedule. The cost risk associated with a third iteration is dominated by the production of new masks and is based on the engineering judgement that it will not be necessary to fabricate a complete set of new masks. A 3-point distribution has been used in the quantitative cost impact based on the number of masks which need to be replaced. The schedule impact is based on the expected turnaround (production and testing) of a prototype run. Based on engineering judgement and experience with chips of similar complexity, the probability of a third cycle is 0.25. If ATLAS and CMS are obliged to share a common procurement for the production chips, there may be additional delays in the ATLAS schedule but presently this is not foreseen in the project plan.

Following review by the RMC, Subject Matter experts, Project Engineers and Project Leaders, the Risk Register has been populated from the compiled list of considered risks with the risk description, its assessment and potential impact in terms of cost, schedule and probability of occurrence and mitigation strategies. Thresholds, integrated into the Risk Register, are applied to the probability of occurrence, schedule and cost risk for elements to categorise the risk as “high”, “medium”, “low” or “negligible”. High and medium threat/opportunity risks are monitored by the RMC, while Pixel Activity Coordinators are responsible for monitoring low and negligible risks. Risks for which a sound mitigation plan is in place, may be identified, assessed and retired while others may be added to the list of risks for which there is a high level threat or opportunity and then subjected to even closer scrutiny.

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