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Design of a high-to-low voltage, low-power, isolated DC/DC converter for EV applications

Etienne Foray, Christian Martin, Bruno Allard, and Pascal Bevilacqua

Univ Lyon, INSA Lyon, Université Claude Bernard Lyon 1, Ecole Centrale de Lyon, CNRS, Ampère, UMR5005, 69621 Villeurbanne, France

Abstract—The design of a low-cost 800V-to-12V, 4 W isolated DC/DC converter for automotive applications is investigated. Such a converter is required to supply tiny systems directly from the high-voltage battery of an Electric Vehicle. In particular, a selected topology based on a Multi-Level Flying-Capacitor stage is analyzed. The converter operating mode selection is studied and simulation results reveal the interest of operating at the limit of the ZVS mode. The design of a planar transformer adapted to the application is described. Design considerations of an IC brick that includes the main blocks required to control the power stage are discussed. The performances of a 4 W prototype with two transformer designs validate the choice of the operating mode. The peak efficiency is 87.4% which confirms the interest of the selected approach compared to existing solutions

Index Terms—DC-DC converter(s), High-frequency transformer, Zero voltage switching, High-efficiency.

I. INTRODUCTION

THE usage of high-voltage DC buses become more and more frequent in several applications, like Electric Vehicles (EV) or PV sources. In the EV context, the battery voltage has increased up to 800 V in some cases [1]. Many measures are being taken to ensure the safety around the HV battery [2] and some systems like the Pyroswitch [3] (used to disconnect the HV battery in case of crash) might require to be supplied from the HV battery using an isolated converter. In the EV context, such a converter could also be used to power small actuators/sensors directly from the HV battery. Another example of applications where this type of converters could be used is to generate a local isolated supply to power the gate-drivers inside of a MVDC converter [4]. In all previous cases, the system requires only a low-voltage, low-power output. In this regard, an isolated DC/DC converter with a high input voltage capability and a low-voltage, low-power output is required. The specifications of the converter in the automotive context focus on its size, cost and efficiency.

A. Context

The design of an isolated High-Voltage Low-Power (HVLP) converter can be challenging, particularly due to the automotive constraints. The isolation requirement creates a conflict with the small size target, since a (bulky) transformer is required to ensure the galvanic isolation. The high input voltage is also an issue, due to the high stress applied on the components, in particular on the switches and the transformer. A more complex power stage architecture might be used to decrease the voltage stress on the switches, to avoid using

wide band-gap devices that are more expensive compared to standard silicon technologies. For the transformer, the high input voltage will significantly increase the no-load losses, making it difficult to reach a reasonable efficiency ($> 85\%$).

The design of an isolated HVLP converter with similar specifications is not extensively covered in the literature.

In [5]–[7] the design of a low-power off-line converter is discussed. [5], [6] present a low-cost solution with a wide input voltage range but with a low efficiency. In [7] the performances of the converter are improved but the size of the converter significantly increases, in particular with the passive components, due to the low operating frequency. In both cases, the input voltage is limited to 400/500 V and a Flyback architecture is selected for the power stage.

In [8], a solution to cope with a high input voltage (> 1.2 kV) is presented, placing several converters in series. However, the efficiency is still not good enough and a bulky transformer is required (although it is partially related to the higher power level).

Some existing products or reference designs can also be found. A solution from Cui Inc (AE5-EW) has a high input voltage (up to 1 kV) but the module size and cost are not in-line with the targeted converter specifications. A reference design from Texas Instrument (PMP7769) shows a high-input voltage as well (up to 860 V) with a reasonable transformer size. However in both cases the efficiency is limited to 70% or less under 800 V (with a load < 10 W).

B. Selected approach

An approach adapted to the particularity of the HVLP converters and in-line with the low-cost, small-size and high-efficiency perspectives is proposed. It focuses on three aspects:

a) *High switching frequency*: Most of presented solutions have a low switching frequency (< 100 kHz). Increasing the frequency should allow to reduce the size of filtering components (required at the input/output of the converter) but also to improve the size-performance trade-off inherent to the transformer design.

b) *Active devices integration with a low-cost Si process*: The integration of the active components of the converter should allow to reduce the size of the converter as well as to enhance its capability to work at high frequency. Although emerging materials like GaN offer better performances [9], the Silicon still remains of interest in a low power context where a low cost solution is targeted [10].

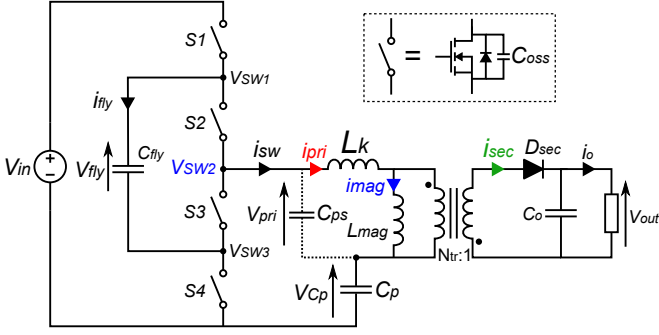


Fig. 1. Schematics of the 3-Level Flying-Capacitor AHBF

c) *Integrated planar transformer*: Planar transformers are selected for their low-profile and integration capability, as their windings can be directly placed on the same Printed Circuit Board (PCB) as the rest of the converter components. The constraints on the PCB manufacturing are released to decrease the cost of this part, taking for example a minimum width for tracks of 100 μm .

C. Choice of the topology

In low-power applications, the Flyback architecture is very often used for the power stage of the converter for its low complexity [5]–[7]. However, it is not compatible with the high-voltage high-efficiency and low-cost solution targeted here, due to its intrinsic limitations (high stress on the switch and on the transformer).

To overcome these limitations some interesting alternatives may be considered: Input Series Converters (ISC) [8], Switched-Capacitor (SC) stages [11] and Multi-Level Flying-Capacitor converters [12]. Previously, a qualitative comparison was built between these structures to determine which of them is suitable for a HVLP converter [13]. The comparison showed that the hybrid 3-Level Flying-Capacitor Asymmetrical Half-Bridge Flyback (3L-FC-AHBF) offers an interesting trade-off between complexity and performances. Being a hybrid topology between a SC stage and an isolated buck topology, it enables a significant reduction in the voltage stress on the transformer and the switches while remaining a single stage compact solution.

II. SELECTED TOPOLOGY

The selected topology is the 3L-FC-AHBF that can be described as an isolated Buck converter. To the best of authors' knowledge, this structure was not studied previously, however, its behavior is similar to the one of a simple AHBF that is already well covered in the literature [14], [15]. For this reason, this article only discussed shortly the power stage architecture because it focuses on the selected operating mode for the converter. The switching scheme is similar to the one used in non-isolated 3L-FC buck topology [16]. The circuit diagram of the 3L-FC-AHBF is shown in Fig. 1. In steady-state, the flying capacitor voltage is close to $V_{in}/2$ and it allows to decrease the voltage stress on the power switches and the transformer. Like in a Buck converter, the voltage

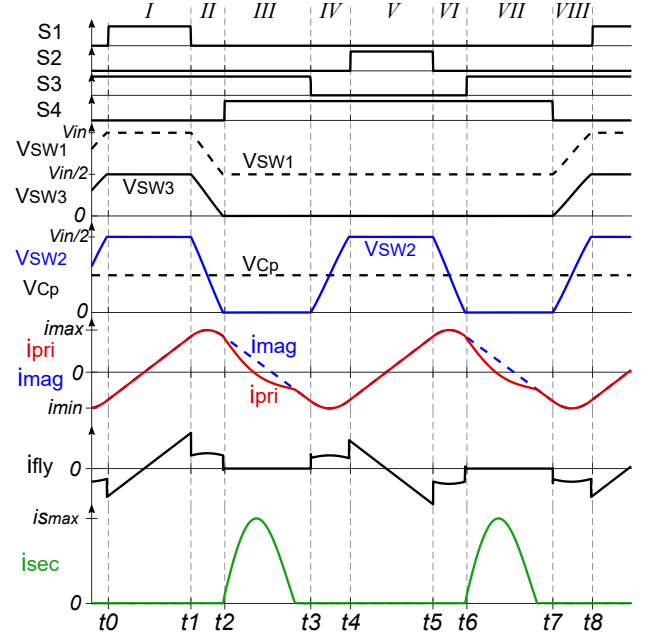


Fig. 2. 3-Level Flying-Capacitor AHBF simulation waveforms

across the capacitor C_p is a portion of the input voltage V_{in} . In this isolated version, V_{Cp} and the transformer turns ratio N_{tr} set the output voltage V_{out} . The main current and voltage waveforms obtained through ideal simulation are plotted in Fig. 2 with the control signals of the power switches.

A. Waveforms analysis

Few assumptions are introduced to simplify the analysis of the converter in steady-state:

- A constant voltage is assumed across the various capacitors in the power stage (i.e. C_p , C_o and C_{fly}).
- No voltage drop due to parasitic resistor is taken into account. Voltage drop due to the body-diode of the power FETs is also neglected.
- The value of the leakage inductance L_k is small compared to the one of the magnetizing inductance L_{mag} .
- The parasitic capacitor C_{ps} represents the contribution of all the parasitic capacitors taken into the account in the transformer model (mutual and self capacitances) referred to the primary side.

As shown by the converter waveforms, a switching period of the 3L-FC-AHBF can be divided into two half-periods with a very similar behavior (from t_0 to t_4 and from t_4 to t_8). In the following analysis the modes with a similar behavior are analyzed together.

Mode I ($t_0 - t_1$) & Mode V ($t_4 - t_5$)

In these modes, one of the high-side switches and the non-complementary low-side switch are ON ($S1/S3$ during mode I, $S2/S4$ in mode V) which forces the middle switching node V_{SW2} to $V_{in}/2$. The voltage across the primary side of the transformer is:

$$V_{pri} = V_{in}/2 - V_{Cp} \quad (1)$$

The current that flows through the primary side of the transformer is entirely due to the magnetizing current:

$$i_{SW} = i_{pri} = i_{mag} \quad (2)$$

The variation of these currents can be described as:

$$\frac{di_{pri}}{dt}(t) = \frac{V_{in}/2 - V_{Cp}}{L_{mag} + L_k} \quad (3)$$

The current through the flying capacitor is also equal to the primary current but its direction depends on the mode:

$$i_{fly} = \begin{cases} i_{pri} & \text{during mode I} \\ -i_{pri} & \text{during mode V} \end{cases} \quad (4)$$

Mode II ($t_1 - t_2$) & *Mode VI* ($t_5 - t_6$)

When the high-side switch turns off, the positive primary current initiates a ZVS transition at the various switching nodes. In these modes, V_{SW2} varies from $V_{in}/2$ to ground.

During these transitions, the parasitic capacitors connected to the various switching nodes are (dis)charged. The total parasitic capacitance in mode II can be expressed as:

$$C_{par_tot\ II} = C_{oss\ S1} + C_{oss\ S4} + C_{ps} \quad (5)$$

In mode VI the expression is:

$$C_{par_tot\ VI} = C_{oss\ S2} + C_{oss\ S3} + C_{ps} \quad (6)$$

If the same output capacitor C_{oss} is assumed for all the power switches, C_{par_tot} is equivalent in both modes. At the same time, the variations of the primary current i_{pri} and of the primary voltage V_{pri} can be expressed as:

$$\frac{di_{pri}}{dt}(t) = \frac{V_{SW2}(t) - V_{Cp}}{L_{mag} + L_k} \quad (7)$$

$$\frac{dV_{pri}}{dt}(t) = \frac{dV_{SW2}}{dt}(t) = -i_{pri}(t)/C_{par_tot} \quad (8)$$

A solution to these differential equations was proposed in [14]. However, they used some simplifications (for example, a constant value of C_{par_tot} is assumed although C_{oss} value drastically varies with the drain-source voltage) which limits the accuracy of the analytical solution. To be able to propose a more accurate solution to these equations, a simple algorithm was implemented (discussed in next Section).

During these modes, the current through the middle switching node (i_{SW}) and the current through the flying capacitor (i_{fly}) can be expressed as a portion of the primary current:

$$i_{SW}(t) = i_{pri}(t) \cdot \frac{2 \cdot C_{oss}}{C_{par_tot}} \quad (9)$$

$$i_{fly}(t) = \begin{cases} i_{pri}(t) \cdot C_{oss}/C_{par_tot} & \text{in mode II} \\ -i_{pri}(t) \cdot C_{oss}/C_{par_tot} & \text{in mode VI} \end{cases} \quad (10)$$

Mode III ($t_2 - t_3$) & *Mode VII* ($t_6 - t_7$)

As V_{SW2} reaches ground level, the low-side complementary switch turns-on ($S4$ in mode III, $S3$ in mode VII). Both low-side switches are ON in these modes, which forces a negative voltage across the primary side of the transformer:

$$V_{pri} = -V_{Cp} \quad (11)$$

Due to the reverse connection of the secondary winding of the transformer, a positive voltage is applied across the secondary, which forward biases the secondary diode D_{sec} and a current flows in the secondary side. The positive secondary current leads to a small difference between i_{pri} and i_{mag} (shown in Fig. 2) that can be expressed as:

$$i_{pri}(t) = i_{mag}(t) - \frac{i_{sec}(t)}{N_{tr}} \quad (12)$$

The dynamic of the secondary current depends on the voltage drop across the leakage inductance L_k but also on the parasitic capacitance of D_{sec} and on the various voltage drops due to the parasitic resistors.

Mode IV ($t_3 - t_4$) & *Mode VIII* ($t_7 - t_8$)

At the beginning of these modes, one of the low-side switches turns off ($S3$ in mode IV, $S4$ in mode VIII). The negative primary current forces V_{SW2} to rise from ground to $V_{in}/2$. The same parasitic capacitors are (dis)charged as in modes II and VI. The same expression can thus be used to described the variations of i_{pri} and V_{SW2} during these modes:

$$\frac{di_{pri}}{dt}(t) = \frac{V_{SW2}(t) - V_{Cp}}{L_{mag} + L_k} \quad (13)$$

$$\frac{dV_{SW2}}{dt}(t) = \frac{dV_{pri}}{dt}(t) = -i_{pri}(t)/C_{par_tot} \quad (14)$$

B. Steady-state behavior analysis

To find the relation between the input and output voltages of the converter, the first step is to compute the volt-second balance on the transformer primary side:

$$\int_{t_0}^{t_8} V_{pri}(t) dt = 0 \quad (15)$$

To simplify the analysis, the slope of the transitions observed at the switching nodes (during modes II, IV, VI, VIII) is assumed constant. In addition, the symmetry between the two half-periods allows to consider a similar on-time for the high-side switches ($t_{ON\ HS}$). The duration of the various ZVS transitions are assumed as follows:

$$(t_8 - t_7) = (t_4 - t_3) = dt_{HS} \quad (16)$$

$$(t_2 - t_1) = (t_6 - t_5) = dt_{LS} \quad (17)$$

Using these considerations, a relation between V_{Cp} and V_{in} can be derived from (15):

$$V_{Cp} = \frac{V_{in}}{T} \cdot \left(t_{ON\ HS} + \frac{dt_{HS} + dt_{LS}}{2} \right) = V_{in} \cdot D_{eff} \quad (18)$$

Where D_{eff} is the effective duty-cycle that takes into account the on-time of the power switch but also the contribution of the dead-times. Using the relation between the output voltage and the voltage across the primary capacitor C_p , it is possible to express the main transfer function of the converter as in (19):

$$V_{out} = V_{in} \cdot D_{eff} \cdot \frac{1}{N_{tr}} \cdot \frac{L_{mag}}{L_{mag} + L_k} - V_D \quad (19)$$

III. SELECTING CONVERTER OPERATING MODE

There are mainly two motivations that will guide the choice of the converter operating mode. First, the primary current ripple must be reduced, since it could generate significant conduction losses in the various parasitic resistors of the power stage. Second, the converter must operate in ZVS mode to maintain low switching losses and avoid issues related to EMI/EMC. However, the previous analysis of the power stage has shown that a ripple is required to operate in ZVS mode (since it is responsible for the negative values of the primary current), so it should not be canceled but minimized.

A. Objectives

To minimize the primary current ripple while maintaining the converter in ZVS mode, three options are considered:

- Decrease the total parasitic capacitor
- Find an optimal value for the transformer turns ratio N_{tr}
- Increase the switching frequency and the magnetizing inductance

As discussed in the analysis, the total parasitic capacitance connected to the switching nodes is mostly due to the output capacitor of the power switches and to the parasitic capacitors of the transformer. The reduction of these capacitance is discussed in the Section dedicated to the design considerations for the power stage.

The transformer turns ratio should be chosen to keep D_{eff} close to 25%. It would allow to release the constraint on the maximum duration of the ZVS transitions. If the transitions can be longer, a smaller current is required to (dis)charge the parasitic capacitors and the ripple can be reduced.

Finally, increasing the frequency (or the primary inductance value) is the other parameter to reduce the current ripple. But the constraint regarding the ZVS mode will put some limits to the maximum value these parameters can take, as discussed in the next paragraphs.

B. Optimization of the frequency/inductance pair

Fig. 3 presents the simulation results of a 3L-FC-AHBF operating at $V_{in} = 800$ V and $f_{sw} = 1$ MHz (note that this frequency is the one measured on the transformer, that is the double of the frequency at which the switches are operated). Three values of magnetizing inductance (350 μ H, 450 μ H, 550 μ H) are selected to present three operating points of the converter. The middle switching node V_{SW2} and the primary current i_{pri} waveforms are plotted for each inductance value. Note that in next Sections, the primary inductance is assumed to be equal to the magnetizing inductance (which is possible since the leakage inductance value is small with the planar technology).

Some significant differences appear in the waveforms depending on the magnetizing inductance. If the value is too large, the ZVS mode is not maintained as V_{SW2} does not reach $V_{in}/2$ before the high-side switch turns on, because the primary current ripple is too small. On the other hand, if L_{mag} value is too small, the converter operates in ZVS mode but a large current ripple is observed in the primary

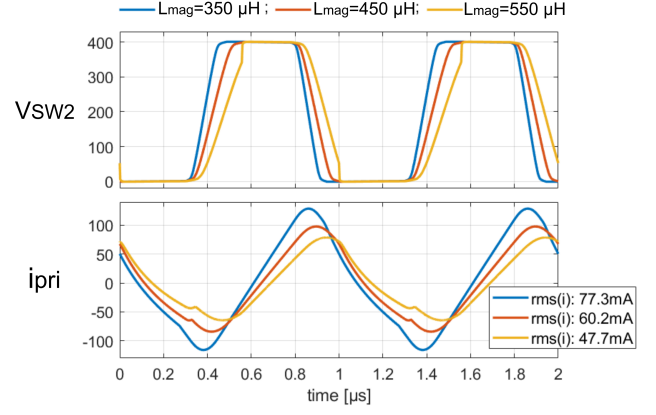


Fig. 3. Simulation waveforms for different values of magnetizing inductance

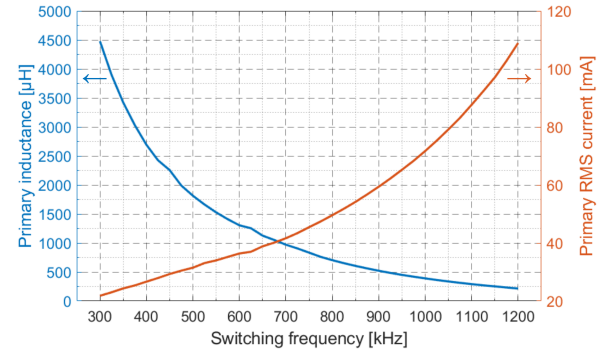


Fig. 4. Maximum L_{mag} vs f_{sw} and minimum $RMS(i_{pri})$ vs f_{sw}

side of the transformer. The targeted operating mode is the third one, represented by the switching waveforms associated to the medium value of L_{mag} (450 μ H). It allows a significant reduction in the primary current ripple (the RMS value is reduced by 22% between the 350 μ H case and the 450 μ H one, so a 40% reduction in conduction losses) while maintaining the ZVS mode.

To find the optimal value of L_{mag} , the switching frequency of the converter should be taken into account. For a given frequency, the maximum L_{mag} value is evaluated using a Mat-Lab routine that computes through iterations the waveforms of V_{pri} and i_{mag} , instead of using an analytical expression. It allows to take into account the reciprocal influence of i_{mag} and V_{pri} as described in (7) and (8) for example, leading to an accurate prediction of the waveforms during the ZVS transitions. Moreover, a more complex model for the switch output capacitors can be included in the routine (a piece-wise linear model of C_{oss} vs V_{DS} is used), which also improves the accuracy compared to a simple analytical expression (for which an equivalent value of C_{oss} is used).

Results presented in Fig. 4 reveal that the higher the f_{sw} , the lower the maximum value of L_{mag} and the higher the RMS current. It is due to the duration of the ZVS transitions that becomes shorter as the frequency increases. To complete the ZVS transitions in a shorter time, a larger current ripple is required, thus the maximum value of inductance must be smaller.

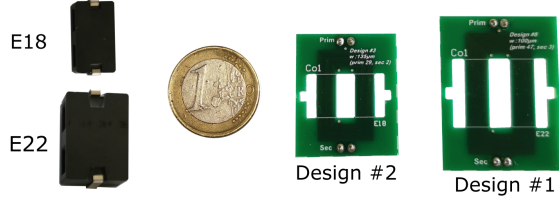


Fig. 5. Photo of selected transformer cores with PCB windings

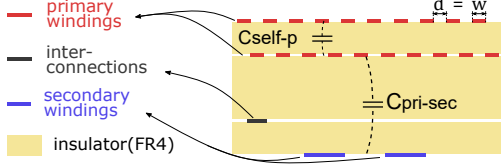


Fig. 6. 2D side-view of transformer's windings arrangements on the PCB layers

IV. DESIGN CONSIDERATIONS

A. Transformer

The use of planar transformers is targeted in the application, as they offer some interesting perspectives for integration (as the winding tracks can be placed on the same board as the rest of the components of the converter). Moreover, they are suitable to operate at high switching frequency due to the limited influence of the skin effects on the winding resistivity. However, they can present large parasitic capacitors in relation to the winding facing areas which must be limited [17], [18].

Two different E-cores are considered to offer two perspectives of the size/efficiency trade-off (E18/4/10R, E22/6/16R). A smaller core (like E14/3.5/5) would lead to large core losses incompatible with the high efficiency target. A larger core (like E32/6/20) could improve the efficiency, but it would considerably increase the converter footprint, thus contradicting with the small-size objective. Both selected cores are based on an E+PLT arrangement. The core material selected is 3F46, that is a soft ferrite (MnZn) with low core losses at the targeted operating frequency [19]. Two examples of transformers built using the two E-cores are shown in Fig. 5.

The transformer windings are distributed into a 4-layer-PCB with FR4 insulator. To reduce the parasitic capacitors between the windings of the transformer, the arrangement of the windings on the PCB layers is adapted with respect to classical design methodology. As shown in Fig. 6, the primary winding is placed on the two top layers while the secondary winding is distributed on one layer at the bottom. The mutual parasitic capacitor $C_{pri-sec}$ is reduced compared to interleaved designs. However, the primary self-capacitor C_{self-p} should also be reduced. The tracks on the two top layers are shifted and their width is chosen equal to the distance between two consecutive tracks ($d = w$). It allows to decrease the overlapping surface and thus to reduce the primary self-capacitance. The characteristics of two transformer designs are presented in Table I. One is built using an E18 core and the other an E22 core. The number of primary turns (N_p) is selected to be quite large to decrease the core losses. But

TABLE I
MAIN CHARACTERISTICS OF TRANSFORMER DESIGNS

Design # & E-core	N_p	N_s	N_{tr}	R_{pri} [Ω]	C_{ps} [pF]	max. L_{mag} [mH]	SRF [MHz]
#1 E22	47	3	15.7	42.7	28	6.7	0.35
#2 E18	29	2	14.5	13.7	17	2.4	1.1

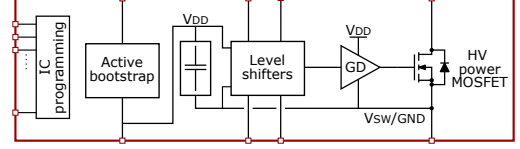


Fig. 7. IC brick with its main functional blocks

it translates into a large resistance of the primary winding, especially for design #1. The design #2 can operate at a frequency higher than design #1, thanks to a lower winding resistance and a smaller total parasitic capacitor.

B. IC brick

As discussed in introduction, a standard high-voltage bulk Silicon process is used to integrate the active components on-chip, to limit the component count and reduce the size of the converter. However, this type of technology presents a significant limitation: HV devices placed on the same die cannot be isolated. In other words, each HV-FET floating at a different voltage level must be placed on a separate die.

To overcome this limitation, an IC brick is designed. It includes one power HV-FET and some circuits useful to control and supply it. Four IC bricks must be inserted and connected together to create the targeted 3L-FC-AHBF. The main functional blocks present inside the IC brick are shown in Fig. 7. One interesting characteristic of the IC brick design is its modularity, as it can be used to create the targeted 3L-FC-AHBF but a simpler 2L-AHBF (with only two switches) could be built using two IC bricks. A higher number of levels could also be reached using more IC bricks (although some aspects of the communication between the IC bricks would need to be refined for these more complex cases).

The integration of four dies into a single package should be possible using System-in-Package (SiP) techniques for example. However, it remains a complex issue and it is not the focus of this study. Here, each IC brick is placed in a separate package and only a limited number of internal blocks are demonstrated here in a first implementation of the 3L-FC-AHBF converter.

The main characteristics of the HV-FET inside the IC brick are measured. The on-resistance is close to 13Ω while the equivalent output capacitor ($C_{oss eq}$ when V_{DS} varies from 0 V to 400 V) is equal to 20 pF. Results are in line with the simulation.

V. EXPERIMENTAL RESULTS

To validate the behavior of the converter and to measure its performances, a prototype of 3L-FC-AHBF is implemented

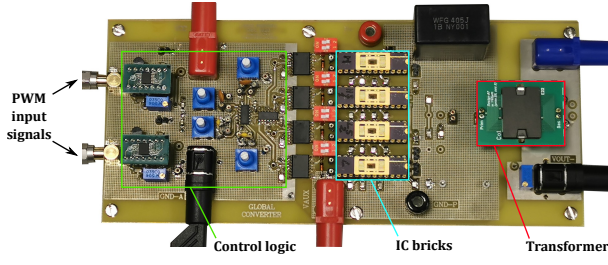


Fig. 8. Converter board

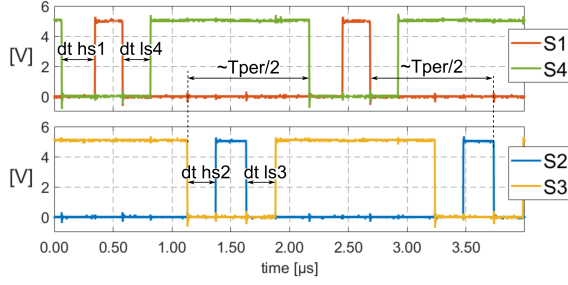


Fig. 9. Control signal waveforms for the 3L-FC-AHBF in Fig. 1

with a 800 V input, a 12 V output and a variable load (1W to 4W). A SMU (Keithley 2410) generates the high input voltage and measures the DC input current. An electronic DC load (BK Precision 8600) sinks a constant output current while measuring the output voltage. A signal generator (Agilent 81130A) is used to generate the PWM signals to control the power switches. The implemented prototype operates here in open loop. The duty-cycle of the high-side switches is set externally to reach the targeted output voltage. The frequency of the control signals is controlled to measure the performances of the converter at different switching frequency (f_{sw} is measured on the transformer). The board in Fig. 8 present a functional prototype that has a volume that is not optimal. The reduction of the converter volume will be studied in the next prototypes, using techniques like System-in-Package (SiP) to integrate the active parts in a small package.

A. Practical implementation

The board is divided into two parts: the power stage and the control circuits. The role of the last one is to generate the signals to drive the four power switches. The power stage is built with four instances of the IC brick, a custom transformer (#1 or #2) and few additional discrete components. Small ceramic capacitors are used, with a high-voltage rating for C_p and C_{fly} (1 μ F, 630 V, X7T) and a low-voltage rating for C_o (1 μ F, 16 V) to limit the output voltage ripple (less than 1% at 500 kHz). A schottky diode D_{sec} is used on the secondary side (PMEG6010CE, NXP) to limit the voltage drop and the parasitic capacitance.

Fig. 9 shows the measured control signals used to drive the four power switches of the 3L-FC-AHBF. The dead-time generated between the on-state of two complementary switches (dt_{hs1} and dt_{hs2} for the high-side switches, dt_{ls3} and dt_{ls4} for the low-side ones) can be externally tuned to match

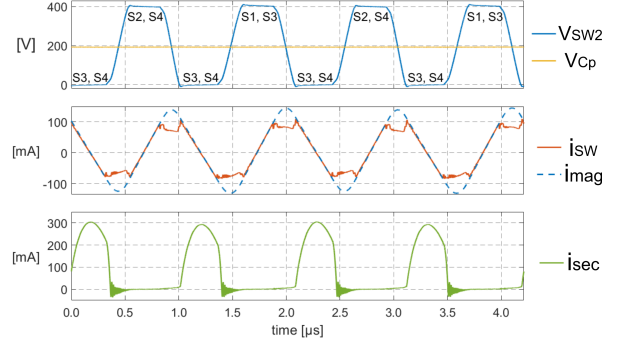


Fig. 10. Measured waveforms in the 3L-FC-AHBF in Fig. 1 with design #2

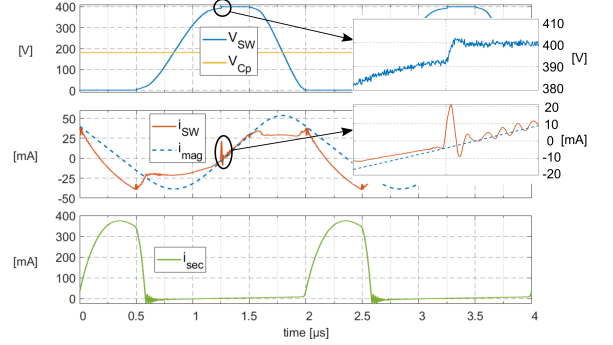


Fig. 11. Measured waveforms in hard-switching mode

the duration of the ZVS transition. The phase-shift between the control signals for the low-side switches is kept close to 180° ($T_{per}/2$) and so is the one between the control signals for the high-side switches.

B. Functional results

The power stage waveforms are shown in Fig. 10. The voltage at the middle switching node (V_{SW2}) and across the primary capacitor (V_{Cp}) are measured and allow to evaluate the voltage across the primary side of the transformer ($V_{pri} = V_{SW2} - V_{Cp}$). The current inside the switching node (i_{SW}) and inside the transformer's secondary (i_{sec}) are also measured. The magnetizing current (i_{mag}) is not directly measured but its waveform is obtained integrating V_{pri} waveform. These waveforms are obtained with a 1 W-load and a switching frequency of 950 kHz (measured on the transformer).

Waveforms in Fig. 10 reveal that the power stage operates in ZVS mode (slow transitions can be noted on V_{SW2}). The voltage across the flying capacitor is naturally close to $V_{in}/2$ (since V_{SW2} high-voltage state is close to $V_{in}/2$ during the two half-periods) thanks to the balanced on-time of the high-side switches and the 180° phase-shift.

C. Limit of the ZVS mode

To explicit the selected operating mode for the power stage (at the limit of the ZVS mode), it is necessary to identify when the converter stops to operate in ZVS mode as in Fig. 11.

Before V_{SW2} reaches its high-voltage state, i_{mag} becomes almost null. Thus the turn-on of the high-side switch forces

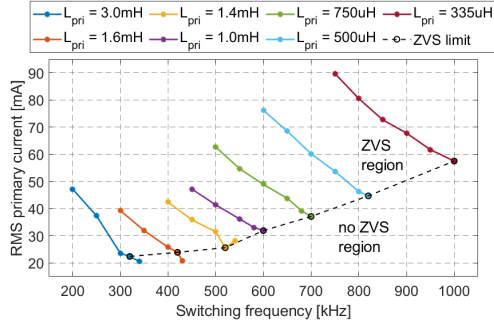


Fig. 12. $RMS(i_{sw})$ vs f_{sw} for different L_{pri} values

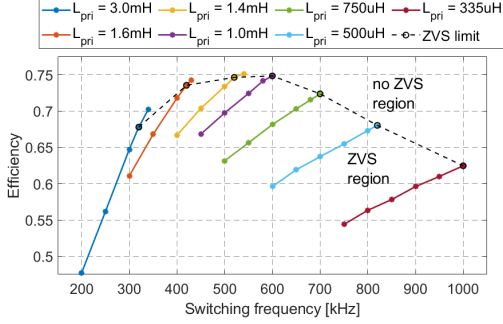


Fig. 13. Efficiency vs f_{sw} for different L_{pri}

the switching node V_{SW2} to $V_{in}/2$, generating a voltage step and a current spike, as shown in the zoomed portion in Fig. 11.

The limit of the ZVS operating mode is identified for a given transformer design but for several values of the primary inductance (the value of L_{pri} can be set by changing the value of the air-gap added to the magnetic path). For each value of L_{pri} , the switching frequency is gradually increased and for each operating point, the RMS value of i_{sw} and the efficiency are measured. The maximum frequency that allows the power stage to operate in ZVS mode defines the ZVS limit. Results are plotted in Fig. 12 for the current and in Fig. 13 for the efficiency.

The results reveal the importance of operating close to the limit of the ZVS mode to reduce the current ripple and to improve the converter efficiency. Although the efficiency could be further increased operating at a frequency slightly above the ZVS limit, it was decided to not sacrifice the ZVS mode as it could translate into poorer performances of the power stage on other aspects, as electromagnetic pollution. The results also confirm the link between the frequency, the primary inductance and the magnetizing current as predicted previously in Fig. 4: the higher f_{sw} , the lower L_{pri} and the larger i_{mag} (and i_{sw}) to remain at the limit of the ZVS mode.

D. Efficiency

The efficiency of the 3L-FC-AHBF in Fig. 1 operating at $V_{in} = 800$ V, $V_{out} = 12$ V and $P_{out} = 1$ W is measured for both transformer designs (detailed in Table I) on a wide frequency range. The results plotted in Fig. 14 are measured at the limit of the ZVS mode as explained previously.

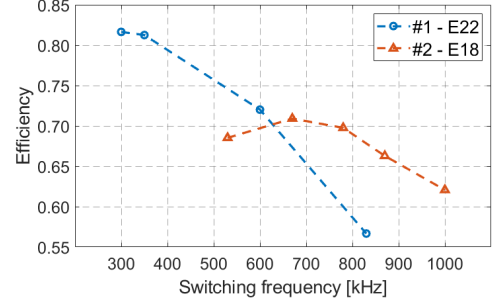


Fig. 14. Efficiency vs f_{sw} for two transformer designs

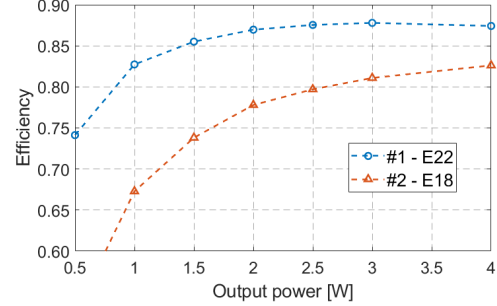


Fig. 15. Efficiency vs P_{out} for two transformer designs

Depending on the transformer design, the optimal operating frequency changes significantly. For the transformer design #1, the optimal operating frequency is close to 300 kHz ($\eta_{peak} = 81.7\%$) whereas for the transformer design #2, it is around 675 kHz ($\eta_{peak} = 70.9\%$). The different optimal frequencies can be explained by the different number of turns of the transformer. Due to the high volt-second product applied to the transformer, designs with a lower number of turns (like #2) may operate at a high frequency to limit the flux density inside the magnetic core. However, designs with a high number of turns (like #1) present a significant efficiency drop at high frequency, that is due to the high resistance of the winding. The optimal operating frequency thus largely depends on the number of turns. The highest efficiency is reached for design #1 when operating at low frequency (about 300 kHz), which might be related to additional losses occurring at high switching frequency that lower performances of design #2.

The efficiency of the converter is measured for different load conditions ($P_{out} \leq 4$ W, Fig. 15). The efficiency of the converter significantly increases when the output power rises. It confirms the majority of the losses are load-independent (essentially core losses and conduction losses in the primary side of the transformer). The results also reveal the interest of advanced control techniques that could allow to increase the efficiency at light-load, like burst mode or similar techniques [7].

E. Comparison with existing solutions

The performances of the 3L-FC-AHBF in Fig. 1 are compared to some existing solutions in Table II. The comparison reveals the proposed solution presents an increased efficiency

TABLE II
COMPARISON WITH EXISTING SOLUTIONS

	This work		Literature	Market references	
Parameters ▼	#1	#2	[8]	Cui Inc. ⁴	TI ⁵
V_{in} [V]	600-1000		1.2k-1.8k	100-1000	400-860
V_{out} [V]	12		24	5	16.5
P_{out} [W]	1-4		16	5	8
Transformer					
- Core ref.	E22	E18	EE35		
- Footprint ¹	34x26	27x22	35x35		18x17
Module size ^{1,2}	38x29	33x25		70x48	
Efficiency	87.4%	82.6%	60%	70%	68%
(at V_{in})	(800V)	(800V)	(1.2kV)	(800V)	(600V)
f_{sw} [kHz]	360	900	50	<75	60
Topology	3L-FC-AHBF		ISMO ³	Flyback	Flyback

¹: All dimensions are in mm; ²: Size estimation based on the sum of the main components footprint; ³: Input Series Multiple Outputs; ⁴: product reference AE5-EW; ⁵: reference design PMP7769

from 70% with existing solutions up to 82.6% for the transformer design #2 and even 87.4% for design #1.

The larger footprint of the planar transformer compared to the one from Texas Instruments' reference design (PMP7769) is due to the large area occupied by the rectangular windings. A different core shape could be selected to lower the total footprint (like EQ core). Nevertheless, the footprint of the transformer in the proposed solution is compensated by the smaller height of this device, that leads to low-profile solutions. Moreover, the higher operating frequency of the converter could translate into smaller filtering components at the input and the output.

The total footprint of a module built with the proposed solutions is estimated, adding the footprint of the main components of the converter (transformer, IC bricks, C_{fly} , C_p , C_o , D_{sec}). The total footprint of the IC bricks assumes they are grouped inside a larger package (e.g. PG-DSO-36-58 package). The size of the module footprint can be compared to the one of product from Cui Inc and the proposed solution clearly allows to improve the size-performance trade-off.

VI. CONCLUSION

Several challenges appear when designing a HVLP converter in a perspective of small size, high efficiency and low-cost. A high switching frequency is targeted and planar technology is used to fabricate the transformer. The active parts are integrated on-chip using a HV bulk Silicon process. The selected topology is the 3L-FC-AHBF, of which behavior and main waveforms were quickly presented. Experimental waveforms agree with the simulation evaluation. The converter is designed to operate at the limit of the ZVS mode, to enhance the efficiency as confirmed by the results on a 800V-to-12V prototype (4 W). The efficiency measured for the two transformer designs show an improvement compared to the state-of-the-art. This validates the interest of the proposed approach to create high-voltage low-power converters in a low-cost perspective.

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