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# Design of high-to-low voltage, low-power integrated isolated DC/DC converters for automotive applications

Design of high-to-low voltage, low-power integrated isolated DC/DC converters for automotive applications, Etienne Foray, Christian Martin, Bruno Allard, Univ Lyon, INSA Lyon, Université Claude Bernard Lyon 1, Ecole Centrale de Lyon, CNRS, Ampère, UMR5005, 69621 Villeurbanne, France

## Abstract

High-to-low voltage, low-power isolated DC/DC converters with strong requirements on size, cost and efficiency are required for some specific applications. The existing solutions with the same power/input-voltage ranges are usually based on the Flyback architecture and yield low performances. To overcome these limitations, this work summarizes an approach to design such converter, going through several aspects of the converter design such as the topology, the transformer and an integrated circuit. The experimental setup allows to verify the converter functionality. The peak efficiency measured for a 4W-prototype is 84% in the case of an 400V-12V converter and 82% for an 800V-12V one.

## 1 Introduction

In several applications, high voltage DC buses are used, like EV that uses 400V or 800V batteries. At the same time, it could be interesting to supply tiny systems (sensors or little actuators like a pyroswitch) directly from the HV battery, to enhance robustness or reduce the number of DC buses. In this regard, an isolated converter is required with a high input voltage capability and a low-voltage, low-power output. The constraints on the converter in the automotive context relates to the size, the cost and the efficiency of the solution.

### 1.1 Context

#### 1.1.1 Limits of the existing solutions

Some solutions that could be used to create such a converter can be found in the literature or on the market (existing products or reference designs). In [1], [2] or [3] the maximum input voltage is limited to 400/500 V and the efficiency is generally lower than 80%. A product from Cui Inc. (AE5-EW - [4]) and a reference design from Texas Instruments (PMP7769 - [5]) can support an 800V input voltage, but the efficiency at this voltage is lower than 75% with a load close to 5W. Most of these solutions are based on a Flyback topology, that is interesting because it is very simple but that also presents some serious limitations in terms of performances.

#### 1.1.2 Challenges linked to HVLP converters

Since the High-Voltage Low-Power (HVLP) isolated converters are not common, it is important to underline the challenges related to the design of this type of converter, in particular in a context where high efficiency, low cost and small size are important.

Because of the low output power targeted for the converter ( $< 5$  W), the main issue will come from the no-load losses. In particular, the losses inside the magnetic core of the transformer increase with the voltage applied to the

transformer winding. The switching losses generated when a power switch is turned-on or turned-off must be reduced as well, because they are proportional to the square of the voltage across the switch. Another challenge is related to the size of the transformer, required to ensure a galvanic isolation between the input and the output of the converter. For this component, a trade-off between size and performances is expected, which may contradict with the small-size and high efficiency targets.

### 1.2 Proposed approach and objectives

The approach proposed here to create HVLP converter focuses on three different aspects: high operating frequency ( $>150$ kHz are targeted), use of a low-cost HV silicon process (a standard 600V BCD technology with a limited number of masks to reduce costs) and small passive components (ceramic capacitor with a 5x5mm footprint are used while the transformer footprint reduction is one key design parameters). A short summary of the converter specifications is presented in **Table 1**.

**Table 1 – General specifications of the converter**

Parameter	Value	
Input voltage [V]	400	800
Output voltage [V]	12	
Output power [W]	1-4	
Efficiency	$>80\%$	
Isolation	Required	

The objectives of this article are to present the developments related to the selected approach. The topology used to create the targeted converters is presented, its behavior and the operating mode are presented. Then, the design considerations related to an IC brick used to integrate all the power-stage actives components are discussed. The main design choices made to create a custom planar transformer are also presented. Finally, the board used to test the converter is shown. Experimental results consist in

validating the converter operating mode and measure the efficiency in soft switching conditions.

## 2 Selected topology

### 2.1 Topology exploration

Most low-power DC-DC converters use a Flyback architecture, that has some serious limitations because of the high voltage stress applied to the transformer and the switch. A high voltage stress on these components will translate into large losses and will force to use complex/bulky components.

To find an alternative to the Flyback architecture, a topology exploration was performed. Few criteria were selected: the reduction in voltage stress on the switches and in the volt-second applied to the transformer, the number of switches and other passive components, the possibility to operate in ZVS conditions. Several architectures were analyzed: switched-capacitor stages [6], Input-Series converters [7], hybrid converters [8]. In the end, the Multi-Level Flying-Capacitor (ML-FC) topology was selected because it offers a good trade-off between the complexity and expected performances of the power stage.

The ML-FC structure (that simply consist in the power switches and the flying capacitor) is connected to a transformer connected like in an Asymmetrical Half-Bridge Flyback (AHBF), that is a topology similar to an isolated Buck.

### 2.2 Selected versions of the topology

To meet the two specifications for the input voltage shown in **Table 1**, it was decided to use two different versions of the selected topology (ML-FC-AHBF). This choice enables a “modular” approach since several components of the power stage can be design for both versions (like the transformer).

For the 400V design, a simple 2L-AHBF topology (shown in **Figure 1**) is used (note that this is the “classical” architecture of the AHBF topology). This version does not reduce the voltage stress on the switches but it is acceptable since the input voltage is lower than the voltage rating of the HV Si-FETs used.

The 3L-FC AHBF shown in **Figure 3** is used for the 800V design. It allows to use power switches with a rating that is lower than the input voltage considered (Si-FETs can usually support up to 600V). It also reduces the amplitude of the voltage excitation on the transformer and thus to decrease the associated core losses.

### 2.3 Converters main operating mode

To simplify the analysis of the 2L-AHBF and 3L-FC-AHBF topologies, a few hypotheses are being made. Note that the analysis of the 2L-AHBF topology was already

detailed in some past work with similar hypotheses [9] [10] but with a larger output power. Simplifying hypotheses are:

- Primary capacitance ( $C_p$ ) value is big enough to consider that its voltage is constant over a switching period.  $V_{Cp}$  is supposed to be equal to the average output voltage referred to the primary side.
- Primary-secondary parasitic capacitor ( $C_{ps}$ ) value is constant and entirely referred to the primary side.
- The value of the leakage inductance ( $L_k$ ) is small in comparison with the value of the magnetizing inductance ( $L_{mag}$ ).
- For the 3L-FC-AHBF, the voltage across the flying capacitor ( $V_{fly}$ ) is supposed constant and equal to its ideal value, that is  $V_{in}/2$ .

#### 2.3.1 Analysis of 2L-AHBF switching waveforms

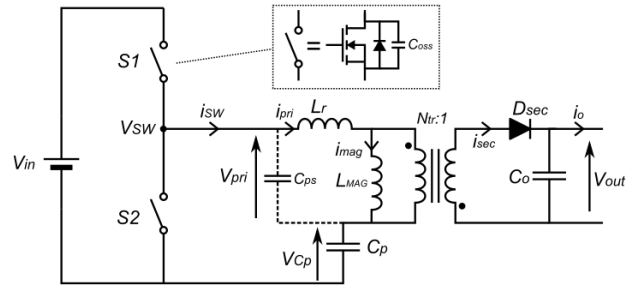


Figure 1 - 2L-AHBF schematic

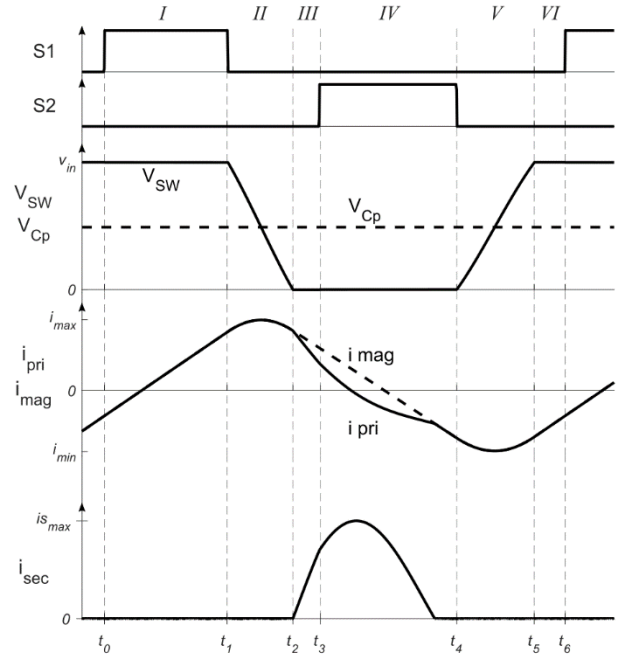


Figure 2 - 2L-AHBF simulation waveforms

As illustrated in **Figure 2**, a switching period of the 2L-AHBF can be divided into 6 modes. In mode I, the power switch  $S1$  is ON and the switching node  $V_{SW}$  is forced to  $V_{in}$ . The primary current rises linearly due to the positive voltage ( $V_{pri} = V_{SW} - V_{Cp}$ ) applied to the transformer primary. In mode II, both power switches are off. The magnetizing current is used to (dis)charge the parasitic capacitors connected to the switching node such that  $V_{SW}$  goes

from  $V_{in}$  to 0V. In mode III, just before  $S_2$  is turned-on, its body-diode already conducts a current and  $V_{SW}$  is forced to ground. A negative voltage is applied to the primary side of the transformer that translates into a positive voltage on the secondary side. The secondary diode  $D_{sec}$  is forward biased and a current can thus flow in the secondary winding ( $i_{sec}$ ). In mode IV, the switch  $S_2$  is turned-on but it does not affect the general aspect of the waveforms. At the beginning of mode V,  $S_2$  is turned-off. It initiates a new transition for  $V_{SW}$ , that changes from 0V to  $V_{in}$  due to the magnetizing current. In mode VI, just before  $S_1$  is turned-on its body-diode already conducts a current and the waveforms are the same as in mode I. When  $S_1$  turns-on, a new period starts.

### 2.3.2 Analysis of 3L-FC-AHBF switching waveforms

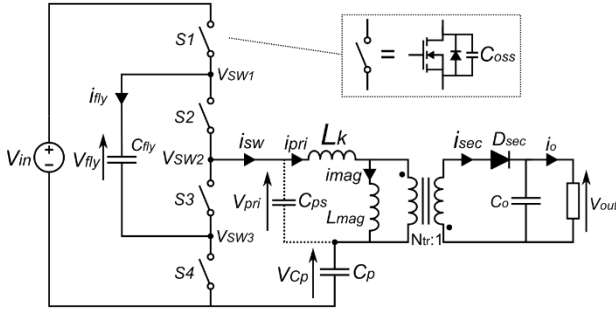


Figure 3 - 3L-FC-AHBF schematic

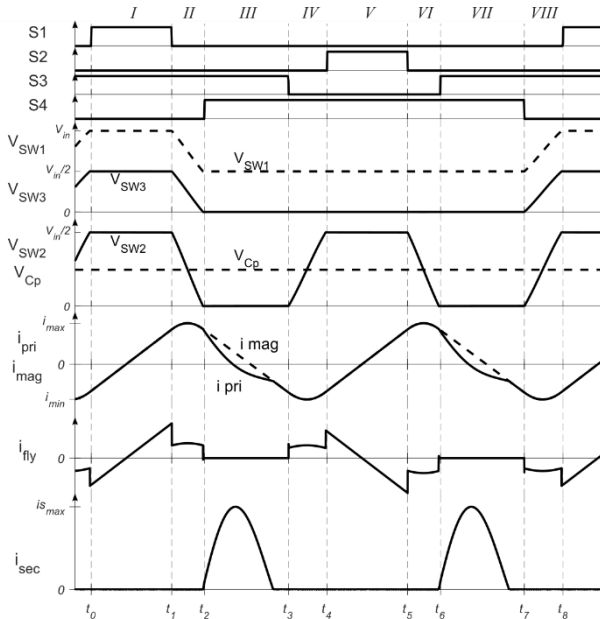


Figure 4 - 3L-FC-AHBF simulation waveforms

The switching period of the 3L-FC-AHBF (Figure 3) can be divided in 8 modes as illustrated in Figure 4 that shows the waveforms for this version of the topology. Moreover, it can be noticed that a switching period can be divided in two half-periods with very similar waveforms, such that the similar modes can be analysed together.

In mode I and IV, one high-side switch and its non-complementary low-side switch are ON ( $S_1/S_3$  in mode I,  $S_2/S_4$  in mode IV). It forces a  $V_{in}/2$  voltage on the middle

switching node  $V_{SW2}$  and the primary current rises linearly. In mode I, the primary current and the flying capacitor current are equals but in mode IV they flow in opposite directions. In mode II and V, a transition is observed on the middle switching node  $V_{SW2}$ . It travels from  $V_{in}/2$  down to 0V because of the magnetizing current. When  $V_{SW2}$  reaches 0V, the other low-side switch turns-on such that both  $S_3$  and  $S_4$  are ON in modes III and VII. A negative voltage is forced on the primary of the transformer ( $V_{pri} = -V_{Cp}$ ) and a current flows on the secondary side. In modes IV and VIII, one of the low-side switches turns-off ( $S_3$  in mode VI,  $S_4$  in mode VIII).  $V_{SW2}$  initiates a new ZVS transition. The parasitic capacitors connected to the various switching nodes are (dis)charged thanks to the magnetizing current. At the end of the transition,  $V_{SW2}$  reaches  $V_{in}/2$  and the other high side switch turns-on.

### 2.3.3 General operating modes

From the analysis of the 2L-AHBF and 3L-FC-AHBF, both versions enable a ZVS mode for all the power switches. It allows to greatly decrease the switching losses. The value of the output voltage is set through the voltage across the capacitor  $C_p$  and the transformer turns ratio  $N_{tr}$ . An expression that links the input and the output voltages of the converter is:

$$V_{out} \approx \frac{V_{in}}{N_{tr}} \times \frac{t_{onHS} + 0.5 \sum dt}{T} - V_D$$

Where  $t_{onHS}$  is the on-time of the high-side switch(es),  $\sum dt$  is the sum of the dead-times associated to the various ZVS transitions,  $T$  is the period of the converter and  $V_D$  is the voltage drop of the secondary diode  $D_{sec}$ . The formula is valid for both versions of the topology.

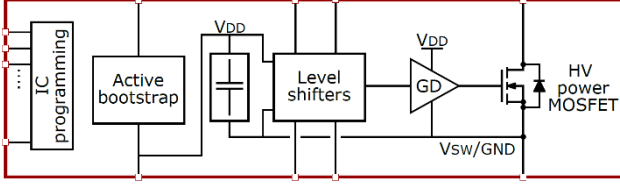
## 3 IC brick

To stay in line with the low cost constraint, a high-voltage bulk Silicon technology is used to integrate the active components of the power stage. Although a HV Si-MOSFET may be less performant than a GaN or SiC device, it could be sufficient in a low power context where the currents that the switches conduct are low [11].

However, these HV bulk Silicon technologies have some limitations, particularly in terms of isolation. With this process, it is not possible to isolate floating HV devices because it is not possible for two switches built in the same substrate to float at different voltages. This is because the "isolation strength" of the process is already used to create the high-voltage devices that can withstand a 600 V drain-source voltage. Thus each power switch composing the 3L-FC-AHBF or the 2L-AHBF topologies must be placed on an isolated die.

To get around this limitation, it was decided to create an IC brick, i.e. a custom chip that contains one HV power switch and all the circuits required to supply/control it. A block-view of the main circuits included in the IC brick is shown

in **Figure 5**. The concept of IC brick is also interesting to create the two versions of the power-stage 2L-AHBF and 3L-FC-AHBF. Thanks to the modularity of the design, two or four IC bricks can be connected to create the targeted version of the topology.



**Figure 5** - IC brick block-view

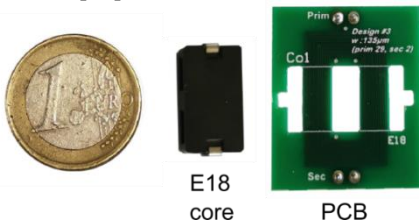
The power switch integrated in the IC brick is a custom FET that is made small enough to ensure low parasitic capacitors ( $C_{oss} \sim 20$  pF) although it translates into a large on-resistance ( $R_{on} \sim 13 \Omega$ ).

In this first prototype, converter volume is not optimized since it is only a functional prototype. Each IC brick is placed in an individual package. In next steps, the use of Multi-Chip Modules (MCM) or System-in-Package (SiP) techniques could be investigated to integrate all the two/four IC bricks in a single package. In a first step, only a few circuits of the IC brick (power-switch and the associated gate-driver) are used to create the power-stage, because the objective of the present prototype is to validate the converter functionality and performances. Note that no particular design effort were made to ease the start-up phase. This point will need to be addressed in the next IC designs to allow the converter to start properly and to ensure a proper voltage sharing among the MOSFETs connected in series.

## 4 Transformer

### 4.1 Early design choices

The planar technology is selected to create the transformer because it allows to reach high operating frequency and because it can enhance the integration since the windings of the transformer can be drawn on the same PCB where the other components of the converter are placed. The planar transformers can however also present large parasitic capacitors [12].



**Figure 6** - Planar transformer core and PCB

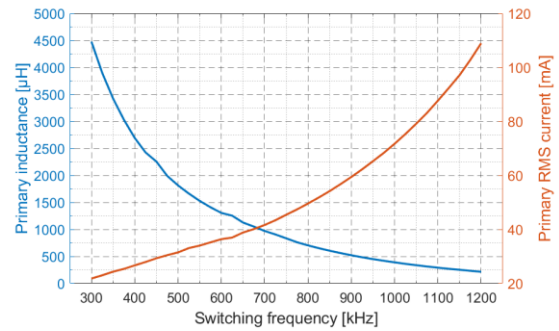
As discussed in the Introduction, the design of the transformer relies on a trade-off between the size and the performances. To maintain the size of transformer limited a small E+PLT core size is selected (E18/4/10R). The E18 magnetic core along with the PCB where the transformer windings are drawn are shown in **Figure 6**.

To enhance the performances, the windings placement on the PCB layers is studied. The arrangement allows to place a high number of turns for the primary winding on two layers while maintain low the various parasitic capacitors (the mutual and the self capacitances) by keeping the primary and secondary windings apart.

### 4.2 Critical design parameters

The number of turns is a key design parameter. It influences both the core and the conduction losses of the transformer, which are the dominant losses in a HVLP context. The optimal number of turns for the primary winding is the one that allows to minimize the sum of the core and conduction losses. This optimal number of turns, that also depends on the operating frequency, is evaluated in this case to be  $N_p = 29$  for a frequency close to 1 MHz. The number of turns of the secondary winding is selected  $N_s = 2$  in order to maintain a turns ratio close to 15 because it allows to reduce to the minimum the amount of current circulating in the primary side of the transformer as discussed in [13].

Finally, the value of the magnetizing inductance is selected such as to ensure a minimum primary current ripple while keeping the converter in Zero Voltage Switching (ZVS) mode. Since the optimal value of magnetizing inductance depends on the operating frequency, a small MatLab routine is used to compute it (it takes into account the various parasitic capacitors in the power stage and the maximum dead-time left to operate the ZVS transition). It is interesting to notice that the optimal  $L_{mag}$  value computed for the two versions of the converter is the same, since the voltage/currents waveforms applied to the transformer are the same. The optimal  $L_{mag}$  value and the associated RMS primary current are shown in **Figure 7** for an operating frequency range between 300 kHz and 1200 kHz.



**Figure 7** - Optimal  $L_{mag}$  and RMS  $i_{pri}$  vs frequency

## 5 Experimental measurements

### 5.1 Converter board

The board used to implement a first prototype of the targeted converter is shown in **Figure 8**. It is divided in two parts: one portion generates the signal controlling the power switches (“control”), to set the dead-times to the suitable value. The other portion is the power stage itself, that is composed of the IC bricks, the custom transformer and few other passive components. The main components used in this portion are listed in **Table 2**. The board can be

used to test the two targeted versions of the topology (2L-AHBF and 3L-FC-AHBF).

A Source Measure Unit (Keithley 2410) generates the high input voltage and measures the DC input current. An electronic DC load (BK Precision 8600) sinks a constant output voltage while measuring the output voltage. A signal generator (Agilent 81130A) is used to generate the PWM signals to control the power switches.

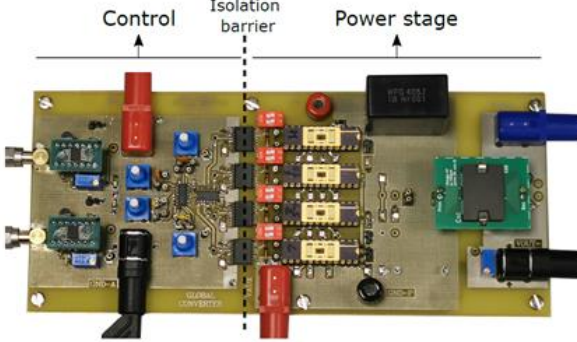


Figure 8 - Converter Printed Circuit Board

Table 2 - Components list

Component	Reference	Characteristics
Digital isolator	ISO7710	
Secondary diode $D_{sec}$	PMEG6010CE	Schottky, 60 V, 1 A
Primary cap. $C_p$	CKG57NX7T2J105	1 $\mu$ F, 630 V, X7T
Flying cap. $C_{fly}$		
Output capacitor $C_{out}$		1 $\mu$ F, 16 V
Custom FET $S1...S4$		600 V, 13 $\Omega$ , 20 pF
Custom transformer		14.5:1, 350 $\mu$ H

## 5.2 Validation of converter behavior

The waveforms measured for the 2L-AHBF topology with  $V_{in} = 400$  V,  $V_{out} = 12$  V,  $P_{out} = 1$  W and  $f_{sw} = 1$  MHz are plotted in **Figure 9**. The measurements for the 3L-FC-AHBF with  $V_{in} = 800$  V and  $f_{sw} = 475$  kHz are plotted in **Figure 10**.

Both versions have very similar switching waveforms. In particular, the transformer voltage and current are almost identical. The ZVS mode is observed in both cases, as revealed by the slow transitions of the switching nodes ( $V_{SW}$  for 2L-AHBF and  $V_{SW2}$  for the 3L-FC-AHBF). For the 3L-FC-AHBF topology, the high voltage reached at the middle switching node  $V_{SW2}$  is very similar during the two half-periods. It means the flying capacitor voltage  $V_{fly}$  is very close to 400V (or  $V_{in}/2$ ) that is its ideal value, even though the converter operates in open loop. Note that the shape of the current flowing through the switches ( $i_{SW}$ ) is not the same as the current flowing through the primary of the transformer ( $i_{PRI}$ ) that was shown in **Figure 2** and **Figure 4**. This is due to the parasitic capacitor of the transformer ( $C_{ps}$  in **Figure 1** and **Figure 3**) that takes a portion of the primary current during the ZVS transitions. It explains why  $i_{SW}$  is lower than  $i_{MAG}$  during the ZVS transitions on the measured waveforms.

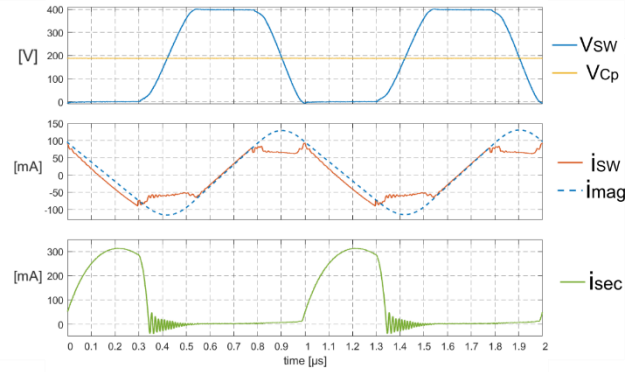


Figure 9 - 2L-AHBF measured waveforms

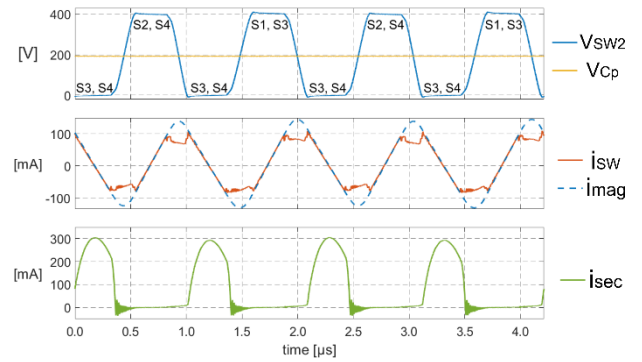


Figure 10 - 3L-FC-AHBF measured waveforms

## 5.3 Efficiency

The efficiency is measured for both versions of the converter, with a load between 0.5 W and 4 W. The evolution of the efficiency with the output power is shown for the 400V converter using the 2L-AHBF topology and the 800V converter based on the 3L-FC-AHBF configuration in **Figure 11**.

The peak efficiency is higher than 80% at 4W for both versions ( $\eta_{peak} = 84\%$  at 400V and  $\eta_{peak} = 83\%$  at 800V). The evolution of the efficiency with the output power confirms that the no-load losses are the main obstacle to create a solution with high efficiency.

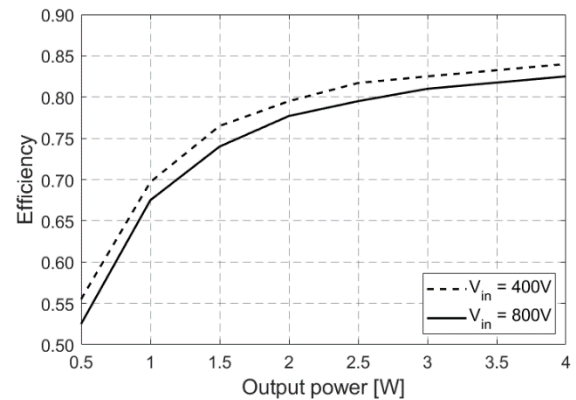


Figure 11 - Efficiency vs Pout for 400V & 800V converter

As expected from the similar waveforms of the 2L-AHBF and the 3L-FC-AHBF, the performances of both versions are very close. The difference in the measured efficiency is

due to the additional switches that compose the 3L-FC-AHBF that generate extra conduction losses.

Comparing the efficiency obtained with our solution to the existing products/papers, it appears that the selected approach allows to improve the efficiency, in particular for the 800V converter (for which existing solutions have an efficiency close to 70%). Although it is not easy to determine with accuracy the losses distribution among the power stage components, several reasons can explain the efficiency improvement. First, the selected topology enables a great reduction in the volt-second applied to the transformer, leading to lower core losses. The voltage amplitude is reduced compared to Flyback and the converter operating frequency is much higher thanks to the ZVS mode (over 900 kHz here while existing solutions are below 150 kHz). The study done for the transformer design also helps improving the efficiency, as this component is usually the main source of losses of the converter.

## 6 Conclusion

Isolated high-voltage low-power converters are required in some applications like in EV. Their design is not straightforward, due to no-load losses and the low-cost/small-size constraints. The existing solutions are based on the Flyback architecture but it limits their performances such that the maximum  $V_{in}$  or the efficiency are not good enough. An alternative topology was proposed: the ML-FC-AHBF. Two versions of this topology are used to meet the 400V and the 800V converter specifications. The operating mode of the two versions was briefly analysed. The design considerations of a planar transformer were presented. The targeted process used to integrate the active parts (HV bulk Silicon) was described along with its limitations. The IC brick designed to come around these limits was introduced. A prototype of the converter was created and measured. Measured waveforms validated the converter behavior. The efficiency measurements showed an improvement compared to state-of-art solutions, thanks to the reduce impact of no-load losses.

In the next steps, the converter size should be further optimized by using MCM or SiP techniques to reduce the space occupied by the active parts. Other performances of the converter like EMC/EMI should also be measured as they are among the crucial parameters in the targeted context. From the authors' perspective, there are mainly two limits for industrialization: the monolithic integration of several ICs, required to reach the targeted integration level, and the reliability of the proposed architecture based on a Multi-Level Flying-Capacitor (ML-FC). If these two points are addressed, then industrialization may become possible and could benefit from this low-cost small-size solution for HVLP converters.

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