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Front and back channels coupling and transport on 28 nm FD-SOI MOSFETs down to liquid-He temperature

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Abstract—28 nm FD-SOI technology is electrically characterized aiming at cryogenic applications. Electrostatics and transport are evaluated and compared while lowering temperature from 300 K down to 4.2 K. Split CV technique is applied in both long and short channel transistors thanks to multiple parallel structures designed to increase the gate area. FD-SOI versatility is shown over a wide temperature range of operation, as the back gate tuning efficiency is preserved at low temperatures. Insights on back gate bias behavior at room and low temperatures are obtained and the electrostatic coupling between front and back channels can be successfully modelled by using 1D Poisson-Schrödinger calculation from 300 K down to 4.2 K. A generic form of empirical models for the effective mobility is found to be useful for cryogenic operation, since the phonon scattering contribution presents strong temperature dependence. While long channel MOSFETs exhibit strong mobility improvement, short channel transistors show lower mobility gain with temperature reduction.

Keywords— FD-SOI, cryogenic applications, electrostatics, transport, back bias

I. INTRODUCTION

Since the 80's, the CMOS technology has been showing its advantages in cryogenic environments [1], [2], targeting a wide range of temperature applications, such as high performance computing, high energy physics, and the space field [3]–[5]. Researches on low-frequency noise and device modeling of MOSFETs operating at liquid-nitrogen (77 K) and liquid-helium (4 K) temperatures were already available in 1989 [6], [7]. Recently, the interest of operating CMOS circuits at deep cryogenic temperatures has been significantly boosted due to its applicability to control and read-out circuitry for quantum computers [8]–[10].

In this context, Fully-Depleted Silicon-On-Insulator (FD-SOI) technology appears as a valuable solution for the co-integration of qubits and control electronics [11]–[15]. 28 nm FD-SOI MOSFETs in particular have shown great performance down to 4.2 K [16], [17]. The threshold voltage (V_{TH}) high tunability of ultra-thin body and buried oxide (UTBB) MOS transistors, which is kept below 1 K, is pointed as one of the key advantages of the technology for performance optimization and circuits design at low temperature [18], [19]. Because of this, the study of the back bias (V_B) influence, and therefore the front and back channels coupling, is of high importance. So far however, these aspects have not being deeply explored in advanced FD-SOI CMOS for cryogenic operation [20], [21]. Although [22] presented

an analysis of back bias effects of 28 nm FD-SOI MOSFETs down to 4.2 K, only long channel transistors were evaluated, and mainly focusing on the electrostatics behavior.

Aiming to fill the gap of available studies in literature, in this work we extend the results presented in [22], by performing additional extensive electrical characterization down to 4.2K. This time we focus not only on long channel transistors, but also in short channel MOSFETs. The effective carrier mobility (μ_{eff}) extracted from split C-V methodology is evaluated for short and long channel FD-SOI transistors for the first time, at deep cryogenic temperatures, in particular accounting for the V_B effect.

The paper is organized as follows: Section II details the devices characteristics (Section II-A) and their overall performance down to 4.2 K (Section II-B). Section III presents the study on the electrostatics and front/back channels coupling by means of gate-to-channel capacitance (C_{GC}) curves, for long (Section III-A) and short channel (Section III-B) MOSFETs. Section IV presents results on transport parameters for long (Section IV-A) and short channel (Section IV-B) MOSFETs. Finally, Section V points out the main conclusions of this work.

II. 28 NM FD-SOI MOSFETS

A. Devices Characteristics

The measurements were performed on 28 nm FD-SOI MOSFETs with Silicon thickness of 7 nm and a buried oxide thickness of 25 nm [23]. N-type and PMOS transistors are processed from (100) handle substrate, with $\langle 100 \rangle$ -oriented channel, and high-k/metal gate (HKMG) Gate-First architecture, using the standard process. Long ($L \geq 1\mu\text{m}$) and short ($L = 28\text{ nm}$) channel MOSFETs were characterized in this work, using a manual cryogenic probe station, from 300 K down to 4.2 K. For the long channel transistors, both thin (GO1, with effective oxide thickness, EOT, of 1.1 nm) and thick (GO2, with EOT = 3.2 nm) front gate oxide devices were analyzed.

Regular (RVT) and low (LVT) threshold voltage (V_{TH}) transistors were obtained with a doped back plane (N-well or P-well, with typical doping concentration in the order of 10^{18} cm^{-3}) below the buried oxide. Figure 1 shows schematics of the studied structures, where RVT MOSFETs were designed to allow reverse back biasing (RBB), whereas LVT MOSFETs allow forward back biasing (FBB).

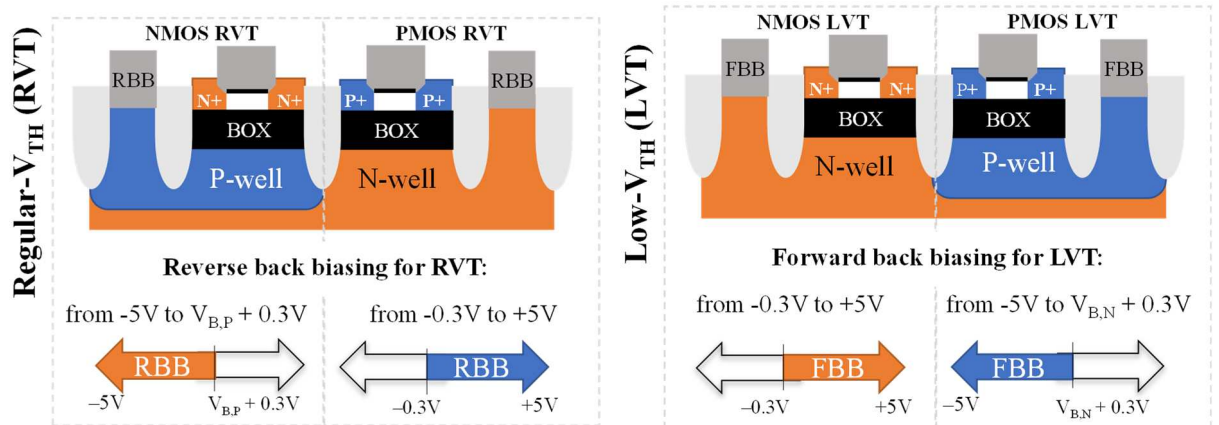


Figure 1. Schematics of 28 nm FD-SOI N- and PMOSFETs with regular (RVT) and low (LVT) threshold voltage flavors. $V_{B,P}$ and $V_{B,N}$ indicate the back bias voltages applied at the PMOS RVT and at the NMOS LVT, respectively.

B. FD-SOI performance at cryogenic temperatures

Figure. 2 shows the drain current (I_{DS}) normalized by the channel width (W) as a function of the front gate voltage (V_{GS}), at 300 K and 4.2 K, and at low drain bias ($V_{\text{DS}} = 50\text{ mV}$). At $V_B = 0\text{ V}$, in linear scale, the arrows indicate

both the threshold voltage and the ON-state current increase with temperature lowering, which leads to the curves crossing at the voltage point known as ZTC (zero temperature coefficient). In logarithmic scale, the arrow indicates the high improvement in performance considering both subthreshold slope (SS) and OFF-state current (I_{OFF}) decrease achieved at cryogenic temperatures. By forward back biasing the transistor with $V_B = 2$ V, at low temperature, the $I_{DS}(V_{GS})$ characteristics can be shifted in order to obtain the same V_{TH} as at 300 K, while the benefits of improved SS, I_{ON} and I_{OFF} are kept.

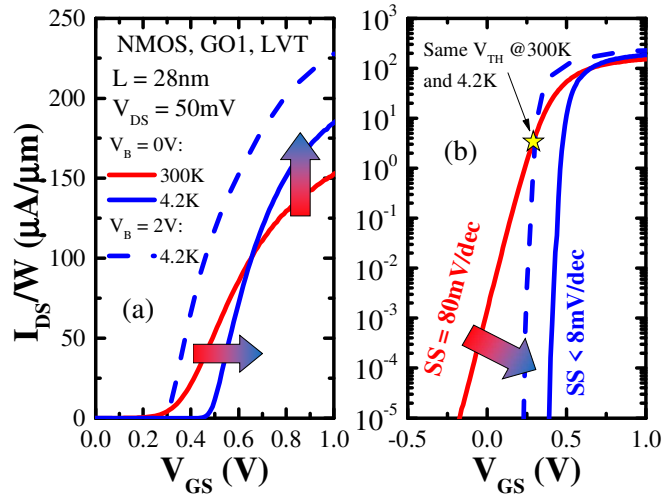


Figure. 2. Normalized drain current as a function of the front gate voltage in linear (a) and logarithmic (b) scales. Short channel NMOS GO1 LVT at 300 K ($V_B = 0$ V) and 4.2 K ($V_B = 0$ V and 2 V), at $V_{DS} = 50$ mV. The subthreshold slope is indicated for each temperature condition.

Figure. 3 presents SS as a function of T for GO1 and GO2 NMOS. The subthreshold slope values were extracted from $\partial V_{GS} / \partial \log(I_{DS})$ curves at $I_{DS} = 500$ pA. From room temperature down to 4.2 K, SS improves about one order of magnitude. As observed in Figure. 2, thanks to this subthreshold slope decrease with T lowering, I_{OFF} is reduced by several orders of magnitude. In fact, I_{OFF} is found to be below the equipment accuracy (< 1 fA). Moreover, it is possible to observe that SS follows a linear dependence with T, according to the theoretical limit trend, down to around 30 K, for both GO1 and GO2 devices. The subthreshold slope saturation below 30 K is explained by a broadened tail in the density of states at the band edges, as discussed in [24], [25]. At higher T, the deviation of SS from the theoretical limit is due to short channel effects, since $SS = \ln(10) \cdot k \cdot T / q$ is only valid for long channel transistors. Higher SS is found for short channel GO2 in comparison to GO1, as expected due to the thicker front gate oxide and smaller gate control over the charges in the channel.

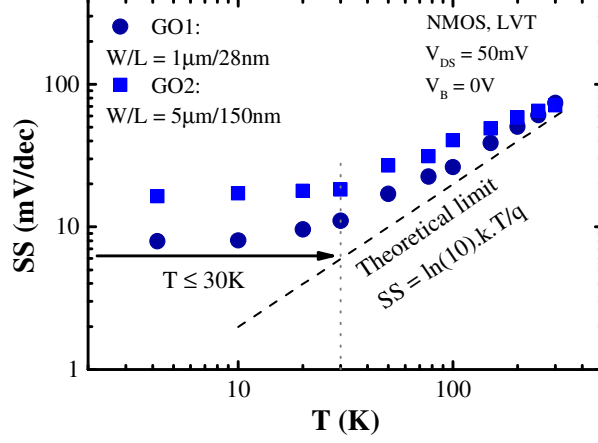


Figure. 3. Subthreshold slope as a function of temperature for NMOS LVT GO1 and GO2, at $V_B = 0$ V and $V_{DS} = 50$ mV. The dashed line indicates the theoretical limit value for the subthreshold slope at each temperature condition.

Figure. 4 presents V_{TH} as a function of L (a) and V_B (b), at 300 K and 4.2 K, and at $V_{DS} = 50$ mV. Results were extracted at constant drain current level given by $I_{DS} = 10^{-7} \times W/L$. By forward back biasing the LVT MOSFETs, it is possible to reduce V_{TH} at 4.2 K to its former value at 300 K, or even lower, in order to maintain the gate voltage overdrive, and thus reduce power consumption. Figure. 4.b indicates that the back bias efficiency, *i.e.* the body factor ($\gamma = \Delta V_{TH}/\Delta V_B$) does not depend on L or T , once γ around -90 mV/V is kept at 300 K and 4.2 K, for $L = 28$ nm and $1\mu\text{m}$.

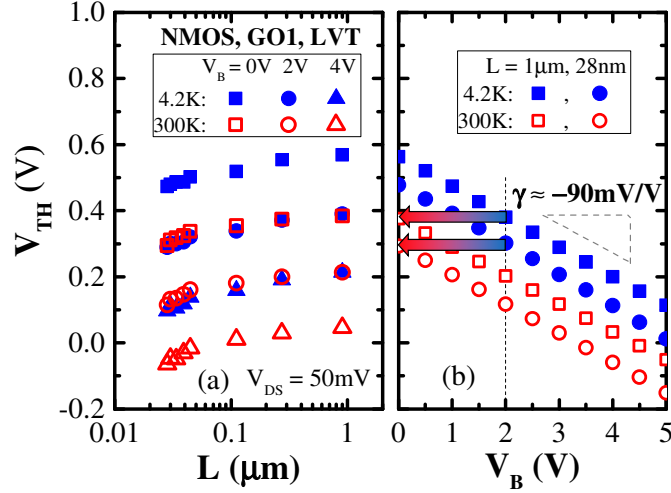


Figure. 4. Measured threshold voltage as a function of the channel length (a) and the back bias (b) for NMOS GO1 LVT, at 300 K and 4.2 K, and at $V_{DS} = 50$ mV.

Table I presents the extracted values of γ for each one of the MOSFETs available in the 28 nm FD-SOI technology, GO1/GO2, LVT/RVT, N/PMOS. Comparing room and low temperatures, the change in the body factor is found to be lower than 7 % for all devices, showing that V_B remains effective down to 4.2 K. The LVT and RVT flavors offer very large threshold voltage tuning by means of forward and reverse back biasing, up to ≈ 0.82 V and 1.60 V for NMOS GO1 and GO2, respectively, at 4.2 K [23].

TABLE I. EXTRACTED BODY FACTOR FOR ALL MOSFETs AVAILABLE IN THE 28 NM FD-SOI TECHNOLOGY.

Body factor, γ (mV/V)

			300 K	4.2 K
GO1	LVT	NMOS	-89	-93
		PMOS	-81	-80
	RVT	NMOS	-59	-59
		PMOS	-65	-68
GO2	LVT	NMOS	-159	-170
		PMOS	-150	-160
	RVT	NMOS	-123	-122
		PMOS	-130	-138

The validation of back bias efficiency and threshold voltage tuning down to 4.2 K confirms that 28 nm FD-SOI technology maintains its unique and powerful strategy to optimize its performance, and allows proper analog design of circuits for cryogenic applications [18].

Once the forward back biasing is more relevant for cryogenic applications than the reverse back biasing, due to significant V_{TH} increase with temperature lowering, only LVT transistors will be considered for the analysis in the next Sections.

III. ELECTROSTATICS AND FRONT/BACK CHANNELS COUPLING

A. Long channel MOSFET

Figure 5 presents C_{GC} as a function of V_{GS} from 300 K down to 4.2 K for N-type and PMOS, GO1 LVT transistors. Lines and symbols indicate experimental data and 1D Poisson-Schrödinger (PS) calculation [26], respectively. Good fitting of the 1D PS model is obtained with respect to the experimental measurements, by considering EOT equal to 1.1 nm for GO1 and 3.25 nm for GO2 MOSFETs. Moreover, it is possible to observe that the electrostatics of the FD-SOI transistors can be fully captured from room temperature down to 4.2 K by the 1D PS calculation applicable at all temperatures. In particular, the threshold voltage increase and the change in the C_{GC} slope are well described by the model.

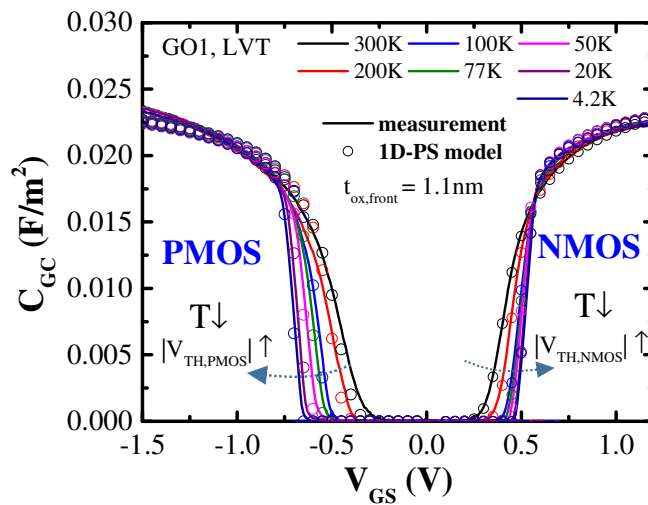


Figure 5. Measured (lines) gate-to-channel capacitance as a function of the front gate voltage for N- and PMOS, GO1 LVT devices, from 300 K down to 4.2 K, at $V_B = 0$ V. ($W = L = 10$ μ m). Corresponding calculation by 1D Poisson-Schrödinger model is indicated (symbols).

The back bias influence on the C_{GC} curves is presented in Figure 6 for NMOS GO1 LVT at 300 K (a) and 4.2 K (b). The comparison between experimental data (lines) and 1D PS calculation (symbols) indicates that the back bias influence can be well described by the model down to 4.2 K. In Figure 6 (a) and (b), for $V_B \leq 0$ V, the slopes between the minima and maxima C_{GC} values correspond to the inversion of the front channel (FC). For positive V_B , the onset of a back channel (BC) can be observed, in addition to the FC, especially in the C_{GC} curves of Figure 6 (b). The same effect is observed for PMOS with FBB (not shown). The corresponding C_{GC} derivative curves, $\partial C_{GC}/\partial V_{GS}$, are presented in Figure 6 (c) and (d) for the measurement results. The activation of the FC and BC can also be distinguished in the $\partial C_{GC}/\partial V_{GS}$ curves. At high FBB, one can observe two peaks in Figure 6 (c) and (d). The first one, at lower V_{GS} , changes with V_B and indicates the front gate voltage value necessary to activate the BC. The second one is fixed with V_B and indicates the threshold voltage of the FC when the BC is operating in inversion regime. By comparing the $\partial C_{GC}/\partial V_{GS}$ curves at room and low temperatures, in Figure 6 (c) and (d), it is possible to state that it is easier to distinguish the FC from the BC peaks at 4.2 K. On the same way, for the two plateaus in the C_{GC} curves in Figure 6 (a) and (b), the front and back channels seem to be better defined at 4.2 K, as highlighted by the dashed lines. This phenomenon will be discussed later.

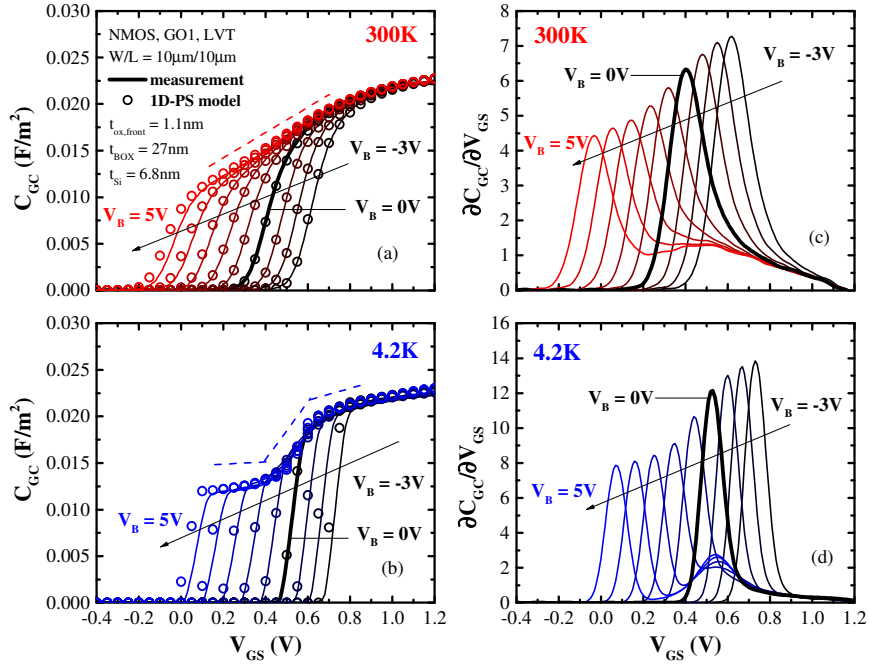


Figure 6. Measured gate-to-channel capacitance (a) and (b), and corresponding derivatives (c) and (d), as a function of the front gate voltage, varying V_B . The corresponding 1D PS model is indicated in symbols in the C_{GC} curves. Results are presented at 300 K (top) and 4.2 K (bottom), for NMOS LVT GO1. ($W = L = 10 \mu\text{m}$).

Figure 7 shows the FC and BC threshold voltages extracted at 4.2 K from $\partial C_{GC}/\partial V_{GS}$ peaks in Figure 6. The bias conditions required to activate front and/or back channels are also emphasized in Figure 7 along with respective schematics for each of the three possible configurations: i) only FC, ii) only BC, iii) both FC and BC. It is possible to observe that the experimental data is in agreement with quantum mechanical (QM) calculation. Moreover, a comparison between V_{TH} values extracted from both $\partial C_{GC}/\partial V_{GS}$ and constant current methodologies proves that the definition of V_{TH} at fixed $I_{DS} = 10^{-7} \times W/L$ is still relevant down to 4.2 K [27].

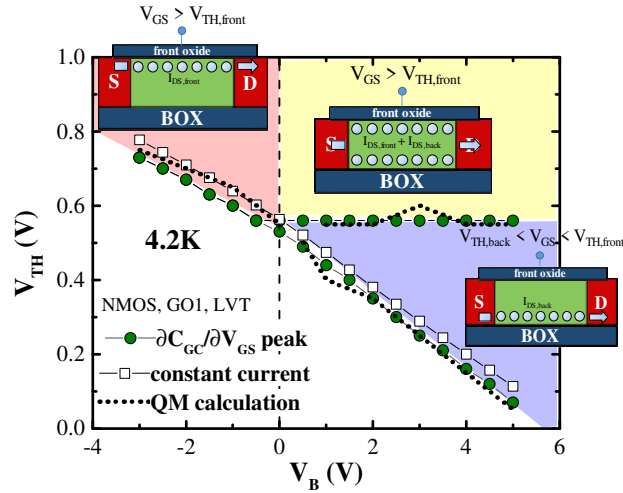


Figure 7. V_{TH} as a function of V_B extracted from maxima of $\partial C_{GC}/\partial V_{GS}$ and constant I_{DS} for NMOS GO1 LVT at 4.2 K. Schematics indicate back and/or front conduction. ($W = L = 10 \mu\text{m}$).

Figure 8 presents the quantum mechanical calculation of the carrier concentration (n_{inv}) as a function of the vertical position along the Si thickness. Two situations are given, providing a further insight. At the top figure, results are calculated at 4.2 K, $V_B = 2 \text{ V}$, and varying V_{GS} . As expected from Figure 7, a single back channel is observed for $V_{GS} = 0.5 \text{ V}$, once V_{TH} of the front channel is found to be around 0.57 V. For $V_{GS} > 0.8 \text{ V}$, both FC and BC are observed. At fixed V_B , once the FC is activated, by increasing V_{GS} , the carrier concentration remains unchanged at the back interface, while it increases at the front interface. At the bottom figure, results are calculated considering fixed inversion carrier density ($N_{inv} = 10^{12} \text{ cm}^{-2}$), at 4.2 K and 300 K, varying V_B . This time, only one channel is formed, either close to the front interface ($V_B = 0 \text{ V}$) or to the back interface ($V_B = 2 \text{ V}$ and 3 V). The n_{inv} peaks are found around 2 nm far from the interfaces, for both FC and BC. By comparing n_{inv} results at room and low temperatures, Figure 8 (bottom) also shows that FC and BC are more decoupled at 4.2 K, i.e. the peak of n_{inv} defining BC or FC is better resolved at low temperature. This effect explains the differences in the shape of capacitance curves between 300 K and 4.2 K (Figure 6), where the two plateaus corresponding to BC and FC are better distinguished at 4.2 K.

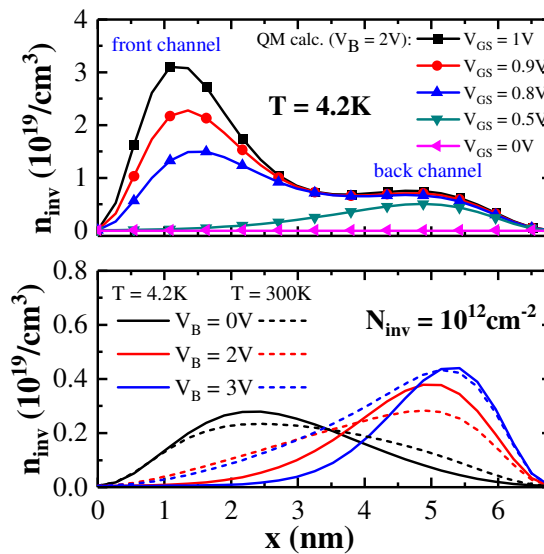


Figure 8. Calculated carrier concentration as a function of the vertical position along the channel thickness, varying V_{GS} at 4.2 K (top), and varying V_B at 300 K and 4.2 K (bottom). (NMOS GO1 LVT).

B. Short channel MOSFET

Contrarily to the transistors with long channel length studied in the previous Section, short channel MOSFETs present maximum C_{GC} level in the order of 0.1 fF, which is well below the accuracy of commercial precision LCR (inductance-capacitance-resistance) meters. To overcome this difficulty, structures with multiple (tens of thousands) parallel MOSFETs were used to increase the device area and allow appropriate capacitance measurements. Moreover, the parasitic and overlap (C_{ov}) capacitances are no longer negligible in such short gate lengths. Therefore they were corrected following the methodology presented in [28], where the intrinsic capacitance of a transistor is calculated from the C_{GC} curves of two transistors with adjacent gate lengths, since C_{ov} is L-independent. The use of two close L is mandatory to avoid V_{TH} mismatch between the two corresponding devices.

Figure 9 presents C_{GC} curves for short channel transistors to illustrate the overlap capacitance correction. Each MOSFET structure has a total area of around $630\mu\text{m}^2$, giving a maximum capacitance level around 10pF. The two different gate lengths used for C_{ov} correction are $L = 34\text{ nm}$ and 28 nm .

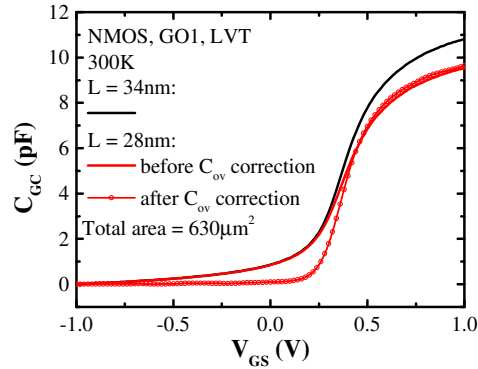


Figure 9. Gate-to-channel capacitance as a function of the front gate voltage for NMOS GO1 LVT with $L = 34\text{ nm}$ and 28 nm before C_{ov} correction, and for $L = 28\text{ nm}$ after C_{ov} correction, at 300 K .

Figure 10 shows the extracted C_{ov} as a function of V_{GS} , varying the back bias (a) and the temperature (b). It is possible to note that C_{ov} does not exhibit significant dependence on T or V_B , besides its shifts across V_{GS} following the threshold voltage behavior.

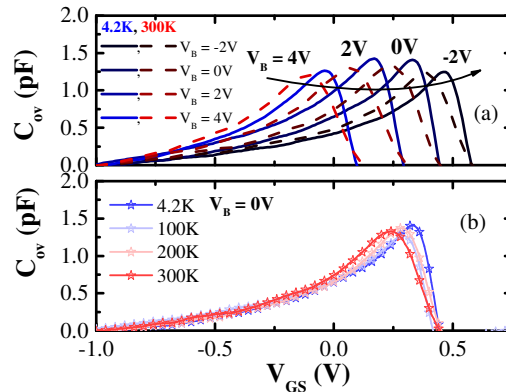


Figure 10. Overlap capacitance *versus* front gate voltage at 300 K and 4.2 K , varying V_B (a), and at $V_B = 0\text{ V}$, varying T (b).

Figure 11 shows the results of C_{GC} as a function of V_{GS} , varying V_B , at 300 K and 4.2 K , after C_{ov} correction. Results are very similar to those obtained for long channel transistors. For example, under high forward back biasing, at

$V_B = 4$ V, one can see that the front and back channels are more decoupled at low temperature, making each one of the two capacitance plateaus more easily distinguishable.

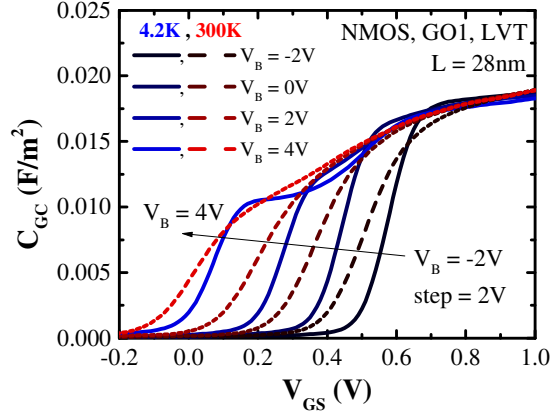
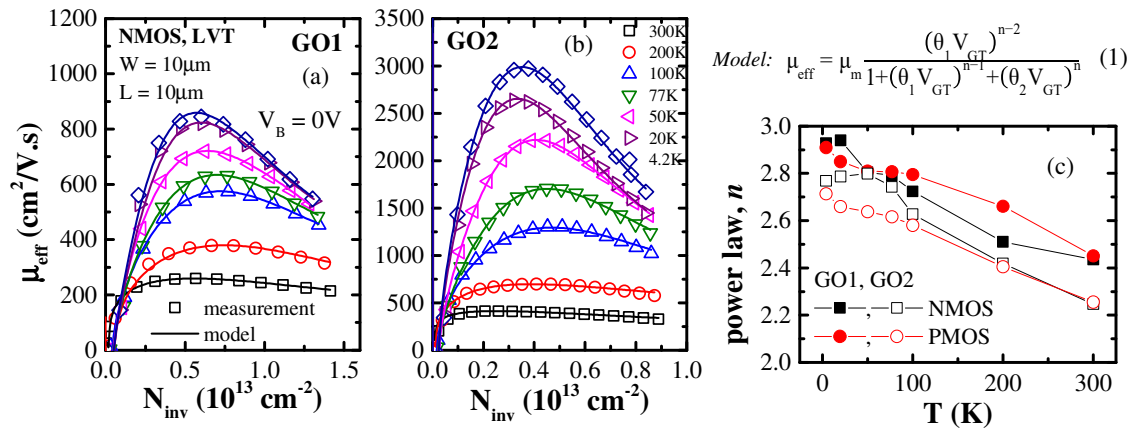


Figure 11. Gate-to-channel capacitance as a function of the front gate voltage for NMOS GO1 LVT with $L = 28$ nm, at 300 K and 4.2 K, varying V_B .

IV. TRANSPORT CHARACTERISTICS

A. Long channel MOSFET

Figure 12 presents μ_{eff} as a function of N_{inv} for NMOS LVT, varying T , and at $V_B = 0$ V. GO1 (a) and GO2 (b) transistors were characterized in order to evaluate the impact of the front gate oxide thickness on the front channel mobility. It is possible to observe that μ_{eff} is highly improved at 4.2 K, as expected due to the T -dependence of the phonon scattering contribution (μ_{ps}), which becomes fully suppressed below ≈ 20 K. From 300 K to 4.2 K, gains of up to $\times 7.2$ and $\times 3.1$ are obtained for the mobility of GO2 and GO1 MOSFETs, respectively. As a result of the μ_{ps} T -dependence, the usual empirical models for mobility at room temperature [3] are no longer valid at cryogenic operation, and a more generic form must be considered [3] in compact models. The lines in Figure 12 (a) and (b) were obtained using the generalized form of the mobility model described in Equation (1), where the power law exponent (n) varies from 2 to 3, as the temperature decreases from 300 K to 4.2 K, as observed in Figure 12 (c). It is valid to mention that Equation (1) consists in a simple empirical model that has found to appropriately fit all the experimental data, for both N- and PMOS, GO1 and GO2, when $V_B = 0$ V. In order to fully describe the transport characteristics of FD-SOI devices under different back bias conditions, and therefore have robust compact models, more complex physically-based mobility models must be developed to take into account effects such as the two-dimensional intersubband scattering [29].



$$\text{Model: } \mu_{\text{eff}} = \mu_m \frac{(\theta_1 V_{\text{GT}})^{n-2}}{1 + (\theta_1 V_{\text{GT}})^{n-1} + (\theta_2 V_{\text{GT}})^n} \quad (1)$$

Figure 12. Experimental (symbols) and corresponding analytical model (lines) results for the effective carriers' mobility as a function of the inversion carrier density for NMOS GO1 (a) and GO2 (b), varying T , at $V_B = 0$ V. Equation of the generalized form of μ_{eff} , valid at any temperature down to 4.2K. Power law exponent used to fit experimental μ_{eff} , as a function of temperature, for GO1 and GO2, N- and PMOSFETs.

Figure 13 presents μ_{eff} as a function of the effective electrical field (E_{eff}) at 300 K and 4.2 K. Front and back channel mobilities have been dissociated and extracted by applying the split CV technique for different back bias [30]. From Figure 13, it is noticed that the front channel mobility of the GO2 MOSFET is close to the universal mobility at room and low temperatures, whereas the front channel mobility of the GO1 MOSFET is degraded compared to its back channel mobility and to the FC mobility of the GO2 MOSFET. This is expected due to additional scattering mechanism induced by the proximity of the high- k layer for thin gate oxide thickness [30]. On the same way as observed for the front channel, the BC mobility is highly improved at low temperatures, where a gain of up to $\times 6.5$ is found from 300 K down to 4.2 K.

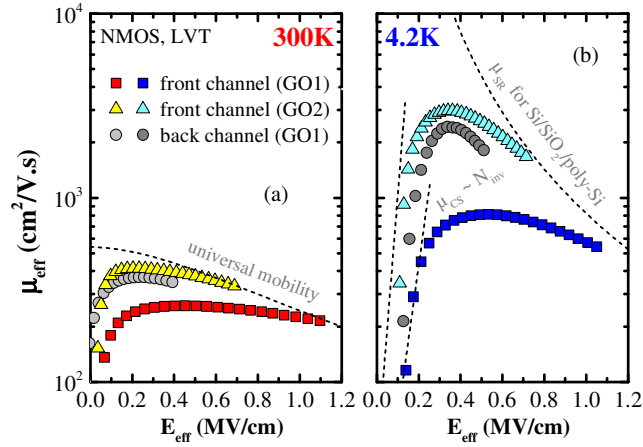


Figure 13. Front and back channel effective mobility as a function of the effective electric field at 300 K (a) and 4.2 K (b) for NMOS LVT. ($W = L = 10 \mu\text{m}$). GO2 results are very close to the universal mobility at 300 K and 4.2 K (dashed lines).

The μ_{eff} improvement at low temperature is reflected in the transconductance ($g_m = \partial I_{\text{DS}}/\partial V_{\text{GS}}$) of the devices. Figure 14 presents the maximum of g_m in linear regime as a function of T (a), and in saturation ($V_{\text{DS}} = V_{\text{DD}}$, where $V_{\text{DD}} = 0.9$ V for GO1 and $V_{\text{DD}} = 1.8$ V for GO2) as a function of V_B (b). The arrows highlight the $g_{m,\text{max}}$ increase at 4.2 K in comparison to room temperature operation. It is also demonstrated in Figure 14 (b) that $g_{m,\text{max}}$ can be further improved by FBB. This is due to the addition of both front and back channels contributions, with in particular higher back channel mobility for GO1 transistors. It is important to mention that in saturation regime the devices operate at high input power, and therefore may suffer from significant self-heating effect, which is stronger at low temperature operation due to thermal resistance increase [31].

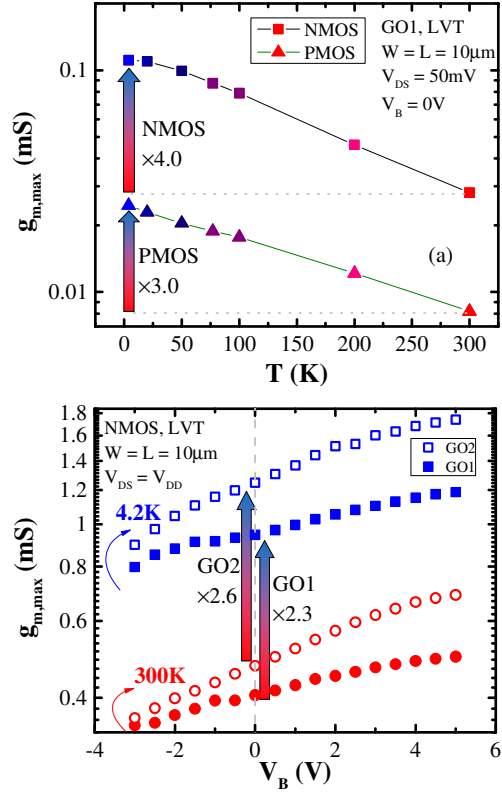


Figure 14. Maximum transconductance as a function of temperature for N- and PMOS GO1 LVT, at $V_{DS} = 50$ mV and $V_B = 0$ V (a). Maximum transconductance as a function of the back bias for NMOS LVT GO1 and GO2 in saturation ($V_{DS} = V_{DD}$), and at 300 K and 4.2 K.

B. Short channel MOSFET

The split CV technique was also used for the mobility extraction of short channel devices. In order to allow for correct μ_{eff} evaluation, the series resistance (R_S) was extracted using the Y-function method [32], [33]. R_S values of 180 Ω and 160 Ω were found at 300 K and 4.2 K, respectively. The observed R_S reduction with T lowering is due to mobility improvement in source and drain regions, which also contributes to drain current enhancement. Equation (2) was used to correct the drain current of the devices, where $I_{DS,c}$ indicates I_{DS} compensated by series resistance correction.

$$I_{DS,c} = \frac{I_{DS}}{1 - \frac{R_S I_{DS}}{V_{DS}}} \quad (2)$$

Figure 15 (a) presents the total μ_{eff} , accounting for both channel conduction, at 4.2 K and varying V_B . An improvement is observed by applying forward back bias due to the appearance of the BC, where the mobility is higher, as observed in Figure 15 (b). From Section IV.A, the FC mobility improvement in long channel GO1 MOSFETs was found to be as high as $\times 3.1$, from 300 K to 4.2 K. Figure 15 (b) shows a reduced μ_{eff} increase ($\times 1.3$) for short channel MOSFETs with T reduction. This phenomenon of lower improvement in short channel transistors, in comparison to long channel ones, could be explained by both neutral defects and quasi-ballistic transport [34], [35]. Similar results were obtained in [36] for 14 nm FD-SOI MOSFETs analyzed down to 77 K.

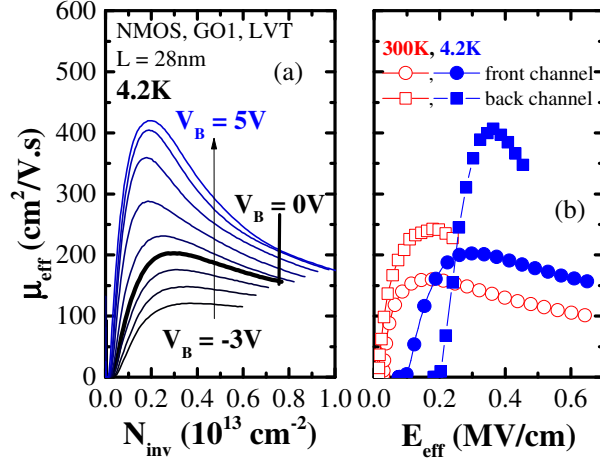


Figure 15. Overall effective mobility as a function of the inversion carrier density at 4.2 K, varying V_B (a). Front and back channels effective mobility as a function of the effective electric field at 300 K and 4.2 K (b).

Figure 16 shows the transport parameters impact on the cut-off frequency (f_T), which is an important figure of merit for qubit control circuits [37]. Results were calculated from Equation (3), where C_{OX} is the oxide capacitance per area.

$$f_T = \frac{g_{m,max}}{2\pi C_{OX}WL} \quad (3)$$

Although Equation (3) consists in an estimation of the f_T values, it is valid to point that results found in this work are similar to those obtained from radiofrequency characterization in [38]. The f_T increase at 4.2 K observed in Figure 16 is due to a combination of μ_{eff} increase and R_S decrease. Moreover, Figure 16 (b) shows that the f_T gain at 4.2 K decreases for short channel transistors, being limited to $\times 1.4$ below $L \approx 100$ nm, following the μ_{eff} trend previously discussed.

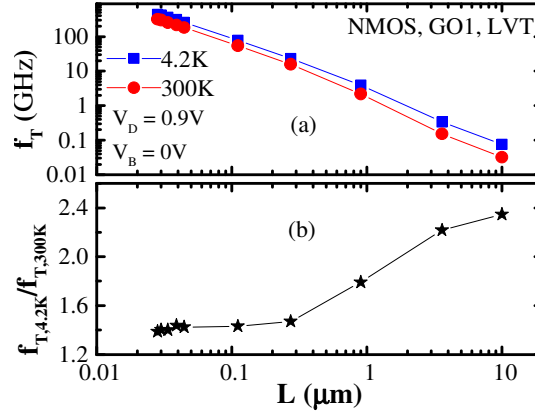


Figure 16. Cut-off frequency *versus* channel length for NMOS GO1 LVT at $V_D = 0.9$ V, $V_B = 0$ V and at 300 K and 4.2 K.

V. CONCLUSIONS

The use of back biasing in ultra-thin body and buried oxide FD-SOI offers a unique way to optimize the electrical performances of 28 nm FD-SOI devices operating at very low temperature, from long to short channel transistors. Forward back biasing allows not only reducing the power consumption by means of threshold voltage shift, but also important overall mobility increase. 1D Poisson-Schrödinger calculation down to 4.2 K provides a full understanding of the electrostatics. In particular, the onsets of front and back channels have to be considered while using

FD-SOI transistors operating at low temperature, since the phenomena considerably affects the carrier concentration position along the Si thickness and the transport properties as well. By adjusting the power law exponent of a generic form of the conventional empiric mobility model, experimental data could be fit from 300 K down to 4.2 K. Short channel transistors could be evaluated using the split CV technique after correcting the parasitic and overlap capacitances and the series resistance. By comparison to long channel transistors, short channel devices indicate to suffer from stronger temperature independent scattering mechanisms such as neutral defects and/or quasi-ballistic transport. Cryogenic operation beneficiates the cut-off frequency of all studied MOSFETs due to improvements in transport. Finally, this work contributed to the understanding of the physical mechanisms that must be considered in future compact models of FD-SOI MOSFETs operating at cryogenic temperatures.

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REFERENCES

- [1] G. Gildenblat, L. Colonna-Romano, D. Lau, and D. E. Nelsen, "Investigation of cryogenic CMOS performance," in *1985 International Electron Devices Meeting*, Dec. 1985, pp. 268–271, doi: 10.1109/IEDM.1985.190948.
- [2] A. K. Henning, N. Chan, and J. D. Plummer, "Substrate current in N-channel and P-channel MOSFETs between 77K and 300K: Characterization and simulation," in *1985 International Electron Devices Meeting*, 1985, pp. 573–576.
- [3] F. Balestra and G. Ghibaudo, *Device and Circuit Cryogenic Operation for Low Temperature Electronics*. Springer Science & Business Media, 2013.
- [4] A. Gupta, M. F. Li, K. K. Yu, S. C. Su, P. Pandya, and H. B. Yang, "Radiation-hard 16K CMOS/SOS clocked static RAM," in *1981 International Electron Devices Meeting*, Dec. 1981, pp. 616–619, doi: 10.1109/IEDM.1981.190160.
- [5] M. J. Deen, "Digital characteristics of CMOS devices at cryogenic temperatures," *IEEE J. Solid-State Circuits*, vol. 24, no. 1, pp. 158–164, Feb. 1989, doi: 10.1109/4.16315.
- [6] S. Selberherr, "MOS device modeling at 77 K," *IEEE Trans. Electron Devices*, vol. 36, no. 8, pp. 1464–1474, Aug. 1989, doi: 10.1109/16.30960.
- [7] I. M. Hafez, G. Ghibaudo, and F. Balestra, "Flicker noise in metal-oxide-semiconductor transistors from liquid helium to room temperature," *J. Appl. Phys.*, vol. 66, no. 5, pp. 2211–2213, Sep. 1989, doi: 10.1063/1.344321.
- [8] E. Charbon *et al.*, "Cryo-CMOS for quantum computing," in *2016 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2016, p. 13.5.1-13.5.4, doi: 10.1109/IEDM.2016.7838410.
- [9] A. M. Tyryshkin *et al.*, "Electron spin coherence exceeding seconds in high-purity silicon," *Nat. Mater.*, vol. 11, no. 2, Art. no. 2, Feb. 2012, doi: 10.1038/nmat3182.
- [10] J. M. Boter *et al.*, "A sparse spin qubit array with integrated control electronics," in *2019 IEEE International Electron Devices Meeting (IEDM)*, Dec. 2019, p. 31.4.1-31.4.4, doi: 10.1109/IEDM19573.2019.8993570.
- [11] L. Hutin *et al.*, "All-Electrical Control of a Hybrid Electron Spin/Valley Quantum Bit in SOI CMOS Technology," in *2018 IEEE Symposium on VLSI Technology*, Jun. 2018, pp. 125–126, doi: 10.1109/VLSIT.2018.8510665.
- [12] L. L. Guevel *et al.*, "19.2 A 110mK 295 μ W 28nm FDSOI CMOS Quantum Integrated Circuit with a 2.8GHz Excitation and nA Current Sensing of an On-Chip Double Quantum Dot," in *2020 IEEE International Solid-State Circuits Conference - (ISSCC)*, Feb. 2020, pp. 306–308, doi: 10.1109/ISSCC19947.2020.9063090.
- [13] M. E. P. V. Zurita *et al.*, "Cryogenic Current Steering DAC With Mitigated Variability," *IEEE Solid-State Circuits Lett.*, vol. 3, pp. 254–257, 2020, doi: 10.1109/LSSC.2020.3013443.

- [14] P. Galy, J. C. Lemyre, P. Lemieux, F. Arnaud, D. Drouin, and M. Piore-Ladrière, "Cryogenic Temperature Characterization of a 28-nm FD-SOI Dedicated Structure for Advanced CMOS and Quantum Technologies Co-Integration," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 594–600, 2018, doi: 10.1109/JEDS.2018.2828465.
- [15] L. Le Guevel *et al.*, "Low-power transimpedance amplifier for cryogenic integration with quantum devices," *Appl. Phys. Rev.*, vol. 7, no. 4, p. 041407, Dec. 2020, doi: 10.1063/5.0007119.
- [16] A. Beckers, F. Jazaeri, H. Bohuslavskiy, L. Hutin, S. De Franceschi, and C. Enz, "Design-oriented Modeling of 28 nm FDSOI CMOS Technology down to 4.2 K for Quantum Computing," *2018 Jt. Int. EUROSIOI Workshop Int. Conf. Ultim. Integr. Silicon EUROSIOI-ULIS*, pp. 1–4, Mar. 2018, doi: 10.1109/ULIS.2018.8354742.
- [17] H. Bohuslavskiy *et al.*, "28nm Fully-depleted SOI technology: Cryogenic control electronics for quantum computing," in *2017 Silicon Nanoelectronics Workshop (SNW)*, Jun. 2017, pp. 143–144, doi: 10.23919/SNW.2017.8242338.
- [18] H. Bohuslavskiy *et al.*, "Cryogenic Characterization of 28-nm FD-SOI Ring Oscillators With Energy Efficiency Optimization," *IEEE Trans. Electron Devices*, vol. 65, no. 9, pp. 3682–3688, Sep. 2018, doi: 10.1109/TED.2018.2859636.
- [19] B. C. Paz *et al.*, "Variability Evaluation of 28nm FD-SOI Technology at Cryogenic Temperatures down to 100mK for Quantum Computing," in *2020 IEEE Symposia on VLSI Technology and Circuits*, pp. 1–2, doi: 10.1109/VLSITechnology18217.2020.9265034.
- [20] R. M. Incandela, L. Song, H. Homulle, E. Charbon, A. Vladimirescu, and F. Sebastiano, "Characterization and Compact Modeling of Nanometer CMOS Transistors at Deep-Cryogenic Temperatures," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 996–1006, 2018, doi: 10.1109/JEDS.2018.2821763.
- [21] H. Bohuslavskiy *et al.*, "Cryogenic Subthreshold Swing Saturation in FD-SOI MOSFETs Described With Band Broadening," *IEEE Electron Device Lett.*, vol. 40, no. 5, pp. 784–787, May 2019, doi: 10.1109/LED.2019.2903111.
- [22] B. C. Paz *et al.*, "Electrostatics and channel coupling on 28 nm FDSOI for cryogenic applications," in *2020 Joint International EUROSIOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSIOI-ULIS)*, pp. 1–4, doi: 10.1109/EUROSIOI-ULIS49407.2020.9365453.
- [23] N. Planes *et al.*, "28nm FDSOI technology platform for high-speed low-voltage digital applications," in *2012 Symposium on VLSI Technology (VLSIT)*, Jun. 2012, pp. 133–134, doi: 10.1109/VLSIT.2012.6242497.
- [24] H. Bohuslavskiy *et al.*, "Cryogenic Subthreshold Swing Saturation in FD-SOI MOSFETs described with Band Broadening," *IEEE Electron Device Lett.*, pp. 1–1, 2019, doi: 10.1109/LED.2019.2903111.
- [25] G. Ghibaudo, M. Aouad, M. Casse, S. Martinie, T. Poiroux, and F. Balestra, "On the modelling of temperature dependence of subthreshold swing in MOSFETs down to cryogenic temperature," *Solid-State Electron.*, vol. 170, p. 107820, Aug. 2020, doi: 10.1016/j.sse.2020.107820.
- [26] M. Aouad, S. Martinie, F. Triozon, T. Poiroux, M. Vinet, G. Ghibaudo, "Poisson-Schrodinger simulation of inversion charge in FDSOI MOSFET down to 0K – Towards compact modeling for cryo CMOS application," presented at the 2020 Joint International EUROSIOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSIOI-ULIS), 2020, doi: 10.1109/EUROSIOI-ULIS49407.2020.9365297.
- [27] T. Rudenko, M. K. Md Arshad, J.-P. Raskin, A. Nazarov, D. Flandre, and V. Kilchytska, "On the gm/ID-based approaches for threshold voltage extraction in advanced MOSFETs and their application to ultra-thin body SOI MOSFETs," *Solid-State Electron.*, vol. 97, pp. 52–58, Jul. 2014, doi: 10.1016/j.sse.2014.04.029.
- [28] K. Romanjek, F. Andrieu, T. Ernst, and G. Ghibaudo, "Improved split C-V method for effective mobility extraction in sub-0.1- μm Si MOSFETs," *IEEE Electron Device Lett.*, vol. 25, no. 8, pp. 583–585, Aug. 2004, doi: 10.1109/LED.2004.832786.
- [29] M. Cassé *et al.*, "Evidence of 2D intersubband scattering in thin film fully depleted silicon-on-insulator transistors operating at 4.2 K," *Appl. Phys. Lett.*, vol. 116, no. 24, p. 243502, Jun. 2020, doi: 10.1063/5.0007100.
- [30] M. Casse *et al.*, "Carrier transport in HfO₂/metal gate MOSFETs: physical insight into critical parameters," *IEEE Trans. Electron Devices*, vol. 53, no. 4, pp. 759–768, Apr. 2006, doi: 10.1109/TED.2006.870888.
- [31] K. Triantopoulos *et al.*, "Self-Heating Effect in FDSOI Transistors Down to Cryogenic Operation at 4.2 K," *IEEE Trans. Electron Devices*, vol. 66, no. 8, pp. 3498–3505, Aug. 2019, doi: 10.1109/TED.2019.2919924.
- [32] J. B. Henry, A. Cros, J. Rosa, Q. Raffhay, and G. Ghibaudo, "Impact of access resistance on New-Y function methodology for MOSFET parameter extraction in advanced FD-SOI technology," in *2017 International Conference of Microelectronic Test Structures (ICMTS)*, Mar. 2017, pp. 1–5, doi: 10.1109/ICMTS.2017.7954269.

- [33] G. Ghibaudo, "New method for the extraction of MOSFET parameters," *Electron. Lett.*, vol. 24, no. 9, pp. 543–545, Apr. 1988, doi: 10.1049/el:19880369.
- [34] G. Ghibaudo *et al.*, "Electrical transport characterization of nano CMOS devices with ultra-thin silicon film," in *2009 International Workshop on Junction Technology*, Jun. 2009, pp. 58–63, doi: 10.1109/IWJT.2009.5166220.
- [35] R. Clerc and G. Ghibaudo, "ANALYTICAL MODELS AND ELECTRICAL CHARACTERISATION OF ADVANCED MOSFETs IN THE QUASI BALLISTIC REGIME," *Int. J. High Speed Electron. Syst.*, vol. 22, no. 01, p. 1350002, Nov. 2013, doi: 10.1142/S012915641350002X.
- [36] M. Shin *et al.*, "Low temperature characterization of 14nm FDSOI CMOS devices," in *2014 11th International Workshop on Low Temperature Electronics (WOLTE)*, Jul. 2014, pp. 29–32, doi: 10.1109/WOLTE.2014.6881018.
- [37] J. C. Bardin *et al.*, "Design and Characterization of a 28-nm Bulk-CMOS Cryogenic Quantum Controller Dissipating Less Than 2 mW at 3 K," *IEEE J. Solid-State Circuits*, vol. 54, no. 11, pp. 3043–3060, Nov. 2019, doi: 10.1109/JSSC.2019.2937234.
- [38] L. Nyssens *et al.*, "28-nm FD-SOI CMOS RF Figures of Merit Down to 4.2 K," *IEEE J. Electron Devices Soc.*, vol. 8, pp. 646–654, 2020, doi: 10.1109/JEDS.2020.3002201.