



HAL
open science

TCAD simulations of FDSOI devices down to deep cryogenic temperature

E. Catapano, M. Cassé, F. Gaillard, S. de Franceschi, Tristan Meunier, M. Vinet, G. Ghibaudo

► **To cite this version:**

E. Catapano, M. Cassé, F. Gaillard, S. de Franceschi, Tristan Meunier, et al.. TCAD simulations of FDSOI devices down to deep cryogenic temperature. *Solid-State Electronics*, 2022, 194, pp.108319. 10.1016/j.sse.2022.108319 . hal-03974981

HAL Id: hal-03974981

<https://hal.science/hal-03974981>

Submitted on 22 Jul 2024

HAL is a multi-disciplinary open access archive for the deposit and dissemination of scientific research documents, whether they are published or not. The documents may come from teaching and research institutions in France or abroad, or from public or private research centers.

L'archive ouverte pluridisciplinaire **HAL**, est destinée au dépôt et à la diffusion de documents scientifiques de niveau recherche, publiés ou non, émanant des établissements d'enseignement et de recherche français ou étrangers, des laboratoires publics ou privés.



Distributed under a Creative Commons Attribution - NonCommercial 4.0 International License

TCAD Simulations of FDSOI devices down to Deep Cryogenic Temperature

E. Catapano^{1,2}, M. Cassé², F. Gaillard², S. de Franceschi³, T. Meunier⁴, M. Vinet² and G. Ghibaudo¹

1) IMEP-LAHC, Univ. Grenoble Alpes, Minatec, 38016 Grenoble, France. 2) CEA-LETI, Univ. Grenoble-Alpes, Minatec, 38054 Grenoble, France. 3) CEA-IRIG, Univ. Grenoble-Alpes, Minatec, 38042 Grenoble, France. 4) CNRS, Institut Néel, Univ. Grenoble Alpes, 38042 Grenoble, France

Abstract — In this paper we demonstrate the feasibility of FDSOI device TCAD simulations down to deep cryogenic temperatures. To this purpose, Maxwell-Boltzmann carrier statistics is replaced by an analytical approximation for the Fermi-Dirac integral with 3D density of states. The device electrostatic is investigated by solving the Poisson equation in 2D, whereas the transport is simulated using the Drift-Diffusion model. We explore the impact of temperature on device performances in linear and saturation regions as well as the impact of short channel effects, accounted for various gate and spacer lengths, at room and deep cryogenic temperatures. Finally, the obtained results are compared to some experimental data, highlighting the role of TCAD simulations in providing insights in device physics and performances.

Keywords – cryogenic electronics, FDSOI, TCAD simulations

I. INTRODUCTION

FD-SOI appears as one of the most promising technologies to be employed in quantum computing, not only for the control readout electronics that must operate at temperatures ranging from 4.2K down to well below 1K [1], but also for the fabrication of the quantum bit itself [2]. Despite the recent interest in cryogenic electronics boosting both technology and low temperature device physics understanding, reliable TCAD modeling at temperatures below 77K is still missing. Recently, efforts were made in simulating an nMOSFET down to 5K [3] but, to the best of our knowledge, no studies have ever been devoted to FD-SOI TCAD modeling at deep cryogenic temperatures.

In this paper, we simulate with a partial differential equation solver (FlexPDE) both the electrostatics and the transport in an n-type FD-SOI device down to deep cryogenic temperature using an analytical approximation of the Fermi-Dirac integral with 3D density of states and even down to zero Kelvin using the metallic statistics. Furthermore, the simulation results are compared with some experimental data, enabling better physical interpretation.

II. TCAD MODELING DESCRIPTION

FlexPDE (at www.pdesolutions.com) was used in this work. It allowed to numerically solve the 2D Poisson equation for the structure depicted in Fig. 1. We set the channel and the spacer length equal to $L_G = 40 \text{ nm}$ and

$L_{SP} = 20 \text{ nm}$, respectively, whereas the silicon film thickness was chosen to be $t_{si} = 15 \text{ nm}$. Finally, the BOX thickness was fixed to $t_{BOX} = 145 \text{ nm}$. The simulated structure was inspired by the LETI qubit technology [2]. In the simulations, in order to improve the mesh, we reduced t_{BOX} , and we increased by the same factor the oxide permittivity, in order to keep the buried oxide capacitance constant.

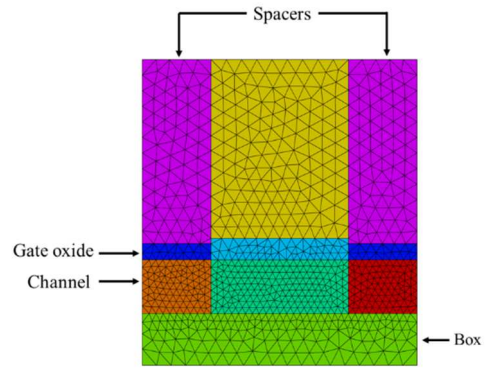


Figure 1. Device structure used in simulations

In order to take into account the influence of source and drain, that were not explicitly considered here, the built-in potential calculated with degenerate statistics $V_{bi} = V_0 + (3 \cdot \sqrt{\pi} \cdot N_D / (4N_{cc0}))^{2/3}$ has been imposed as boundary condition, where V_0 is the intrinsic Fermi potential, N_D is the source/drain doping level and $N_{cc0} = 2 \cdot 10^{19} / (k_B \cdot 300)^{3/2} \left(\frac{eV^{3/2}}{cm^3} \right)$ a constant. At cryogenic temperatures, the Fermi-Dirac statistics must be considered and the carrier density reads [4]

$$n = \int_{E_C}^{\infty} N(E) f(E) dE = N_C(T) \frac{2}{\sqrt{\pi}} F_{1/2}(u) \quad (1)$$

where E_C is the bottom of the conduction band, $N(E)$ is the 3D density of states, $N_C(T) = 2 \cdot 10^{19} \cdot (T/300)^{3/2}$ is the effective density of states and $F_{1/2}$ is the Fermi-Dirac integral, given by [4]

$$F_{1/2}(u) = \int_{E_C}^{\infty} \frac{E^{1/2}}{1 + \exp(E - u)} dE \quad (2)$$

where $u = E_F/k_B T$ is the reduced Fermi energy. In the simulations, an analytical approximation of Eq.(2) was used:

$$F_{app}(u) = \frac{\sqrt{\pi}}{2} \ln \left(1 + \exp \left(2 \frac{u}{3} \right) \right)^{\frac{3}{2}} \cdot \left(1.2 + 0.2 \tanh \left(\frac{u}{3} \right) \right) \quad (3)$$

Note that this simple approximation for $F_{\frac{1}{2}}$ provides less than 10% of error with u varying between -15 and +15 as shown in Fig. 2.

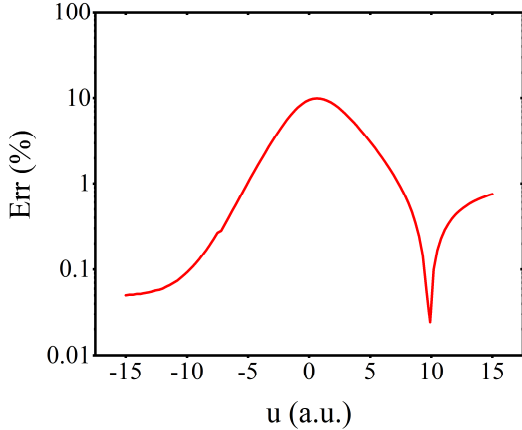


Figure 2. Percentage error between $F_{1/2}$ and F_{app} versus u .

The results at deep cryogenic temperatures were also compared to those obtained using the fully degenerate metallic statistics, i.e. the zero temperature approximation (ZTA):

$$n_{deg}(E_F, T) = N_C(T) \cdot \frac{2}{\sqrt{\pi}} \left(\frac{2}{3} \cdot \left(\frac{E_F}{k_B T} \right)^{\frac{2}{3}} \right) \quad (4)$$

The quantum confinement effect close to $Si - SiO_2$ interfaces was accounted for using the Hansch correction [5].

III. NUMERICAL SIMULATION RESULTS

In Fig. 3 are reported the carrier densities across the channel as function of temperature. The gate voltage was set equal to $V_G = 2V$, where the channel is fully inverted, and the bias was set to $V_D = 0$. As the temperature is lowered, the carriers are more confined at the $Si - SiO_2$ interface, since the statistics becomes more degenerate. It is worth to point out that at $T = 0 K$ the carrier density follows the same trend as that obtained at $T = 20 K$ until the middle of the channel, where it suddenly drops down to zero. The carrier density and the electrostatic potential using the same bias conditions were simulated also along the channel (see Fig. 4). From both Fig. 3 and Fig. 4, it is possible to conclude that the ZTA well reproduces the device electrostatics at deep cryogenic temperatures, i.e. $T \leq 20 K$.

In Fig. 5 the drain current characteristic $I_D(V_G)$ is reported both at $T = 300 K$ and $T = 20 K$, with a drain voltage equal to $V_D = 5 mV$. It was simulated solving the Poisson equation coupled with the current continuity equation in stationary conditions. In Fig. 5 (a), a constant mobility value equal to $\mu_0 = 100 cm^2/Vs$ was used,

whereas in Fig. 5 (b), the mobility attenuation law with local electric field described in [6] was employed.

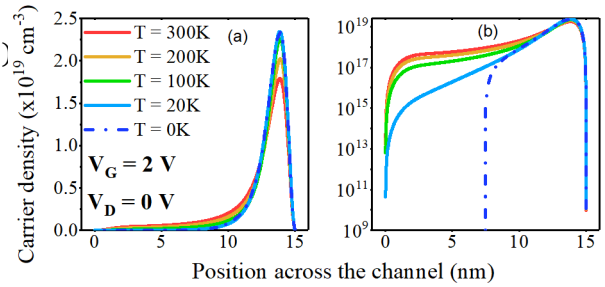


Figure 3. Simulated carrier density across the channel in linear (a) and logarithmic (b) scale.

As can be seen, the simulations well reproduce the typical experimental behaviors [7], i.e. a decrease of the threshold voltage V_{th} and of the subthreshold swing SS as the temperature is reduced. It is also worth noting that, despite the presence of the spacers, the channel is still conducting at low temperatures.

A. Short channel effects

Short channel effects can be studied at both room and cryogenic temperature. In Fig. 6 is shown the impact of the channel length L_G on the electrostatic potential when the channel is fully inverted ($V_G = 2 V$). The temperature does not influence the effect of channel reduction, at least in strong inversion. In fact, as can be seen from $I_D(V_G)$ curves of Fig. 7, the SCE are reduced at cryogenic temperature, especially the I_{OFF} is strongly decreased thanks to the steepness of the subthreshold swing.

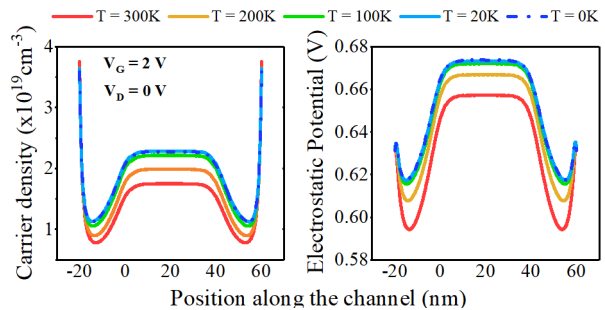


Figure 4. Carrier density (a) and electrostatic potential (b) along the channel.

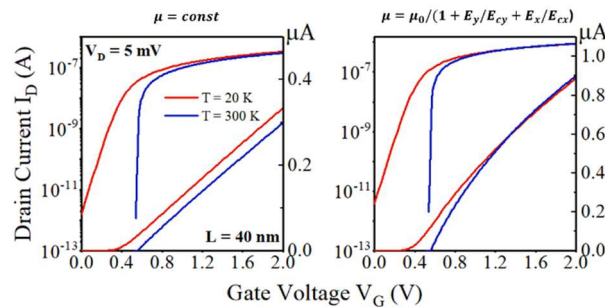


Figure 5. Simulated $I_D(V_G)$ with constant (a) and field dependent (b) mobility

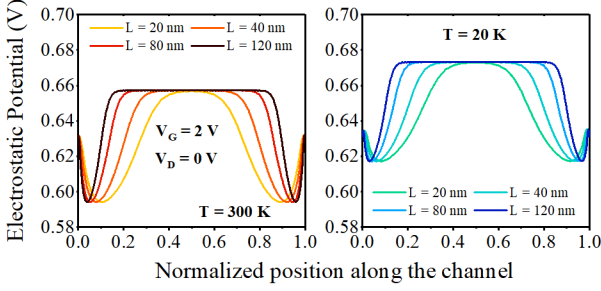


Figure 6. Electrostatic potential for different L_G at (a) $T = 300 K$ and (b) $T = 20 K$

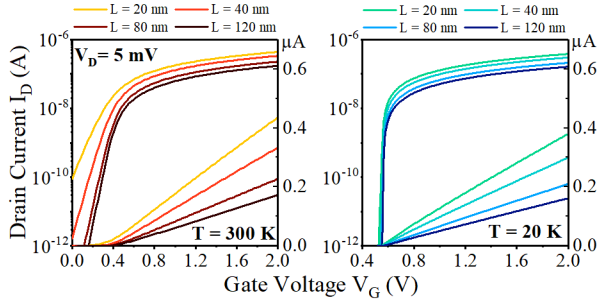


Figure 7. Simulated $I_D(V_G)$ for different L_G at $T = 300 K$ (a) and $T = 20 K$ (b).

It is also possible to investigate the impact of the spacers' length and its temperature dependency. As shown in Fig. 8, the device performances above threshold are worsen as the spacers' length is increased, due to their higher resistive contribution both at low and high temperatures.

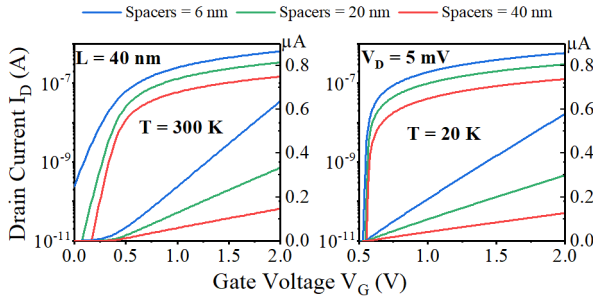


Figure 8. Simulated $I_D(V_G)$ for different L_{SD} at $T = 300 K$ (a) and $T = 20 K$ (b).

B. Simulations at high drain bias

In Fig. 9 (a) are reported several $I_D(V_D)$ curves from room to cryogenic temperature. It is possible to observe that below $V_D = 0.15V$, the device is in linear regime, independently on temperature. Above this value the current leaves the ohmic regime and starts to saturate. Moreover, the current does not increase as the temperature is lowered, since a constant mobility was used in this case. In Fig. 9 (b), $I_D(V_G)$ in saturation regime at both $T = 300 K$ and $T = 25 K$ are sketched. The subthreshold slope SS as well as the threshold voltage V_{th} increase at cryogenic temperature, following the trend already observed at low V_D values.

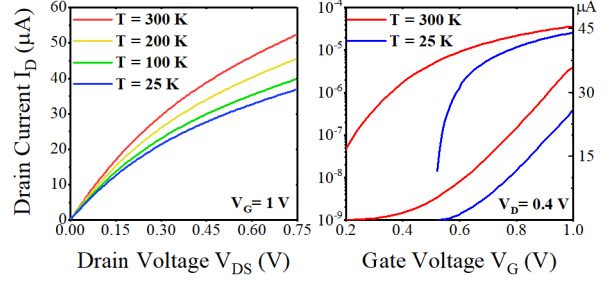


Figure 9. (a) $I_D(V_D)$ for different T and (b) $I_D(V_G)$ at $V_D = 0.4 V$.

C. Comparison with experimental data

A p-type *Si* Trigate nanowire was characterized down to deep cryogenic temperature. It is based on CEA-LETI FD-SOI NanoWire (NW) process flow [8] [9]. The device channel width is $W = 75 nm$, whereas its channel and spacer lengths are $L_G = 50 nm$ and $L_{SD} = 25 nm$, respectively. The silicon film thickness is $t_{si} = 17.9 nm$. Finally, the BOX thickness is $t_{BOX} = 145 nm$. The device longitudinal structure is close to that used in simulations and reported in Fig. 1. It is important to mention that p-type device's characteristics can be compared with simulations of n-type structure with no loss of information. Experimental $I_D(V_D)$ curves down to $T = 10 K$ are shown in Fig. 10 (a). It is worth to be noted that the current decreases with temperature. This is likely due to the mobility, which is fairly constant in temperature in this kind of structures [10]. Furthermore, $I_D(V_D)$ curves do not show a linear behavior for small V_D values below $T = 100 K$.

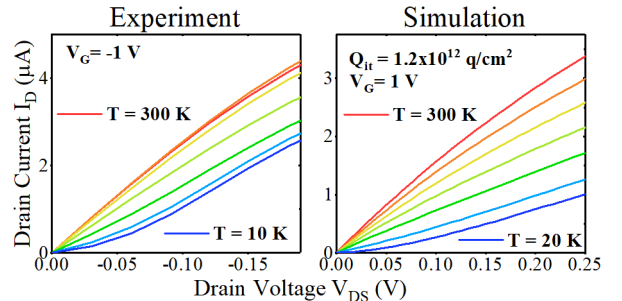


Figure 10. Experimental (a) and simulated (b) $I_D(V_D)$ for various T with a fixed amount of interface charges.

The reason could be linked to the presence of charges at the interface between the *Si* channel and the spacers. Indeed carriers, in order to populate the channel, must overcome a potential barrier caused by the thick spacers, that is enhanced by the presence of fixed charges [11] (Fig. 11 (a)). At low temperature, because of the reduced thermal energy, carriers hardly populate the regions underneath the spacers, as shown in Fig. 11 (b). Using a reasonable value for the fixed charge density, that is $Q_{it} = 1.2 \cdot 10^{12} q/cm^2$, it was possible to qualitatively reproduce the non-linear behavior of the $I_D(V_D)$ (see Fig. 10 (b)).

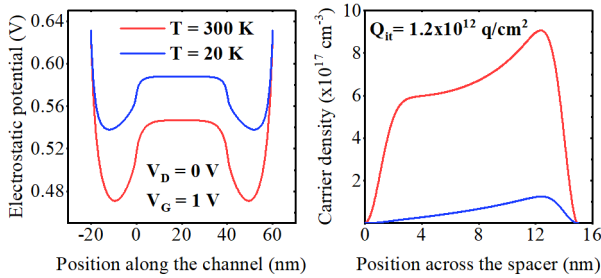


Figure 11. (a) Electrostatic potential and (b) carrier densities in strong inversion at $T = 300\text{K}$ and $T = 20\text{K}$, for a given amount of interface charges.

IV. CONCLUSIONS

In this paper, we demonstrated the feasibility of performing TCAD simulations of FD-SOI devices down to deep cryogenic temperatures and even at zero Kelvin. In order to do so, an approximated function of the Fermi-Dirac integral was introduced as well as the metallic degenerate statistics valid at zero temperature. Improvement of FDSOI device electrical performances at very low temperatures was clearly shown both in terms of threshold voltage, subthreshold slope and short channel effects. Moreover, the possibility of performing simulations at high drain bias voltages was proved. Finally, an unconventional behavior experimentally observed at temperatures below $T = 100\text{K}$ in devices with S/D spacers and similar to structure used in simulation was qualitatively reproduced and explained.

ACKNOWLEDGMENT

The author are grateful to Labex MINOS of French ANR ANR-10-LABX-55-01, the ERC Synergy QuCube (Grant No. 810504), and EU H2020 RIA project SEQUENCE (Grant No. 871764).

REFERENCES

- [1] B. C. Paz *et al.*, “Variability Evaluation of 28nm FD-SOI Technology at Cryogenic Temperatures down to 100mK for Quantum Computing,” in *2020 IEEE Symposium on VLSI Technology*, Honolulu, HI, USA, Jun. 2020, pp. 1–2. doi: 10.1109/VLSITechnology18217.2020.9265034.
- [2] R. Maurand *et al.*, “A CMOS silicon spin qubit,” *Nat Commun*, vol. 7, no. 1, p. 13575, Dec. 2016, doi: 10.1038/ncomms13575.
- [3] P. Dhillon, N. C. Dao, P. H. W. Leong, and H. Y. Wong, “TCAD Modeling of Cryogenic nMOSFET ON-State Current and Subthreshold Slope,” in *2021 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*, Dallas, TX, USA, Sep. 2021, pp. 255–258. doi: 10.1109/SISPAD54002.2021.9592586.
- [4] S. M. Sze and K. K. Ng, *Physics of semiconductor devices*, 3rd ed. Hoboken, N.J: Wiley-Interscience, 2007.
- [5] W. Hänsch, Th. Vogelsang, R. Kircher, and M. Orlowski, “Carrier transport near the Si/SiO₂ interface of a MOSFET,” *Solid-State Electronics*, vol. 32, no. 10, pp. 839–849, Oct. 1989, doi: 10.1016/0038-1101(89)90060-9.

- [6] S. Cristoloveanu and G. Ghibaudo, “Intrinsic Mechanism of Mobility Collapse in Short MOSFETs,” *IEEE Trans. Electron Devices*, vol. 68, no. 10, pp. 5090–5094, Oct. 2021, doi: 10.1109/TEDE.2021.3105083.
- [7] B. Cardoso Paz *et al.*, “Performance and Low-Frequency Noise of 22-nm FDSOI Down to 4.2 K for Cryogenic Applications,” *IEEE Trans. Electron Devices*, vol. 67, no. 11, pp. 4563–4567, Nov. 2020, doi: 10.1109/TEDE.2020.3021999.
- [8] L. Hutin *et al.*, “Si CMOS platform for quantum information processing,” in *2016 IEEE Symposium on VLSI Technology*, Honolulu, HI, USA, Jun. 2016, pp. 1–2. doi: 10.1109/VLSIT.2016.7573380.
- [9] S. De Franceschi *et al.*, “SOI technology for quantum information processing,” in *2016 IEEE International Electron Devices Meeting (IEDM)*, San Francisco, CA, USA, Dec. 2016, p. 13.4.1-13.4.4. doi: 10.1109/IEDM.2016.7838409.
- [10] E. Catapano *et al.*, “Modeling and simulations of FDSOI five-gate qubit MOS devices down to deep cryogenic temperatures,” *Solid-State Electronics*, p. 108291, Mar. 2022, doi: 10.1016/j.sse.2022.108291.
- [11] T. M. Frutuoso *et al.*, “Impact of spacer interface charges on performance and reliability of low temperature transistors for 3D sequential integration,” in *2021 IEEE International Reliability Physics Symposium (IRPS)*, Monterey, CA, USA, Mar. 2021, pp. 1–5. doi: 10.1109/IRPS46558.2021.9405107.