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Quentin Berlingard, Jose Lugo-Alvarez, Maryline Bawedin, Lauriane Contamin, Philippe Galy, et al.. Study of threshold voltage extraction from room temperature down to 4.2 K on 28 nm FD-SOI CMOS technology. *Solid-State Electronics*, 2022, 194, pp.108325. 10.1016/j.sse.2022.108325 . hal-03974969

HAL Id: hal-03974969

<https://hal.science/hal-03974969v1>

Submitted on 22 Jul 2024

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Study of threshold voltage extraction from room temperature down to 4.2K on 28nm FD-SOI CMOS technology

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Abstract – This paper aims to benchmark the threshold voltage extraction at cryogenic temperature. It presents two DC and for the first time one RF methods to extract the threshold voltage down to 4.2K for channel lengths down to 28 nm. Measurements are performed on CMOS transistors integrated in 28nm Fully Depleted Silicon-On-Insulator (FDSOI). First, two methods based on DC measurement are explained: the constant-current and the second derivative technique. Besides, the gate-channel capacitance derivative method based on RF measurements is presented. Finally, we discuss and compare the advantages and limits of these different methods.

Keywords – Threshold voltage extraction, FDSOI, CryoCMOS, cryogenic RF measurements

I. INTRODUCTION

Nowadays, with the development of electronics for aerospace or the control and read-out in quantum computing [1][2], many different circuits are designed to work at cryogenic temperature such as Low Noise Amplifiers (LNA) [3], or Voltage-Controlled Oscillators (VCO) [4]. The threshold voltage is a key parameter to design circuits with CMOS transistors. This voltage physically corresponds to the transition from weak inversion, where the inversion charge is exponentially dependant on the gate voltage V_{GS} , to strong inversion regime, where the inversion charge varies linearly with V_{GS} [5]. The transistor geometry induces variation in the threshold voltage: small transistors are subject to short channel effects and Drain Induced Barrier Lowering (DIBL) [5]. This transition voltage depends on the measurement temperature: at low temperature, it shifts to higher absolute values with a sensitivity around 0.5 to 1mV/K [6][7]. Whereas for bulk MOSFETs, the shift is explained by the temperature dependence of the Fermi level in the silicon channel, in FDSOI it is mainly due to the Fermi-Dirac distribution [5]. Therefore, it is important to define an accurate and physical extraction of the threshold voltage valid down to deep cryogenic temperature. FDSOI circuits appear as a very promising choice for cryogenic applications, thanks to their high electrostatic integrity, their

low variability and the threshold voltage control through the back gate [6][8–10]. Here, we study the extraction of the threshold voltage of CMOS transistors fabricated in 28nm FDSOI UTBB technology from STMicroelectronics [11]. We analyse, test and compare three different extraction methods using DC and RF measurements down to 4.2K.

II. EXPERIMENTS

We measured short and long NMOS transistors connected on common source configuration, fabricated in 28nm FDSOI technology, with an equivalent oxide thickness EOT of 1.1 nm [6]. Measurements were performed on a Lakeshore EMTTP4 cryogenic probe station between 300K and 4.2K. The whole set-up is presented in [12] along with the measurement protocol. We performed both DC and RF measurements on the same devices, using RF probes in Ground-Signal-Ground (GSG) configuration and bias tees.

There are many different methods to extract the threshold voltage with DC measurement [13]. This paper focuses on the constant current method [14] and on the second derivative technique [15] because they correspond to the threshold voltage condition $C_{inv}=C_{ox}$ in FDSOI transistors, with $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$ and C_{inv} the derivative of the inversion charge with respect to the surface potential [16][17].

a. CONSTANT-CURRENT METHOD

The constant-current method is often used in industry due to its straightforward application. The threshold voltage is extracted by taking the gate voltage for which a given fixed drain current level is reached. This critical drain current value is usually arbitrarily chosen in moderate inversion. Here as a first approximation, we chose [14]:

$$I_{d,const,300K} = \left(\frac{W}{L}\right) \times 10^{-7} [A] \quad (1)$$

However, if this value is independent of the temperature, it will not guarantee the same V_{th} condition within the temperature range [18]. In ref. [18], the author proposed to

use instead a Temperature-dependent criterion, to ensure a constant inversion charge Q_{inv} at inversion:

$$I_{d,const,T} = \left(\frac{T}{300}\right)^{1.6} I_{d,const,300K} \quad (2)$$

where T is the temperature in K. Figure 1 presents the $I_d(V_g)$ curves for different temperatures, and the corresponding $I_{d,const,T}$ criteria.

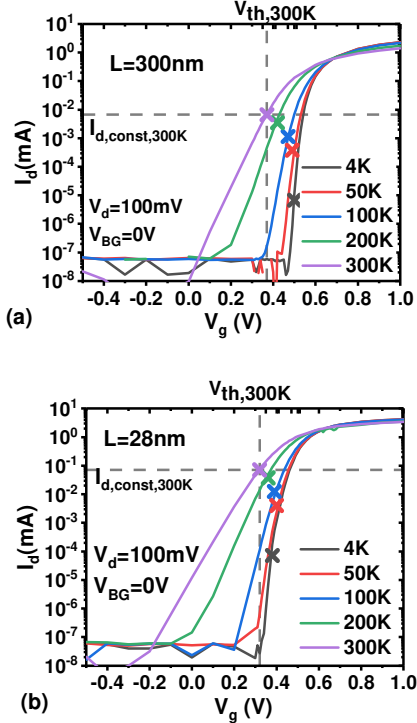


Figure 1. DC drain current versus gate voltage. The dotted lines correspond to the constant current value and to the threshold voltage at 300K. The extraction points of the threshold voltage are marked with a cross. (a) For device of $L=300\text{nm}$ and $W=20\mu\text{m}$. (b) For device of $L=28\text{nm}$ and $W=20\mu\text{m}$.

The limits of this method are the choice of the initial constant drain current $I_{d,const,300K}$ and the fact that the formula (2) is only accurate in the ohmic regime. According to [13], $I_{d,const,300K}$ is different depending on the condition chosen to determine the threshold voltage. For the small device on figure 1 (b), the curves at 4K exhibit a lower V_{th} than the one at 50K or 100K. This is due to Subthreshold behaviour which exhibits tunnelling through defects [19].

b. SECOND DERIVATIVE METHOD

The second derivative method consists in deriving twice the drain current with respect to the gate voltage. This method can be understood by considering an ideal transistor. In an ideal transistor, the drain current is equal to zero for $V_g < V_{th}$, and becomes proportional to V_g for $V_g > V_{th}$. Under these assumptions, the first derivative of the drain current with respect to the gate voltage is a Heaviside function $\theta(V_g - V_{th})$. Therefore, the second derivative is infinite when $V_g = V_{th}$. With a real transistor, this second derivative will not be infinite but it will reach a maximum at $V_g = V_{th}$, as it can be seen in Figure 2.

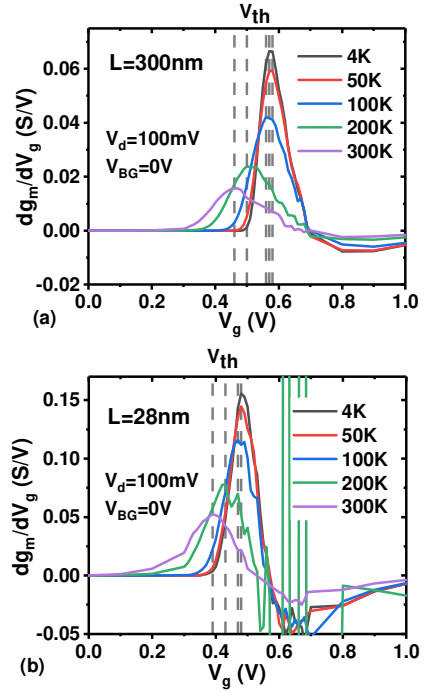


Figure 2. Derivative of the DC transconductance g_m with respect to the gate voltage versus gate voltage. The dotted lines correspond to gate voltage when dg_m/dV_g is maximum (i.e. to V_{th}). (a) For device of $L=300\text{nm}$ and $W=20\mu\text{m}$. (b) For device of $L=28\text{nm}$ and $W=20\mu\text{m}$.

Figure 2 (b) shows the limitations of this extraction method related to the measurement noise, which is amplified by the second derivative. In the short transistors, there are fewer carriers and the recombination centres are less active. Indeed, it leads to inaccurate value of threshold voltage. According to the measurement, the uncertainty is $\pm 0.01\text{V}$ for the large transistor and $\pm 0.05\text{V}$ for the small one.

c. RF EXTRACTION METHOD

Mathematically, the transition point between the weak inversion regime, where Q_{inv} is exponentially dependent of V_g , and the strong inversion regime, where Q_{inv} is linear with V_g , is given by the maximum of second derivative of Q_{inv} with respect to V_g [16]. It is equal to the maximum of the first derivative of the gate-to-channel capacitance C_{gc} with respect to V_g :

$$\max_{V_g} \left(\frac{d^2 Q_{inv}}{dV_g^2} \right) = \max_{V_g} \left(\frac{dC_{gc}}{dV_g} \right) \quad (3)$$

In RF measurements, this capacitance is evaluated by the gate capacitance C_{gg} , given as follows:

$$C_{gg} = C_{gd} + C_{gs} = \frac{\text{Im}(Y_{11})}{2\pi f} \quad (4)$$

Where f is the frequency and Y_{11} is the input admittance on the transistor gate [20] measured with the Vector Network Analyser (VNA). The gate capacitance (C_{gg}) is mainly due to the channel capacitance (C_{gc}) contribution and increases with the inversion charge. The gate capacitance and its derivative with respect to gate voltage are presented in Figure 3.

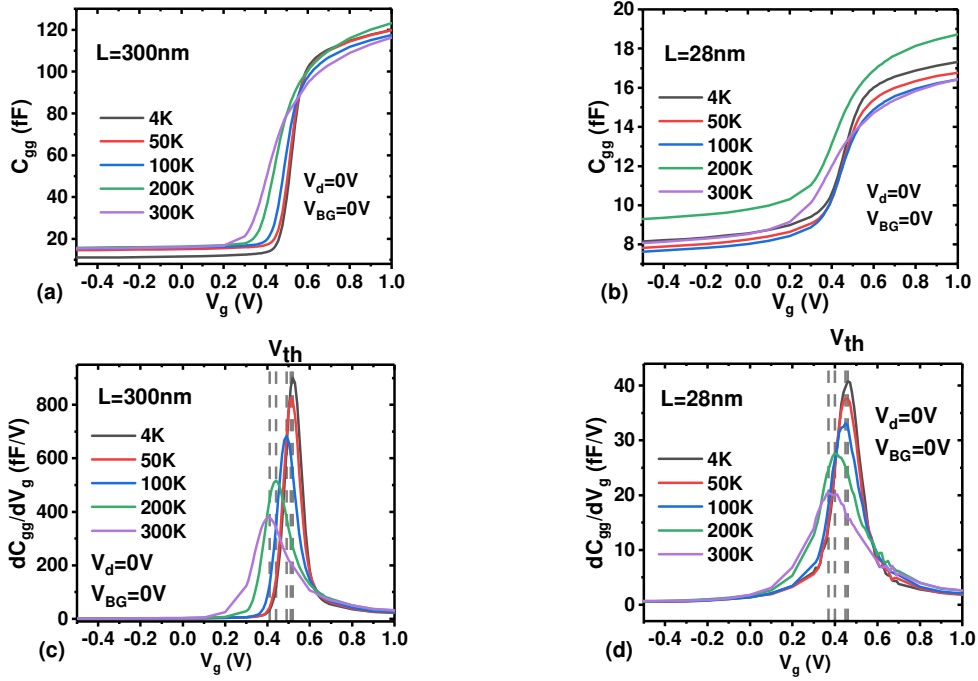


Figure 3. (a) and (b) Gate capacitance averaged between 1 to 5 GHz versus the gate voltage. (c) and (d) Derivative of the gate capacitance with respect to the gate voltage. The dotted lines correspond to gate voltage when dC_{gg}/dV_g is maximum (i.e. to V_{th}). (a) and (c) For device of $L=300\text{nm}$ and $W=20\mu\text{m}$. (b) and (d) For device of $L=28\text{nm}$ and $W=20\mu\text{m}$.

The limits of this method is the measurement noise introduced by the first derivative. The advantages regarding the other extraction techniques are two-fold: it is independent of series resistance and of transport properties of the channel carriers. The second advantage is the accuracy of this method. The errors bar is $\pm 0.01\text{V}$ for all measured transistors and temperature. It is low compared to the DC methods, as shown in Figure 4. and 5. Even if there are parasitic capacitance contributions, the transition between weak and strong inversion leads to a net change in the capacitance value (Figure 2 (b)) and to a precise maximum for the derived capacitance (Figure 2 (d)). Thus, the threshold voltage can also be performed on very small gate area with a good accuracy.

III. RESULTS AND DISCUSSION

As shown in Figure 4. and Table 1. for relatively long devices, we see that all the methods present a similar variation of the threshold voltage with respect to the temperature decrease, differing only by a shift smaller than 80mV. On the other hand, for small devices (Fig.5 and Table 2), the CC method diverges from the other ones below 50K. The second derivative and the RF capacitance methods present similar variation.

The temperature sensitivity of V_{th} is 0.3-0.4mV/K from 300K to 100K. Below 100K the threshold voltage tends to saturates as reported for other technologies [7].

The shift between V_{th} values given by the different methods can be explained as RF capacitance method is purely based on a charge variation, whereas the DC ones are mediated by the current.

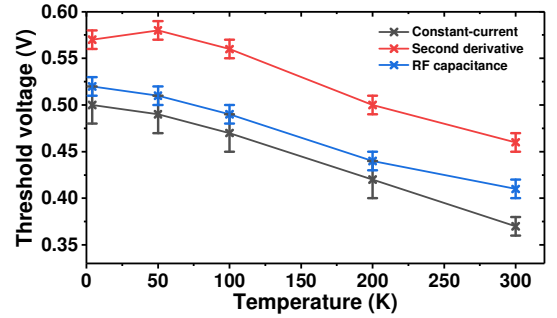


Figure 4. Threshold voltage extracted by different methods as a function of temperature ($V_d=100\text{mV}$ and $V_{BG}=0\text{V}$). For device of $L=300\text{nm}$ and $W=20\mu\text{m}$

Temp.	CC	SD	RF capa.
300K	$0.37 \pm 0.01\text{V}$	$0.46 \pm 0.01\text{V}$	$0.41 \pm 0.01\text{V}$
200K	$0.42 \pm 0.02\text{V}$	$0.5 \pm 0.01\text{V}$	$0.44 \pm 0.01\text{V}$
100K	$0.47 \pm 0.02\text{V}$	$0.56 \pm 0.01\text{V}$	$0.49 \pm 0.01\text{V}$
50K	$0.49 \pm 0.02\text{V}$	$0.58 \pm 0.01\text{V}$	$0.51 \pm 0.01\text{V}$
4.2K	$0.50 \pm 0.02\text{V}$	$0.57 \pm 0.01\text{V}$	$0.52 \pm 0.01\text{V}$

Table 1. Threshold voltage values for different extraction methods and different temperature. (CC = Constant Current method with temperature correction, SD = Second Derivative method and RF capa. = gate capacitance channel derivative method). For device of $L=300\text{nm}$ and $W=20\mu\text{m}$

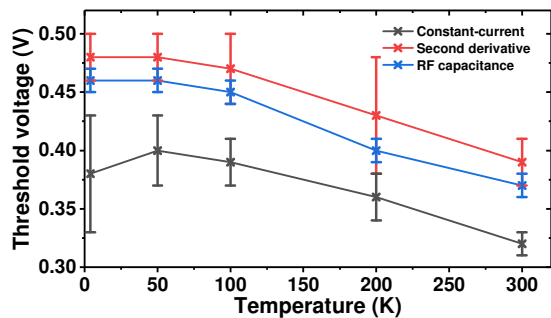


Figure 5. Threshold voltage extracted by different methods as a function of temperature ($V_d=100\text{mV}$ and $V_{BG}=0\text{V}$). For device of $L=28\text{nm}$ and $W=20\mu\text{m}$.

Temp.	CC	SD	RF capa.
300K	$0.32 \pm 0.01\text{V}$	$0.39 \pm 0.02\text{V}$	$0.37 \pm 0.01\text{V}$
200K	$0.36 \pm 0.02\text{V}$	$0.43 \pm 0.05\text{V}$	$0.4 \pm 0.01\text{V}$
100K	$0.39 \pm 0.02\text{V}$	$0.47 \pm 0.03\text{V}$	$0.45 \pm 0.01\text{V}$
50K	$0.4 \pm 0.03\text{V}$	$0.48 \pm 0.02\text{V}$	$0.46 \pm 0.01\text{V}$
4.2K	$0.38 \pm 0.05\text{V}$	$0.48 \pm 0.02\text{V}$	$0.46 \pm 0.01\text{V}$

Table 2. Threshold voltage values for different extraction methods and different temperature. (CC = Constant Current method with temperature correction, SD = Second Derivative method and RF capa. = gate capacitance channel derivative method). For device of $L=28\text{nm}$ and $W=20\mu\text{m}$

IV. CONCLUSION

In this work, we presented three different methods under interest at low temperature to extract the threshold voltage. We highlighted that the RF extraction method is the most performant one at cryogenic temperature because it is insensitive to the series resistance, still valid at cryogenic temperature and can be performed on every transistor sizes.

V. ACKNOWLEDGEMENTS

The authors are grateful to Labex MINOS of French ANR ANR-10-LABX-55-01. The authors acknowledge Spintec and especially Cécile GREZES, Aurélie KANDAZOGLU and Laurent VILA for their help with the experimental setup. This work benefited from the facilities and expertise of the OPE(N)RA characterization platform of FMNT (FR 2542, fmnt.fr) supported by CNRS, Grenoble INP and UGA. We would like also to thank STMicroelectronics for 28nm FDSOI samples delivery.

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