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Reconfigurable Complementary and Combinational Logic Based on Monolithic and Single-Crystalline Al-Si Heterostructures

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Metal-semiconductor heterostructures providing geometrically reproducible and abrupt Schottky nanojunctions are highly anticipated for the realization of emerging electronic technologies. This specifically holds for reconfigurable field-effect transistors, capable of dynamically altering the operation mode between n- or p-type even during run-time. Targeting the enhancement of fabrication reproducibility and electrical balancing between operation modes, here a nanoscale Al-Si-Al nanowire heterostructure with single elementary, monocrystalline Al leads and sharp Schottky junctions is implemented. Utilizing a three top-gate architecture, reconfiguration on transistor level is enabled. Having devised symmetric on-currents as well as threshold voltages for n- and p-type operation as a necessary requirement to exploit complementary reconfigurable circuits, selected implementations of logic gates such as inverters and combinational wired-AND gates are reported. In this respect, exploiting the advantages of the proposed multi-gate transistor architecture and offering additional logical inputs, the device functionality can be expanded by transforming a single transistor into a logic gate. Importantly, the demonstrated Al-Si material system and thereof shown logic gates show high compatibility with state-of-the-art complementary metal-oxide semiconductor technology. Additionally, exploiting reconfiguration at the device level, this platform may pave the way for future adaptive computing systems with low-power consumption and reduced footprint, enabling novel circuit paradigms.

1. Introduction

Modern society is highly depending and relying on electronic computing devices, as for example, employed in efficient servers, personal computers, and mobiles, and currently being explored toward the realization of emerging computing paradigms, such as "artificial intelligence" and the "Internet of Things".[1] A key enabler for these paradigms is the complementary metal-oxide-semiconductor (CMOS) technology, which utilizes the concept of complementary n- and p-type field-effect transistors (FET) to construct Boolean logic gates. Importantly, in CMOS technology the logic functions are fixed by the physical layout of interconnects and the definition of doped regions and thus do not allow for a flexible alteration of the circuits after production. The continuous shrinking of feature sizes of these Si metal-oxide-semiconductor field-effect transistors (MOSFETs) has been providing performance enhancement and higher power efficiency throughout the last decades. However, classical scalability is limited[2] and the static nature of the MOSFET primitives was not developed to provide runtime-adaptability as required for new circuit paradigms. A concept to overcome the static nature in CMOS technology and reduce overall circuit area and power consumption are reconfigurable FETs (RFETs),[3–5] encompassing a broad family of devices that enable a reconfiguration of the dominant carrier type based on either Schottky-barrier field-effect transistors (SBFET),[4,6–9] or steep slope band-to-band tunneling transistors (TFET),[10–13] capable of dynamically altering the device operation between n- and p-type. This device concept thus gives rise to a paradigm change where devices, circuits, and even systems are actively and dynamically reconfigured after manufacturing or, as particularly noteworthy, even during run-time, enabling an adaption to the needed logic function of a circuit. Importantly, this "fine-grain" approach is fundamentally different to the already available "coarse-grain" approach followed in field programmable gate arrays (FPGAs)[14] based on signal routing to predefined logic blocks, resulting in high latency in data

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transfer and substantial chip area consumption. Reconfigurable electronics utilizing RFETs on the other hand is enabled by a device layout with independent gates inducing in addition to the gated region in conventional FETs an additional energy barrier along the channel, effectively blocking the undesired charge carrier type, and thus enabling unipolar n- or p-type operation. In this respect, the most common approach is utilizing metal-semiconductor heterostructures embedded in a SBFET.[15] In this configuration, RFETs have already been fabricated based on Si,[4,8,16] Ge,[17–19] and also on 2D layered systems, like WSe_2,[20,21] or $MoTe_2$,[22,23] and recently with black phosphorous.[24] Latest generation RFETs facilitate a device layout with three independent top-gates to induce additional energy barriers in the channel, enabling an even more effective suppression of the undesired charge carrier type and therefore favoring n- or p-type operation, respectively.[4,25] Simultaneously with more sophisticated device architectures, the development of the first logic gates, exploiting reconfiguration on a logic gate level, emerged. A graspable example is a NAND gate, which can be dynamically reprogrammed to NOR functionality when built from RFETs.[26] Additionally, it has been predicted by simulations that exploiting three-gate RFETs, compact realizations of XOR and majority (MAJ) based combinatorial circuits can be envisioned using a lower number of transistors than in classical CMOS technology.[8] Based on these investigations a number of circuit level features, such as dynamic reconfiguration,[26,27] intrinsic XOR,[28] and wired-AND capabilities[29] as well as control of threshold voltage,[30] and suppression of parasitic charge sharing effects in dynamic logic gates,[31,32] have been demonstrated for RFETs, providing additional benefits over their CMOS counterparts. In this respect, fabricating reliable and reproducible metal-semiconductor junctions is essential, as the injection of charge carriers highly depends on the metal-semiconductor interface, junction area, and its incorporated energy barrier. In consequence the on-current as well as the threshold voltage symmetry depends on the material choice. For Si and Ge based RFETs and SBFETs this has been achieved by thermally induced solid state reactions forming different kinds of intruded metal-silicide[33,34] and -germanide[35] segments. In the latter case of Ge channels a thermally driven exchange reaction is also able to provide intruded single elementary metals providing a flat, clean and sharp junctions.[36] Such exchange reacted Al-Ge[37] and Al-Si[38] junctions overcome difficulties with the reproducibility of Schottky junctions as the process avoids instability issues otherwise common during intermetallic phase formation of metal silicides and germanides.[33,39] For RFETs and other emerging devices an accurate control of phase formation becomes necessary as different phases and related lattice strain yield a variability in barrier heights and thus in the electronic injection properties.[40] Further on, phase instabilities lead to a junction patchiness that translates into additional variability of electrical performance.[41] Indeed, commonly employed metal-silicides make the addition of further alloying elements such as for example, Pt or Sn in nickel-silicides necessary to improve morphology and stabilize crystallographic phases.[42,43] Thus, it can be argued that the addition of further elements restricts the flexibility in semiconductor processing and introduces a change in Schottky barrier height,[44] that would be otherwise avoided with the appropriate use of single element metals as exploited here with Al. In this context, the Al-Si exchange mechanism forming single-elementary Al contacts to Si channels, shows less device-to-device variation[38,45] and allows subsequent annealing steps without changing the composition of the metallic lead.

2. Results and Discussion

In this paper, we report on a CMOS compatible RFET platform utilizing nanoscale monolithic Al-Si heterostructures, obtained from a thermally induced heterostructure formation, with abrupt single-elemental metal-Si interfaces and highly symmetric effective Schottky barriers for electrons and holes. Across the discussion of results, the metal-semiconductor combination and its suitability for the proposed devices will become evident for realizing complementary logic gates.

For device fabrication and as a simple integration vehicle, vapor–liquid–solid (VLS)-grown, single-crystal, nominally intrinsic Si nanowires (NWs) with ⟨112⟩ orientation and diameters of approximately $d_{NW} = 80$ nm are employed. Measured by scanning transmission electron microscopy (STEM), the NWs are enwrapped in a 8.5–9.7 nm thick thermally-grown SiO_2 shell and are further integrated into a SBFET architecture. A thermally induced Al-Si exchange reaction at $T = 774$ K was utilized to define the Si channel length monolithically embedded in an Al-Si-Al NW heterostructure providing the necessary single elementary metal contacts and sharp metal-semiconductor junctions.[38] In this work, NWs are used as a prototyping vehicle to demonstrate the capabilities of Al-Si based RFETs and logic circuits. In this respect, the exact placement of VLS-grown NWs bears a challenge in CMOS integration and the realization of complex logic circuits. Nevertheless, a feasible approach to overcome this issue is to use in-plane solid–liquid–solid grown NWs[46] in combination with guided or patterned ledges. Thereby, NW thickness, alignment, orientation, and pitch can be controlled even when stacking NWs vertically along sidewall grooves.[47] Notably, it was shown that the Al-Si exchange mechanism also works in silicon-on-insulator (SOI) based nanosheets and thus should allow the realization of RFETs and more complex logic circuits using top-down fabrication.[38] Due to the stable crystal phase of the intruded metallic segments, the applied Al-Si exchange appears to show significantly reduced geometric, crystallographic, and morphologic variabilities compared to state-of-the-art thermally induced Ni_xSi_{1-x}-Si NW heterostructures.[48,49] Embedded in a three-independent gate transistor architecture the functionality enhanced operation compared to that of a conventional MOSFET is reached (see Figure S1, Supporting Information). Through the use of the polarity gate (PG) electrodes, which are placed directly atop the abrupt Al-Si junctions, the off-current is efficiently suppressed and furthermore reconfiguration of transistor polarity is achieved. Setting a positive program voltage V_{PG} leads to predominant electron conduction and blocking of holes, whereas a negative V_{PG} results in predominant hole conduction. Thus, the device operation can be altered between n- and p-type modes even at run-time. In correlation to a conventional MOSFET the control gate (CG) allows to adjust the

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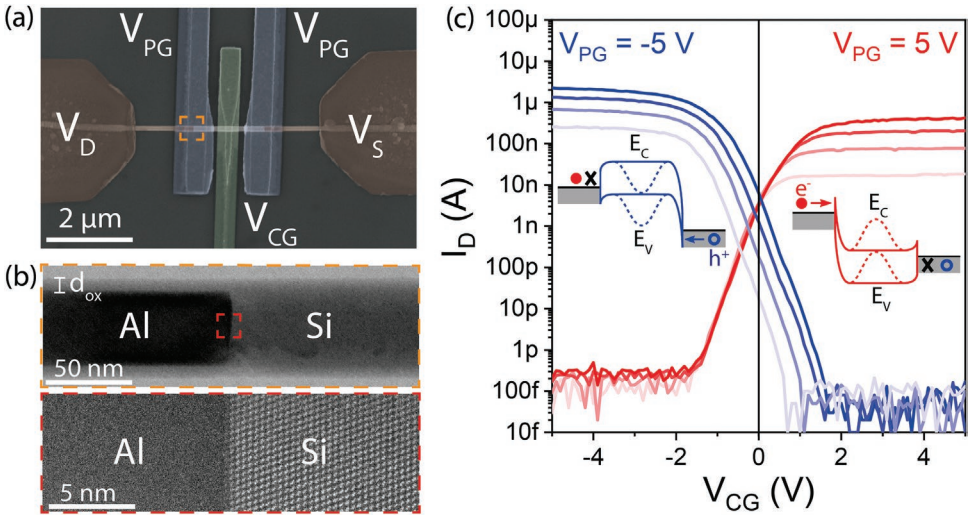

Figure 1. a) Colored SEM image of an Al-Si-Al heterostructure with L_{Si} = 1.5 µm embedded in a three-gate FET architecture enabling RFET operation. b) BF STEM image showing the Al-Si interface of the NW heterostructure, where the Si region is oriented in the [110] zone axis. The NW is enwrapped in a thermally grown SiO_2 shell with a thickness of d_{ox} = 9 nm. The lower panel shows a HAADF STEM zoomed-in view of the Al-Si interface indicating a sharp metal-semiconductor junction. c) Subthreshold transfer characteristic for bias voltages of V_D = 0.25, 0.5, 0.75, and 1 V showing unipolar n-type (red) and p-type (blue) operation set by V_{PG}. The schematic band diagrams of n- and p-type device operation are inserted, where the solid and dotted lines depict the on- and off-states for n- and p-type operation, respectively.

charge carrier density in the channel and thus to turn the transistor on and off by setting the corresponding voltage. The detailed underlying physical mechanism of RFETs was thoroughly elaborated and investigated in the past.[50–52] Although different operation modes exist[50] the most efficient gate-tunability is achieved by placing the CG top-gate electrode in-between the PGs, allowing to directly capacitively couple to the semiconductor active region and avoiding coupling to the Schottky junctions.[53] **Figure 1**a shows a scanning electron microscopy (SEM) top view image of such a RFET with L_{Si} = 1.5 µm. Importantly, the PGs are electrically interconnected, which supports the realization of a symmetric device architecture. Electrically connecting the PGs allows to increase the performance in terms of reducing the complexity as well as achieving low off-currents in comparison to asymmetrically biasing the PG electrodes. Note that independently (and asymmetrically) biasing the PGs would, under some circumstances, lead to more symmetric currents, but with considerable costs in reduced on-currents and signal overhead. Self-aligned techniques have readily been shown for the fabrication of such structures,[8] simplifying device fabrication and facilitating downscaling of the devices. Although we focus on fairly large channel lengths for demonstration purposes the RFET concept is physically scalable, [54] recently scalability down to 10 nm nodes has been verified by device TCAD simulations.[55,56] Nevertheless, the structural sizes of RFETs are by far exceeding state-of-the-art CMOS MOSFETs. However, they allow a circuit design that significantly reduces the chip area for the same logic operation compared to standard CMOS technology. Bright field (BF) and high angle annular dark field (HAADF) STEM images of the Al-Si junction enwrapped in a 9 nm thick SiO_2 shell of the abrupt Al-Si interface are shown in Figure 1b. The shown NW was grown in ⟨111⟩ direction. Figure 1c shows the subthreshold transfer characteristic of both program modes for different drain biases V_D, ranging from 250 mV to 1 V in 250 mV steps. Note that, V_D was set to positive biases and thus causing the fanning to be evident in the p-type transfer characteristic due to the induced band bending mechanism (see Figure S2, Supporting Information). Remarkably, at V_D = 1 V an I_{on}/I_{off} ratio of 10^7 is achieved for $|V_{CG}|$ = 5 V. Importantly and different to conventional MOSFETs, the off-current is V_D-independent and ultra-low (below the sensitivity limit of our measurement equipment). This indicates efficient suppression of the static power consumption in the off-state as well as suppression of gate induced barrier lowering (GIDL) as enabled by the RFET device principle. Interestingly, the on-current (in brackets normalized to the diameter of the NW) for n-type operation is I^n_{on} = 422 nA (4.7 µA µm^{-1}) and I^p_{on} = 2.26 µA (25.4 µA µm^{-1}) for p-type operation. Regarding the on-currents the diameter (here: d_{NW} = 80 nm) needs to be taken into account as well, as it is not possible to fully deplete the semiconductor in comparison to thinner NWs.[57] Lately, it was shown that the Al-Si exchange can also be used on SOI-based nanosheets,[38] allowing a convenient way to increase on-current by fabricating parallel arrays of nanosheets. It was also shown that contact printed NWs allow to be integrated in parallel arrays as well.[58] Consequently, the proposed Al-Si NW RFET, revealed an on-current level symmetry factor of ≈5 between n- and p-type operation. At a first glance the difference seems large but it is substantially lower compared to prior-art Si based RFETs with state-of-the-art nickel silicide contacts,[57,59–61] reaching asymmetry ratios 2–5 times larger than with the here proposed Al-Si system. The relatively high symmetry was achieved without any additional efforts, as that is, precise strain engineering[62] or asymmetric biasing of program voltages. A more detailed comparison of the most relevant transistor parameters of Si- and Ge-based RFETs can be found in the supporting information (see Table S1, Supporting Information).

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Analyzing the effective Schottky barrier heights (eSBHs) of the proposed material system at different biases, reveals 119 meV for electron injection and 82 meV for hole injection, indicating substantial barriers for both polarities and explaining the observed level of symmetry of the on-currents. Although, somewhat similar effective eSBHs for both carrier types were measured,[38] a small difference is still evident. This can be attributed to the fact, that the effective tunneling masses of electrons and holes in Si differ, further influencing the tunneling probability[63] and thus the on-state of the RFET. Due to the excellent quality of the thermally grown SiO_2 gate dielectric in respect to the density of trap states[63] and fixed charges, as well as minimal Au and amorphous Si contamination of the as-grown NW surface,[64] no remarkable shift of the threshold voltage is observable. The high quality of the surface oxide is also reflected in the minimal hysteresis, observed when sweeping V_{CG} (see Figure S3, Supporting Information). Evaluating temperature-dependent transfer characteristics at elevated temperatures showed that the characteristic gets shifted to higher current values, likely reflecting a higher intrinsic carrier concentration and higher rate of injection of charge carriers from the Al-Si heterojunctions (see Figure S4, Supporting Information). In n-type operation a threshold voltage of V_{th} = 500 mV and in p-type operation V_{th} = −600 mV was extracted by utilizing the transconductance method (see Figure S5, Supporting Information).[65] The presented device shows subthreshold slopes of S = 216 and 366 mV dec^{-1} for n- and p-type, respectively. In order to lower the inverse subthreshold slope S and the threshold voltage V_{th} for future implementation of the presented Al-Si based RFET platform, the effective gate oxide thickness (EOT) needs to be reduced, either by thinning down the SiO_2 or implementing conventional high-κ gate dielectrics.[66]

To complement the electrical characterization of the proposed Al-Si NW RFET, the output characteristic as well as the conductance map of the n- and p-type operation mode is discussed. **Figure 2**a shows the I/V characteristic for n-type operation in combination with the corresponding drain–source conductance map for positive drain biases V_D and positive V_{PG}. The respective I/V characteristic as well as conductance map for the p-type operation is illustrated in Figure 2b with negative bias voltages V_D and negative V_{PG}. In both operation modes, a nonlinear increase of the V_{CG}-dependent I/Vs is evident, which is a signature of the progressive tuning of the barrier shape and is a typical feature of SBFETs.[53,62] Importantly, the conductance maps reveal the well-defined on- and off-state of the proposed Al-Si NW RFET. This representation

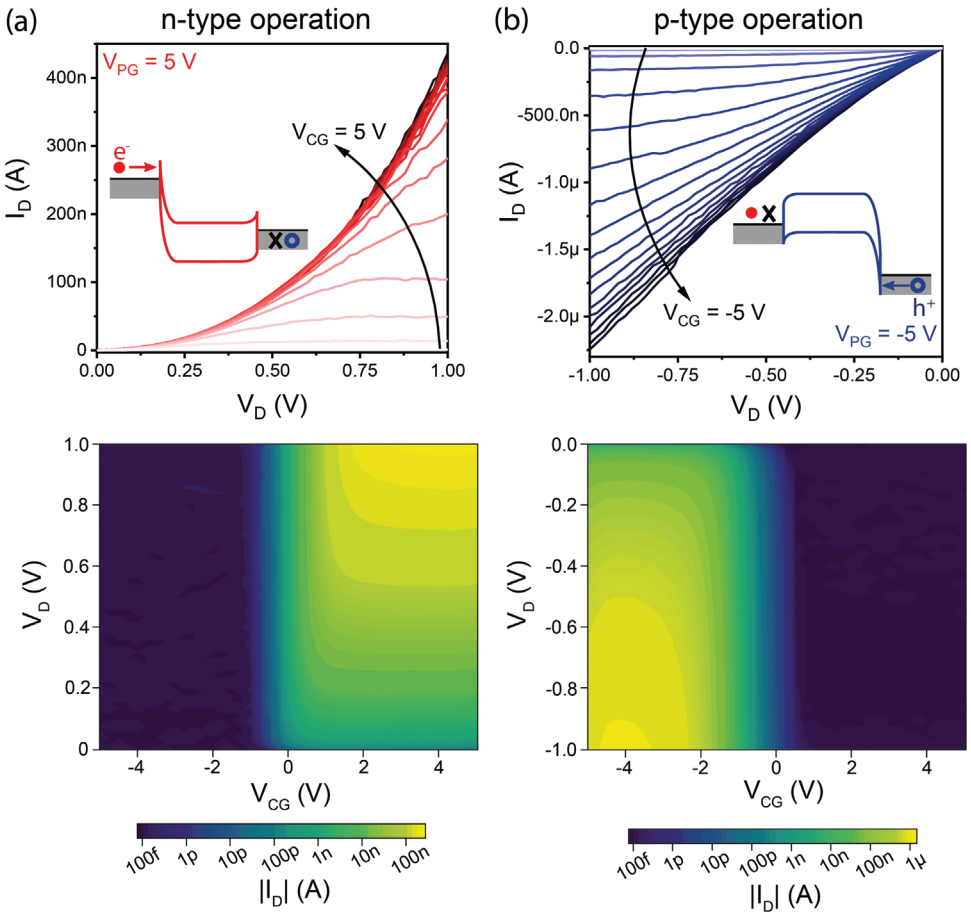

Figure 2. Linear I/V characteristic and semi-logarithmic conductance map of the a) n-type (V_{PG} = 5 V) and b) p-type (V_{PG} = −5 V) operation. Here, V_{CG} was increased in 250 mV steps. The respective band diagrams for the on-state are shown in the insets. The conductance maps reveal unipolar characteristics and well-defined on- and off-states in both operation modes.

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confirms the operational stability of our devices, for example, due to voltage variabilities in the applied circuits. Consequently, these conductance maps allow us to derive optimal operation points of the device. Due to the relatively high on-current as well as threshold voltage symmetry, the Al-Si material system allows the realization of well-defined operation modes of RFETs, enabling reconfigurable logic gates. For the Al-Si-Al based RFET, an absolute value of $|V_{PG}| = |V_{CG}| = V_D = 3$ V was determined for the ideal operation of logic gates, as this bias level sufficiently tunes the incorporated energy landscape of the semiconductor as well as drives an appropriate drain current. In this respect, additional investigations (see Figure S6, Supporting Information) were carried out to evaluate equal voltage levels for the top-gate voltages as well as drain biases. We want to note, that the application of a shorter channel region and a thinner or different gate-dielectric with higher κ would allow to decrease the supply voltages without performance penalty.[54]

To illustrate the capabilities of the Al-Si material system for reconfigurable logic, the proposed RFETs were first integrated into a complementary inverter utilizing the presented Al-Si RFET devices. To this end, one RFET is operated in n-mode (pull-down transistor) by applying $V_{PG} = 3$ V, whereas the pull-up transistor is operated in p-mode with $V_{PG} = -3$ V. This reveals one of the key advantages of RFETs, which is the capability to use the exact same device layout that is, geometry and composition for both n- and p-type operation, enabling a vast variety of applications such as functional diverse adaptive computing and hardware secure circuits.[24,27,67] Demonstrating this fundamental logic gate, the proposed Al-Si NW RFET architecture proofs the applicability of the Al-Si RFET platform to be implemented in complementary logic gates. **Figure 3** shows the realized complementary inverter based on the presented Al-Si RFET device. As the NWs exhibit overall lengths of $L \approx 20$ µm, the inverter can be implemented in 1D, that is, along a single NW, as also showed by Heinzig et al., in $NiSi_2$-Si NW RFETs[68] encompassing in our case two Si regions and three Al segments. Therein one segment is configured deliberately as n- or p-type mode. Figure 3b shows the transient operation of the inverter: V_{IN} is driven by a function generator to determine the response on the output. Utilizing this configuration allows us to analyze the output signal V_{OUT} and shows the expected toggling between the supply voltages V_{DD} and V_{SS}, where $V_{DD} = 3$ V and $V_{SS} = 0$ V. Note that the input signal is fed to both RFETs via the CGs. Importantly, the operation is ensured with a single voltage of 3 V. The complementary nature of the proposed inverter becomes evident by evaluating the current through the two RFETs in series, which reveals negligible current flow at the stable states and only current-peaks of ≈200 pA at the transient condition exactly at the switching points of the input voltage. Exchanging the potential of V_{PG} and in consequence also configuring both RFETs to the opposite mode, leads to qualitatively the same results, which is an important prerequisite for circuit and layout designers, as the flexibility of the proposed inverter is highly increased in comparison to static CMOS technology when building up more complex combinational logic gates. Care was taken to adjust the supply-rail voltages V_{DD} and V_{SS} appropriately. To manage this signal overhead in more complex gates a concept for exchanging the supply line voltages on-the-fly was presented by Trommer et al.[26] Through the use of a single inverter the supply lines as well as the program voltage can be flipped jointly, allowing for a full output swing of the logic gates.

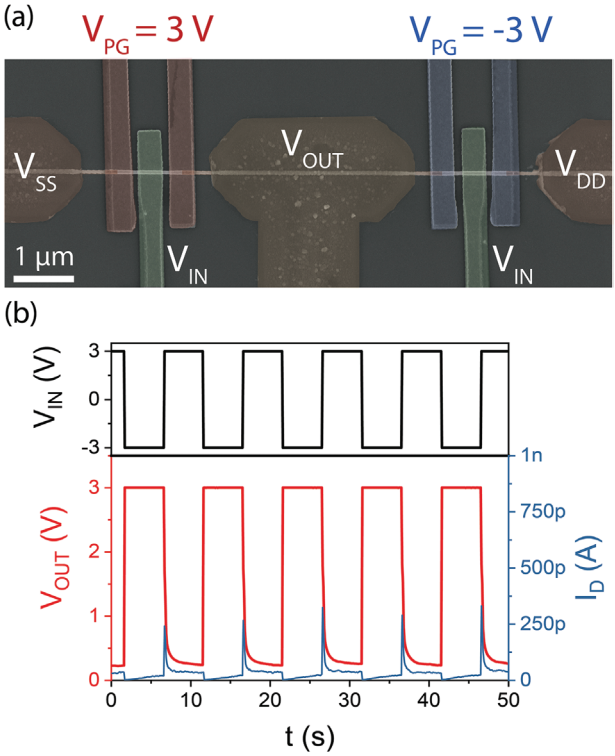

Figure 3. a) Colored SEM image of two Al-Si-Al NW heterostructure-based RFETs in series, realizing a complementary inverter by exploiting reconfiguration on transistor level. b) Transient operation of the proposed inverter with top-gate voltages as well as a drain bias of |3 V|. The drain current I_D shows an explicit complementary function of the presented inverter.

As an extension to the complementary design of the inverter, the realization of a wired-AND gate can be facilitated by adding a second CG in the middle of the Si channel, resulting in an additional electrode to turn the RFET on and off. Consequently, the two CGs can be used as input signals enabling a wired-AND gate.[25,29] **Figure 4**a shows a colored SEM image of the used device architecture with two CGs between the PGs. As for the wired-AND gate the current through the transistor defines the logical output, adapting to conventional CMOS technology, a resistor or even another three top-gate Al-Si NW RFET can be used to convert the current to a logical output at a desired voltage level. This once more underscores the flexibility of the presented device architecture. Due to its suitability to drive appropriate currents, it is well-suited as a replacement for NAND logic realized with conventional MOSFET technology (see Figure S7, Supporting Information). Moreover, it allows the reduction of the transistor count in multiple input NAND and NOR circuits, as two MOSFETs can be combined in a single device (inset in Figure 4a). Importantly, the number of inputs can be increased for the realization of multi-input logic cells, as its capability is merely limited by the length of the semiconducting channel. In this respect, top-down fabricated nanostructures[38] are of high relevance as the NW

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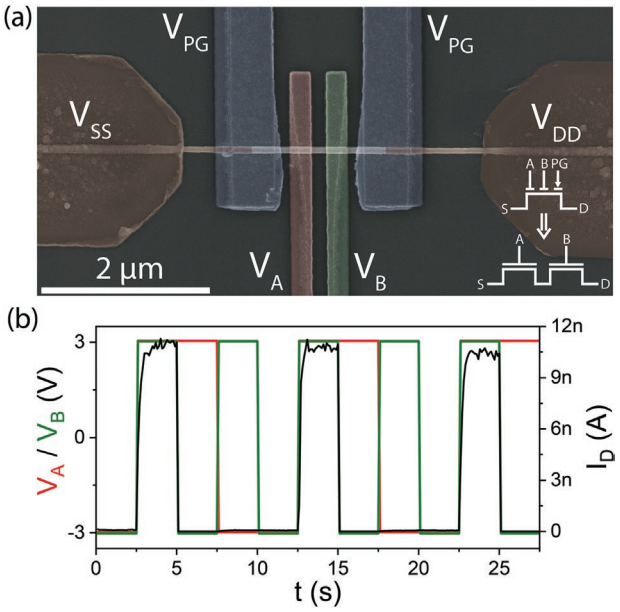

Figure 4. a) Colored SEM image of a multi control-gate Al-Si-Al NW heterostructure based RFET, realizing a wired-AND gate. In the right lower inset the equivalent symbol in comparison to conventional CMOS technology is illustrated. b) Transient operation of the proposed gate operated in *n*-mode (V_{PG} = 3 V). V_A is driven with 0.1 Hz and V_B with 0.2 Hz. Here, V_{DD} = 3 V and V_{SS} = 0 V. The current I_{DD} through the device defines the output of the wired-AND gate.

positioning can be carried out deterministically. Analyzing the transient operation mode of the wired-AND gate in Figure 4b reveals its capability of properly suppressing the current in the off-state as well as shows on-currents of ≈10 nA in n-type operation mode. The excellent current driveability allows the realization of logical gates with dedicated pull-up and pull-down networks, as proposed alternatively to conventional NAND logic cells (see Figure S7, Supporting Information). While the current levels of a device based on a single NW reveals currents in the nA range, utilizing a parallel array of NWs by top-down fabrication would allow an effective up-scaling of the current.[69] As the wired-AND gate is an extension of the previously presented RFET, this logic cell can also be operated in p-type operation mode by setting V_{PG} = −3 V. In this configuration the current is driven when both input signals, V_A and V_B are at −3 V, expressing a high degree of flexibility for circuit and layout designers in addition to the symmetric device layout of the RFET device architecture. As this paper demonstrates the capability of the Al-Si material system to be integrated as basic logic cells, no dedicated investigations on higher frequencies were done. Nevertheless, mixed mode TCAD simulations have already shown operability of Si-based RFETs in the GHz-regime.[54]

3. Conclusion

In conclusion, we have embedded a monocrystalline Al-Si-Al NW heterostrucutre with abrupt Schottky nanojunctions and single elementary metal leads into a three-gate RFET architecture capable of dynamically switching between n- and p-type operation. Key advantage of the proposed platform is a high degree of symmetry in terms of on-currents and threshold voltages. Operating the device in n- or p-type operation mode lead to on-currents I^{n}_{on} = 422 nA/I^{p}_{on} = 2.26 µA, threshold voltages V^{n}_{th} = 500 mV/V^{p}_{th} = −600 mV and subthreshold slopes S^{n} = 216 mV dec^{-1}/S^{p} = 366 mV dec^{-1}. Evaluating the output characteristic and investigating the corresponding conductance maps, an optimal operation point for the realization of a complementary inverter was determined operating at the same voltage levels for both the supply and the input voltage (here: |3 V|). The inverter was realized implementing two RFETs in series based on a single NW. Underlining the flexibility of the presented RFET platform, a CMOS compatible wired-AND gate is shown based on a dual CG device architecture. Such multi-CG RFETs allow a reduction in the transistor count in logic circuits such as NAND gates, where multiple MOSFETs can be combined in a single device. Most importantly, systematically investigating multi-gate transistor architectures, we have demonstrated a high degree of flexibility of the proposed Al-Si based RFETs, which can become a key enabler for the realization of reconfigurable electronics based on single elementary metal-semiconductor heterostructures. Most notably, concepts like the proposed wired-AND feature a high potential as an extension to conventional CMOS technology. In this respect, our investigations might provide a significant step toward beyond-CMOS logic enabling diversification and alternative computing paradigms.

4. Experimental Section

Device Fabrication: The Si NWs used were grown by a Au particle mediated growth via the vapor liquid solid growth mechanism. The NWs typical had diameters of d_{NW} = 80 nm and predominant ⟨111⟩ crystal axis direction. The nominally undoped nanowires were thermally oxidized at T = 1174 K in O_2 atmosphere for 3 min and annealed for 3 min in N_2 atmosphere to employ a high-quality SiO_2 gate-oxide. The oxidized Si NWs were drop-casted onto a 100 nm thick thermally grown SiO_2 layer atop of a 500 µm thick highly p-doped Si substrate. Al contacts to the Si NWs were patterned by electron beam lithography, 15 s of BHF (7:1) etching to remove the SiO_2-shell at the contact area, and subsequent 125 nm Al sputter deposition and lift-off techniques. Rapid thermal annealing at a temperature of T = 774 K in forming-gas atmosphere was employed to initiate the Al-Si exchange to achieve the desired Si channel length. For RFET integration, omega-shaped Ti/Au top gates were fabricated using electron beam lithography, Ti/Au evaporation (8 nm Ti, 125 nm Au), and lift-off techniques.

BF and HAADF STEM: BF STEM was performed on Al-Si-Al NW heterostructures fabricated on 40 nm thick Si_3N_4 membranes using a probe-corrected FEI Titan Themis, working at 200 kV. The Al-Si interface in the shown images was viewed along the [110] direction of observation of the Si crystal.

Electrical Characterization: The electrical measurements were performed using a combination of a HP 4156B semiconductor analyzer and a probe station. To minimize the influence of ambient light as well as electromagnetic fields, the probe station was placed in a dark box. The input signals for the inverter and wired-AND gate were generated by a Yokogawa FG300 function generator connected to VMUs of the semiconductor analyzer. Temperature dependent measurements as well as measurements to extract the effective Schottky barrier heights were performed in vacuum using a LakeShore PS-100 cryogenic probe station and a Keysight B1500A semiconductor analyzer.

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Supporting Information

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

M.S. and R.B. performed the device fabrication. R.B., L.W., and M.S. conducted the electrical measurements. M.I.d.H. carried out the TEM analysis. Z.S.-M. fabricated the SiN membranes used for TEM investigation. C.G.E.M. and J.F.C. have grown the Si NWs. M.S and W.M.W. conceived the project and contributed essentially to the experimental design. All authors analyzed the results and agreed on the manuscript.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

aluminum, logic gates, metal-semiconductor heterostructures, reconfigurable electronics, Schottky barrier field-effect transistors, silicon

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